ELECTRONIC SWITCHING SYSTEMS
5ESS® SWITCHING EQUIPMENT
DIGITAL LINE TRUNK UNIT - EXPORT
CIRCUIT

CHANGES

B. Changes in Apparatus

B.1 New Circuit packs (ANN6B and ANN36) added.

F. Changes in Description of Operation or Changes in CD Sections

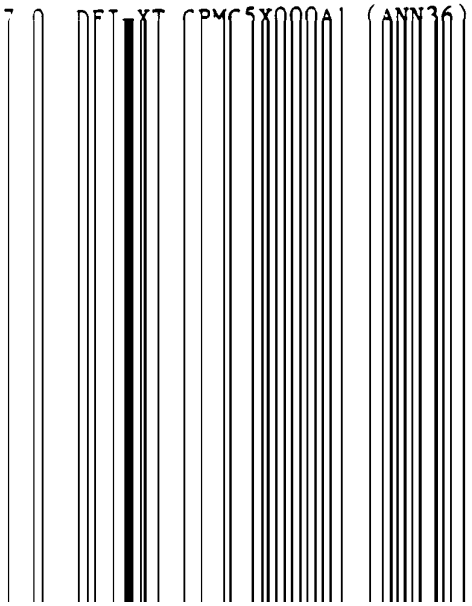
6.0 DFI-EP, CP MC5X401A1B (ANN6B)

6.1 The ANN6B performs all of the functions of the ANN6 with the addition of a means to skew or offset time slots between the facility and the PIDB. The ANN6B also provides "true" AIS transmission to the distant facility under software control and also by autonomous actions resulting from on-board hardware/firmware fault conditions.

6.2 Under software control, the DFI-EP can be programmed to provide a time slot offset (skew) from the facility to the PIDB side, and vice versa. The offset value can be in the range of 0 to 31 and is set once during initialization. If no value is written to the DFI-EP by the SMP, then the DFI-EP uses a zero default offset and behaves as an ANN6. The offset value is routinely audited and mismatches are reported to the SMP.

6.3 Under software control, the DFI-EP can generate a "true" Alarm Indication Signal (AIS) to the distant facility. A "true" AIS signal consists of all logic ones in all time slots including time slot zero and sixteen. Hence, no frame or multiframe alignment signals are transmitted during AIS.

6.4 The DFI-EP autonomously generates AIS to the distant facility in the event of ANN6B hardware/firmware troubles. Activating conditions for AIS include PIDB loss of clock, PIDB loss of sync, and microcomputer sanity (watchdog) timer.



ELECTRONIC SWITCHING SYSTEMS
5ESS* SWITCHING EQUIPMENT
DIGITAL LINE TRUNK UNIT-EXPORT
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The digital line and trunk unit for export (DLTU-E) is a peripheral of the 5ESS. The DLTU-E allows the 5ESS to terminate digital trunks with a 2048-Kb/s 30+2 channel CCITT format.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The DLTU-E consists of one 8-inch high shelf, one power start pack, and up to 16 digital facility interface (DFI) circuit packs. Each DFI terminates one 2048-Kb/s 30+2 channel facility and converts it to the 5ESS peripheral interface data bus (PIDB) format. The PIDB then goes to the duplicated 5ESS time slot interchanger unit (TSIU).

2.02 Each DFI communicates with the duplicated 5ESS Switching Module Processor (SMP) via the peripheral interface control bus (PICB). The DFI monitors the facility and reports to the SMP, via the PICB, the following facility information:

- Service Alarm Red for Frame
- Service Alarm Red for Multiframe
- Remote Alarms
  - Alarm Indication Signal (AIS)
  - Remote Frame Alarm (RFA)
  - Remote Multiframe Alarm (RMA)
- Service Alarm Major (SAM)
- Protection Switching (PS) at 1E-4, 1E-5, 1E-6
- Deferred Maintenance Alarm (DMA)
- Slip count
- Errored Seconds (ES)
- Change of Frame Alignment (COFA) count
- Out-Of-Frame (OOF) count.

This facility monitoring meets or exceeds the requirements described in CCITT recommendations Q.501 through Q.507. In addition to monitoring, the SMP may diagnose the DFI via the PICB.

SECTION II - DETAILED DESCRIPTION

1. POWER START PACK (CP SN346)

1.01 The power start pack prevents the DLTU-E from powering up when the

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-48 volt supply is first applied. This is to prevent current surges when the 5ESS is powered up. To turn on power, push the switch on the front of the power start pack. Once power is on, power cannot be turned off, even if circuit packs are replaced. A red LED indicator lights up if the DLTU-E is shut off. Two leads are distributed to the DFIs to turn power on, while two leads enter the power start pack to indicate that the DFI power is on.

2. DFI-E, CP MC5X401 (CP ANN6)

2.01 The ANN6 terminates the 30+2 channel 2048-Kb/s facility and converts it into a 32 time slot 4.096 Mb/s 5ESS PIDB format that is synchronized to the 5ESS system timing. Separate circuitry is provided for both the receive and transmit direction of transmission. In the receive direction, the clock is extracted from the 2048-Kb/s facility. The framing is done to determine the time slot positions and the signaling frames. Next the line frame is synchronized with the PIDB frame. Finally, the signaling is extracted from the 2048-Kb/s signaling frame and put into the PIDB format.

2.02 In the transmit direction, the PIDB format is converted to the 2048-Kb/s line format. A phase lock loop is used to derive a synchronized 2.048-MHz clock from the 4.096-MHz PIDB clock.

2.03 Electrically, the 30+2 channel facility is a 2048-Kb/s, 3-level, bipolar return-to-zero digital signal (HDB3 or AMI coding). The plus and minus levels correspond to a logic one while zero is a logic zero. The polarity of the logic one levels alternates between plus and minus according to the rules for HDB3.

2.04 Each DFI-E in the DLTU-E has two PICB interfaces: One PICB goes to side 0 while the other goes to side 1 of the duplicated 5ESS SMP. The PICB consists of five twisted pairs of wire used to control the DFI-E from the 5ESS SMP. One pair sends serial address and data to registers on the DFI-E from the SMP. Another pair returns data to the SMP when the SMP reads DFI-E registers. This control data is clocked by a third signal from the SMP. The clock is active only when control data is being sent or received. Another signal, the peripheral service request, is an active low signal sent by the DFI-E to the SMP to indicate that the DFI-E needs service. Finally, one side of the 5ESS SMP can gain control from the other side by changing state on the side select lead of the PICB.

2.05 The PICB interfaces to a microcomputer on the DFI-E pack which monitors the 2048-Kb 30+2 channel facility for such things as slips, out-of-frames, etc, as mentioned in paragraph 2.02 of Section I.

2.06 Each DFI-E pack in the DLTU-E has two PIDB interfaces: One PIDB goes to side 0 while the other goes to side 1 of the duplicated 5ESS TSIU. The PIDB consists of four twisted pairs of wire. Two pairs are used to send the PCM data to and from the DFI-E. This data consists of 32 16-bit time slots clocked at 4.096 Mb/s. Eight bits of each time slot are used for signaling and control. The two remaining pairs of wire supply a 4.096-MHz clock and an 8-KHz sync to the DFI-E for the time slot data.

2.07 The 2048-Kb/s facility has a frame structure consisting of 32 eight-bit time slots. The frame repetition rate is 8 KHz. Sixteen frames are combined to form a 2-msec multiframe. Time slot 0 in every frame is used to carry frame alignment and control bit information.

A. ANN6 Signaling Options

2.08 The ANN6, under software control, can do one of two signaling methods. The first option provides 16-state signaling using the A, B, C, and D bits extracted from time slot 16 of every frame.

2.09 The second option is signaling inhibit, whereby no signaling is extracted or updated. Time slot 16 is a 64-Kb/s clear channel that can carry traffic, signaling, or other services.

B. ANN6 Line-Format Options

2.10 The ANN6 may, under software control, be put into one of two line-format modes. The first mode is HDB3 and the second is AMI.

C. ANN6 Frame-Format Options

2.11 The ANN6, under software control, can be put into one of three multiframe modes. The first is common channel signaling (CCS) and it applies to a facility in which the traffic-related signaling is handled through a separate signaling system. Time slots 1-31 are 64-Kb/s clear channels. In this mode, there is no multiframe alignment signal.

2.12 The second frame-format option is per-channel signaling (PCS0) in which case signaling information is carried in time slot 16 in all frames except frame 0. Time slot 16 in frame 0 carries the multiframe alignment signal along with control and alarm bits. In the PCS0 mode, the frame alignment signal is aligned with the multiframe alignment signal. As a result, all even frames contain the frame alignment word.

2.13 The third frame-format option is PCS1 and is similar to PCS0 except that the frame alignment signal is not aligned with the multiframe alignment signal. As a result, all odd frames contain the frame alignment word.

2.14 Additional options for ANN6 that can be software controlled include a trigger threshold for the loss of frame alignment alarm, transmit reserve bit squelch on/off, and masks for fast and slow response of DFI-E actions.

3. DFI-ER, CP MC5X402 (CP ANN7)

3.01 The ANN7 performs all of the functions of the ANN6 with the addition of a data link sent over the 2048-Kb/s 30+2 channel facility. The E control bit is also transmitted over the facility. The 4-Kb/s data link uses the "M bits" of the European facility format. This data link uses a BX.25 level 2 protocol for data link control.

3.02 The link layer (level 2) of BX.25 is compatible with CCITT recommendation x.25 "Link Access Procedure" (LAPB); "International Standards Access Procedure" (ISO) standard; "High Level Data Link Control Procedure" (ADCCP). For more information see TA 70 and PUB 54001.

3.03 The first application of the ANN7 is to remote a 5ESS interface module over a 2048-Kb/s facility. The ANN7, therefore, provides two additional outputs for the remote switching module (RSM). This is the 2.048-MHz clock that provides synchronization of the RSM with the host 5ESS and a facility status lead to indicate the status (good/bad) of the 2048-Kb/s facility.

4. DFI-ES, CP MC5X403 (CP ANN8)

4.01 The ANN8 performs all of the functions of the ANN6 with the addition of a bridging function to provide a duplicated line reference output for Export Network Clock synchronization with the distant facility.

4.02 Each of the two synchronization outputs provides a 3-level bipolar, return-to-zero digital signal (HDB3 or AMI Coding). The impedance of each output is 120 ohms balanced and the signals are compatible with CCITT recommendations for 2048-Kb/s digital transmission systems.

5. DFI-ERS, CP MC5X404 (CP ANN9)

5.01 The ANN9 performs all of the functions of the ANN7 with the addition of a bridging function to provide a duplicated line reference output for Export Network Clock synchronization with the distant facility.

5.02 Each of the two synchronization outputs provides a 3-level bipolar, return-to-zero digital signal (HDB3 or AMI Coding). The impedance of each output is 120 ohms balanced and the signals are compatible with CCITT recommendations for 2048-Kb/s digital transmission systems.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The DLTU-E has an operating temperature range of 0°C to 70°C.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Packs:

Designation	Meaning
(none)	Power Start Pack
DFI-E	Digital Facility Interface for Export
DFI-ER	Digital Facility Interface for Export RSM
DFI-ERS	Digital Facility Interface for Export RSM Synchronization
DFI-ES	Digital Facility Interface for Export Synchronization

2.02 Interface Cables:

Designation	Meaning
PIDB	Peripheral Interface Data Bus
PICB	Peripheral Interface Control Bus

3. FUNCTIONS

3.01 The primary DLTU-E functions are:

(a) To frame on incoming 2048-Kb/s facility and synchronize to system timing.

(b) To convert from 2048-Kb/s 30+2 channel format to PIDB format.

(c) To monitor the 2048-Kb/s 30+2 channel facility and report problems to the 5ESS SMP.

(d) To provide a 4-Kb/s data link on the 2048-Kb/s facility (ANN7 and ANN9 only).

(e) To provide the 2.048-MHz clock and facility status to the FIU (ANN7 and ANN9 only).

(f) To provide the 2048-Kb/s bridging signal for Export Network Clock synchronization (ANN8 and ANN9 only).

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

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(a) The 2048-Kb/s facility interfaces with customer office equipment. Details for this connection and the type of equipment depend on the specific application. Refer to customer provided information.

(b) The PIDB interfaces to the 5ESS data interface (DI) circuit pack (CPS 836, CPS 837), which is part of the 5ESS interface module's TSIU (SD-5D045-01).

(c) The PICB interfaces to the 5ESS control interface (CI) circuit pack (CPS TN 876), which is part of the 5ESS interface module SMP (SD-5D040-02).

(d) The synchronization outputs (ANN8 and ANN9 only) interface to the 5ESS Export Network Clock (CPS TN 1275).

(e) The RMS synchronization and facility status leads interface to the 5ESS Facility Interface Unit (FIU).

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are contained in the following X-specifications:

(a) X-18928: Power Start Pack, CPS SN346

(b) X-19578: Digital Facility Interface for Export, CPS ANN6, CPS ANN8

(c) X-19579: Digital Facility Interface for Export RSM Application, CPS ANN7, CPS ANN9.

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