5ESS® SWITCHING EQUIPMENT
ECHO CANCELER SIGNALING UNIT
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The Echo Canceler Signaling Unit (ECSU) provides echo cancellation and C5 signaling for digital trunks that are terminated on the Digital Line and Trunk Unit - Export (DLTU-E).

2. GENERAL DESCRIPTION OF OPERATION

2.01 The ECSU is a single-shelf unit mounted in the Switching Module Controller (SMC) cabinet. It consists of a power start pack (SN346B) and up to twenty ECS (TN1511) circuit packs, or ten ECS/ECD pairs.

2.02 The ECS pack is capable of providing echo cancellation for end path delays as great as 32 ms. For end path delays greater than 32 ms, another circuit pack designated as ECD (TN1512) is paired with the ECS pack.

When these packs are used together, the combination can provide echo cancellation for end path delays of as much as 64 ms.

2.03 Each ECS circuit pack resides in series on the Peripheral Interface Data Bus (PIDB), between the Time Slot Interchange Unit (TSIU) and the Digital Facility Interface (DFI). The Switching Module Processor (SMP) sends control orders to the ECS on a Peripheral Interface Control Bus (PICB).

2.04 The ECS pack is configured in a 1:1 ratio with the DFI; that is, each ECS or ECS/ECD pair relates to one DFI. Each DFI has a separate PICB connection to the SMP, but any DFI that requires echo cancellation or C5 signaling receives its PIDB from the ECS pack.

2.05 For those DFIs that do not require either of these functions, the corresponding ECS slot will be vacant, and a (Berg type) jumper is placed on the ECSU backplane in the vacant slot position that provides continuity for the PIDB from the TSIU to the DFI.

2.06 Power to the ECSU circuit packs (-48V) is distributed among the slot positions over five separately fused power busses.

SECTION II - DETAILED DESCRIPTION

1. POWER START PACK (CP SN346B)

1.01 The Power Start pack prevents the ECS from powering up when the office -48 Volt supply is first applied. This is to prevent large current surges when the 5ESS is powered up. To turn power on, the push-to-start switch on the faceplate of the Power Start pack is pressed. Once power is on, it remains on to all ECS and ECD packs in the shelf. Individual ECS packs subsequently removed from the shelf do not affect the power to the ones remaining. As additional ECS and ECD packs are added to the shelf, they are automatically powered up (providing that power is already on to other packs).

1.02 A red LED on the faceplate of the Power Start pack turns on to indicate that power to the ECS packs in the shelf is shut off, indicating that the power start switch needs to be pressed. Once power is applied to both power bus groups (A and B) of the shelf (there must be at least one ECS pack per group), then the LED will extinguish.

2. ECHO CANCELER SIGNALING (ECS) CIRCUIT PACK (CP TN1511)

A. -48V Power Conversion Circuit

2.01 The -48V Office voltage that feeds the ECSU is converted to a regulated +5V supply through on-board power converter modules on each ECS circuit pack. Protection for over-current conditions is provided by an on-board 750 mA fuse placed in-line with the -48V feed to the power converter input pin.

B. MCTSIU PIDB (Near-End PIDB) Interface

2.02 Line receivers convert the twisted-pair, balanced signals from the MCTSIU to single-ended, TTL-level signals used by the ECS circuitry. These signals are the standard 8 KHz sync, 4 MHz clock, and PIDB output data that are duplicated (PIDB0, PIDB1) and sourced by the MCTSIU. In the other direction, line drivers convert the single-ended,

TTL-level output data from the ECS to the balanced, twisted-pair PIDB input data sourced to the MCTSIU.

2.03 Maintenance on the near-end PIDB is accomplished through the use of a parity loopback scheme implemented in a Programmable Array Logic (PAL) device. The PAL circuitry calculates parity over the first fifteen bits in each timeslot from the MCTSIU and inserts the same sense of the parity on the corresponding timeslot going back to the MCTSIU.

2.04 Since the MCTSIU sources two PIDBS to the ECS, PIDB side 0 or 1 selection is done through a 2:1 demultiplexer circuit controlled by an on-board register bit accessed through the PICB.

Timing Reference and Generation

2.05 The ECS uses a Phase-Locked Loop (PLL) circuit to generate the 8.192 MHz and 4.096 MHz system master clocks that are locked to the selected near-end PIDB, and are used as the reference from which several on-board clocks and sync signals are derived. The PLL is designed around a 4044 phase detector with a 16.384 MHz VCXO and a divide-by-4 counter (implemented as two D-FFs in series) placed in its loop.

2.06 Two 2Kx8-registered PROM, addressed by a 10-bit counter (clocked by the 8.192 MHz system master clock and reset by the 8 KHz sync pulse), provide the remaining timing for the ECS pack.

Echo Canceler

2.07 The ECS pack provides echo cancellation on a per-timeslot basis for echo paths of up to 32 ms delay. Echo cancellation is performed using the Third Generation Echo Canceler Chip Set consisting of a control chip, a tone disabler chip, and sixteen data chips.

A. Echo Canceler Control Chip

2.08 The control chip (327DJ) forms the main interface between the incoming and outgoing traffic channels (via 4 I/O leads) and the data processing devices (via 8-bit output bus, 9-bit input bus). It serially receives 159 global option bits and seventeen local option bits, and sources an 8-bit error report stream every frame (125 us).

B. Echo Canceler Data Chips

2.09 Sixteen data chips (1000AJ) are used to provide echo cancellation for thirty-two channels with up to 32 ms of end path delay. The data chips interface directly to the control chip via the input and output busses.

C. Echo Canceler Tone Disabler

2.10 The tone disabler chip (1000R) is used in conjunction with the control chip to provide for 2100 Hz (with or without phase-reversal) echo canceler disabling. The chip receives an 87-bit serial option stream that repeats every 125 us.

CCITT5 Line Signaling Transceiver

2.11 The Line Signaling Transceiver (LST) is the VLSI device that performs Signaling System No. 5 functions on a per-channel basis.

A. Transmitter

2.12 The transmitter section of the device generates in-band signaling tones of 2400 Hz, 2600 Hz, and dual-tone 2400+2600 Hz under control of the PIDB signaling bits sourced from the switch or near end, as shown in the following table.

LST Tone Generation			
G-Bit	C-Bit	D-Bit	Tone
0	0	0	None (Transparent)
0	1	0	2400 Hz
0	0	1	2600 Hz
0	1	1	2400+2600 Hz
1	x	x	None (Transparent)

B. Receiver

2.13 The receiver section detects valid signaling tones on the facility or far end, overwrites the incoming (far-end) C and D signaling bits, and passes this information to the MCTSIU via the near-end PIDB (NEPIDB) as shown in the following table. (LST enable/disable is controlled by the G-bit sourced to the LST from the MCTSIU on the NEPIDB.)

LST Tone Detection			
Tone	G-bit	C-Bit	D-Bit
2400 Hz	0	1	0
2600 Hz	0	0	1
2400+ 2600 Hz	0	1	1
x	1	No Overwrite	No Overwrite

PIDB Maintenance and Timing Generator (Far-End PIDB)

2.14 The PIDB Maintenance and Timing Generator (PMTG) is a custom VLSI device which emulates the front-end functions of a TSIU and sources the far-end PIDB (FEPIDB) to the DFI-E.

A. Primary Functions

2.15 Its primary functions are as follows:

1. Generate timing (clock and sync) to the DFI-E on the FEPIDB.
2. Perform walking parity maintenance scheme on the FEPIDB.
3. Provide a single PIDB Timeslot (PTS-7) loop-back path to the NEPIDB.
4. Detect and report FEPIDB parity errors when the parity walker is off.

The PMTG contains several internal registers that are used to configure the device for walking parity, PTS-7 loop, etc., which can be accessed via the PICB Interface described below.

PIDB Interface

2.16 The PICB Interface provides for communication between the ECS circuit pack and the Switch Module Processor (SMP). Line receivers convert the twisted-pair, balanced signals from the SMP to single-ended, TTL-level signals used by the ECS circuitry. These signals are the standard 2 MHz burst clock, interrupt, side select, and output data that are duplicated (PICB0, PIDB1) and sourced by the SMP. In the other direction, line drivers convert the single-ended, TTL-level output data from the ECS to

the balanced, twisted-pair PICB input data that is sourced to the SMP.

A. Control Link Receiver/Transmitter (CLRT)

2.17 The CLRT VLSI device terminates the PICB and acts as the scan and distribute point center for SMP messages to and from the ECS circuit pack. These messages are passed on to the Control Communications Buffer (CCB) device that is accessible by both the SMP (through the CLRT) and the ECS's on-board microprocessor (uP).

B. Control Communication Buffer (CCB)

2.18 The CCB VLSI device is a dual-port mailbox for messages that pass between the SMP and the ECS's uP. There are sixty-two data registers and sixty-two flags for each side, with the read/write permissions for each side enforced by the device's internal hardware. Each data register (8 bits) has a flag location (1 bit) associated with it. To write a message, one side (uP or SMP) writes the message data and sets the corresponding flag. The other side recognizes the set flag as an indication that a message should be read. Once the other side has read the data, it resets the flag as an acknowledgement.

2.19 Most of the CCB data registers hold messages to change echo canceler options, configure the LST and PMTG devices, and to report various ECS circuit pack errors to the SMP.

Microcomputer Complex

2.20 The microcomputer complex consists of an Intel 16 MHz, 80188 microprocessor with memory comprised of a 64K x 8 EPROM and a 2K x 9 Dual Port RAM.

A. Microprocessor (uP)

2.21 The ECS on-board uP interfaces to the CCB and handles the requests contained in the CCB message registers. The uP also has access to the LST and EC error bits through its interrupt leads.

B. Dual Port RAM (DPR)

2.22 The Dual Port RAM is used as scratch RAM for the uP, except for the first 256 bytes which are reserved for the echo canceler global and local options that are sourced (via option registers) to the EC control chip every frame.

2.23 Port A of the DPR is written and read by the uP, while Port B is configured as write-only. Port B interfaces with the parallel-to-serial option registers that source the echo canceler options.

Data Path Multiplexers and Delay Registers

2.24 There are several places along the ECS data path where data multiplexers and bit delay flip-flops are used.

A. Echo Canceler and LST Multiplexers

2.25 A set of multiplexers are used at the EC output to re-insert the PIDB signaling bits into each timeslot, since the EC will only pass the first eight incoming PCM data bits and ignore the signaling bits. Another set of multiplexers are used at the EC outputs to bypass EC data totally (via CCB message) for maintenance purposes. Similarly, multiplexers are used at the LST outputs to bypass the LST data completely, again for maintenance purposes.

B. Delay Registers

2.26 Both the near-end and far-end out-going PCM timeslots must align with the 8 KHz sync pulse in a specified manner. This bit alignment is accomplished with D Flip-Flops (1.5 bit delay) in the out-going (ECS to DFI-E) direction on the FEPIDB, and with a 1K x 8 delay RAM (469.5 bit delay) in the out-going (ECS to MCTSIU) direction on the NEPIDB.

3. ECHO CANCELER DATA (ECD) CIRCUIT PACK (CP TN1512)

A. -48V Power Conversion Circuit

3.01 The -48V Office voltage that feeds the ECSU is converted to a regulated +5V supply through on-board power converter modules on each ECD circuit pack. Protection for over-current conditions is provided by an on-board 500 mA fuse placed in-line with the -48V feed to the power converter input pin.

B. Echo Canceler Data Chips

3.02 The ECD is comprised of sixteen data chips which, when used with the ECS circuit pack, provide for echo cancellation for end path delays of up to 64 ms. The data chips interface to the control chip through the input and output busses that are buffered on the ECD circuit pack.

C. Interpack Signal Buffers

3.03 All of the timing and bus signals that are routed on the backplane from the ECS to the ECD or from the ECD to the ECS are buffered immediately upon entering or leaving the ECD pack.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The ECSU has an operating temperature range of 0°C to 70°C.

2. FUNCTIONAL DESIGNATIONS

Circuit Packs

Designation	Meaning
(none)	Power Start Pack
ECS	Echo Canceler Signaling Pack
ECD	Echo Canceler Data Pack

Interface Cables

Designation	Meaning
NEPIDB	Near-End Peripheral Interface Data Bus
FEPIDB	Far-End Peripheral Interface Data Bus

3. FUNCTIONS

3.01 The primary ECSU functions are:

a. To provide echo cancellation for digital trunks that are terminated on the Digital Line and Trunk Unit for Export (DLTU-E).

b. To provide C5 line signaling for digital trunks that are terminated on the Digital Line and Trunk Unit for Export (DLTU-E).

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon is to be followed.

a. The Near-End PIDB (NEPIDB) interfaces to the 5ESS Data Interface (DI) circuit pack (CPS 836, CPS 837), which is part of the 5ESS Interface Module's TSIU (SD-5D045-01).

b. The Far-End PIDB (FEPIDB) interfaces to the 5ESS Digital Facility Interface for Export (DFI-E).

c. The PICB interfaces to the 5ESS Control Interface (CI) circuit pack (CPS 876), which is part of the 5ESS Interface Module's SMP (SD-5D040-02).

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are contained in the following documents:

a. X-Specification (X-18928): Power Start Pack, CPS SN346B

b. DS5UE3.00.06.10.00 - Issue 1 - 5ESS Echo Canceler and CCITT No. 5 Signaling Unit (ECSU) Hardware Test Plan Development Specification, Appendix 5, Manufacturing Tests.

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