13

PBX SYSTEMS
701A, 701B, 711A, 711B OR 740E
"TOUCH-TONE " TO DIAL PULSE
SOLID STATE CONVERTER CIRCUIT
14 DIGITS

CHANGES

B. Changes in Apparatus

B.1 Superseded	Superseded by
App Fig. 1	App Fig. 2

D. Description of Changes

D.1 App Fig. 1 is rated Mfr Disc. and App Fig. 2 is added to replace Mfr Disc. apparatus.

D.2 Notes 106, 107, 108, and 302 are clarified and notes 109, 110, 205, 403, and 404 are added.

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DEPT 3224-GRJ-RVL

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NO. 701A, 701B, 711A, 711B or 740E
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14 DIGITS

CHANGES

B. Changes in Apparatus

B.1 REMOVED	REPLACED BY
Resistors R7 and R8 237A, 36.5 Ohms	Resistors R7 and R8 237A, 28.7 Ohms
CM53-CM58, 1B Core, 17-Turn Output	CM53-CM58, 1B Core, 26-Turn Output

D. Description of Changes

D.1 CADs 1 and 3 are revised and Note 202 is added to cover the application of Z and Y options by the installer.

D.2 -27V leads between printed wiring boards are run as 22 gauge, BW wire and connected as shown in Note 203.

D.3 TRW leads between printed wiring boards are rerouted and are run as 22 gauge, BW wire, as indicated in Note 204.

BELL TELEPHONE LABORATORIES, INCORPORATED

DEPT 5333-FWW-RDW

PBX SYSTEMS
NO. 701A, 701B, 711A, 711B OR 740E
"TOUCH-TONE" TO DIAL PULSE
SOLID STATE CONVERTER CIRCUIT
14 DIGITS

CHANGES

D. Description of Changes

D.1 Options V and W are added. These options permit this circuit to replace the 10-digit converter (SD-66887-01) which is rated Mfr Disc.

D.2 In SECTION II add 18.06 as follows:

18.06 If this circuit is used to replace a 10-digit converter per SD-66887-01, option V or W must be employed. If option W is employed, release of the converter is accomplished by a signal on lead 29, which releases the converter through an EC break contact of the rotary dial repeating and interface circuit. If option V is used, release is by a signal on lead 13 to the above mentioned circuit. Option W is employed whenever rotary dial repeating and interface circuit (SD-66886-01) issue 7B or later is provided, otherwise option V is used with this circuit. Option V and W are not to be employed when this circuit is used with interface circuit per SD-1E054-01 or SD-66891-01.

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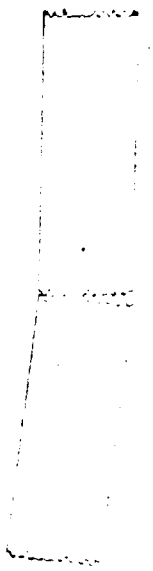
DEPT 5332-LES-GES



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"TOUCH-TONE" TO DIAL PULSE
SOLID STATE CONVERTER CIRCUIT
14 DIGITS

TABLE OF CONTENTS

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This circuit is for use in step-by-step dial PBXs for operation with station lines which are equipped with TOUCH-TONE dial telephone sets. This circuit works in conjunction with a TOUCH-TONE receiver. The TOUCH-TONE signals are fed to the TOUCH-TONE receiver, and the receiver and converter convert these signals into rotary dial pulses. These pulses are then used to establish a connection within the PBX. After the connection is established, the converter is released so that it can be used by other stations.

2. GENERAL DESCRIPTION OF OPERATION

2.01 When a number is dialed from a TOUCH-TONE dial telephone set, a TOUCH-TONE signal is sent out of the set for each digit that is dialed. These signals consist of a high-frequency and a low-frequency tone. There is a different combination of the two tones for each digit.

2.02 These tones are separated in the TOUCH-TONE receiver, by means of filters, into low- and high-frequency groups. The outputs of the filters are then fed into groups of tuned circuits, with each tuned circuit responding to a particular frequency. After the signals pass through the tuned circuits, they are demodulated and passed through amplifiers which actuate relays. Two relays are operated every time a digit is dialed.

2.03 The relays are wired to close through one-out-of-ten leads. This is the input to the converter. The output of the pretranslation circuit is wired to change this to a one- or two-out-of-six input code to the coincident fluxor memory. The closing of these leads provides a path for one-half of the write current necessary to set the cores in the coincident fluxor memory.

2.04 The operation of the two relays in the TOUCH-TONE receiver also completes a path for the steering signal. This steering signal is used to trigger the write control and advance the write stepping switch. This stepping switch provides the other half of the required write current. It is the

function of the write stepping switch to store the digits in the coincident fluxor memory in the same order that they are received.

2.05 The read control is free running and continually scans the coincident fluxor memory. If it finds a digit stored in the memory, a signal is sent to the output amplifiers. The output amplifiers convert the low-level voltage pulse to a high-level current pulse. This current pulse sets the digit in the translation shift register, which is used as a temporary storage device. The current pulse also provides a signal which stops the read control from scanning the coincident fluxor memory for further digits. The translation process now starts in the translation shift register.

2.06 The translation shift register is a temporary storage device. Each digit is stored in it in the sequence in which it is received, but only for the time it is necessary to pulse it out. This shift register generates output pulses equal to the number corresponding to the digit that is stored in it. The pulses are used to trigger a monostable multivibrator which has a pulsing relay as its load. The pulsing relay is used to send the pulses into the step-by-step PBX equipment. The monostable multivibrator, used as a generator, converts the 1-usec duration trigger pulse into the required 60-percent break and 40-percent make of the pulsing relay contacts.

2.07 Five hundred msec after the digit is pulsed out, a signal is sent from the translation shift register to stop the translation process and to start the read-control scanning for the next digit.

2.08 Other features, such as pretranslation and time-out, have been provided. The inclusion of these features reduces the number of converters required for handling the traffic for a given number of station lines. The pretranslation feature provides a means for disconnecting the converter when certain codes are dialed. The function of the time-out feature, using Z option, is to dial the digit zero 10 seconds after the converter is seized in cases where there has been no attempt to dial any digits. With Y option, and without dialing, the station is cut through to the first selector. The time-out feature is also used to disconnect the converter 10 seconds after the last digit is pulsed out in cases where a code is dialed for which there is no pretranslation.

2.09 Power for performing most of the functions of the converter is supplied by a pulse power supply. It supplies -27 volt pulses with a repetition rate of 160 pps and has a maximum current capability of 5 amps. The -27 volt power for this pulse power supply and for the remainder of the converter is obtained from the -48 volt supply by means of a dropping resistor and a voltage regulating diode.

SECTION II - DETAILED DESCRIPTION

1. GENERAL

1.01 The solid state converter has power applied directly from the -48 volt fuse panel. Since power is applied at all times, the converter is ready for immediate use. To prevent the operation of pulsing relay PLS during the time when the converter is idle, the operating path of this relay is partly under control of the rotary dial repeating and interface circuit.

1.02 The following conventions are used throughout this circuit description.

(a) Any core, as indicated by the associated mirror symbol, switched to the right or up is in the reset state while any core switched to the left or down is in the set state.

(b) The initial converter reset pulse which occurs when the converter is seized does not reset all of the cores but sets and resets them into a predetermined pattern.

2. SEIZURE OF CONVERTER

2.01 When a TOUCH-TONE dial telephone is removed from the switch hook, a converter is connected to it by means of its assocated rotary dial repeating and interface circuit. The rotary dial repeating and interface circuit closes part of the operating path of the PLS relay, and momentarily closes and then opens the converter reset leads 22 and 23. It also starts the timing circuit, the operation of which will be covered later on.

3. DC POWER SUPPLY - PS9

3.01 The solid state converter operates from -27 volts dc, which is obtained from the local -48 volt dc supply by the use of dropping resistors R20 and R21 and the voltage regulating diode CR46. The system reset current is sent through R18 and C10 in parallel with R19. This is a single pulse created when C10 is charged. The converter reset circuit is closed by relays of the rotary dial repeating and interface circuit only for a short time when the converter is seized. Resistor R19 is used to discharge capacitor C10.

4. PULSE POWER SUPPLY - PS13

4.01 When the converter is seized through the rotary dial repeating and interface circuit, a ground is placed on lead 24. This starts current flowing through resistors R57, R52, capacitor C12, and resistors R54 and R55. Capacitor C12 will charge, and ultimately forward bias CR57 and the base-emitter junction of PNPN transistor Q27, turning Q27 on. This results in a current, limited by R54, flowing through the series connection of C11, in parallel with R56, Q27, CM59, R54, C12, CR54, and CR55. This current,

flowing through CM59, is converted by transformer action into a base current turning Q28 on. When Q28 turns on, an additional current flows through CM59 through the series connection of Q28, CM59, and the TRW load. This current regeneratively saturates Q27, bringing the Q28 collector to ground and clamping the Q27 n-emitter to ground through diode CR53. During the initial operation of Q27, capacitor C11 was partially charged. This charge on C11, in combination with the clamping action of Q28 and CR53, reverse biases Q27 and turns it off.

4.02 Q28 sustains itself in saturation until magnetic core CM59 saturates and transformer action ceases. At this time, capacitor C12 has been charged to approximately 18 volts through the series combination of Q28, CR53, CM59, R54, C12, CR54, and CR55. When Q28 turns off, the positive terminal of C12 is returned to -27 volts through R54 and R55. This puts the junction of C12, R58, CR57, and CR54 at approximately -46 volts. Current now flows through R57, R52, C12, R54, and R55 charging C12 until CR57 and the base-emitter junction of Q27 are again forward biased, turning Q27 on and causing the pulser to repeat its cycle. Adjusting R57 controls the rate of discharging of C12,and hence controls the pulse repetition rate.

4.03 Resistor R56 serves to discharge C11 during the pulser off-time. CR56 protects the base-emitter junction of Q28 and also limits transients occurring in the magnetic circuit when power is initially applied to the converter. Capacitor C13 provides an energy reservoir for the pulser and reduces transients appearing on the power supply leads. The 10-turn winding through CM59, which goes to the converter dc power supply, FS9, serves to reset CM59 to its set state during the pulser off-time, readying it for the next pulse.

4.04 When the converter is released through the rotary dial repeating and interface circuit, the ground is removed from lead 24. Any pulse that was started is completed; however, no additional pulses occur until this ground is again placed on lead 24.

5. CONVERTER RESET CIRCUIT - FS9

5.01 Before any of the magnetic circuits will operate properly, the converter must be reset. The converter reset current magnetizes the cores in a predetermined pattern. After the pattern is set, the succeeding pulses will switch specific cores to produce the correct outputs.

5.02 The reset circuit is an RC configuration. When the converter is seized, the rotary dial repeating and interface circuit momentarily closes through leads 22 and 23. This starts the charging of C10 through R18 and the reset winding which passes through each core. Initially a large charging current pulse is obtained through this circuit. After the reset pulse is completed, the closure on leads 22 and 23 is removed. This permits C10 to discharge through R19. When the converter is again seized, the reset current will again put all of the cores in the correct state.

6. PULSE DISTRIBUTOR - FS7

6.01 The pulse distributor continually alternates the output of the pulse power supply into two phases, TR and TW. The converter reset pulse sets CM43 and resets CM44. The next TRW pulse, through R15, resets CM43. This generates a positive signal on the base of Q16 and turns it on allowing the TRW pulse to pass through Q16, CM44, and R17 and out on lead 3. The current through CM44 sets this core in preparation for the next TRW trigger pulse through R15. A tap-off on the n-emitter of Q16 pin 1 is made to provide a steering current. The current through Q16 is of the TR phase.

6.02 The next TRW pulse through R15 resets CM44 and generates a positive signal on the base of Q15. This turns Q15 on and permits the TRW pulse to pass through Q15, CM43, and R16 and out on lead 1. A tap-off is made from the n-emitter of Q15 pin 1 to provide the memory bit current. The current through CM43 sets it in preparation for the next TRW pulse. This current through Q15 is of the TW phase.

6.03 When a button on the TOUCH-TONE set is depressed, 9 for example, the L3 and H3 relays in the TOUCH-TONE receiver are operated. The closure of these relays allows the TW pulses to flow through the 1 memory bit winding, lead B, the H3 and L3 relays, lead D9 to the pretranslation circuit, the 8-memory bit winding, and R1 to -27 volts. This provides one-half of the current required to store a digit in the coincident fluxor memory.

6.04 The steering circuit is wired so that closure of the P and STR leads is made only if a relay in the H group and one in the L group is operated. This closure enables TR pulses from the pulse distributor to pass through to the write control.

7. WRITE CONTROL AND DISTRIBUTOR - FS1

7.01 TR pulses are continually flowing from the pulse distributor, on lead 4, to the write control, setting CM4. They leave on lead 16 and reset CM7 in the read control and terminate on -27 volts. TW pulses from the pulse distributor pass through lead 1 and CM13 in the frequency divider distributor, CM3 in the write control, and terminate on -27 volts. When closure is made in the receiver steering circuit, pulses in the TR phase will flow on lead STR through voltage divider R2 and R1 to -27 volts. The

1.5-volt pulse developed across R1 on the base of Q1 turns Q1 on and TRW pulses flow through R3, CM3, CM4, and Q1 to -27 volts. These TR-phase pulses will set CM3 but will not reset CM4 at this time because they cannot overcome the heavier TR pulses coming through on lead 4.

7.02 The next TW pulse on lead 12 will reset CM3 and produce a positive signal on the base of Q2. This will turn Q2 on and allow a TRW pulse to pass through Q2, CM4, R8, and lead 13 of the pretranslation circuit to -27 volts. This current pulse resets CM4 and generates a signal in the transfer loop coupling CM4 to CM1 and CM2. The pulse in the transfer loop resets core CM1. The switching of CM1 generates a positive signal on the base of Q4 turning it on and enabling a TRW pulse to pass through R5, Q4, CM1, CM2, and out on lead 17 to the write stepping switch. In passing through CM2, the pulse sets it in preparation for the next digit. Whenever Q2 turns on, a pulse also passes via lead 28 through the interface circuit to the Early Cut and Double Registration Control Circuit.

7.03 The TR pulse through Q1 following the TW pulse, described previously, sets CM3 but is not of sufficient magnitude to override the TR winding on CM4 in order to reset CM4. Hence, the next TW pulse arriving on lead 12 will reset CM3 and again turn Q2 on. However, the TRW pulse passing through R4, Q2, and then CM4 does not switch CM4 at this time, since CM4 was previously reset. Since CM4 is not switched, no current is induced in the transfer winding linking CM4 with CM1 and CM2. A current flows in the transfer winding only once for each digit written into the converter memory.

7.04 After the digit is registered and the STR lead is opened by the TOUCH-TONE receiver, no more TR pulses will be passed by Q1 until the registration of the next digit. However, the next TR pulse on lead 4 will now set CM4.

7.05 The second digit again activates the write control and sends a pulse through the transfer loop, as described previously. However, at this time CM2 is switched, turning Q3 on. With Q3 conducting, a pulse is passed through R5, Q3, CM2, CM1, and out on lead 2 to the write stepping switch. In a similar manner, the registration of alternate digits supplies pulses on leads 2 and 17, respectively.

8. WRITE STEPPING SWITCH - FS4

8.01 When the converter is seized, cores CM15 to CM27 are set by the system reset pulse and at the same time CM28 is reset by the same pulse. The advance pulse from Q4 of the write control and distributor comes through on lead 17 when a digit is received in the TOUCH-TONE receiver. This advance pulse sets CM28, inducing a voltage in its 11-turn winding. A current now flows through the 3-turn winding of CM15, diode CR2, and out on lead 16 to the coincident fluxor memory. This current resets CM15 in preparation for the next advance pulse and provides one-half of the coincident current necessary to store the digit in the coincident fluxor memory. The arrival of the next digit causes an advance pulse on lead 2 from the write control and distributor.

8.02 This advance pulse sets CM15, inducing a voltage in its 11-turn winding, causing a current in the 3-turn winding on CM16, CR3, and out on lead 15 to the coincident fluxor memory. This current resets CM16 in preparation for the next advance pulse coming in on lead 17, and provides one-half of the coincident current necessary to store the digit in the coincident fluxor memory. The alternate advance pulses arrive either on lead 2 or 17, as the remaining digits are dialed. As these pulses come through, the cores CM17 to CM27 are reset, one at a time, and the digits are stored in the coincident fluxor memory cores. The number of cores that are reset depends on the number of digits that are dialed.

8.03 The coincident fluxor memory can store 14 digits sequentially. However, the write stepping switch can recycle and additional digits can be stored, provided that vacant storage slots are available due to digits being pulsed out. Also note that the write stepping switch advances only when a digit is received in the TOUCH-TONE receiver and that a TR pulse followed by a TW pulse is necessary to trigger the write control and distributor.

9. COINCIDENT FLUXOR MEMORY - FS6

9.01 When the converter is seized, the reset current sets rungs 1 and 2 up and 3 and 4 down in the coincident fluxor memory. When the word current through the write stepping switch and the bit current through the closed relay contacts of the TOUCH-TONE receiver are coincident through a core, then rungs 1 and 2 of the core are set down and 3 and 4 are set up. This is the way a digit is stored in the coincident fluxor memory. Current through either the word or the bit winding is not sufficient to set a core. Each digit is assigned six cores in the coincident fluxor memory. The digits are stored by setting one- or two-out-of-six cores in this memory.

9.02 Table A shows the assignment of cores for the various digits and numbers.

9.03 The memory contains a spare bit slot that can be wired into use in case a single memory bit slot becomes defective. Cores 85 through 98 constitute the spare bit slot that can be utilized by moving the input and output wires from the defective slot to the corresponding terminals of the spare slot.

TABLE A

FS6

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Number	Cores Set													
1	78	71	79	72	80	73	81	74	82	75	83	76	84	77
2	64	57	65	58	66	59	67	60	68	61	69	62	70	63
3	78 64	71 57	79 65	72 58	80 66	73 59	81 67	74 60	82 68	75 61	83 69	76 62	84 70	77 63
4	50	43	51	44	52	45	53	46	54	47	55	48	56	49
5	78 50	71 43	79 51	72 44	80 52	73 45	81 53	74 46	82 54	75 47	83 55	76 48	84 56	77 49
6	36	29	37	30	38	31	39	32	40	33	41	34	42	35
7	78 36	71 29	79 37	72 30	80 38	73 31	81 39	74 32	82 40	75 33	83 41	76 34	84 42	77 35
8	22	15	23	16	24	17	25	18	26	19	27	20	28	21
9	78 22	71 15	79 23	72 16	80 24	73 17	81 25	74 18	82 26	75 19	83 27	76 20	84 28	77 21
0	8	1	9	2	10	3	11	4	12	5	13	6	14	7

10. READ CONTROL AND DISTRIBUTOR - FS2

10.01 The converter reset pulse sets CM5 and CM7, and resets CM6. The next TR pulse from the pulse distributor on lead 16 resets CM7 and produces a positive signal on the base of Q5, turning it on and enabling the TRW pulse to pass through CM5, Q5, R6, CM6, and CM7. This resets CM5 and sets CM7, but does not switch CM6. The switching of CM5 generates a positive signal on the base of Q7, turning it on and allowing a TRW pulse to pass through the R7 and R8 parallel combination, Q7, and CM6 to the read stepping switch on lead 21. This pulse sets CM6 in preparation for the next trigger pulse.

10.02 An output on lead 21 causes the read stepping switch to read out a memory slot. If a digit is found in the memory, an output amplifier signal is received on lead 8, resetting CM7. This signal overrides the effect of the current in the 9-turn winding on CM7, which is connected to the n-emitter of Q5. The read control and distributor stops until the digit that was transferred into the shift register is dialed out and an interdigital time of 600 msec elapses. At the end of the interdigital time, the translation shift register sends out a pulse in the TW phase on lead 7, setting core CM7. The next TR pulse on lead 16 resets CM7, turning on Q5. This time the TRW pulse through Q5 resets CM6, turning Q6 on. When Q6 is turned on, a TRW pulse passes through the parallel combination of R7 and R8, Q6, CM5, and out on lead 20 to the read stepping switch. The read stepping switch then sends a signal to the coincident fluxor memory to read out the next digit that was stored.

10.03 When a pulse is sent out on lead 20 but no digit is stored in the coincident fluxor memory, then no signal is received on lead 8 from the output amplifiers. Hence, the current in the 9-turn winding of CM7 will switch CM7 to the set condition so that the next TR pulse on lead 16 will again reset CM7, turning Q5 on. When Q5 turns on, it turns Q7 on, thus sending a TRW pulse out on lead 21 to the read stepping switch.

10.04 If a digit is read out, a pulse will be received from the output amplifiers on lead 8 and this circuit will again stop operating until the digit is pulsed out and the 600-msec interdigital time has elapsed.

10.05 The read control and distributor is free running and it will send a signal to the read stepping switch every time a TR pulse is received on lead 16, provided there is no readout of a digit.

11. READ STEPPING SWITCH - FS5

11.01 In the read stepping switch, cores CM29 to CM41 were initially set while CM42 was reset. The advance pulse on lead 21 sets CM42 and generates a pulse in the 8-turn winding on it. The current flow in this winding passes through the 2-turn winding on CM29, diode CR20, and out on lead 22 to the coincident fluxor memory. This current resets CM29 in preparation for the next advance pulse. If a digit is stored in the first slot of the coincident fluxor memory, this digit is read out and the read control and distributor is stopped. If nothing is stored in the first word slot of the memory,

the read control and distributor continues to scan the remainder of the fluxor memory.

11.02 If the digit 9 is stored in the first slot in the form of an 8 and a 1, cores CM78 and CM22 have rungs 1 and 2 switched down and rungs 3 and 4 switched up. The read current has the effect of resetting the cores in the first slot, thus producing a positive signal on the output winding of any core that has its magnetic state switched. The read current causes an output on leads 26 and 25 for the digit 8 and on leads 18 and 17 for the digit 1. This is a low-level voltage pulse and it must be changed to a high-level current pulse to perform its necessary function.

11.03 Alternate pulses on leads 20 and 21 from the read control and distributor switch cores CM29 to CM42 in sequence in the read stepping switch, causing an output to occur on one of the corresponding leads 22 to 35 to the coincident fluxor memory.

12. OUTPUT AMPLIFIERS - FS12

12.01 The output of the coincident fluxor memory is coupled to the output amplifiers of FS12. The changeover from a low voltage to a high-current pulse is accomplished in the following manner. The low coincident fluxor memory output voltage is first stepped up through a transformer and then coupled to a PNPN solid state device. The stepped up voltage is now of a sufficient magnitude to fire the PNPN and, when this solid state device breaks down, a high current pulse is created. These transformers are wound on cores CM53 for a 1 and CM55 for an 8. The output of CM53, digit 1, is coupled to the base of Q21. This signal turns Q21 on and enables a TR pulse to pass through Q5 of FS2, R39, Q21, and out on lead 15 to the translation shift register. The output of CM55, digit 8, is coupled to the base of Q23, turning it on and allowing a TR pulse to pass through R51, Q5 of FS2, Q23, and out on lead 11 to the translation shift register.

12.02 These two inputs into the translation shift register come together in a common output which sets CM14 in the translation control. The common output of the translation shift register also resets CM7 in the read control, which stops the read control from scanning the coincident fluxor memory for any further digits, until the existing one is pulsed out.

13. TRANSLATION CIRCUIT - FS3

13.01 The translation control circuit is part of FS3 and consists of R12, Q11, and CM13. Initially, CM13 is reset by the converter reset pulse when the converter is seized. CM13 is later set by a TR pulse on lead 17 when any of the output amplifiers are turned on. The following TW pulse arriving on lead 1 resets CM13 which induces a positive signal on the base of Q11, turning it on. The conduction of Q11 allows a TRW pulse to override the TW pulse attempting to reset CM13 on lead 1 and switches CM13 into the set state. Succeeding TW pulses will turn Q11 on until an end-of-digit signal from Q10 overrides the TRW setting of CM13 and resets CM13, which stops the translation circuit.

13.02 The end-of-digit pulse occurs 600 msec after each digit has been pulsed out, when transistor Q10 is triggered on. A current in lead 20 from the translation shift register, which occurs 500 msec after a digit is outpulsed, resets CM10. The next advance pulse to the translation shift register sets CM10 and induces a voltage in the 1-turn winding coupled to Q10, turning it on. A TRW pulse is now permitted to flow which is called the end-of-digit signal.

13.03 The frequency divider distributor circuit consists of R11, Q12, Q13, CM11, and CM12. The system reset current sets CM11 and resets CM12. When Q11 in the translation control circuit conducts, CM11 is reset, which induces a positive signal on the base of Q13 which is sufficient to turn Q13 on. When Q13 conducts, a TRW pulse passes through R11, sets CM12, and provides an advance current to the frequency divider stepping switch through lead 4. The next output from Q11 resets CM12 which induces a voltage on the base of Q12, turning it on.

13.04 A conducting Q12 provides a TRW current pulse through R11 which sets CM11 and provides an advance current to the frequency divider through lead 3. The third pulse from Q11 finds the same condition in the frequency divider distributor as the first pulse did, and hence alternating advance pulses are supplied to the frequency divider stepping switch via leads 3 and 4.

13.05 When the converter is idle, C1 is charged through R66 and R68 to -27 volts. This negative voltage is coupled through diode CR97 to the base of transistor Q35. The emitter of Q35 is held at -18.7 volts supplied on lead 1 from FS10. Thus Q35 is reverse biased by 8.3 volts. Since Q35 is not conducting, Q14 is turned off and its base emitter junction is reverse biased by 6 volts developed across voltage regulator diode CR96 and resistor R63. Thus, the DR relay in the interface circuit is not operated at this time. When a digit is dialed and read out of the converter memory, transistor Q11 begins firing at an 80-pps rate. Each time Q11 fires, it discharges C1 through transistor Q11, diode CR98, and

resistor R69. When Q11 first fires and C1 is discharged, the base of Q35 becomes forward biased and Q35 conducts. The conduction of Q35 forward biases transistor Q14, which also conducts and operates the DR relay in the interface circuit. This operation of the DR relay occurs approximately 100 msec before the first digit is outpulsed. Transistor Q11 continues to fire as long as there are digits stored in the converter memory or as long as there are digits being processed. Thus Q14 continues to conduct and the DR relay remains operated. After the last digit of a call has been processed, Q11 stops firing. Capacitor C1 begins to charge through R68, CR97, and Q35 to -18.7 volts, and through R68 and R66 to -27 volts. When the junction of R68 and R66 reaches -18.7 volts, the current through R66 and R68 continues to charge C1 to -27 volts. When C1 has charged sufficiently, the base emitter junction of Q35 is again reverse biased, which turns Q35 off. When Q35 turns off, it turns Q14 off, which releases the DR relay. The charging time constant of the RC circuit composed of C1, R68, CR97, and R67 was chosen to provide 800 msec between the last pulse of a digit and the release of the DR relay.

14. FREQUENCY DIVIDER STEPPING SWITCH - FS8

14.01 The frequency divider stepping switch consists of cores CM45 through CM52, diodes CR36 through CR45, and varistor RV4. The reset current sets cores CM45 through CM51 and resets CM52. An advance pulse arriving from the frequency divider distributor on lead 4 sets CM52. This switching induces a voltage in the 11-turn winding on CM52. A current flows through the 3-turn winding of CM45, resetting it, and then through CR36 and RV4 to -27 volts. The second advance pulse arriving from the frequency divider distributor via lead 3 sets CM45. The voltage induced in the 11-turn winding of CM45 by this switching action drives current through CR37, CM47, and RV4, resetting CM47. The alternating advance pulses cycle this resetting action through the eight stages as long as advance pulses are present. Current flows in each transfer winding once every eight advance pulses. The current in the transfer winding linking CM51, CM52, and CR43 provides a 10-pps signal to the translation distributor on lead 5.

15. TRANSLATION DISTRIBUTOR - FS3

15.01 The translation distributor consists of R9, Q8, Q9, CM8, and CM9. The converter reset pulse sets CM8 and resets CM9. An output pulse from the frequency divider stepping switch on lead 5 resets CM8, which induces a positive signal on the base winding of Q9. This positive signal turns Q9 on and provides the advance current pulse for the translation shift register on lead 9 as well as setting CM9. The second pulse from the frequency divider stepping switch resets CM9. When CM9 is switched to reset, Q8 is turned on and conducts an advance current pulse to the translation shift register on lead 8 as well as setting CM8 and CM10. The third frequency divider stepping switch output pulse sees the same condition in the translation distributor as the first pulse did. Hence, the advance pulses to the translation shift register are supplied alternately at 5 pps each.

16. TRANSLATION SHIFT REGISTER - FS15

16.01 The translation shift register consists of cores CM65 through CM80, diodes CR78 through CR94, and varistor RV3. Cores CM66 through CM80 are initially set by the converter reset current. Operation of the translation shift register for a 9 digit is now described. CM69 and CM66 are reset by a current pulse from the output amplifiers through leads 11 and 15, respectively. An advance pulse from the translation distributor on lead 9 sets CM66. A voltage induced in the 3-turn winding on CM66 causes a current to flow through CR78 and through the 1-turn winding on CM65. CM65 is reset by this current. The TR pulse following the advance pulse sets CM65 via lead 3. This switching action induces a voltage in the 4-turn winding of CM65 which triggers the dial pulse generator. When the second advance pulse occurs on lead 8, it sets CM69. This action induces a current in the 11-turn winding of CM69 which resets CM70, passes through CR81, and resets CM65. The TR pulse, following the advance pulse, sets CM65 and induces an output in the 4-turn winding which triggers the dial pulse generator.

16.02 The advance pulse on lead 9 now sets CM70 which induces a transfer current to reset CM71 and resets CM65. A TR pulse again produces a dial pulse output. Hence, in the translation shift register, an input signal results in a single reset core in CM67 through CM80. This reset condition of a core is shifted through the translation shift register to produce dial pulse outputs. An 8 written into CM69 is shifted through eight stages which produce dial pulses and five stages for interdigit timing. When 400 msec of interdigit timing is completed, a voltage induced in the 11-turn winding of CM80 causes a current to flow through CR94 and out on lead 20 to FS3. One hundred msec later FS3 generates an end-of-digit signal to indicate that the next digit can be translated, and 100 msec after the end-of-digit signal is generated, the next digit begins to be pulsed out. An even digit causes operation in a similar manner except CM66 is not reset. The operation of the translation shift register is slightly different for a digit 1. In this case, CM77 is reset

in addition to CM66. Resetting of CM77 starts the interdigit timing in the last four stages, CM77 through CM80.

17. DIAL PULSE GENERATOR - FS11

17.01 The dial pulse generator is a monostable multivibrator. It extends the 1-usec trigger pulse to 60-msec break and 40-msec make of the PLS relay contacts. The correct break-make ratio is adjusted by means of potentiometer R32.

17.02 When there is no pulsing, Q19 is cut off and Q20 is in saturation. The drop across varistor RV2 provides the reverse bias on the base of Q19 to keep it cut off. Capacitors C4 and C5 charge to the supply voltage through R30 and the base-emitter junction of forward-biased transistor Q20.

17.03 A positive pulse is applied through the 4-turn winding on CM65 via lead 1 through CR52 to the base of Q19. This causes Q19 to begin conduction, causing the collector of Q19 to go negative. This negative-going voltage is coupled to the base of Q20 through the C4, C5 parallel combination and diode CR51, decreasing the base current into Q20 which starts to bring it out of saturation. The collector of Q20 starts going more positive. A portion of this positive-going voltage is coupled to the base of Q19 through R34, thereby increasing its positive potential. This results in a rapid switch in the state of both transistors. Q19 is driven into saturation and Q20 is cut off. Since the parallel combination of C4 and C5 was initially charged to nearly the full supply potential, the anode of CR51 is at a negative potential almost equal to twice the supply voltage.

17.04 Capacitors C4 and C5 begin to discharge through resistors R31 and R32 and the low-saturation resistance of Q19. The discharge time of this capacitor and hence, the percent break of the PLS relay, can be varied by adjusting R32. When the base voltage of Q20 becomes slightly positive, Q20 will again begin to conduct. The collector potential of Q20 will increase negatively. This reduces the current supplied to the base of Q19 through R34 and drives Q19 into cutoff. Q19 is then at cutoff and Q20 is in saturation. This stable condition is maintained until the next trigger pulse.

17.05 The PLS relay is the load on the output of Q20. When the converter is seized, power is applied to it and Q20 goes into saturation operating the PLS relay. This relay releases when a trigger pulse causes Q19 to conduct, since the conduction of Q19 takes Q20 out of saturation.

18. PRETRANSLATION - FS14

18.01 The pretranslation circuit is designed to determine from the first digit dialed the total number of digits in the call, up to a maximum of four. After the predetermined number of digits is pulsed out, a signal is sent to the rotary dial repeating and interface circuit to release the converter. Strapping is used to provide the desired pretranslation. This information is given in CAD 2 and its associated note.

18.02 The pretranslation circuit input consists of bit-current pulses on leads D1 through D0 from the TOUCH-TONE receiver. Diodes CR58 through CR77 prevent feedback from the pretranslation circuit to the converter memory and vice versa.

18.03 These inputs are energized each time a digit is dialed. To limit pretranslation to the first digit of a call, an enable gate is employed. It consists of Q29 and CM64. Upon seizure of the converter, CM64 is set by the reset current. When the first digit is dialed, a start write signal on lead 13 from the write control resets CM64 and turns on Q29. A bit-current pulse can then pass through one of the number-of-digits cores CM60 through CM63. Subsequent start write pulses cannot turn on Q29 because CM64 is already reset. Only after the converter is released and again seized can Q29 turn on.

18.04 As an example, suppose a first digit 5 is programed to release the converter after two digits are dialed. For this example, connector pin 20 will be cross-connected to connector pin 68. Then, when a 5 is dialed as a first digit, Q29 is triggered and a bit-current pulse will flow through lead D5, core CM62, R58, and Q29 to -27 volts. Core CM62 will be reset by this current, thus indicating that 5 is to be a 2-digit call.

18.05 After each digit is outpulsed, an end-of-digit pulse appears on lead 5. Since CM62 was reset by the bit-current pulse, it is now set by the end-of-digit pulse and Q32 is turned on. When Q32 turns on, a TRW pulse flows through R59, Q32, and CM63 to -27 volts. Core CM63 is reset by this pulse. The next end-of-digit pulse on lead 5 sets CM63 and turns Q33 on. Ground is applied to lead 14 whenever the converter is seized. Diode CR95 is a voltage regulator diode and, in conjunction with R60, serves to keep the base emitter junction of Q34 reverse-biased by about 6 volts. When Q33 is turned on, the base of Q34 is forward-biased and Q34 conducts. When Q34 conducts, a signal is transmitted on lead 27 to the rotary dial repeating and interface circuit, which releases the converter through a break contact on the EC relay.

19. TIME-OUT CIRCUIT - FS10

19.01 When the converter is idle, the rotary dial repeating and interface circuit applies ground to lead 3 and battery, through a resistor, to lead 6. This charges the C2 and C3 capacitors to -48 volts. When the converter is seized, the above-mentioned ground and battery are removed. Lead 3 now has battery supplied to it through a resistor. This drops the negative side of capacitors C2 and C3 to -96 volts. The rotary dial repeating and interface circuit also closes lead 6 to lead 5 and lead 7 to -48 volts. The emitter of Q17 is biased to -18 volts by a voltage divider made up of R22, R23, and R24. This makes CR48 reverse-biased by approximately 78 volts. The time-out circuit starts timing as soon as the converter is seized. The rotary dial repeating and interface circuit closes through several leads to start the timing sequence.

19.02 Capacitors C2 and C3 now start to discharge toward ground through R29. After 10 seconds, the voltage across C2 and C3 reaches the emitter potential of Q17, which is -18 volts, forward-biasing CR49. This turns on the two-stage amplifier, consisting of Q17 and Q18. The conduction in Q18 operates the DO relay. With Z option, the operation of the DO relay stores a 0 in the first storage slot of the coincident fluxor memory. This digit is then read and pulsed out and the pretranslation circuit releases the converter. With Y option, the operation of the DO relay supplies a ground directly to lead 13 of the rotary dial repeating and interface circuit, releasing the converter and cutting the station through to the first selector.

19.03 If outpulsing had occurred before the 10 seconds were up, the rotary dial repeating and interface circuit would have recharged C2 and C3 to -96 volts. At the end of outpulsing, these capacitors again start discharging toward ground. After 10 seconds, the DO relay is operated in the same manner as before. However, once a digit is pulsed out, the converter does not dial the digit 0. In this case it cuts the station through and then it releases.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

None.

2. FUNCTIONAL DESIGNATION

None.

3. FUNCTIONS

3.01 Convert the output of the relay closures in the TOUCH-TONE Receiver Circuit into dial pulses.

3.02 Store the digits and pulse them out in the correct order at a 10-pps rate.

3.03 Pretranslate on certain codes and release the converter immediately after pulsing is completed.

3.04 Time out on codes which are not pretranslated to release the converter a specified time after the last digit is pulsed out.

4. CONNECTING CIRCUITS

(a) TOUCH-TONE Receiver Circuit - SD-67027-01 (typical).

(b) Interface Circuit - SD-1E054-01, or SD-66891-01 (typical).

(c) TOUCH-TONE Calling Receiver Applique Circuit - SD-66888-01.

(d) Central Office Digit Class and Pad Control Circuit - SD-1E033-01.

(e) Early Cut and Double Registration Control Circuit - SD-1E061-01.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 On FS4, R4 is rewired from position in series with p-emitter of Q2 to position in series with n-emitter. Lead 28 is wired to n-emitter of Q2. The pretranslation output signal is brought out to the interface circuit on a lead separate from the Y option time-out lead. These changes are made to allow the converter to provide desired signals to interface circuits having the Early Cut and Double Registration Control Circuit as a plug-in circuit pack.

D.2 Cross-Connection Note 401 and the associated table are changed to provide for pretranslation cross-connecting to be done on the connector.

D.3 The 27D transistor is substituted for all 27A transistors to improve the circuit operation reliability in applications where large switching transients may be present in the associated interface circuit.

D.4 CR49 is changed from 458A diode to 446F diode to provide better protection against transient damage of transistor Q20.

D.5 R20 and R21 are changed from 133 ohms to 215 ohms to extend the service life of CR39 by reducing its power dissipation. The winding of CM59 from terminal 4 of FS13 is increased to 10 turns as part of this change.

D.6 R60 is changed from 10K, 146C to 51.1K, 237A to reduce power dissipation in R60.

D.7 CR50 is deleted.

D.8 R2 is changed from 1250 ohms to 1240 ohms in order to specify standard value.

D.9 The windings of CM8 and CM9 from terminal 12 on FS3 are changed from 2 turns to 3 turns. R64 is changed from 20,000 ohms to 5620 ohms. R65 is changed from 3160 ohms to 2050 ohms. R63 is changed from 10,000 ohms to 51,100 ohms. R11 is changed from 34.8 ohms to 38.3 ohms. RV4 is added to FS8. These changes are made to improve circuit operation reliability at high temperatures (60°C).

D.10 The following errors on the SD are corrected:

(a) CM30 was not labeled on FS5. The terminal labeled 61, 3A8 is corrected to read terminal 59 on FS6.

(b) CR44 was incorrectly labeled CM44.

(c) The terminals on resistors R32 and R57 were labeled incorrectly.

(d) The lead from terminal 5 of FS13 was incorrectly designated.

D.11 Sheet H-1 is changed to provide an accurate block diagram.

D.12 In order to correct errors in Circuit Note 101, the battery voltage range is changed from 48-50 volts to 44-52 volts. To correct an error in Circuit Note 102, the option routing the call to the attendant should read option Z. The option not routed to the attendant should read option Y.

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