

22

COMMON SYSTEMS  
 13A ANNOUNCEMENT SYSTEM  
 CIRCUIT FOR RECORDING AND  
 REPRODUCING DIAL FACILITIES  
 MANAGEMENT ANNOUNCEMENTS

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This circuit provides means for recording and reproducing dial facilities management announcements.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 13A is an all-electronic multichannel announcement system that uses adaptive delta modulation to convert the analog voice signal into a digital format which is then stored electronically. In earlier systems the digital data was stored in 29A bubble memory. In new systems the digital data is stored in random access memories (RAMs). The system can handle a maximum of eight channels, with each channel announcing a specific recorded message.

2.02 Handset jacks are provided to accept a handset for local recording. These jacks may also be used for connection of a tape recorder to dub announcements from precorded KS-22550 cassette tapes. A KS-22566,L2 interface unit is required to connect the tape recorder to the handset jacks.

2.03 Terminals are provided for connections to a dedicated circuit for remote recording.

2.04 The 13A has three common circuit packs that control the system. The UD1 Power Supply converts the -48 Vdc into the voltages required. The UD2 Encoder Driver digitally encodes the speech during recording and provides the field drive for the magnetic bubble packages used in earlier systems. New systems use random access memories (RAMs) which require no field drive. The UD3 Timing and Control circuit pack provides the logic for system timing and control. UD3B timing and control replaces UD3 (rated Mfr Disc) but provides the same control functions.

2.05 In addition to the above common circuit packs, there are three kinds of message module circuit packs for storage and announcement of the recorded message. The three kinds of message modules can be intermixed in any combination to occupy the eight channel positions available.

2.06 The UD4 (3-24) VML (Variable Message Length) message module is the storage and playback circuit for an audio recording of 24 seconds maximum. The length of storage can be varied in 3-second increments from 3 to 24 seconds.

2.07 The old style UD4 (series 1-14) stored digitally encoded speech in two 29A bubble memories. The new model UD4 (series 15 and higher) replaces the old and uses random access memories (RAMs). The old UD4 is now manufacture discontinued but is perfectly compatible with the new

system. The bubble memory UD4 will still be used in existing systems; any replacement of old UD4s will be with the new RAM-type UD4.

2.08 The UD5 FML (Fixed Message Length) message module is a circuit for storage and playback of an audio recording 12 seconds long. The 12-second period is fixed, and a shorter recording will be followed by a silent period up to the 12-second limit. UD5 is rated Mfr Disc and replaced by UD4 and UD6.

2.09 The UD6 (3-12) VML (Variable Message Length) message module functions in the same way as UD4, except that the recording is limited to 12 seconds.

2.10 The old style UD6 (series 1-14) stored digitally encoded speech in one 29A bubble memory. The new model UD6 (series 15 and higher) replaces the old and uses random access memories (RAMs). The old UD6 is now manufacture discontinued but is perfectly compatible with the new system. The bubble memory UD6 will still be used in existing systems; any replacement of old UD6s will be with the new RAM-type UD6.

2.11 Local controls are POWER OFF, RECORD, FIELDS DOWN, CHANNEL ACCESS, MESSAGE LENGTH ADJUSTMENT, and OUTPUT LEVEL ADJUSTMENT. The local indicators are POWER OFF, CURRENT LIMIT, CUT-THROUGH, REQUEST RECORD, FIELDS DOWN, DIGITAL VOICE ALARM, CHANNEL ACCESS, and VOICE ALARM.

2.12 Each channel provides:

- (a) A transformer-coupled audio output on leads T1( ), R1( )
- (b) A contact closure (cut-through) to indicate the beginning of the message
- (c) A contact closure for voice alarm
- (d) A channel access lead requiring a ground to put the channel in a ready-to-record mode for remote recording.

2.13 The UD4 and UD6 circuits also provide:

- (a) A start lead requiring a closure to ground to start the message output or to start the channel for remote recording
- (b) MU2, 3, and 4 leads for a contact closure between MU3 and 4 during the announcement and a contact open during the silent period at the end of the announcement
- (c) MU2 and 3 combination for the opposite state to the MU3-4 pair
- (d) An STP lead which is grounded during the announcement and momentarily open at the end of the announcement
- (e) An LIM lead for the opposite state to the STP lead.

SECTION II - DETAILED DESCRIPTION

1. UD1 - POWER SUPPLY

GENERAL DESCRIPTION

1.01 UD1 is a pulse-width modulated dc to dc converter. It converts the -48V to +15.75V at 1.6A, -15.75V at 0.5A, and +5.2V at 3.2A. Also, two low-current supplies, -4V at 100 mA and -8V at 100 mA, are derived from the -15.75V. When supplying these currents, which are a maximum for a fully equipped 13A, UD1 draws between 1.1 and 1.6A from the -48V supply. This depends on the combination of UD4/UD6 board types used. For all new RAM type boards, the current drawn by UD1 is 1.1A; for the bubble memory-type, the current drawn is 1.6A. For a mixture of RAM-type and bubble memory-type UD4/UD6 boards, the current drawn by UD1 will be in the range 1.1-1.6A. The voltage outputs have a tolerance of +5 percent, except for the +5V supply. It has a tolerance of +3 percent.

1.02 Circuitry is also provided for electronic shutdown if currents exceed the specified values, or if the voltages exceed their tolerance. Also, the +5V and +15V outputs are monitored, and both must be higher than the minimum values to result in a high level on the PWR SENSE output.

1.03 The UD1 circuitry described below is identical as it applies to the old and new UD4/UD6 boards. Any references that are specific to a particular type (RAM or bubble memory) are explicitly stated.

CIRCUIT DESCRIPTION

1.04 The -48V input is fused by F1, goes through switch S1 and a low-pass filter, formed by L4 and C33, to attenuate any noise on the supply. CR10 prevents the voltage at the filter output from going more than one diode drop below the input voltage. The supply must be within the range of -42.5V to -52.5 for UD1 to perform properly. The -48V powers the pulse-width modulator IC1. The output of IC1 is negative-going pulses at a 20-kHz repetition rate. These appear alternately on pins 21 and 25 of IC1. When a pulse is present on pin 21, transistors Q1, Q2, and Q3 are turned on, and current flows from ground through one-half of the primary of T1 to the -48V supply. Similarly, when a pulse is present on pin 25 of IC1, transistors Q4, Q5, and Q6 are on and current flows in the other half of the primary of T1. The output of T1 on winding G, H, J is full-wave rectified to provide both the +15.75V and -15.75V supplies. These outputs are filtered by L1, C6, C8 and L2, C12, C14, respectively. The other secondary winding of T1 is similarly rectified and filtered to provide the +5.2V output.

1.05 The output voltage regulation is accomplished by feedback of the +5V output to IC1 through R17, R16, Q8, and R15. IC1 controls the width of the output pulses on pins 21 and 25 in order to maintain the +5V output. Regulation of the +15V and -15V outputs is accomplished indirectly via the turns ratios of the secondaries of T1.

1.06 C39 and R40 provide ac feedback for a soft turnon of the converter when power is applied. When UD1 has reached steady-state operation, these components no longer affect the voltage regulation.

1.07 The power supply will shut down electronically if the current drawn from the -48V is excessive. The voltage across R33 indicates the current in the -48V RTN lead. As the current drawn increases, the voltage at pin 5 of IC2 becomes more negative. If this voltage goes below the 1.36V present on pin 14 of IC2, Q12 conducts, causing Q7 to turn on. This turns on current-limit LED CR7 and shuts down IC1, which shuts down the power supply. To restart the supply, power must be turned off at switch S1 and then turned on. In a 13A system, each message board (UD4, 5, or 6) adds a 4.64-ohm resistor in parallel with the current-sensing resistor, R33. This raises the current at which shutdown will occur. Thus, a fully equipped 13A will limit at a higher current than will a 13A with only one message module.

1.08 CR15 serves as protection for R33 and the message module resistors. During normal functioning of UD1, CR15 does nothing. If a component failure occurs, such as a short-circuit in Q3 or Q5, current will flow through CR15. Then, CR15 protects the resistors by not allowing the voltage across them to go above 4.7 volts.

1.09 If the output voltages are too high, the supply will shut down. If the +15V supply exceeds 16.9V, or the +5V supply exceeds 5.45V, IC5C or IC5D, respectively, will go low (-15V). Q15 then conducts, Q7 turns on, and the supply shuts down via the same circuit used for over-current shutdown. The indication of overvoltage shutdown is the same as that for overcurrent, namely, CR7 is lit.

1.10 The PWR SENSE output is high (+15V) when the output voltages are high enough for the 13A system to function correctly. In this state, IC5A and IC5B are high, Q17 is off and Q18 is on. If the +15V supply falls below 14.6V, IC5A goes low. If the +5V supply falls below 4.9V, IC5B goes low. Either, or both, cause Q17 to conduct and Q18 to turn off, and the PWR SENSE output goes low. In a 13A system, correct operation of this circuit is necessary for retention of messages in the memory during loss of power.

2. UD2 - ENCODER DRIVER

## GENERAL DESCRIPTION

2.01 UD2 performs two separate and distinct functions:

(a) It conditions input speech and encodes the speech into a digital pattern. The conditioning of the speech involves conversion of the differential input into a single-ended signal, automatic gain control, high-frequency preemphasis, and low-pass filtering. Encoding of the conditioned speech is done at a rate of 24K bits per second via adaptive delta modulation.

(b) It generates and amplifies two sinusoidal waveforms which are used to drive the rotating fields of the 29A memory. The frequency of the sinusoids is 48 kHz, and the outer coil drive (OCDR) leads the inner coil drive (ICDR) by 95 degrees. Provision is made for starting and stopping the sinusoids under control of two input leads, SOC and SIC.

2.02 The UD2 circuitry described below is identical as it applies to the old and new UD4/UD6 boards. Any references that are specific to a particular type (RAM or bubble memory) are explicitly stated.

## CIRCUIT DESCRIPTION

2.03 The speech input is the differential between VOICE IN and VOICE IN RET. The proper level of speech input is between -40 VU and -10 VU. R1 and R4 provide the 60 mA of current for a carbon microphone. IC1A does the conversion from differential to single-ended signal. IC1B and IC1C, together with Q11 and Q12, form the automatic gain control. The AGC voltage is generated at C15 and controls Q11 and Q12, which are used in the inverted mode. C9 and R16 form a high-pass filter with a -3 dB point at 10 kHz. This provides the high-frequency preemphasis. IC1D and associated components form a three-pole low-pass filter with a -3 dB point at 2.8 kHz. IC5D and Q8 provide a squelch of the input signal if the level is too low, thus attenuating background noise in the absence of an input signal. At this point, the conditioning of the input speech is complete and the signal is fed into the adaptive delta modulation encoder by R25.

2.04 The adaptive delta modulation (ADM) encoder takes the difference between the input speech from R25 and the existing ADM description of the speech from R35 and R37. If the difference is positive, the ADM takes a positive step in order to more closely approximate the input signal. IC5B functions as a comparator and determines whether the next step will be positive (IC5B output is high) or negative (IC5B output is low). This is the binary encoding of the input speech. It is latched by IC4 and output on pin 22. IC5C, R32, R33, R34, and C21 decode the data back

into analog form for comparison with the input speech. The input signal DCLK determines the data rate of the ADM encoding. It has a 24-kHz repetition rate, and is high for 5  $\mu$ s.

2.05 The encoder also adapts to the amplitude of the input signal. If the input signal is large, the ADM will be unable to keep up with the rate of change, and the digital data will have a large number of ones or zeros in a row. The ADM uses this information to increase the step size. Pin 17 of IC4 is an output which is low only when there are four ones or four zeros in a row in the digital data. When pin 17 is low, Q1 is on and charges C22 through resistors internal to IC6. IC6 converts the voltage at pin 6 into a current at pin 24. This current controls the size of the step taken by IC5C.

2.06 In a 13A system, a data pattern of 15 ones is a special pattern, known as a preamble. This pattern must not occur in the encoded speech. IC7, IC8, IC9, and associated gates inhibit both 15 ones and 15 zeros from occurring in the ENCODE output. If there are 15 ones in a row, IC8 generates a carry output which changes a one to a zero in the middle of the 15 ones. Similarly, IC9 changes a zero to a one in the middle of 15 zeros.

2.07 The 48-kHz sine waves are synthesized by IC14, IC15, IC16, and R82 through R111. After power up, the circuit is initialized by clocking SWC for at least 24 cycles while holding CSR high, which clocks all ones into the shift registers. CSR is low during normal operation. When input CSR is low, the shift registers alternately shift in 16 ones followed by 16 zeros. A weighting factor is applied to each shift register output by the corresponding resistor. Fifteen outputs are combined to form each sine wave. The positive peak in a sine wave occurs when all the 15 outputs are high. This occurs on two successive clock cycles, since 16 ones are shifted through the registers. As the 16 zeros are shifted in, the half of the sine wave with a negative slope is being formed. Thus, 32 clock cycles are necessary to generate one cycle of a sine wave. Because they differ by 8 positions of the shift register, OCDR1 leads ICDR1 by 90 degrees. Both signals are 12 volts peak to peak, and they have a 6-volt dc component. Since the amplitude of the generated sinusoids depends on the shift register power supply voltage, IC22 is used to provide a precise voltage to power these ICs.

2.08 Once the sinusoids are generated, each goes to a power amplifier. C33, C34, R41, and R42 remove the dc component and provide high-frequency filtering of OCDR1. IC17 is a unity gain stage which provides a low-impedance source. IC18A and IC18D switch the input to the power amplifier between the output from IC17 and ground, respectively. Only one of the two switches is on at one time. The state of

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the switches is controlled by SOC. The power amplifier, consisting of IC19, Q3, Q4, Q7, Q8, Q9, and associated components, provides the necessary gain and low output impedance needed to drive the outer coils of the 29A memories. Up to 16 memories can be driven by this amplifier. SB1 provides the inductance necessary to prevent unwanted oscillations at high frequencies.

2.09 The circuit for driving the inner coils is similar to the outer coil driver. The two circuits have different phase shift capacitors, C34 and C50, in order that the OADR waveform leads the IADR waveform by 95 degrees. Both OADR and IADR have a peak-to-peak amplitude of 22.9V minimum and 25.4V maximum. Q18, Q19, and Q20 ensure that there are no perturbations on the OADR and IADR outputs during power up and power down.

2.10 While the OADR and IADR outputs are present on all series UD2, they are not used in new systems employing RAM memory.

### 3. UD3 and UD3B - TIMING AND CONTROL

#### GENERAL DESCRIPTION

3.01 In the 13A, UD3 controls the rotating field generation and provides bubble memory and RAM memory timing signals. It also controls the sequencing of the bubble memories from one chip to the next, and provides placement of the recording of new messages. UD3 also generates a DVA, or digital voice alarm, if the data in the 29A memories is incorrect. All the outputs from UD3 are TTL signals, except for REC RLY 1 and REC RLY 2. These two leads provide a contact closure during a record interval.

3.02 The functions of UD3B are identical to those of UD3 except for those described below.

3.03 The UD3/3B circuitry described below is identical as it applies to the old and new UD4/UD6 boards. Any references that are specific to a particular type (RAM or bubble memory) are explicitly stated.

#### CIRCUIT DESCRIPTION

3.04 Y1 is a 9.216-MHz oscillator which provides the basic clock for UD3 and the 13A. IC6A and IC6B divide this by 3. The output of IC6 clocks IC22 and IC16, which form the address inputs for IC23. IC23 is a read-only memory (ROM) with 64 eight-bit words. The addresses of IC23 are cycled through in consecutive order. There is one cycle through the ROM for each rotating field cycle. The ROM determines the timing of signals needed to operate the 29A bubble memory. These signals are REPL, REPH, DET RST, GEN, and STROBE. DET RST and REPH are not used for message modules employing RAM memory. It also controls the timing of CSR, SOC, and SIC, which control the sine wave generation of UD2. The

outputs from the ROM are latched by IC12 and IC29. Via the SEL (pin 10) input, IC29 also provides blanking of the timing signals on every other rotating field cycle.

3.05 When power is applied to UD3, CLR1 initializes the logic by clearing IC10A and IC13B. After a 640-microsecond delay, IC15B is enabled and IC10A is set under control of the ROM output B2. This causes output CSR to go low. It remains low until power is removed and reapplied. Via IC15D and IC8B, CLR1 sets IC10B during power up. After a one-millisecond delay, IC15C is enabled and the output SOC goes low at the leading edge of the ROM output B1. IC10B is cleared at the trailing edge of B1. IC10B cleared:

- (a) Keeps SOC low via pin 2 of IC9A.
- (b) Causes the output SIC to be low.
- (c) Enables the outputs REPL, REPH, DET RST, and STROBE via IC11D pin 14.

This controls UD2 to turn on the rotating fields (OADR and IADR). IC10B remains cleared until a field-down signal is generated by IC13B.

3.06 IC13B is cleared upon powering up by CLR1. When input PWDN goes high, IC13B is set if IC10A is high. This is typically the case, as described above. IC13B set:

- (a) Lights the FIELD DOWN INDICATOR, CR1.
- (b) Disables gates IC15B and IC15C.
- (c) Enables the timing signal BO from the ROM to set IC10B.

When IC10B is set, outputs SIC and SOC go high. In a 13A system, this controls UD2 to turn off the rotating fields (OADR and IADR).

3.07 A 24-kHz clock signal, generated by IC16 and buffered by IC44G, is used to clock a 20-stage binary counter, consisting of ICs 31, 43, 36, 41, and 46. This counter normally cycles in sequence with the chips in a 29A bubble memory. Since each bubble memory chip contains 68,121 bits, (each RAM contains 65,536 bits) the counter also cycles every 68,121 counts of the 24-kHz clock. This is done by resetting the counter to all zeros after a count of 68,120 is reached. The signal which resets the counter is CNT68120, formed by IC42A, IC42B, and IC37C. This sets the flip-flop formed by IC38A and IC38B, which puts a low on the load inputs to the counter, loading in all zeros.

3.08 CNT68120 is buffered by IC44A and IC44B to form the CHCLK output. This output is used by UD4 and UD6 to switch from one 29A memory chip to the next. It is 20 microseconds long and occurs every 2.84 seconds. This signal is

used as a timing signal on message modules employing RAM.

3.09 Various other states of the counter are decoded and used to create signals. Some of these are used for timing internal to UD3, others are outputs which are used mainly by UD4, UD5, and UD6. One such signal is CNT47. At count 68120, IC48A is preset. When the CP output from IC31 and the QB output from IC43 both go high for the first time after count 68120, the counter is at count 47. This output also clocks a zero into IC48A at the trailing edge of CNT47. This disables IC32C from putting out more pulses until after IC48A is preset again at count 68120.

3.10 Output LIMRST is formed in a similar manner. It occurs at count 4096. Output CT GATE is formed by IC27A. It is low from count 32K to count 0, which is a time duration of about 1.5 seconds.

3.11 Output STENAB is formed by IC47A, IC47B, IC42C, and IC38D. At count 68120, both IC47A and IC47B are cleared. At count 29, IC47B is set by IC42C and STENAB goes low. At count 49K, IC37A sets IC47A and STENAB goes high. It remains high for the rest of the cycle of the counter.

3.12 IC48B is set by IC37B at count 68117. It is reset at count 15 by the carry output of IC31. The output from IC48B is used to create several signals which occur during the interval from count 68117 to count 15. It enables IC45B, which creates a pulse at count 14. It also enables IC45C. The other input to IC45C comes from IC30, which is a BCD-to-decimal decoder. It is low when inputs at pins 13, 14, and 15 are high and the input at pin 12 is low. By combining these two inputs, IC45C is high only during count 68119. Thus, IC13A is set at count 68119. It is reset by IC21B at count 13. The input at pins 10, 11, and 12 of IC21B ensure that IC13A remains reset from count 15 to count 68117.

3.13 UD3 also controls the recording of new messages. A recording process is begun by a momentary closure of the LOCAL RECORD SWITCH, or by a momentary closure between the inputs REM REC and REM REC RET. The closure sets IC25A which lights CR2, the RECORD REQUEST INDICATOR. In order to place a new recording in step with existing messages, the UD3 may remain in this state for up to 15 seconds before the recording starts.

3.14 In UD3B the closures described above set the record request flip-flop formed by IC7B and IC7C which lights the RECORD REQUEST INDICATOR.

3.15 At the end of the record request, all inputs to IC35C go high, and a 300-microsecond pulse is output on the ERASE output. At the end of the ERASE pulse, IC25B is set. This locks out IC35C from issuing further pulses. It also puts a

high on the D input of IC40A. This is clocked into IC40A at the leading edge of CNT68117. IC40A going high:

- (a) Puts a low on output SOR (start of record) which is used to initialize logic on UD4 or UD6 circuit packs.
- (b) Puts a high on the clock lead of IC25A, which clears IC25A and extinguishes the RECORD REQUEST INDICATOR.
- (c) Selects the PREAM input of IC21A.
- (d) Sets IC40B, the record flip-flop.

IC40B going high:

- (a) Puts a low on the REC output.
- (b) Operates relay KREC.
- (c) Lights CR3, the RECORD INDICATOR.

The recording of a new message begins at this time. The message starts with the preamble.

3.16 In UD3B at the end of the record request sequence all inputs of IC35C are high, causing a low at its output. This low appears at the D input of IC25B. When CB8 goes high, the Q output of IC25B goes low, generating the leading edge of the erase pulse and sets IC25A causing the Q output to go high. Pin 10 input of IC35 is now low, which disables the record request function and makes the D input of IC25B high. The next positive going CB8 pulse causes the Q output of IC25B to go high ending the erase pulse. The duration of the erase pulse is 667 microseconds. When CNT68117 occurs:

- (a) SOR (START OF RECORD) goes low which is used to initialize logic on UD4 or UD6 circuit packs.
- (b) The record request flip-flop is reset which extinguishes the RECORD REQUEST INDICATOR.
- (c) LOCAL or REM RECORD REQUEST is disabled, preventing any closures on these functions from setting the record request flip-flop during the recording interval.
- (d) The PREAMB input of IC21A is selected.
- (e) The REC output is enabled.
- (f) Relay KREC operates, and CR3 the RECORD INDICATOR is lighted.

The recording of a new message begins at this time. The message starts with the preamble.

3.17 A preamble is 2 zeros followed by 15 ones followed by a zero. The two zeros in the preamble are generated because

the PREAM input to IC21A stays low for two counts, until count 68119. The PREAM input then goes high and stays high until count 13. This generates the 15 ones. The final zero is generated at count 13.

3.18 At count 14, IC45A resets both IC25B and IC40A. Output SOR goes high at this time. Also, the PREAM input of IC21A is disabled and the ENCOD input is enabled. This input comes from the encoder on UD2. At this point, the recording of the preamble has been completed and the recording of the encoded speech begins. For the message modules employing RAM, the preamble is not recorded.

3.19 In a 13A system, different messages may have different lengths. The recording interval must match the message length. This is accomplished with the LST CHP input. When this input goes low, the last chip in the memory is being recorded. At the end of this chip, at count 68117, the output of IC45D goes high. This clocks a zero into IC40B. IC40B going low:

- (a) Causes the REC output to go high.
- (b) Releases the KREC relay.
- (c) Extinguishes the RECORD INDICATOR.
- (d) In UD3B the record request flip-flop is enabled.

This ends the recording interval.

3.20 In UD3B during the interval from CNT65536 to CNT68120 (approximately 108 milliseconds) pin 13 input of IC35C is low. If, during this interval, a closure occurs on LOCAL RECORD REQUEST or REM REC, the record sequence will be disabled. When the next CI interval occurs IC35C will be enabled and the record sequence is started.

3.21 UD3 also has circuitry for initializing logic to a known state upon powering up. IC7A and IC11B form a flip-flop. It has one input, PWRSEN, which is held low during power up. When power is applied to UD3, R44 holds the output of IC7A low. Also, R45 holds the output of IC11B high. When the power supply voltages reach their normal level, IC11B will remain high since both its inputs are low. This puts a high on CLR 41 and a low on CLR1 and CLR2. Also, output PWR OFF is low.

3.22 Since the input PWRSEN is low, the output of IC12A is high. This makes IC11A low, signal PWDN high, and signal CLR3 low. When input PWRSEN goes high, the output of IC12A goes low, and the flip-flop formed by IC7A and IC11B changes state. This puts a low on CLR 41 and a high on CLR1 and CLR2. IC12A going low also causes PWDN to be low and CLR3 to be high. This is the state of the initializing circuitry during normal operation. The circuit will remain in this state until either PWRSEN goes low or the FIELD DOWN SWITCH is depressed.

3.23 If input PWRSEN goes low, the output of IC12A goes high. This puts a high on PWDN and a low on CLR3. The flip-flop formed by IC7A and IC11B will not change state, since pin 6 of IC11B is high. Therefore, signals CLR1 and CLR2 will remain high, and CLR 41 will stay low. If the FIELD DOWN switch is depressed for at least 3 seconds, PWDN will go high and CLR3 will go low at count 14. The other clear signals remain unchanged. Either condition will result in UD3 turning off the rotating fields to the 29A memory. The PWRSEN input will turn off the fields within 21 microseconds. The FIELD DOWN switch will stop the fields within 3 seconds, when count 14 is reached.

3.24 In a 13A, UD3 also provides signals to select memory chips on a UD5. These are the CHIP 1 through CHIP 4 outputs. When power is applied to UD3, CLR3 sets IC34A and clears IC24. This makes CHIP 1 low and CHIP 2, CHIP 3, and CHIP 4 high. Since the input at pin 1 is high, a one is clocked into IC24 at the leading edge of count 68120. At the same time, a zero is clocked into IC34A. This makes CHIP 1 high and CHIP 2 low. At the next count 68120, 2.84 seconds later, the one advances to the QB of IC24. This makes CHIP 2 high and CHIP 3 low. Similarly, another count 68120 makes CHIP 4 low and the others high. Another count 68120 makes CHIP 1 and FMLCT low, lights CR7, and operates relay KCT. The next count 68120:

- (a) Makes the four outputs of IC24 low.
- (b) Clocks a one into IC34A.
- (c) Extinguishes CR7.
- (d) Releases relay KCT.
- (e) Puts a high on FMLCT.
- (f) Leaves CHIP 1 low.

This is the initial state of this circuit. It repeats this sequence until UD3 is powered down.

3.25 UD3B generates signals to select memory chips on UD5, CHP1 through CHP4. When power is supplied to UD3B, CLR3 sets IC34A (Q output high) and clears IC24 (all Q outputs low). All CHP outputs are high at this time. The leading edge of CNT68120 clocks the high on pin 9 input of IC24 to the Q1 output. At the trailing edge a low is clocked to the Q output of IC34A. A high on Q1 output of IC24:

- (a) makes CHP1 low.
- (b) lights the CUT THROUGH INDICATOR CR7.
- (c) makes CT1 high and FMLCT low.
- (d) closes relay KCT.

The next leading edge of CNT68120, (2.84 seconds later) clocks the low now on the pin 9 input of IC24 to the Q1 output. The

high on Q1 now advances to the Q2 output. At this time:

- (a) CHP1 is still low.
- (b) CR7 extinguishes.
- (c) CT1 goes low and FMLCT goes high.
- (d) Relay KCT releases.

The next CNT68120 leading edge makes Q2 go low and Q3 go high. Since Q5 of IC24 is connected to the D input of IC34A, when Q5 goes high on the leading edge of CNT68120, the Q output of IC34A goes high on the trailing edge. The next leading edge of CNT68120 causes the Q1 output to go high and the Q5 output to go low.

This completes the UD5 chip select cycle. This cycle repeats as long as UD3B is powered.

3.26 IC1A is a counter which is clocked on the negative edge of T60 CLK IN. In a 13A system, T60 CLK OUT and T60 CLK IN are connected together. In this configuration, IC1A will change state at the beginning of FMLCT. After 4 cycles of FMLCT, output QD will go high, and 20 microseconds later, the input at pin 4 will go high. This resets IC1A and the QD output goes low. Thus, IC1A puts out a short pulse every 60 seconds at the start of FMLCT.

3.27 In a 13A system, the chip counter must be synchronized with information in the 29A memory. This is especially important when power is turned on to a system which has prerecorded messages. This synchronization is accomplished when the MATCH input to UD3, is generated by the preamble pattern stored in the 29A memory. Synchronization is not necessary when message modules employing RAMs are used. Thus no match signals are generated.

3.28 When power is applied to UD3, the CLR 41 signal is high. This holds the output of IC5A low, which sets IC14A. IC14A set:

- (a) Enables gate IC35A.
- (b) Clears IC34B.
- (c) Puts a low on the DS input to IC3.

At this point, a low on the MATCH input produces a low on the output of IC35A and a high on lead CNTPS. This forces the chip counter to count 48. At the end of the low on the MATCH input, IC14A is cleared. This disables IC35A and prevents future MATCH inputs from affecting the chip counter.

3.29 The remaining circuitry associated with the MATCH input is for the digital voice alarms (DVA). This circuit looks for MATCH inputs that are not coincident with count 47. If there are two or more within a 60-second interval, the

DVA INDICATOR is lit. During power up, IC3 is cleared. Until the end of the first MATCH input, pin 1 of IC3 is low, as described above. The first MATCH thus clocks a zero into IC3. After the first MATCH, pin 1 of IC3 is high. Following MATCH inputs will clock ones into IC3 unless the MODE input, pin 6, is high. The MODE input will be high only at count 47. Thus, MATCH inputs which are coincident with count 47 will not clock IC3; those that are outside of count 47 will clock ones into IC3. Every 60 seconds, the pulse from IC1A will clear IC3 by forcing the MODE input high and clocking zeros from the parallel data inputs into the register. If two ones are clocked into IC3, the QB output goes high. This lights the DVA INDICATOR, CR5, holds the output of IC9C high, and clocks IC4A.

3.30 The action next taken by the DVA circuit is dependent on the state of IC34B. When UD3 is first powered up, IC34B is cleared. In this state, output DT COMP SW is low. In a 13A system, this output is used by UD4, UD5, and UD6 to complement the data going to the preamble detector. If DT COMP SW is low, the preamble detectors are looking for a preamble, 15 ones. If a DVA occurs when IC34B is cleared, pin 10 of IC5A will be high. Pin 12 will go high when the DVA occurs because of the clocking of IC4A. Thus, pin 11 is enabled and the next pulse from IC1A will cause a low on the output of IC4A. The pulse on MLORS sets IC14A. IC14A set:

- (a) Holds IC34B cleared.
- (b) Enables IC35A.
- (c) Puts a low on the DS input of IC3.

The next match will reset the chip counter, as described above. It will also clear IC3 and extinguish the DVA INDICATOR. If no more errors in the MATCH input are detected in the next 60 seconds, IC1A will clear IC4A and the DVA circuit will be restored to its original state. However, if two or more MATCH inputs out of step with count 47 are again detected in the next 60 seconds:

- (a) The DVA INDICATOR will again be lit.
- (b) IC9C will be inhibited, preventing the next pulse from IC1A from clearing IC4A.
- (c) IC4A will be clocked, making the QB output low and the QC output high.

The next pulse from IC1A will be gated through IC5B, putting a low on VATPS. This sets IC14B, which makes output VA TEST low. In a 13A system, this causes a voice alarm from all channels. It also resets IC4A.

3.31 In subsequent 60-second cycles, VA TEST will remain low if the MATCH inputs remain out of step with the chip counter. The DVA INDICATOR will go off and back on when IC4A output QB is high. If

there are no more erroneous MATCH inputs, the DVA INDICATOR will go out, and 60 seconds later, IC4A and IC14B will be cleared and output VA TEST will go high. At this point, the DVA circuit will be reset back to its normal (no error) state.

3.32 If no errors are detected by the DVA circuit, IC34B and output DT COMP SW will change state once every 60 seconds. When IC34B is set, DT COMP SW is high, and the preamble circuits are looking for 15 zeros in the memory output. Two false MATCH inputs within 60 seconds will again light the DVA INDICATOR. This will inhibit IC34B, and DT COMP SW, from changing state. It will also clock a one into IC4A, making the QB output high. Since pin 14 of IC5B is high, the next pulse from IC1A will cause a low-going pulse on VATPS. This will set IC14B and make output VA TEST low. This is similar to the sequence followed when IC34B is cleared, except that the MLORS and the loading of the chip counter are skipped.

3.33 The DVA circuit will keep output VA TEST low as long as erroneous MATCH inputs are present. If the error condition clears, the DVA INDICATOR will go out, and 60 seconds later, IC14B will be cleared and output VA TEST will go high. This sequence is similar to that followed when IC34B is cleared, except that the loading of the chip counter is skipped.

3.34 For message modules employing RAMs, a DVA will never occur because synchronization is not necessary.

#### 4. UD4-3-24 SECOND VML MESSAGE MODULE (SERIES 1-14 USING 29A BUBBLE MEMORY)

##### GENERAL DESCRIPTION

4.01 UD4 stores and plays back up to 24 seconds of speech. It has a variable message length (VML) which can be adjusted from 3 to 24 seconds in 3-second increments. UD4 stores the digitally encoded speech in two 29A bubble memories. It converts the stored information back into analog speech using adaptive delta modulation, and it amplifies and buffers the output to drive up to 500 trunk circuits. Signaling closures and voice alarm are also provided by this circuit pack.

##### CIRCUIT DESCRIPTION

4.02 Most inputs to UD4 are TTL compatible and are low active. Exceptions are:

- (a) OCDR and ICDR require 24V peak-to-peak sinusoidal signals at 48 kHz. OCDR leads ICDR by 95 degrees. These inputs provide the rotating field for the 29A memories. C1 and C2 plus the outer coils of IC14 and IC15 form a parallel resonant circuit at 48 kHz. Similarly, C19, C20, and the inner coils form another resonant circuit at 48 kHz.

- (b) START and CH ACCESS require a contact closure to ground to be active. They may be open when inactive.

Most of the TTL inputs are provided with 10-kohm pullup resistors to increase the noise margins in the high state.

4.03 In a 13A, the CH ACCESS input is used to access the desired UD4 for monitoring or recording. A closure to ground on the CH ACCESS input or operation of CHANNEL ACCESS switch S1 will:

- (a) Enable the ERASE, SOR, and REC inputs. (These are used in the recording of new messages.)
- (b) Operate the CA relay. (This connects the audio to the MON AUD output.)
- (c) Light CR2, the CHANNEL ACCESS LED.
- (d) Enable the LST CHP output.
- (e) Disable the MATCH output.

4.04 When enabled by CH ACCESS, a low on the ERASE input will turn on Q1 and Q2, causing a current of 300 mA to 500 mA to flow in the Z coil (pins 15 and 16) of the 29A memories. This erases all data in the memories.

4.05 When enabled by CH ACCESS, a pulse on the SOR (start of record) input will clear IC3 and IC5A. A low on the REC input will, when enabled by CH ACCESS, put a one on pins 10 and 11 of IC7C. This enables a low on the GEN INFO input to turn on Q4 through Q7. Normal GEN INFO pulse width is 325 ns. This results in a 280-mA pulse of current, 400 ns in duration, in the G (generator) inputs of IC14 and IC15 (pins 22 and 31). Each pulse generates a one in the 29A memory if a replicate pulse is also present.

4.06 Each 29A memory contains four chips. Each chip stores 68,121 bits of information. Both write (generate) and read lines are common to all four chips. The replicate leads act as chip select leads to determine which chip is being written or read. The REPL and REPH inputs determine the timing and shape of the replicate pulse. When REPL is low, Q15 and Q16 are on, and 30 mA of current flows through R34 and the selected replicate leads. At the beginning of the REPL pulse, REPH is also turned on, but for a shorter duration (640 ns). REPH low turns on Q8 and Q9, and 80 mA of current flows through R33. In the replicate lead, the two currents are added for a total of 110 mA.

4.07 Selection of the desired replicate lead is done by IC3, IC4, IC5A, and IC10 through IC13. IC3 is the chip counter. Its count is decoded by IC4. Only one output of IC4 is low at a time. If IC3 is cleared, pin 1 of IC4 will be low. If all outputs QA, QB, and QC of IC3 are high, pin 12 of IC4 will be low. The

output transistors of IC10 through IC13 will be off unless the corresponding input is low. If an input to these ICs is low, the output transistor will be on. Therefore, only one of the eight output transistors of IC10 through IC13 will be on. Its corresponding replicator will be the active replicate lead, and the output from IC14 and IC15 will be from that chip.

4.08 When the START input is not grounded, signal GST1 is low. This holds IC5A set. When the START input is grounded, and there is a low on ST ENAB, the flip-flop formed by IC7A and IC7B is set, and GST1 is high. It will remain high as long as the START input is grounded, whether ST ENAB is low or not. When the ground on START is removed, GST1 will not go low unless input REPL is high.

4.09 To record new data in the 29A memories, IC14 and IC15, both the CH ACCESS and START inputs must be grounded. The old information in the 29A memories must first be erased by a pulse on the ERASE input. Since the START input is active, GST1 will be high. A pulse on the SOR input resets IC3 and clears IC5A. Recording on the first chip in IC14 starts. This chip is filled completely before switching to the next chip. At the data rate of 24 kHz, this takes 2.84 seconds. Switching to the next chip is accomplished with a pulse on the CHP CLK input. Switching occurs at the trailing edge of this pulse, which advance IC3 to a count of one. The second chip in IC14 is then filled completely before switching to the third chip.

4.10 This process continues until the last chip is reached, as determined by MESSAGE LENGTH switch S2. When S2 is set to anything but the first position (3), the LAST CHP signal, at IC2D pin 7, is determined from the appropriate output of IC4. For example, when S2 is set to 18, the LAST CHP signal will be high only when pin 14 of IC4 is low. This is true when recording the second chip of IC15, which is the sixth chip to be recorded. If S2 is set to 3, the LAST CHP signal is the inverted Q output of IC5A. For this case, the LAST CHP signal will be high during the recording of the first chip.

4.11 When the CH ACCESS input is grounded, and the LAST CHP signal is high, IC18D will hold the LST CHP output low. This is an open collector output. In a 13A, all LST CHP outputs from all message modules are tied together. The pullup resistor is on UD3. Only the channel which has been accessed for recording will have an active LST CHP output. At the end of the last chip, UD3 ends the recording process. Thus, if the MESSAGE LENGTH switch is set to 3, only the first chip in IC14 will be recorded.

4.12 Regardless of the setting of S2, at the end of the last chip the CHP CLK pulse will set the flip-flop formed by

IC25A and IC25B. This operates the STP relay. This produces a closure between output LIM and ground, and an open between output STP and ground. A pulse on the LIM RST input, which occurs 200 milliseconds later in a 13A, resets the flip-flop and releases the STP relay. The same CHP CLK pulse also clocks a one into IC5A. IC5A set:

(a) Clears IC3 via pin 11 or IC1C. (This resets the chip selection back to the first chip of IC14.)

(b) Enables pin 10 of IC19B. (This selects the SILEN input as the data input to the ADM decoder. In a 13A, this puts a silence pattern of alternating ones and zeros into the ADM which produces silence at the audio outputs.)

(c) Enables IC29B and IC29C. (This allows the next pulse on the CT GATE input to operate the CT relay. This produces a closure between outputs CT1 and CT2.)

(d) Releases the MU relay. (This produces a closure between outputs MU2 and MU3, and an open between outputs MU3 and MU4.)

This forms a silence period at the end of the recording. Since there is nothing in this sequence that is dependent on recording, this also forms the silence period between message repetitions.

4.13 Regardless of the setting of S2, the LAST CHP signal will be low during the silence period. The next pulse on the CHP CLK input will clock a zero into IC5A. IC5A cleared:

(a) Removes the clear from IC3, allowing IC3 to cycle through all the chips in the message.

(b) Disables the SILEN input and enables pin 5 of IC19B. (This allows the data from the 29A memories to go to the ADM decoder.)

(c) Releases the CT relay.

(d) Operates the MU relay.

This ends the silence period which, in a 13A, has a duration of 2.84 seconds. The playing back of the message begins at this time. In order to obtain an output signal from the 29A memory, constant currents of about 4.5 mA must be supplied to pins 2 and 3 of IC14. These are supplied by pins 3 and 16 of IC16. The output signal from IC14 is the voltage difference between pins 2 and 3. The signal amplitude is small, only a few millivolts. IC16 amplifies this by about 35. The amplified signal is present at pin 6 of IC16. Further signal conditioning occurs in IC16 with the timing information supplied by the STROBE input. When this input is high, an internal switch

inside IC16 shorts pin 7 to ground. When STROBE goes low, this switch opens and the voltage on pin 7 follows the voltage on pin 6, except for a dc offset. Pin 7 is also an input to a comparator inside the IC. The threshold at which the comparator changes state is determined by the dc voltage on pin 10, which is preset in manufacture of the circuit pack. Pin 13 is a TTL compatible output. It is high if the waveform at pin 7 exceeds the threshold voltage, and low if the waveform stays below the threshold. The data at pin 13 is latched, and is present almost until the next STROBE input. The latch is reset by a pulse, 100 ns or longer, on the DET RST input. Because the data output is open collector, a pullup resistor is provided. IC17 and associated components provide the same data detection function for IC15.

4.14 IC19A provides the switching between the data outputs of IC16 and IC17. IC19A is controlled by IC5B. The state of IC5B is controlled by IC3 and the ST ENAB input. When IC3 is selecting a chip from IC14, output QC is low. At the leading edge of ST ENAB, the state of QC is clocked into IC5B. In this case, IC5B will be cleared, and the data output from IC16 will be selected. When IC3 switches to IC15, QC goes high. At the next leading edge of ST ENAB, IC5B is set and the data output from IC17 is selected. In a 13A, the leading edge of ST ENAB occurs 30 data cycles after CHP CLK. This compensates for the 30-bit delay between replication and data output in the 29A memories.

4.15 IC20, IC21, IC22, and associated components form the adaptive delta modulation (ADM) decoder. It converts the digital data, stored in the 29A memories, back into an analog signal. The data present at pin 2 of IC20 is latched and is output at pin 20. Pin 16 is low only when there are four ones or four zeros in a row in the data. When pin 16 is low, Q10 is on and charges C21 through resistors internal to IC21. IC21 converts the voltage at pin 11 into a current at pin 17. This current controls the size of the step taken by IC22A. The polarity of the step is controlled by the data, which is present at pin 5 of IC22A.

4.16 The positive or negative steps produced by IC22A are integrated by C22. The result is amplified differentially by IC22B. IC22B also provides a high-frequency deemphasis which is the opposite of the high-frequency preemphasis provided by UD2 before encoding the speech. This is accomplished by C23 and R38, which make IC22B into a low-pass filter with a -3 dB point at 80 Hz. IC22C and associated components form a three-pole low-pass filter with a -3 dB point at 3 kHz. The signal at TP4 is the decoded speech. It is about 100 mVrms.

4.17 After OUTPUT LEVEL ADJ R55, the speech goes to IC23, which has a gain of 30. T1 provides output isolation and a

low output impedance of about one ohm at terminals T1 and R1. The turns ratio between input winding at pins 7 and 8 and output at pins 2 and 5 is 5 to 1. C55 provides an ac ground for the center tap between T1 and R1. CR17 and CR18 provide transient protection. Maximum output level between T1 and R1 is -9 VU.

4.18 The other winding of T1, pins 9 and 10, provides a step-up from the input of 5 to 1. This provides the signal for the MON AUD output, as well as driving the voice alarm circuit, through R64. The voice alarm circuit monitors the average level of the output speech. If it falls below a minimum level, the VA relay is released and a closure is made on outputs VA1 and VA2. Because the relay must be operated to be in the no-alarm state, loss of power in a 13A will result in a voice alarm.

4.19 Because the voice alarm circuit monitors the output speech, the setting of OUTPUT LEVEL ADJ R55 also affects the signal level to the voice alarm circuit. If there are no gaps within a message, an output level at T1 and R1 of -26 VU or greater will satisfy the voice alarm circuit. If a message occupies only the first 6 seconds of a 12-second message length, the output level must be greater than -24 VU to keep the circuit in a no-alarm state.

4.20 The output speech to the voice alarm circuit, after R64, is limited in amplitude by CR4. At this point, the signal is limited to a negative amplitude of 0.6 volt and a positive amplitude of 12 volts. CR5 and CR6 provide a 0.8-volt deadband that the signal must exceed in order to trigger the voice alarm circuit. This prevents most background noise from satisfying the voice alarm, and the diodes also allow C46 to charge to a positive voltage only. Positive peaks of the signal will charge C46, with a 10-millisecond time constant. In the absence of speech, C46 will discharge slowly through R66. The discharge time-constant is 5 seconds. IC24, a high input impedance amplifier connected for a gain of 10, compares the voltage on C46 to the voltage at the node of R71, R72, and R75. The comparison voltage at this node is 0.76 volt. If the voltage at C46 exceeds this, the output of IC24 is high, Q11 is on, and the VA relay is operated. If the voltage at C46 falls below 0.76 volt, the output of IC24 goes low, Q11 turns off, the VA relay releases (signaling an alarm), and voice alarm LED CR12 lights.

4.21 The voice alarm circuit must be held in a no-alarm state when the message is stopped. When the message module is stopped, SILENCE 0 is low, and Q12 is off. When Q12 is off, a voltage of 1.5 volts, present at the node between R71 and R74, is allowed to charge C46 through R70. This voltage is sufficient to keep the voice

alarm off. During a message, Q12 is on, preventing this voltage from charging C46.

4.22 If the input VA TEST is grounded, C46 is discharged through CR7, simulating a loss of audio. This input can be used to test the operation of the voice alarm circuit.

4.23 In a 13A, a special bit pattern, consisting of 15 ones, called a preamble, is used to mark the beginning of a message. IC26 and associated gates form a preamble detection circuit. It holds the MATCH output low for 40  $\mu$ s if a preamble pattern is detected in the data being read from memory. If input DT COMP SW is low, noninverted data from the 29A memories will be present at TP9. A zero at this point will load all zeros into IC26, resetting the circuit. If there are 15 ones in a row, IC26 will count to 15 and generate a carry output at pin 15. If the UD4 is not accessed, IC18C is enabled and the carry will generate a low on the MATCH output. If the CH ACCESS input is grounded, IC18C inhibits the carry from generating a MATCH output. In a 13A, this can be used to isolate DVAs to a particular message board. The MATCH output is an open collector output. In a 13A, the pullup resistor is provided by UD3.

4.24 If the input DT COMP SW is high, the data at the load input of IC26 (TP9) is inverted. In this case, IC26 is checking the contents of the memory for 15 zeros in a row. Gates IC8D and IC29D inhibit the preamble circuit when QC is low and IC5B is set. The PWR OFF input will clear and inhibit the preamble circuit when it is low. In a 13A, this lead is used to initialize the preamble circuit upon powering up.

#### 5. UD4-3-24 SECOND VML MESSAGE MODULE (SERIES 15 OR HIGHER USING STATIC RAM MEMORY)

5.01 UD4 stores and plays back up to 24 seconds of speech. It has a variable message length (VML) which can be adjusted from 3 to 24 seconds in 3-second increments. The record and playback functions of UD4 are controlled by the Intel 8051 micro-processor, IC15. The 8051 stores the digitally encoded speech in eight random access memories from which it will retrieve the data upon request. The UD4 reconverts the data to analog speech using adaptive delta modulation. It amplifies and buffers the output to drive up to 500 trunk circuits. UD4 has a battery on board to save the recorded message in memory in case of a power loss to the circuit pack.

#### CIRCUIT DESCRIPTION

5.02 Most inputs to UD4 are TTL compatible and are low active. The exception is that START and CH ACCESS require a contact closure to ground to be active. They may be open when inactive. All of the TTL

inputs are provided with 10-Kohm pull-up resistors to increase the noise margins in the high state.

5.03 In a 13A, the CH ACCESS input is used to access the desired UD4 for monitoring or recording. A closure to ground on the CH ACCESS input or operation of CHANNEL ACCESS switch S1 will:

- (a) Enable the SOR (start of record) input via IC2C which is used in the recording of new messages.
- (b) Operate the CA relay. This connects the audio to the MON AUD output.
- (c) Light CR2, the CHANNEL ACCESS LED.
- (d) Enable the LST CHP output via IC3D.

5.04 When enabled by CH ACCESS, a pulse on the SOR input will clear IC29 and IC5A. This, in turn, enables the STROBE input via IC7A, which the 8051  $\mu$ P uses as the sampling clock (pin 4 of IC15) when recording or playing back the digitized speech.

5.05 Each of the eight static RAMS, IC's 16-19, and 24-27, stores 65,536 bits (8 bits X 8,192) of information (about 2.73 seconds of speech). The write and read lines (pins 16 and 17) of the 8051 are common to all RAMs. The low order address/data lines AD0 through AD7 are bi-directional through the latch IC23. When reading or writing memory the ALE (address latch enable) pin 30 of IC15 will be active when latching the low order address byte. The latch is disabled when AD0 through AD7 become the data bus. To access all locations within each RAM, additional addressing is needed. This is provided by address lines A8 through A12 of IC15. Sequencing through the RAMs is accomplished by IC22, which decodes address lines A13, A14, and A15 to provide the proper chip select. Only one output of IC22 is low at a time.

5.06 When the start input is not grounded, signal GST1 (which is also STRT pin 3 of IC15) is low. This holds IC5A set. When the start input is grounded and there is a low on ST ENAB, the flip-flop formed by IC7C and IC7D is set, and GST1 goes high. The 8051 responds to the high on pin 3, performs an initialization routine, and is ready to play-back or record speech. GST1 will remain high as long as the START input is grounded whether or not ST ENAB is low. When the ground on START is removed, GST1 will go low.

5.07 Depending on which timing board is used in a 13A System (UD3 or UD3B) the format of the digitized speech coming into UD4 can be different. IC32 is used to reformat the data, so that it is the same regardless of which timing board is used. IC32 is a dual retriggerable monostable which takes in the data (GEN INFO) on pin 2 and takes in an associated timing signal

(REC) on pin 1. With logic internal to the chip and the time constant generated by the external components R29 and C66, each bit of data (either a 0 or 1) at the output (pin 13) has an equal pulse width of approximately 28  $\mu$ sec. The data is now ready to be processed by the 8051.

5.08 To record new data in the RAMs, both the CH ACCESS and START inputs must be grounded. A 740- $\mu$ sec active low pulse on the SOR input interrupts the 8051 on pin 12 of IC15 to initialize the record sequence. It also clears IC5A and IC29. Recording begins on the rising edge of the SOR pulse. The 8051 takes in the data on pin 1 of IC15. Using the STROBE input as the sampling clock (pin 4 of IC15), the processor inputs each bit at 24 KHz serial data rate. The 8051 then writes the data in byte format to memory. Each byte is sequentially stored in RAM.

5.09 The recording length is determined by switch S2. CHP CLK with a period of 2.84 seconds, continually advances the count on IC29, which is then decoded by IC30. Only one output of IC30 is low at a time. Since each RAM can store 2.73 seconds of speech, a CHP CLK period actually results in completely filling one RAM and about 300 bytes of the following RAM. The slack is taken up by increasing the silence period during a 24-second message. This timing discrepancy results from the redesign which was done to provide a plug-compatible replacement for the UD4 circuit packs series 14 and lower. Thus, for it to function in all previously designed 13A announcement systems, the timing signals into the board had to remain the same. Recording will continue until the CHP CLK pulse clocks a change in the LAST CHP signal (determined by S2) into IC5A. This results in interrupting the processor on pin 13 (End Of Speech) telling the 8051 to stop recording. It also clears IC29 and disables the sampling clock via IC7A.

5.10 When the CH ACCESS input is grounded, and the LAST CHP signal is high, IC3D together with Q9 (providing an open collector output) will hold the LST CHP output low. In a 13A, all LST CHP outputs from all message modules are tied together. The pull-up resistor is on UD3B. Only the channel which has been accessed for recording will have an active LST CHP output. UD3B ends the recording process on the rising edge of the LST CHP output.

5.11 Regardless of the setting of S2, at the end of the LST CHP signal, the CHP CLK pulse will set the flip-flop formed by IC10C and IC10D. This operates the STP relay which produces a closure between output LIM and ground, and an open between output STP and ground. A pulse on the LIM RST input (occurring about 170 ms later in a 13A) resets the flip-flop and releases the STP relay. The same CHP CLK pulse also clocks a "one" into IC5A. IC5A, when set, will:

(a) Clear IC29 via pin 2 of ICA2A. This allows the full length of the message, according to switch S2, to be played back.

(b) Enable pin 13 of IC9B via pins 2 and 3 of IC9A. This selects the SILEN input as the data input to the ADM decoder. In a 13A this puts a silence pattern of alternating "ones" and "zeroes" into the ADM decoder. This, in turn, produces silence at the audio outputs.

(c) Enable IC4A and IC4C. This allows the next pulse on the CT GATE input to operate the CT relay. This produces a closure between outputs CT1 and CT2.

(d) Release the MU relay. This produces a closure between outputs MU2 and MU3, and an open between outputs MU3 and MU4.

(e) Disable the sampling clock to the 8051 via IC7A.

(f) Halt the record or playback process via an interrupt to the 8051 on pin 13 (End of Speech). This tells the 8051 that the silence period has begun, thus initializing the software, so that playback (or recording) of the speech will begin immediately after the silence period has ended.

This forms a silence period at the end of the recording. Since there is nothing in this sequence that is dependent on recording, it also forms the silence period between message repetitions.

5.12 Regardless of the setting of S2, the LAST CHP signal will be low during the silence period. The next pulse on the CHP CLK input will clock a zero into IC5A. IC5A, when cleared, will:

(a) Remove the clear from IC29, allowing IC29 to cycle through, so that the full length of memory is accessed during playback.

(b) Disable the SILEN input and enable pin 10 of IC9B. This allows the data read from memory and processed by the 8051 to go to the ADM decoder.

(c) Release the CT relay.

(d) Operate the MU relay.

(e) Enable the sampling clock to the 8051.

The clearing of IC5A then ends the silence period of 2.84 seconds (in a 13A). The playing back of the message begins at this time. If the START is still grounded the next CHP CLK will clock a "one" into the Q output of IC5A, thus enabling the STROBE input (or sampling clock). The 8051 begins reading the data starting with RAM 0 and continuing until CHP CLK pulse again clocks

in a change in the LAST CHP signal at IC5A. This disables the STROBE input, and interrupts the processor (pin 13 of IC15) which halts the playback routine. Halting the playback routine is identical to halting the record routine. It depends on switch S2's setting which determines the number of CHP CLK pulses before the silence interval is initiated. The playback routine itself is opposite the record routine in that the 8051 reads the data from memory 8 bits at a time, formats it, and outputs it serially on pin 2 of IC15 (DOUT).

5.13 IC14, IC20, IC21, and associated components form the adaptive delta modulation (ADM) decoder. They convert the digital data stored in the RAMs back into an analog signal. The data present at pin 2 of IC14 is latched and output at pin 20. Pin 16 is low only when there are four "ones" or four "zeros" in a row in the data. When pin 16 is low, Q3 is on and charges C21 through resistors internal to IC20. IC20 converts the voltage at pin 11 into a current at pin 17. The polarity of the step is controlled by the data at pin 5 of IC21A.

5.14 The positive or negative steps produced by IC21A are integrated by C51. The result is amplified differentially by IC21B. IC21B also provides a high-frequency de-emphasis which is opposite of the high-frequency pre-emphasis provided by UD2 before encoding the speech. This is accomplished by C52 and R38 which make IC21B into a low-pass filter with a -3 dB point at 80 Hz. IC21C and associated components form a three-pole low pass filter with a -3 dB point at 3 kHz. The signal at TP4 (about 100mV rms) is the decoded speech.

5.15 After OUTPUT LEVEL ADJ R55, the speech goes to IC31 (gain=30). T1 provides output isolation and a low output impedance of about one ohm at terminals T1 and R1. This turns ratio between input winding at pins 7 and 8 and output at pins 2 and 5 is 5 to 1. C55 provides an ac ground for the center tap between T1 and R1. CR17 and CR18 provide transient protection. Maximum output level between T1 and R1 is -9 VU.

5.16 The other winding of T1, pins 9 and 10, provides a step-up from the input of 5 to 1. This provides the signal from the MON AUD output, as well as driving the voice alarm circuit through R58. The voice alarm circuit monitors the average level of the output speech. If it falls below a minimum level, the VA relay is released and a closure is made on outputs VA1 and VA2. Because the relay must be operated to be in the no-alarm state, loss of power in a 13A will result in a voice alarm.

5.17 Because the voice alarm circuit monitors the output speech, the setting of OUTPUT LEVEL ADJ R55 also

affects the signal level to the voice alarm circuit. If there are no gaps within a message, an output level at T1 and R1 of -26 VU or greater will satisfy the voice alarm circuit. If a message occupies only the first 6 seconds of a 12-second message length, the output level must be greater than -24 VU to keep the circuit in a no-alarm state.

5.18 The output speech to the voice alarm circuit after R58 is limited in amplitude by CR4. At this point, the signal is limited to a negative amplitude of 0.6V and a positive amplitude of 12V. CR5 and CR6 provide a 0.8V deadband that the signal must exceed in order to trigger the voice alarm circuit. This prevents most background noise from satisfying the voice alarm, and the diodes also allow C46 to charge to a positive voltage only. Positive peaks of the signal will charge C46 with a 25 ms time constant. In the absence of speech, C46 will discharge slowly through R60. The discharge time-constant is 6 seconds. IC28, a high input impedance amplifier connected for a gain of 10, compares the voltage on C46 to the voltage at the node of R65, R53, and R50. The comparison voltage at this node is 0.76V. If the voltage at C46 exceeds this, the output of IC28 is high, Q4 is on, and the VA relay is operated. If the voltage at C46 falls below 0.76V, the output of IC28 goes low, Q4 turns off, the VA relay releases (signaling an alarm), and voice alarm LED CR12 lights.

5.19 The voice alarm circuit must be held in a no-alarm state when the message is stopped, SILENCE0A is low, and Q5 is off. When Q5 is off, the 1.5V present at the node between R65 and R51 is allowed to charge C46 through R64. This voltage is sufficient to keep the voice alarm off. During a message, Q5 is on, preventing this voltage from charging C46.

5.20 The 8051 can also activate the voice alarm by putting a low on pin 6 of IC15. This will turn Q8 on, discharging C46 through CR20 simulating a loss of audio. The 8051 will activate the voice alarm if one of the following conditions exists:

- (a) Failure of code diagnostics due to an error in program memory. This will also cause the FAIL pin (pin 11 of IC15) to oscillate at a frequency of about 42KHz.
- (b) A failure in one or more RAMs i.e. IC16 through IC19 and IC24 through IC27.
- (c) Invalid data stream i.e. bit pattern consisting of 15 or more "ones" in a row, or 15 or more "zeroes" in a row.
- (d) Failure of the sampling clock i.e. the STROBE input.

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- (e) A short or open in the address and/or data lines or circuitry associated with data transfer between the 8051  $\mu$ P and RAM.
- 5.21 If the input VA TEST is grounded, C46 is discharged through CR7, simulating a loss of audio. This input can be used to test the operation of the voice alarm circuit.
- 5.22 IC13, the battery BT1, IC8, and associated components form a backup circuit. This will retain the recorded message in memory if a power failure occurs or if power to the 13A is turned off on UD1. IC13 is a voltage regulator which actually performs two functions. First, it regulates the +15V supply down to +5.7V. This is then reduced further to +5V in two places; through CR19 generating VCC to drive the 8051, and through CR16 to generate VCCR which power the RAMS. This was done since the +5V supply into the circuit pack was insufficient to handle the additional load. The second purpose of IC13 is that it sets up a reference voltage for the comparator IC18 at pin 2. The nominal voltage at pin 2 is about 2.85V and at pin 3, about 3V.
- 5.23 When power goes down in a 13A, the 5.7V output of IC13 will be maintained much longer than the +5V supply input. Thus, when the voltage at pin 3 of IC8 goes below the threshold set up at pin 2, it triggers the comparator and disables the Chip Selects to all RAMS. This is done before the supply voltage to the RAMS has dropped significantly, to prevent any data loss. As power to the board keeps reducing, the battery BT1 (nominally 3V), finally takes over (through switch H1) when CR1 begins conducting. This maintains about 2.8V at VCCR to keep the memory in a data retention mode.
- 5.24 On power up in a 13A, the Chip Select signals to the RAMS are not enabled until the PWR OFF signal on pin 13 of IC11D goes high. The PWR OFF input does not go high until all power to the circuit pack is stable. This again prevents the possibility of altering the stored data. The PWR OFF signal also goes to pin 5 of IC15. This prevents the 8051 from doing any processing or memory accessing until power is stable.
- 5.25 To reset the 8051  $\mu$ P, an active high pulse must be applied to pin 9 of IC15. There are three ways a reset can be accomplished. First, there is a power-up reset. As power is applied, the voltage at pin 4 of IC11B will rise with a 50 ms time constant formed by R8 and C63. While pin 4 is low, IC5B is preset. This places a high on the Q output and resets the 8051. Now the Q output of IC5B is fed back to pin 5 of IC11B. So with pin 4 still low and pin 5 high, C42 will be charged up. When pin 4 rises sufficiently (removing the preset from IC5B), pin 6 of IC11B will go low and C42 will discharge through R26 with a 50 $\mu$ sec time constant. This will clear IC5B turning off the reset. With the Q output just low, pin 6 of IC11B goes high charging C42 and removing the clear from IC5B.
- 5.26 With the circuit pack powered, there are two ways to reset the processor. If pin 11 or 12 of IC2D goes high, this will clock a "one" into IC5B, and according to the mechanism just described, this will result in a 50 $\mu$ sec reset pulse. Pin 11 of IC2D will go high if the ground on the START input is removed. This causes the flip-flop formed by IC7C and IC7D to reset. Pin 12 of IC2D is tied to pin 8 (TORST) of the 8051. If the processor gets into a "stuck at" condition for more than 54 seconds (determined by monitoring the CHP CLK pulses on pin 14), an internal sanity timer will initiate an interrupt and cause the 8051 to put a high out on pin 8; this results in an automatic reset.
- 5.27 The 8051 does have the capability of performing a complete memory test intended for use in manufacturing in-circuit testing. By grounding pin 15 of IC15, the 8051 will initiate a 6-minute test on the eight RAMS. If a failure exists, the 8051 will hold the address of the failed RAM on the address lines and light the voice alarm LED (CR12) for about 5 seconds. The test is then repeated if pin 15 is still grounded. The test can be interrupted by removing the ground and resetting the processor.
- 5.28 There are straps on the board that are used to distinguish between the UD4 and UD6 circuit packs. For the UD4, pin 10 of the 8051 processor is strapped (W3) to ground. This tells the 8051 that 8 RAMS are on board. Straps W1 and W4 are used to extend the silence period during a 24-second message. This is because the actual total storage time for this design is shorter by 0.8 seconds than the UD4 series 14 (or lower) circuit packs it replaces. When the last location in memory is accessed the 8051 clears pins 26, 27, and 28 which then put a high on pin 7 of IC22. And with pin 7 of IC30 still low, pin 6 of IC9A is low enabling pin 13 of IC9B. 0.8 seconds later IC29 is cleared and the silence period continues in the normal fashion. Therefore, during a 24-second message the silence period is longer by 0.8 seconds.

## 6. UD5 - FML MESSAGE MODULE

### GENERAL DESCRIPTION

6.01 UD5 stores and plays back 12 seconds of speech. It stores the digitally encoded speech in a 29A bubble memory. It converts the stored information back into analog speech using adaptive delta modulation, and it amplifies and buffers the output to drive up to 500 trunk circuits. Cut-through and voice alarm signals are also provided by this circuit pack.

## CIRCUIT DESCRIPTION

6.02 Most inputs to UD5 are TTL compatible and are low active. Exceptions are:

(a) OCDR and ICDR require 24V peak-to-peak sinusoidal signals at 48 kHz. OCDR leads ICDR by 95 degrees. These inputs provide the rotating field for the 29A memory. C1 plus the outer coil of IC4 form a parallel resonant circuit at 48 kHz. Similarly, C2 and the inner coil form another resonant circuit at 48 kHz.

(b) CH ACCESS requires a contact closure to ground to be active. It may be open when inactive.

Most of the TTL inputs are provided with 10-kohm pull-up resistors to increase the noise margins in the high state.

6.03 In a 13A, the CH ACCESS input is used to access the desired UD5 for monitoring or recording. A closure to ground on the CH ACCESS input or operation of CHANNEL ACCESS switch S1 will:

(a) Enable the ERASE and REC inputs. (These are used in the recording of new messages.)

(b) Operate the CA relay. (This connects the audio to the MON AUD output.)

(c) Light CR2, the CHANNEL ACCESS LED.

(d) Enable the LST CHP output.

(e) Disable the MATCH output.

6.04 When enabled by CH ACCESS, a low on the ERASE input will turn on Q5 and Q6, causing a current of 300 mA to 500 mA to flow in the Z coil (pins 15 and 16) of the 29A memory. This erases all the data in the memory.

6.05 A low on the REC input will, when enabled by CH ACCESS, put a zero on pin 3 of IC8A. This enables a low on the GEN INFO input to turn on Q3 and Q4. Normal GEN INFO pulse width is 325 ns. This results in a 280-mA pulse of current, 400 ns in duration, in the G (generator) input of IC4 (pins 22 and 31). Each pulse generates a one in the 29A memory if a replicate pulse is also present.

6.06 Each 29A memory contains four chips. Each chip stores 68,121 bits of information. Both write (generate) and read lines are common to all four chips. The replicate leads act as chip select leads to determine which chip is being written or read. The REPL and REPH inputs determine the timing and shape of the replicate pulse. When REPL is low, Q11 and Q12 are on, and 30 mA of current flows through R22 and the selected replicate lead. At the beginning of the REPL pulse, REPH is also turned on, but for a shorter duration (640 ns). REPH low turns on Q1 and Q2, and 80 mA of current flows through

R21. In the replicate lead, the two currents are added for a total of 110 mA.

6.07 Selection of the desired replicate lead is done by IC2, IC3, and IC6. A low on one of the inputs CHIP 1, CHIP 2, CHIP 3, or CHIP 4 will turn on the corresponding output transistor in IC3 or IC6. The corresponding replicator will be the active replicate lead, and the output from IC4 will be from that chip. At any given time, only one of these inputs should be low, and the other three should be high.

6.08 To record new data in the 29A memory, the CH ACCESS input must be grounded (or S1 operated). The old information in the 29A must first be erased by a pulse on the ERASE input. Recording on the first chip starts when inputs REC and CHIP 1 are brought low. This chip is filled completely before switching to the next chip. At the data rate of 24 kHz, this takes 2.84 seconds. Switching to the second chip is accomplished by bringing input CHIP 1 high and input CHIP 2 low. The second chip in IC4 is then filled completely before switching to the third chip.

6.09 This process continues until the end of CHIP 4 is reached. During the time input CHIP 4 is low, pin 6 of IC18 is high. When the CH ACCESS input is grounded, as it is during recording, IC18 will hold the LST CHIP output low. This is an open collector output. In a 13A, all LST CHIP outputs from all message modules are tied together. The pull-up resistor is on UD3. Only the channel which has been accessed for recording will have an active LST CHIP output. At the end of the last chip, UD3 ends the recording process by bringing input REC high.

6.10 In a 13A, input FMLCT is held low for the next 2.84 seconds. This selects the SILEN input as the data input to the ADM decoder. A silence pattern (alternating ones and zeros) on the SILEN input goes to the ADM and produces silence at the audio outputs. During this period, a contact closure generated on UD3 is input on leads FML CTRLY 1 and FML CTRLY 2. This closure is output from UD5 on leads CT1 and CT2.

6.11 At the end of the silence period, input FMLCT is brought high and input CHIP 1 is brought low. The playing back of the message begins at this point. As in recording, message playback is accomplished by accessing, in turn, the four chips in the 29A memory. At the end of each message repetition, there is a silence interval and cut-through closure, just as there is at the end of the record cycle.

6.12 In order to obtain an output signal from the 29A memory, constant currents of about 4.5 mA must be supplied to pins 2 and 3 of IC4. These are supplied by pins 3 and 16 of IC5. The output signal from IC4 is obtained by looking

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differentially between pins 2 and 3. The signal amplitude is small, only a few millivolts. IC5 amplifies this by about 35. The amplified signal is present at pin 6 of IC5. Further signal conditioning occurs in IC5 with the timing information supplied by the STROBE input. When this input is high, an internal switch inside IC5 shorts pin 7 to ground. When STROBE goes low, this switch opens and the voltage on pin 7 follows the voltage on pin 6, except for a dc offset. Pin 7 is also an input to a comparator inside the IC. The threshold at which the comparator changes state is determined by the dc voltage on pin 10, which is preset in manufacture of the circuit pack. Pin 13 is a TTL compatible output. It is high if the waveform at pin 7 exceeds the threshold voltage, and low if the waveform stays below the threshold. The data at pin 13 is latched, and is present almost until the next STROBE input. The latch is reset by a pulse, 100 ns or longer, on the DET RST input. Because the data output is open collector, a pull-up resistor is provided.

6.13 IC10, IC12, IC13, and associated components form the adaptive delta modulation (ADM) decoder. It converts the digital data, stored in the 29A, back into an analog signal. The data present at pin 2 of IC10 is latched and output at pin 20. Pin 16 is low only when there are four ones or four zeros in a row in the data. When pin 16 is low, Q8 is on and charges C25 through resistors internal to IC12. IC12 converts the voltage at pin 11 into a current at pin 17. This current controls the size of the step taken by IC13A. The polarity of the step is controlled by the data, which is present at pin 5 of IC13A.

6.14 The positive or negative steps produced by IC13A are integrated by C18. The result is amplified differentially by IC13B. IC13B also provides a high-frequency de-emphasis which is the opposite of the high-frequency preemphasis provided by UD2 before encoding the speech. This is accomplished by C17 and R38, which make IC13B into a low-pass filter with a -3 dB point at 80 Hz. IC13C and associated components form a three-pole, low-pass filter with a -3 dB point at 3 kHz. The signal, about 100 mV rms, at TP4 is the decoder speech.

6.15 After R64, the OUTPUT LEVEL ADJ, the speech goes to IC14, which has a gain of 30. T1 provides output isolation and a low output impedance of about one ohm at terminals T1 and R1. The turns ratio between input winding at pins 7 and 8 and output at pins 2 and 5 is 5 to 1. C43 provides an ac ground for the center tap between T1 and R1. CR13 and CR14 provide transient protection. Maximum output level, between T1 and R1, is -9 VU.

6.16 The other winding of T1, pins 9 and 10, provide a step-up from the input of 5 to 1. This provides the signal for the MON AUD output, as well as driving the

voice alarm circuit, through R50. The voice alarm circuit monitors the average level of the speech. If it falls below a minimum level, the VA relay is released and a closure is made on outputs VA1 and VA2. Because the relay must be operated to be in the no-alarm state, loss of power in a 13A will result in a voice alarm.

6.17 Because the voice alarm circuit monitors the output speech, the setting of OUTPUT LEVEL ADJ R64 also affects the signal level to the voice alarm circuit. If there are no gaps within a message, an output level, at T1 and R1, of -26 VU or greater will satisfy the voice alarm circuit. If a message occupies only the first 6 seconds of the 12-second message length, the output level must be greater than -24 VU to keep the circuit in a no-alarm state.

6.18 The output speech to the voice alarm circuit, after R64, is limited in amplitude by CR4. At this point, the signal is limited to a negative amplitude of 0.6 volt and a positive amplitude of 12 volts. CR5 and CR6 provide an 0.8-volt deadband that the signal must exceed in order to trigger the voice alarm circuit. This prevents most background noise from satisfying the voice alarm, and the diodes also allow C38 to charge to a positive voltage only. Positive peaks of the signal will charge C38, with a 10-millisecond time-constant. In the absence of speech, C38 will discharge slowly through R51. The discharge time-constant is 5 seconds. IC15, a high input impedance amplifier connected for a gain of 10, compares the voltage on C38 to the voltage at the node of R59, R60, and R61. The comparison voltage at this node is 0.76 volt. If the voltage at C38 exceeds this, the output of IC15 is high, Q9 is on and the VA relay is operated. If the voltage at C38 falls below 0.76 volt, the output of IC15 goes low, Q9 turns off, the VA relay releases signaling an alarm), and voice alarm LED CR9 lights.

6.19 The voice alarm circuit must be held in a no-alarm state during the silence interval between message repetitions. During the silence interval, FMLCTO is low, and Q10 is off. When Q10 is off, a voltage of 1.5 volts, present at the node between R58 and R59, is allowed to charge C38 through R57. This voltage is sufficient to keep the voice alarm off. During a message, Q10 is on, preventing this voltage from charging C38.

6.20 If the input VA TEST is grounded, C38 is discharged through CR10, simulating a loss of audio. This input can be used to test the operation of the voice alarm circuit.

6.21 In a 13A, a special bit pattern consisting of 15 ones, called a preamble, is used to mark the beginning of a message. IC16 and associated gates form a preamble detection circuit. The MATCH

output is held low for 40  $\mu$ s if a preamble pattern is detected in the data being read from memory. If input DT COMP SW is low, noninverted data from the 29A memory will be present at the load input to IC16. A zero at this point will load all zeros into IC16, resetting the circuit. If there are 15 ones in a row, IC16 will count to 15 and generate a carry output at pin 15. If the UD5 is not accessed, IC1D is enabled and the carry will generate a low on the MATCH output. If the CH ACCESS input is grounded, IC1D inhibits the carry from generating a MATCH output. In a 13A, this can be used to isolate digital voice alarm (DVAs) to a particular message board. The MATCH output is an open collector output. In a 13A, the pull-up resistor is provided by UD3.

6.22 If the input DT COMP SW is high, the data at the load input of IC16 is inverted. In this case, IC16 is checking the contents of the memory for 15 zeros in a row. The PWR OFF input will clear and inhibit the preamble circuit when it is low. In a 13A, this lead is used to initialize the preamble circuit upon powering up.

#### 7. UD6-3-12 SECOND VML MESSAGE MODULE (SERIES 1-14 USING 29A BUBBLE MEMORY)

##### GENERAL DESCRIPTION

7.01 UD6 stores and plays back up to 12 seconds of speech. It has a variable message length (VML) which can be adjusted from 3 to 12 seconds in 3-second increments. UD6 stores the digitally encoded speech in a 29A bubble memory. It converts the stored information back into analog speech using adaptive delta modulation, and it amplifies and buffers the output to drive up to 500 trunk circuits. Signaling closures and voice alarm are also provided by this circuit pack.

##### CIRCUIT DESCRIPTION

7.02 A UD6 is essentially a UD4 without the second 29A memory and associated components. The two codes share the same printed circuit board. The detailed description of UD4 also applies to UD6. In the operation of a UD6, The MESSAGE LENGTH switch, S2, should not be set to greater than 12. In a 13A, this would result in a DVA.

#### 8. UD6-3-12 SECOND VML MESSAGE MODULE (SERIES 15 OR HIGHER USING STATIC RAM MEMORY)

##### GENERAL DESCRIPTION

8.01 UD6 stores and plays back up to 12 seconds of speech. It has a variable message length (VML) which can be adjusted from 3 to 12 seconds in 3-second increments. The record and playback functions of UD6 are controlled by the Intel 8051 micro-processor, IC15. The 8051

stores the digitally encoded speech in four random access memories, IC's 16-19, from which it will retrieve the data upon request. The UD6 reconverts the data to analog speech using adaptive delta modulation. It amplifies and buffers the output to drive up to 500 trunk circuits. UD6 has a battery on board to save the recorded message in memory in case of a power loss to the circuit pack.

##### CIRCUIT DESCRIPTION

8.02 A UD6 is essentially a UD4 with 4 RAMs instead of 8. The two codes share the same printed circuit board. The detailed description of UD4 also applies to UD6. In the operation of a UD6, the MESSAGE LENGTH switch, S2, should not be set to greater than 12. In a 13A, this would result in the extension of the silence interval between message repetitions. A voice alarm will also result if the additional silence time is greater than 8 seconds.

8.03 There are straps on the board used to distinguish between the UD4 and UD6 circuit packs. For the UD6, strap W3 is left open, resulting in pin 10 of IC15 being pulled to VCC, via R73. This tells the 8051 that 4 RAMs are on board. Straps W2 and W5 are used to extend the silence period during a 12-second message. This is because the actual total storage time for this design is shorter by 0.4 seconds than the UD6 series 14 (or lower) circuit packs it replaces. When the last location in memory is accessed, the 8051 clears pins 26, 27, and 28 which then puts a high on pin 12 of IC22. With pin 12 of IC30 still low, pin 6 of IC9A is low enabling pin 13 of IC9B. 0.4 seconds later IC29 is cleared and the silence period continues in the normal fashion. Therefore, during a 12-second message the silence period is longer by 0.4 seconds.

#### 9. ANNOUNCEMENT RECORD - SC1

9.01 This section describes the I/O timing of the 13A during a record operation. Designation of leads such as START( ) refers to the START lead for a particular channel. The actual lead used depends on the channel desired. For example, if a recording is to be made on channel three, the leads used would be START(3) and CH ACCESS(3).

9.02 Before recording, it is necessary to select the desired channel by putting the CH ACCESS switch in the access position or by grounding the START( ) and CH ACCESS( ) leads. It is possible, but not usually desirable, to record the same message on more than one channel. For multiple channel recordings, all accessed channels should be set to the same message length.

9.03 After the desired channel is accessed, the recording process is initiated by a momentary closure (1 ms

minimum) between leads REM RECORD and REM RECORD RTN, or by a momentary closure of the LOCAL RECORD SWITCH. The RECORD REQUEST LED lights, signaling that a record process is requested. After a maximum time of 15 seconds:

- (a) The RECORD REQUEST LED (red) is extinguished.
- (b) The RECORD LED (green) is lit.
- (c) The KREC relay operates.

This starts the recording.

9.04 The recording of the message continues for the time set by the MESSAGE LENGTH switch. The recording interval can be from 3 to 24 seconds long. At the end of the recording interval:

- (a) The RECORD LED is extinguished
- (b) The KREC relay releases.

9.05 After the end of the recording interval, the CH ACCESS switch, if accessed, should be returned to the normal (unaccessed) position. If the CH ACCESS( ) and START( ) leads were grounded for the recording, the ground should be removed at this time.

#### 10. ANNOUNCEMENT REPRODUCE - SC2

10.01 This section describes the I/O timing of the 13A during an announcement reproduce cycle. Designation of leads such as START( ) refers to the START lead for a particular channel. The actual lead used depends on the channel desired. For example, if it is desired to reproduce an announcement on channel 3 the leads used would be START(3), CT1(3), etc.

10.02 If a channel is not started, no message is played back. To start the desired channel, put the CH ACCESS switch

in the access position or ground the START( ) lead. After 0 to 2.2 seconds, relay CT operates, shorting leads CT1( ) and CT2( ). This closure lasts for 0.84 to 1.48 seconds, after which:

- (a) Relay CT releases, removing the short from leads CT1( ) and CT2( ).
- (b) Relay MU operates, shorting leads MU3( ) and MU4( ), and removing the short from leads MU2( ) and MU3( ).

The announcement begins at this time.

10.03 The length of the announcement depends on the setting of the MESSAGE LENGTH switch. At the end of the announcement, relay STP operates, grounding lead LIM( ) and removing the ground from lead STP( ). At the same time, relay MU releases, shorting leads MU2( ) and MU3( ) and removing the short from leads MU3( ) and MU4( ), and 200 milliseconds later, relay STP releases, grounding lead STP( ) and removing the ground from lead LIM( ). After 1.16 seconds, relay CT operates, shorting leads CT1( ) and CT2( ). The CT relay remains operated for 1.48 seconds. When the CT relay releases, the announcement starts again, as described above. The total silence interval between message repetitions is 2.84 seconds.

10.04 The announcement continues to cycle as long as the CH ACCESS switch is in the access position or the START( ) lead remains grounded. When the CH ACCESS switch is returned to normal, or the ground removed from the START( ) lead, the announcement stops immediately. When the announcement is stopped, relay MU releases, the short is removed from leads MU3( ) and MU4( ), and leads MU2( ) and MU3( ) are shorted.

## SECTION III - REFERENCE DATA

### 1. WORKING LIMITS

- 1.01 The -48 Vdc is supplied by the talk battery through a separate dedicated filter located in the same frame containing the 13A. (See Circuit Note 104 in the SD.)
- 1.02 Maximum current drain on the -48 Vdc supply is 1.1 to 1.6A.
- 1.03 To minimize interference to the audio signals, this circuit should not be located in the same frame or adjacent to circuits that produce extraordinary electrical activity (ringing and tone equipment, selector switches, crossbar switches, or interrupter circuits).
- 1.04 All connections to this circuit shall be twisted pairs.
- 1.05 For minimum loss with multiple trunk connections and maximum crosstalk rejection and talk-through rejection, the loop resistance of the twisted pairs that connect the audio output on T1-R1 to the point where distribution is made to multiple trunk circuits shall be as low as possible. (See Circuit Note 107 in the SD.)
- 1.06 Operating temperature range is 0° to 47°C.

### 2. FUNCTIONAL DESIGNATIONS

#### 2.01 Relays

<u>Designation</u>	<u>Meaning</u>
CA	CHANNEL ACCESS
CT	CUT THROUGH
KCT	FML CUT THROUGH
KREC	RECORD
MU	MUTE
STP	STOP
VA	VOICE ALARM

### 3. FUNCTIONS

- 3.01 Provides for recording and reproducing up to eight channels of audio announcements.
- 3.02 Provides handset jacks for local recording from a G3CR-type handset or from a tape recorder via the KS-22566,L2 Interface Unit.
- 3.03 Provides, on a per-channel basis, transformer-coupled audio output and contact closures for timing.
- 3.04 Provides, on a per-channel basis, a voice alarm contact closure which is closed (in the alarm state) if there is a

loss of announcement on that channel. An alarm also occurs if the 13A is powered down or if a digital voice alarm is detected.

### 4. CONNECTING CIRCUITS

- 4.01 The following are typical connecting circuits:
- SD-1A461-01 - Electronic Switching Systems Common Recorded Announcement Frame Equipped with 13A Announcement System
  - SD-3H411-01 - Coin, Tone, Announcement and Conference Circuit
  - SD-25574-01 - Miscellaneous Circuit
  - SD-25736-01 - Coin Supervisory Circuit
  - SD-26121-01 - Crossbar Systems No. 5 Intercepting Trunk Circuit
  - SD-27980-01 - Common Systems Voice Alarm and Control Circuit
  - SD-27984-01 - Crossbar Systems No. 1 Voice Alarm Circuit
  - SD-27985-01 - Crossbar Systems No. 1 Announcement Trunk Circuit for Use with No. 6A, No. 7A, or 13A Announcement System
  - SD-32202-01 - Step-By-Step System Intercepting Trunk Circuit
  - SD-32370-01 - Step-By-Step Systems Permanent Signal Holding Trunk Circuit
  - SD-32538-01 - Step-By-Step Systems Auxiliary Coin/Trunk Circuit
  - SD-32539-01 - Step-By-Step Systems Coin Trunk Circuit
  - SD-33034-01 - Step-By-Step Systems Receiver Off-Hook Tone Connector Circuit
  - SD-35001-01 - Step-By-Step Systems Auxiliary Line Circuit
  - SD-35011-01 - Step-By-Step Systems Intercepting Trunk Circuit
  - SD-35067-01 - Step-By-Step Systems Alarm Circuit
  - SD-95959-01 - Common Systems Voice Alarm Circuit

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- SD-96510-01 - Common Systems Vacant Code or Overflow Trunk Circuit
- SD-99329-01 - Common Systems Auxiliary Permanent Signal Holding Trunk Circuit
- SD-99372-01 - Announcement Control Circuit for Centralized Repair Service
- J33017EE - Step-By-Step Systems Alarm Unit for 13A Machine

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements are contained in the following specifications:

- X-79397 - Manufacturing Testing Requirements for 13A Announcement System J1C121A (SD-97753-01)
- X-18414 - Manufacturing Testing Requirements for UD1 through UD6 Circuit Packs Used in 13A Announcement System (SD-97753-01)
- CPT-UD4/6 - Circuit Pack Test (series 15 and higher)

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SECTION IV- REASONS FOR REISSUE

B. Changes in Apparatus

Superseded

UD4-3-24 second  
VML Message  
Module, Series 1  
through 14,  
Option N

Superseded by

UD4-3-24 second  
VML Message  
Module, Series 15  
and higher, Option  
M

Superseded

UD6-3-12 second  
VML Message  
Module, Series 1  
through 14,  
Option N

Superseded by

UD6-3-12 second  
VML Message  
Module, Series 15  
and higher, Option  
M

D. Description of Changes

The 29A Magnetic Bubble Memory type UD4 and UD6 modules (option N) have been rated MFR DISC. The RAM-type UD4 and UD6 modules (option M), rated STD, have been added. The RAM-type and 29A Magnetic Bubble Memory type modules are plug-in compatible.

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DEPT 52213-RDT-REC

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