COMMON SYSTEMS
14A ANNOUNCEMENT SYSTEM
CIRCUIT

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1. PURPOSE OF CIRCUIT

1.01 This circuit provides the means for recording and reproducing standard network-type announcements preceded by special information tone (SIT) encodings.

1.02 A 14A channel, which provides reproduce-only-type service, is equipped with an ALD1 circuit pack, and a channel that provides record/reproduce-type service is equipped with an ALD2 circuit pack.

1.03 If the circuit is to be used for connection to standard announcement trunks, as in a host local central office, only the ALD1 or ALD2 circuit pack is required; one ALD1 or ALD2 for 1-channel operation, and any combination of ALD1s or ALD2s for 2-channel operation.

1.04 If the circuit is to be used for connection to a 2-wire telephone line, as in an RSM, the AWH1 circuit pack must be included along with one ALD1 or ALD2 circuit pack for 1-channel operation or any combination of ALD1s or ALD2s for 2-channel operation.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The 14A is a 2-channel microcomputer-controlled electronic announcement system that can be equipped to provide reproduce-only or record/reproduce-type service.

2.02 The 14A uses either one or two ALD1 or ALD2 circuit packs or one or two ALD1 or ALD2 circuit packs in combination with one AWH1 circuit pack, depending upon whether announcement service is to be provided to announcement trunks or to a 2-wire telephone line.

2.03 A 14A channel providing reproduce-only service is equipped with an ALD1 circuit pack that uses a multipulse linear predictive coding (MPLPC) speech synthesis algorithm to generate high-quality speech. The digital data used to generate the SIT encoding and speech is stored in an erasable programmable read-only memory (EPROM) that is mounted on a plug-in announcement module that plugs into the ALD1 circuit pack. Each announcement module provides a single announcement of up to 26 seconds in length depending on

whether a 128 kilobit or a 256 kilobit EPROM is installed in the announcement module. Each channel of the system provides a specific announcement. Announcements are changed by unplugging the installed announcement module and plugging in the announcement module for the new announcement. Announcement modules are preprogrammed to provide the specific announcement desired. Diagnostic, timing, and control functions are provided by a WE-4000 single-chip microcomputer.

2.04 A 14A channel providing record/reproduce service is equipped with an ALD2 circuit pack that uses 32-kilobit adaptive differential pulse-code modulation (ADPCM) to generate SIT encodings and high-quality speech. The digital data for the SIT encodings and the speech is stored in battery backed up 1-megabit static random-access memory (SRAM). The SRAM can store digitized speech data for announcements of up to 30 seconds in length and can retain this data even if power to the 14A is interrupted. A message can be recorded on the 14A either by speaking into a standard telephone handset or by dubbing a prerecorded message from a tape recorder or from a remote location over a telephone line. Special information tone encodings preceding a message can either be derived from a prerecorded tape or be generated by the 14A. A front panel mounted 8-character light-emitting diode (LED) display displays the programmable functions and the operating status of the system. Diagnostic, timing, and control functions are provided by an Intel 8051 single-chip microcomputer.

2.05 The AWH1 circuit pack provides for detecting and tripping the ring on the 2-wire telephone line, connecting the ALD1s or ALD2s to the line or lines, and starting the announcement or announcements.

2.06 Each channel provides (at the connector of an ALD1 or ALD2 circuit pack):

(a) a transformer-coupled audio output on leads T and R

(b) leads START and START RET, which require a closure to start the announcement

(c) a contact closure between CT1 and CT2 (cut-through), which indicates the beginning of the announcement

(d) leads MU2, MU3, and MU4 for a contact closure between MU3 and MU4 during the announcement and a contact open during the silent period at the end of the announcement

(e) the MU2 and MU3 combination for the opposite state to the MU4 and MU3 pair

(f) an STP lead, which is grounded during the announcement and is momentarily open at the end of the announcement

(g) an LIM lead for the opposite state to the STP lead

(h) a contact open between VA3 and VA2 and a contact closure between VA2 and VA1 to indicate an alarm condition

(i) leads VATST1 and VATST2, which require a closure to test the voice alarm circuit

(j) leads to connect the system to the -48 volt central office TALK battery.

2.07 Each channel equipped with an ALD2 circuit pack also provides at its connector:

(a) an RMIN input and RMOUT for interfacing an ALD2 to a remote record circuit

(b) inputs RRECN and RRECP used to input audio to the ALD2 from the remote record circuit

(c) outputs RREC3 and RREC4 used to output audio from the ALD2 to the remote record circuit

(d) the D0 through D7 inputs/outputs used to receive/send program data from/to the remote record circuit.

2.08 Each channel provides (on the front panel of an ALD1 circuit pack):

(a) an AUDIO MONITOR jack used for local monitoring of the announcement

(b) a manual RESET switch

(c) a SET LEVEL/NORMAL switch used for setting transmission level

(d) a light-emitting diode (LED) to indicate whether the system is in normal operation or in the transmission level set mode

(e) a VOICE ALARM LED to indicate a voice alarm condition

(f) a MEMORY FAILURE LED to indicate an announcement module memory failure

(g) a LEVEL ADJUST potentiometer to set the transmission level.

2.09 Each channel equipped with an ALD2 circuit pack (Record/Reproduce) provides on the front panel:

(a) a modular telephone jack used to record or monitor an announcement through a telephone handset

(b) a tape jack used when recording an announcement from a tape recorder

(c) a VOICE ALARM LED to indicate a voice alarm condition

(d) an 8-character alphanumeric LED display to indicate the program options and the operational status of the channel

(e) a MENU switch used to step through the program menu displayed on the alphanumeric display

(f) a SLECT switch to select the desired program option

(g) a LEVEL ADJUST potentiometer to set the transmission level.

2.10 Each channel provides (at the connector of an AWH1 circuit pack):

(a) leads T and R to connect to the 2-wire telephone line being served

(b) leads START and START RET, which provide a closure to the ALD1 circuit pack to start the announcement

(c) leads CT1 and CT2 (cut-through), which receive a closure from the ALD1 circuit pack to indicate the beginning of the announcement

(d) leads to connect the circuit to the -48 volt central office TALK battery

(e) leads T and R for connection to the audio output T and R leads of the ALD1 circuit pack.

SECTION II - DETAILED DESCRIPTION

1. ALD1 CIRCUIT PACK

GENERAL DESCRIPTION

1.01 All the circuitry for storage, generation, and control of an announcement for each channel of a 14A providing reproduce-only service is contained on the ALD1 circuit pack. The principal components of this circuit are a WE-4000 microcomputer, a 439B2 speech synthesizer, a plug-in EPROM announcement module, a digital-to-analog converter, a transformer-coupled audio output, and a set of relays to provide signaling to the announcement trunk circuits.

1.02 A family of announcement modules provides for playback of all standard network announcements. One ALD1 is installed for 1-channel operation, and two ALD1s are installed for 2-channel operation.

DETAILED DESCRIPTION

1.03 Power for the circuit is derived from a board-mounted dc to dc converter that converts the -48 volt central office TALK battery to the voltages required by the circuit. These voltages are +5, +15, and -15 volts.

1.04 The 8.192 MHz master clock signal is derived from the oscillator circuit (IC14). The output of IC14 (pin 8) is supplied to the CLKIN input (pin 1) of the 439B2 speech synthesizer (IC15). The 439B2 uses the 8.192 MHz signal as its clocking frequency and also provides a buffered output through the CKO output (pin 2). This buffered output is fed to the input (pin 1) of a dual 4-bit binary counter (IC10). The signal at the QD2 output (pin 8) of IC10 is divided by 256, which produces a frequency of 32 kHz. This frequency is supplied to the input (pin 1) of IC11. The output of QB1, IC11 (pin 4), is the input frequency divided by 4 or 8 kHz. This is the sampling rate frequency of the pulse-code modulation (PCM) output from the SDO (pin 19) output of the 439B2. The 8-kHz signal is fed to the CLK input (pin 3) of the D-type flip-flop (IC13A). The Qbar output (pin 6) is fed to the SYN input (pin 6) of the 296B codec (IC4). The Q output (pin 9) is fed to the OSYN (pin 18) of the 439B2. This signal synchronizes the output PCM data from the 439B2 to the input of the codec. The QB1 (pin 4), divide-by-four output of IC10, supplies the 2.048-MHz clock required by the codec to clock in the 8-bit PCM data word derived from the 439B2. The inverted 2.048-MHz signal is supplied to the OCLK (pin 17) input of the 439B2, where it is used to clock out the serial 8-bit PCM data.

1.05 The QA1 (pin 3), divide-by-two output of IC10, supplies the 4.096-MHz clock signal to the WE-4000 microcomputer (IC7). The WE-4000 used in the 14A (coded 377CBA) is a single-chip microcomputer with its program data stored in a masked programmed ROM. The 377CBA is a custom device and is used only in the 14A. The 377CBA provides the necessary diagnostic, timing, and control functions required.

1.06 When the system is powered up, the reset inputs of the 377CBA and the 439B2 are held at a logic low level (low) because of the action of R5 and C22. The combination of R5 (10 kilohms) and C22 (100 microfarad) produces a time-constant of 1 second. In about this time, C22 has charged from 0 volts (input to IC1E, pin 11 low) to 3 volts [input to IC11E, logic high (high)]. At this time, transistor Q1 switches off, removing the low-impedance connection to ground from the CLOCKOUT/RESET (pin 21) of the 377CBA.

At the same time, the reset inputs (pins 3, 14, and 29) of the 439B2 go high. Both devices have now been reset. During the reset interval, both LEDs (CR7 and CR13) are lighted and should extinguish at the end of the reset interval (about 1 second). If CR13 remains on, a voice alarm condition exists, and the unit will not function. The causes of voice alarms are described below.

1.07 After initialization, the 377CBA performs diagnostic tests that check its own operation and the speech data stored in the announcement module memory. The first diagnostic test checks the internal random-access memory (RAM) locations used by the 377CBA. The second test checks the IOL0-IOL6 output latches of the 377CBA. In the third test, the 377CBA calculates the checksum of its program data stored in its internal ROM. When these tests have been completed, the data in the announcement module memory is checked. This is accomplisned by having the 377CBA calculate the checksum of the data in the announcement module memory and compare this value with the value stored in the announcement module memory. If any of these diagnostic tests should fail, the 377CBA is reinitialized (not reset), and all tests are repeated. If the test that failed the first time fails the second time, the voice alarm relay is de-energized, and the VOICE ALARM LED lights. If the failure is in the announcement module memory, the MEMORY FAILURE LED also lights. Each test must fail twice in a row before a voice alarm is actuated. This is done to minimize voice alarm actuations caused by glitch-induced soft errors.

1.08 The 377CBA has a mechanism that provides a sanity check of program operation. If some type of fault causes the program control to go awry, the CPU of the 377CBA causes the program control to go to a particular program memory location called a trap. At this location, a routine is executed when a trap condition occurs. This routine attempts to clear the trap condition by reinitializing the 377CBA. If the trap condition is not cleared, because of some failure, the voice alarm circuit is actuated. Another sanity check is provided by the dual long delay timer (IC16). One of these timer circuits is used in a retriggerable monostable mode. If the PT (pin 4) input does not have a low-to-high transition in less than 50 seconds, the timer will time out causing the Q output (pin 7) to go low, which will trigger the monostable flip-flop (IC17A). This produces about a 4-microsecond pulse, which resets the 439B2 and the 377CBA. The PT input (pin 12) of IC16B is now high, which enables the second timer circuit. If the PT input of IC16A does not receive a low-to-high transition in another 50-second time period, IC16B times out, and the voice circuit is actuated.

1.09 A request for an announcement is signaled to the 14A in two ways:

(1) a closure of START to START RET

(2) the insertion of a handset in the AUDIO MONITOR phone jack.

The 377CBA recognizes any of these events when a low occurs at the IN0 input (pin 2). While IN0 is high, the 377CBA generates addresses that allow it to read the first and last locations in the announcement module memory. These locations contain data that is the same for all announcement module memories. If a failure should occur here, the response is the same as that described in paragraph 1.07. This procedure is repeated as long as the IN0 remains high. When an announcement request has been acknowledged by the 377CBA (IN0 low), the announcement sequence begins by the energizing of relays K1 and K5. The energizing of K1 causes a closure of contacts CT1 and CT2 (CUT THRU), and the energizing of K5 causes the output of the audio amplifier, IC5 (pin 8), to be disconnected from transformer T1 and the input of T1 to be connected to R35. The 377CBA now writes data to the 439B2 causing it to synthesize a 1-kHz tone. The 1-kHz analog output of the codec, IC4 (pin 13), is amplified by audio amplifier IC5 and supplied to the input of the 1-kHz bandpass filter (IC6). The output of IC6 is fed through resistor R44 to the base of transistor Q6. The combination of Q6 and CR9 half-wave rectify the 1-kHz sine-wave signal. Capacitor C26 charges to about 5.7 volts because of the clamping action of CR8. The input (pin 13) of IC1F is high, and the output (pin 12) is low. The 377CBA now polls input IN2 (pin 4) expecting a low. A high on the IN2 input is an indication of a failure in the audio circuit. The 377CBA resets the 439B2 and repeats the test. If the test fails again, the voice alarm circuit is actuated. If the test passes, the CUT THRU interval (1 second) ends, and relays K1 and K5 are de-energized. Contacts CT1 and CT2 open; the audio amplifier is connected to T1; and R35 is disconnected from the input of T1. Relay K2 is now energized, which causes a contact opening between MU2 and MU3 and a contact closure between MU4 and MU3. The announcement now begins. The announcement is produced when the 377CBA generates addresses in sequence and supplies these addresses to the announcement module memory and writes the data to the 439B2. This is accomplished after the 377CBA reads the contents of the first six locations in the announcement module memory (address

locations 0-5. The data in these locations is as follows (in hex):

Address	Data
0x0	0x11
0x1	Low byte of byte count
0x2	High byte of byte count
0x3	0x11
0x4	2s complement of announcement module memory checksum
0x5	Announcement module memory checksum.

The 0x11 is a no-op instruction to the 439B2, which causes it to ignore the next two bytes of data written to it. At this time, the 377CBA ignores 0x11 and the 2s complement of the announcement module memory checksum. It, however, reads the byte count and announcement module memory checksum data and stores these values in its internal RAM. The 377CBA now begins to write the data stored in the announcement module memory (starting at address 0x0) to the 439B2. The announcement now starts. The first eight address bits (A0 through A7) are derived from the IOB0 through IOB7 ports of the 377CBA, and address bits A8 through A14 are derived from the IOL0 through IOL6 ports. The IOB0 through IOB7 ports are bidirectional in that they may be configured as outputs or inputs. The IOB0 through IOB7 ports are connected to the D (data) inputs of an 8-bit transparent latch (IC8). As long as the ENG (pin 11) input remains high, the Q outputs are the same as the inputs. However, when the ENG input goes low, the Q outputs are held in the state they were in when input ENG went low. Thus while input ENG is low, address bits A0 through A7 are held on the Q outputs of IC8, and ports IOB0 through IOB7 can then be changed from outputs to inputs. At this time, data from the announcement module memory can be placed on the bus. This is done when the IOL9 (pin 33) port of the 377CBA goes low. This signal changes the data outputs of the announcement module memory from a high-impedance state (tri-state) to an active state. The data from the announcement module memory may now be read by the 377CBA and written to the 439B2 when the IOL10 (pin 34) port of the 377CBA goes low. Handshaking communication between the 439B2 and the 377CBA is obtained through the connection of the IBAI (pin 35) output of the 439B2 to the IN3 (pin 5) input of the 377CBA. After writing to the 439B2, the 377CBA polls the IN0 and IN3 inputs. If IN3 is high (START-START RET opened); the 439B2 is reset; the announcement stops; and no more data is written to the 439B2. If IN3 is high, the 377CBA waits until IN3 goes low before writing the next byte to the 439B2. During the time the data is valid on the bus, the 377CBA reads the data and adds its value to the sum of the previous values. This is the procedure for calculating the checksum of the announcement module memory data. At the end of each read-write cycle, the address value is incremented by one, and the value of the byte count stored in the RAM is decremented by one. The above procedure is then repeated for the new address value. This procedure continues until the value of the byte count reaches zero. This marks the end of the announcement. Relay K2 is de-energized, which closes contacts MU2 and MU3 and opens contacts MU4 and MU3. Relay K3 is then energized for 200 microseconds, closing the LIM and GRD contacts and opening the STP and GRD contacts for this time. The PT input (pin 4) of IC16A is pulsed, which prevents it from timing out. The 377CBA now compares the value of the announcement module memory checksum calculated during the previous announcement cycle with the value read from the announcement module memory at the beginning of the cycle. If the values do not compare, the 377CBA is reinitialized and the diagnostic tests described in paragraph 1.07 are repeated. If the announcement module memory test fails the second time, the voice alarm circuit is actuated, and both alarm LEDs are lighted. If the values compare, the 377CBA again polls the IN0 input after a 0.5-second delay.

1.10 A front panel switch (SET LEVEL/NORMAL) is provided to enable the transmission level of the announcement to be set easily. When switch S1 is actuated, a low appears at the IN1 input of the 377CBA. When the 377CBA acknowledges this low, it writes a tone instruction to the 439B2. The 439B2 then synthesizes a 1-kHz tone. This tone is at a reference level that is used to set the transmission level. The output level is changed by adjusting the LEVEL ADJUST control (R19). With R19 turned fully clockwise, the nominal level of this 1-kHz tone at the T(20) and R(50) terminals of the connector is +7.3 dBm. When the level set function is actuated, LED CR1 is lighted. Normal operation (announcement mode) is indicated when CR1 is extinguished.

1.11 A voice alarm condition can be cleared by actuating the RESET switch. If the alarm condition was caused by some temporary malfunction (soft error), the alarm condition will clear; the alarm LED will extinguish; and the system will function normally. However, if the alarm condition was caused by some permanent failure, the alarm condition will not clear, and the system should then be taken out of service.

2. AWH1 CIRCUIT PACK

GENERAL DESCRIPTION

2.01 All the additional circuitry required for connecting the 14A in a 2-wire telephone line application is contained on the AWH1 circuit pack. The principal components of this circuit are a TI 1520A ring detector, a WE 2C opto-isolator, a binary counter, an announcement repeat switch, and a relay.

DETAILED DESCRIPTION

2.02 The AWH1 circuit pack contains two circuits, one for each of the ALD1s or ALD2s that can be installed. Both circuits are identical and have the same function. Each circuit is connected by factory-installed surface wires to each of the connectors of the ALD1 or ALD2 circuit packs. Thus, with a 14A equipped with an AWH1, 1-channel announcement service can be provided if one ALD1 or ALD2 is installed, and 2-channel announcement service can be provided if two ALD1s or ALD2s are installed. Power for the circuit is derived from a board-mounted dc to dc converter that converts the -48 volt central office TALK battery to the +5 volt direct current required by the circuit.

2.03 Ring detector IC1 (or IC101) is actuated by a ring voltage in the range of 40 volts at 16 hertz through 150 volts at 68 hertz, which generates a signal suitable to drive opto-isolator U1A (or U101A) whose output is noninverting and will be at a high level during ringing. The output (pin 7) of U1A (or U101A) is supplied to the CLK input (pin 3) of flip-flop IC3A (or IC103A), whose output signal on pin 5 will operate relay K1 (or K101). With the K1 (or K101) relay operated, the TIP (pin 20) and RING (pin 50) leads of the ALD1 circuit pack are connected through the AWH1 circuit pack to the TIP and RING leads of the 2-wire telephone line being served. With relay K1 (or K101) operated, a closure is also applied to the START (pin 26) and START RET (pin 5) leads of the ALD1, which starts the announcement and trips the ringing signal. At the beginning of each announcement, the ALD1 or ALD2 circuit pack generates a CT pulse. This pulse (after being inverted) is supplied to the input (pin 10) of multivibrator IC4B (or IC104B) whose output (pin 5) is free from any debounce problems and whose width (7 microseconds) is determined by R12 and R112 (30.1 kilohms) and C8 and C108 (680 picofarads). This output is fed into the input CLK (pin 2) of 4-bit binary counter IC5 (or IC105) and to the input clock (pin 11) of flip-flop IC3B (or IC103B) whose output is used to load the previously mentioned counter. A 4-pole announcement repeat dual in-line package (DIP) switch (S1 or S101) is connected to the data input of the counter, and by selecting the desired sequence of switch settings, the announcement that has a maximum length of 13 (or 26) seconds can be repeated up to 15 times. When the counter reaches the preset value of repeats, it will generate a pulse that (after being inverted) is used as the input of an AND gate (IC7B, pin 4) (or IC7C, pin 9). The output is supplied to the input (pin 1) of multivibrator IC4A (or IC104A), whose output will clear flip-flops IC3A and IC3B (or IC103A and IC103B), which will open the K1 (or K101) relay and consequently reset the 14A and signal an on-hook line condition. A loop current detector circuit is also provided in case the user hangs up before the selected number of announcements have occurred. Opto-isolator U1B (or U101B) will detect an interruption in the loop current in the line, and the output level (pin 6) will slowly change from almost zero volts direct current to 5 volts direct current. This output will be supplied to the input clock (pin 3) of flip-flop IC6A (or pin 11 of IC6B), whose output is used as an input (pin 5) to AND gate IC7B (or pin 10 to IC7C). The pin 6 (or pin 8) output is fed into the input (pin 1) of multivibrator IC4A (or IC104A), whose output will clear flip-flops IC3A and IC3B (or IC103A and IC103B), which opens the K1 (or K101) relay and consequently resets the 14A and signals an on-hook line condition. The purpose of multivibrator IC4A (or IC104A) is to extend the input pulse and make the reset more stable. The pulse width is determined by the values of capacitor C12 (or C112) and resistor R13 (or R113). The circuit is provided with back-to-back diode CR1 (or CR101) for lightning surge protection, in addition to PTC devices RT1 and RT2 (or RT101 and RT102) for protection against ac line failure. In the event that an ac line falls across a telephone line, protection will be provided up to 600 volts alternating current.

3. ALD2 CIRCUIT PACK

GENERAL DESCRIPTION

3.01 Purpose of Circuit

The ALD2 circuit pack is designed to provide a means for recording and reproducing network-type announcements for the 14A announcement system. Recordings are made by speaking the message into a telephone handset or by dubbing a prerecorded message from a tape recorder or from a remote location over a telephone line. The speech is encoded using a 32-kilobit per second adaptive differential pulse-code modulation (ADPCM) algorithm. The digitized speech data for the announcement is stored in a battery backed up 1-megabit static random-access memory (SRAM). The ALD2 therefore can provide announcements of up to 30 seconds in length and can retain the encoded speech data in the memory if power to the ALD2 is interrupted. The special information tones (SIT) that precede some announcements can be derived from prerecorded tapes of these announcements or can be generated by the ALD2. All diagnostic and control functions

for the ALD2 are provided by an Intel 8051 single-chip microcomputer.

DETAILED DESCRIPTION

3.02 Major Components

The ALD2 circuit pack contains digital and analog circuitry. The major digital circuit components of the ALD2 are an 8051 microcomputer, an ADPCM speech processor, a 1-megabit SRAM, and an 8-character light-emitting diode (LED) alphanumeric display. The major analog circuit components of the ALD2 are a unity gain input buffer amplifier, an automatic gain control circuit, lowpass filters, and a transformer-coupled audio output amplifier.

3.03 Digital Circuit

(a) Bus Structure

The ALD2 has three buses: an 8-bit data bus, a 16-bit main address bus, and a 3-bit device-select address bus. The data bus links the 8051 microcomputer (IC9) to the ADPCM speech processor (IC10), the announcement memory (IC14), the 8-character LED display (IC23), the relay function latch (IC7), and the octal bus transceiver (IC11). The 16-bit main address bus is used when the 8051 accesses the announcement memory and when programming the 8-character LED display. The 3-bit device-select address bus is used when the 8051 accesses the peripheral devices.

(b) 8051 Microcomputer

The main control element on the ALD2 is the 8051 microcomputer (IC9). The 8051 handles all control and diagnostic functions for the ALD2. It operates at 12 megahertz and has an internal 4096-byte read-only memory (ROM) for program storage and four 8-bit input/output ports (P0-P3). The P0 port is the multiplexed low-order main address and data bus during accesses to the announcement memory and peripheral devices. The P2 port supplies the high-order address bits. The P1 port supplies the 3-bit device-select address bus and special control functions. The P3 port provides two interrupt inputs: read/write, and additional special control functions. When accessing announcement memory, the P0 port is first configured to provide the low-order address bits. At this time, the address latch enable (ALE) is high (logic level 1), and the outputs (1Q through 8Q) of IC13 are the same as the inputs (1D through 8D). The address latch enable (ALE) then goes low (logic level 0), and the P0 port is configured as a data input/output port. The low-order address bits are latched on the outputs of IC13, and the high-order address bits are provided by P2. The announcement memory and each peripheral device has a 3-bit device-select address that is provided by P11, P12, and P13. The P11, P12, and P13 ports are connected to the inputs (A, B, and C) on a 3-to-8 line decoder (IC12). The outputs (0 through 7) of IC13 are connected to the chip select (CS) inputs of each peripheral device. A 3-bit value on the input of IC13 causes one of its eight outputs to be low, and the device whose CS is connected to the low output is the one selected. The announcement memory also requires a seventeenth address bit, which is provided by P10.

(c) Powerup Reset

The ALD2 has circuitry to ensure that it is properly initialized after powerup. When the ALD2 is powered up, the 8051 is held in a reset state (input RST high) until the power supply voltages have stabilized. Capacitor C56 charges from 0 to 5 volts through a 10-kilohm resistor. The RST stays high until the voltage on pin 9 of IC1 exceeds about 2.5 volts. When the RST goes low, the 8051 becomes active. After initializing internal registers, the 8051 performs diagnostic tests on the ALD2 to ensure proper operation. If a diagnostic test fails, the display blinks and the voice alarm relay will be in the alarm state. If an announcement has not been previously recorded, the display will blink RECORD, and the voice alarm relay will be in the alarm state. The display will blink and the voice alarm will remain in the alarm state until the record mode is selected.

(d) Eight-Character Alphanumeric LED Display

A front panel mounted 8-character alphanumeric LED display is used to display to the user the programmable functions and the operational status of the ALD2. The display is a "smart display" in that character decoding and programmable functions are provided by the display. When programming the display, the 8051 generates its device-select address on P1, and accesses the display control word register or the character RAM. The control word register is an 8-bit register that performs five functions. They are brightness control, flash RAM control, blinking, self-test, and clear. During normal operation, the display is programmed for a minimum brightness of 13 percent and for a steady display (not blinking). If a failure is detected by the 8051, the display is programmed to blink on and off at about a 2-hertz rate and for a brightness of 27 percent of maximum. The flash function is not used. When the CHK SYS function is selected, the self-test function of the display is invoked. During the self-test function, major portions of the display circuitry are exercised, and all LEDs are illuminated. D5 (pin 26) is set to 1 if the self-test passes and to 0 if the self-test fails. The character RAM stores the ASCII data for each character

displayed. Address lines A0 through A3 are used to select the location in the character RAM when the 8051 writes the ASCII data to the display.

(e) Speech Processor

The ALD2 uses an ADPCM speech processor (SP) (IC10) to encode and decode the SITs and the speech for the announcements. This device has both analog-to-digital (AD) and digital-to-analog (DA) converters and ADPCM analysis and synthesis circuitry integrated into a single-chip, 40-pin dual in-line package (DIP). When encoding, the SP has as an input the analog speech and as an output the digital ADPCM data that is sent to the announcement memory for storage. When decoding, the SP inputs the ADPCM speech data stored in the announcement memory and outputs the analog speech for the announcement. The SP has two modes of operation controlled by the data command (D/$\overline{C}$) input. When the D/$\overline{C}$ is low, the SP is in the command mode, and the 8051 can command the SP to start encoding (record) or to start decoding (playback). The D/$\overline{C}$ input is connected to P15 of the 8051. To start recording, the 8051 makes P1 equal C0 Hex (D/$\overline{C}$ and $\overline{CS}$ low) and writes 04 Hex to the SP through the data bus. To start playback, P1 equals C0 Hex and 02 Hex is written to the SP. When the D/$\overline{C}$ and $\overline{CS}$ inputs go high (data mode), P1 equals FF Hex, and the record/playback functions of ALD2 begin. During the record function, the SP samples the incoming analog speech signal every 125 microseconds (8-kHz rate) and encodes each sample into 4-bit ADPCM data. An internal buffer stores the ADPCM data until two samples of the speech have been accumulated. The SP then signals the 8051 that data is available by pulsing its MCK output high. When the MCK output goes high, the $\overline{INT0}$ input of the 8051 goes low, because of the inversion of MCK by IC2D. The 8051 outputs the device-select address for the SP (P1 equals F0 hex). As a result, the D/$\overline{C}$ input is high (data mode), and the $\overline{CS}$ input is low. The ADPCM data in the SP buffer is supplied to the data I/O pins of the SP. The 8051 reads the ADPCM data into its internal RAM and then writes it to a location in the announcement memory. When the 8051 has read the ADPCM data from the SP, it computes a checksum of the data by adding each byte read to the sum of all the previous data. When the recording ends, the final value of the checksum and the number of bytes read by the 8051 is written to the first five locations of the announcement memory. The playback function is essentially the reverse of the record function. During the playback function, the SP pulses its MCK output high to signal the 8051 that the SP requires ADPCM data. The 8051 reads the ADPCM data from the announcement memory, computes the checksum, and writes the data to the SP. Each byte of ADPCM data contains two samples of the analog speech. Therefore, the record/playback write/read cycle time is equal to 250 microseconds, twice the sample period. The record/playback functions are ended when the 8051 resets the SP by making P1 equal FB Hex.

(f) Announcement Memory

The ADPCM data for the SIT encodings and speech is stored in the announcement memory (a 1-Mb SRAM). The announcement memory requires 17 address bits (A0 through A16) for complete access to all locations. The 8051 addressing capability is only 16 bits (A0 through A15). The seventeenth address bit is provided by P10. The announcement memory is organized into two halves: the lower half with address range 0 through 0FFFF Hex and the upper half with address range 10000 through 1FFFF Hex. The value of P1 determines which half of the memory is accessed. When P1 equals FC Hex, the lower half of the announcement memory is accessed, and when P1 equals FD Hex, the upper half is accessed. In addition to the ADPCM speech data, the announcement memory contains data used by the 8051 during announcement playback. The first three locations (addresses 0 through 2) contain the maximum address range of the ADPCM data. This determines the length of the announcement. The next two locations (addresses 3 and 4) contain the checksum of the ADPCM data that was calculated during the record function. During playback, the checksum of the speech data in the announcement memory is computed by the 8051. At the end of the announcement, the playback checksum is compared with the value stored in memory locations 3 and 4. This provides a check of the integrity of the ADPCM data and a mechanism for activating a voice alarm if a failure of the announcement in the memory should occur. The 8051 counts the number of times the announcement is played when the ALD2 is in the IN-SERVICE mode. This count, called the PEG count, is stored in four memory locations (address 1F100 through 1F103 Hex). These addresses are accessed by the 8051 and are shown on the 8-character LED display when the PEG CNT function is selected. If the power is interrupted while the ALD2 is in the IN-SERVICE mode, the 8051 is capable of automatically placing the ALD2 in the IN-SERVICE mode once power is restored. When the ALD2 is placed in the IN-SERVICE mode, the 8051 accesses a memory location (address 1F104 Hex) and writes 5A Hex into this location. After the ALD2 is powered up, the 8051 reads the value in address 1F104 Hex, and if the value read by the 8051 is equal to 5A Hex and powerup diagnostics have passed, the 8051 places the ALD2 in the IN-SERVICE mode. If the 8051 reads a value of 0 in address 1F104 Hex, and powerup diagnostics have passed, the 8051 places the ALD2 in the local mode (LOC MODE). In order to prevent the loss of the data in the announcement memory, the supply

voltage to the announcement memory is backed up with a battery. When the power to ALD2 is interrupted, the comparator circuit (IC22) senses the loss of the +5 volt supply voltage. The output of IC22 (pin 1) is normally high. When the +5 volt supply has dropped by about 0.4 volt, the output of IC22 switches low. The enabling input of IC16A (pin 1) is connected to the output of IC22. A low on pin 1 of IC16A causes its output (pin 3) to switch to a high-impedance state, which disables the CS input (pin 22) of the announcement memory (IC14). When the +5 volts has reached about 2.6 volts, the announcement memory is powered from the backup battery.

(g) Sanity Timer

The ALD2 has a timer circuit that provides for a sanity check of the 8051 program operation. This circuitry is provided by ICs 4, 5, and 6. During normal operation, the 8051 resets this circuit periodically to prevent it from timing out. If the 8051 fails to reset this circuit for 32 milliseconds, the circuit times out. The first time-out resets the 8051 by pulsing the RST input high. If the time-out was caused by a soft error condition cleared by the reset, the 8051 resumes normal program operation. If the error condition is not cleared, the 8051 fails to reset the sanity timer, and a second time-out period occurs. This second time-out actuates the voice alarm (VA) relay and lights the VOICE ALARM LED on the front panel.

(h) Remote Record

Announcements can be recorded on the ALD2 from a remote location over a standard telephone line when the ALD2 is connected to a remote record circuit. The ALD2 is programmed by the remote record circuit over the D0 through D7 external input/output data lines. The ALD2 can be programmed by the remote record circuit to record, playback, generate the appropriate SIT encoding, run diagnostics, and go into the IN-SERVICE mode. The ALD2 is signaled for programming by the remote record circuit by bringing the RMIN input low. If the ALD2 is playing an announcement, the announcement is completed before responding to the remote record request. When the ALD2 responds, the 8051 reads the data on D0 through D7 through the octal bus transceiver (IC11). If a valid program code is received, the ALD2 brings RMOUT low and sends the remote record circuit 20 Hex through IC11. If the program code from the remote record circuit is not valid, the ALD2 sends 10 Hex. Valid program codes are shown in Table A.

TABLE A

PROGRAM CODE	MEANING
01	RECORD
02	PLAYBACK
03	GO IN-SERVICE
04	DIAGNOSTIC REQUEST
05	NO-OP
06	NO-OP
07	EXIT
80 Hex + N	GENERATE SIT NO. N

Where N = 01 to 20 Hex

Recording and playback are stopped by the remote record circuit by making RMIN low. When recording or playback is ended, the ALD2 makes RMOUT low and sends 20 Hex through IC11. A diagnostic request from the remote record circuit causes the ALD2 to test the 8051 program memory, the announcement memory, and the audio output circuit. When the diagnostic function is completed, the ALD2 sends the remote record circuit 20 Hex if all tests have passed and 09 Hex if any test fails. If a diagnostic request detects a failure or the remote record circuit fails to respond to the ALD2 signals or if two invalid opcodes in sequence are received by the ALD2, the ALD2 has a means for exiting the remote mode. If no recording was made during the remote mode session, the ALD2 returns to the IN-SERVICE mode. However, if a recording was made and the GO IN-SERVICE command was not received by the ALD2, the ALD2 voice alarm relay is actuated, and the display flashes REM MODE.

3.04 Analog Circuit

(a) Audio Input

The audio for the announcement to be recorded can be supplied to the ALD2 through three different inputs: the remote record input line (RRECN-RRECP), the tape jack (J1), and the telephone handset jack (J2). All these inputs are connected to a unity-gain audio amplifier (IC17). The output of the unity-gain amplifier is supplied to the automatic gain control (AGC) circuit (IC18). The AGC circuit maintains a constant audio level of about -3.0 Vu at the input of the speech processor (IC10) for audio levels between -20 and +10 Vu at any of the above inputs of the ALD2. The output from the AGC circuit is filtered by IC19 before being supplied to the speech processor for encoding. Integrated circuit IC19 contains two low-pass switched capacitor filters, each with a cutoff frequency of 3 kilohertz.

(b) Audio Output

The decoded audio output of the speech processor is first filtered by IC19 and then supplied to the audio output amplifier (IC20) through the level adjust potentiometer (R22). Transformer T1 provides output isolation and an output impedance of about 1 ohm. An additional winding on T1 supplies audio to the telephone handset jack (J2) and to the remote record circuit through output lines RREC3-RREC4. During each cut-through interval, the audio output section is checked. This is done by having the speech processor (IC10) generate a 1-kilohertz tone during the cut-through interval. The 1-kilohertz tone is supplied to the input of a 1-kilohertz bandpass filter (IC21). The detected output of IC21 charges C49 to +5 volts (logic 1) if the 1-kilohertz tone is present. If the 1-kilohertz tone is present, the input to the 8051 (pin 15) is low, and the announcement starts at the end of the cut-through interval. If the 1-kilohertz tone is not present, pin 15 of the 8051 is high; the voice alarm relay actuates; and the display will blink AUD FAIL.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 The -48 volt direct current is supplied by the TALK battery to minimize electrical noise interference. The SIGNAL battery can be used if the TALK battery is not available.

1.02 The typical current drain on the -48 volt dc supply is 0.16 ampere for each ALD1 or ALD2 and 0.030 ampere for the AWH1.

1.03 To minimize interference to the audio signals, this circuit should not be located in the same frame or adjacent to circuits that produce extraordinary electrical activity (ringing and tone equipment, selector switches, crossbar switches, or interrupter circuits).

1.04 Connections to this circuit can be made with single-wire grounded connections when required. However, minimum noise interference will be achieved with twisted pair connections.

1.05 For minimum loss with multiple trunk connections and for maximum crosstalk rejection, the loop resistance of the twisted pairs that connect the audio output T-R leads to the point where distribution is made to multiple trunk circuits shall be as low as possible. (See Circuit Note 103 on SD-97798-01.)

1.06 The operating temperature range is 0 through 55 degrees Celsius.

2. FUNCTIONAL DESIGNATIONS

2.01 Relays

Designation	Meaning
CT	Cut Through
MU	Mute
STP	Stop
LIM	Limit
VA	Voice Alarm

3. FUNCTIONS

3.01 The 14A Announcement System equipped with an ALD1 circuit pack or packs (reproduce only) has the following features.

(a) It provides for reproducing up to two channels of audio announcements preceded by SIT encodings.

(b) It provides for changing announcements through nonvolatile preprogrammed plug-in circuit modules.

(c) It provides an AUDIO MONITOR jack.

(d) It provides, for each channel, a transformer-coupled audio output and contact closures for signaling.

(e) It provides, for each channel, a continuous automatic self-diagnosis by a microcomputer.

(f) It provides, for each channel, a voice alarm closure or an opening (in the alarm state) if loss of power or loss of the announcement should occur.

(g) It provides, for each channel, a 1-kHz reference tone for announcement level adjustment.

(h) It provides for connection to standard announcement trunks or to a 2-wire telephone line.

3.02 The 14A Announcement System equipped with an ALD2 circuit pack or packs (Record/Reproduce) has the following features.

(a) It provides for recording and reproducing up to two channels of announcements, which can be preceded by SIT encodings.

(b) It provides for changing announcements by recording from a telephone handset, from a tape recorder, or from a remote location over a telephone line.

(c) It provides an 8-character LED display to indicate program options and operational status.

(d) It provides for programming the system from front panel mounted switches.

(e) It provides for the selection and optional internal generation of SIT encodings.

(f) It provides, for each channel, a transformer-coupled audio output and contact closures for signaling.

(g) It provides, for each channel, continuous automatic self-diagnosis by a microcomputer.

(h) It provides, for each channel, a voice alarm closure or an open circuit (in the alarm state) if loss of power or loss of the announcement should occur.

(i) It provides, for each channel, a 1-kHz reference tone for announcement level adjustment.

(j) It provides for connection to standard announcement trunks or to a 2-wire telephone line.

(k) It provides for connection to a remote record circuit.

4. CONNECTING CIRCUITS

4.01 The following are typical connecting circuits.

SD-5D015-01	5ESS* Switching Equipment, Modular Metallic Service Unit
SD-5D130-01	5ESS* Switching Equipment, Miscellaneous Cabinet (6 Ft) Circuit
SD-25574-01	Miscellaneous Circuit
SD-25736-01	Coin Supervisory Circuit
SD-26121-01	Crossbar System, No. 5 Intercepting Trunk Circuit
SD-27980-01	Common Systems, Voice Alarm and Control Circuit
SD-27984-01	Crossbar System, No. 1 Voice Alarm Circuit
SD-27985-01	Crossbar System, No. 1 Announcement Trunk Circuit for use with No. 6A, 7A, 13A, or 14A Announcement System
SD-32202-01	Step-by-Step System, Intercepting Trunk Circuit
SD-32370-01	Step-by-Step System, Permanent Signal Holding Trunk Circuit
SD-32538-01	Step-by-Step System, Auxiliary Coin/Trunk Circuit
SD-32539-01	Step-by-Step System, Coin Trunk Circuit
SD-33034-01	Step-by-Step System, Receiver Off-Hook Tone Connector Circuit
SD-35011-01	Step-by-Step System, Intercepting Trunk Circuit
SD-35067-01	Step-By-Step System, Alarm Circuit
SD-95959-01	Common Systems, Voice Alarm Circuit
SD-96510-01	Common Systems, Vacant Code or Overflow Trunk Circuit
SD-99329-01	Common Systems, Auxiliary Permanent Signal Holding Trunk Circuit
CRI-1A139-13	1ESS+ and 2ESS+ CRI/DCS for Recorded Announcement Frame

* Registered trademark of AT&T
\+ Trademark of AT&T

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The manufacturing testing requirements for the 14A Announcement System are in the X-80062 specification.

SECTION IV - REASONS FOR REISSUE

A. Changed and Added Functions

A.1 The ALD2 circuit pack (shown in CPS 4) has been added (as option V) to provide a record/playback capability.

B. Changes in Apparatus

B.1 Removed	Replaced By
CR1, CR101 Diode MKT1V200B - CPS 3	CR1, CR101 Diode WP-90282,L6 - CPS 3
IC15 Integrated Circuit 439B - CPS 1	IC15 Integrated Circuit 439B2 - CPS 1

B.2 Added

Circuit Pack ALD2 - CPS 4, App Fig 4, FS 3, FS 4 - V Option

D. Description of Changes

D.1 In CPS 1, speech synthesizer 439B (designated IC15) has been removed and replaced by 439B2.

D.2 In CPS 1 Drawing Note 103, designation IC15 has been changed.

D.3 The ALD2 circuit pack (shown in CPS 4, App Fig 4, FS 3, and FS 4) has been added (as option V) to provide a record/playback capability.

D.4 In CPS 1, the Record of Changes table has been changed by the addition of Drawing Issue 8B, Series Number 4, and See Note 203.

D.5 Drawing Issue 8B has been added in the CPS 2 Record of Changes table.

D.6 Drawing Issue 8B has been added in the CPS 3 Record of Changes table.

D.7 In Information Note 303, options X, W, V, U, and T have been added.

D.8 Old Information Note 304 has been changed to 309. A new Information Note 304 has been added.

D.9 Old Information Note 305 has been changed to 310. A new Information Note 305 has been added.

D.10 Information Notes 306 through 308 have been added on the drawing.

D.11 On the drawing, CAD 2 has been changed and CAD 3 has been added.

D.12 In the Option Index table, options Z, Y, X, W, V, U, and T have been added.

D.13 In the Supporting Information table, Equipment Design Requirements J1C194 has been removed and PDP 8705-801-0001 has been added, and AT&T Practice 801-603-165 has been changed to 201-521-101.

D.14 Circuit Note 106 has been added on the drawing.

D.15 In CPS 3, contact 14 on relay K1 has been corrected to contact 4.

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