COMMON SYSTEMS
J99329A CONTROL UNIT (60A)
CIRCUIT

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SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 This control unit, when installed with "Transmission Test Line or Test Trunk Circuit - SD-98100-01," or SD-1B277-01 and SD-1B123-01, provides a means of eliminating unauthorized telephone service connections, while permitting the nominal 1000 Hz loop-around transmission tests to be made. The control unit provides proper terminations for the two lines under test so that improper terminations due to impedance errors are eliminated.

2. GENERAL DESCRIPTION OF OPERATION

2.01 The control unit is connected in series with the two test lines to be measured. The circuit provides an output sinusoidal tone equal in frequency to an incoming sinusoidal tone in the frequency range from 990 Hz to 1030 Hz. The output tone level will match the input tone level within ±0.1 dB. The circuit will not reproduce speech or multifrequency tones.

2.02 The control unit circuitry will detect a tone within the acceptable frequency range on either line between -15 dBm and 0 dBm. The control unit will connect its input to the line with the incoming nominal 1000 Hz test tone and its output to the other line. Since there is no direct connection of the input and output, the possibility of fraudulent usage is eliminated.

2.03 Both 600-ohm and 900-ohm termination impedances are available. Printed circuit board ED99653-32 has 900-ohm termination impedances. Printed circuit board ED99653-33 has 600-ohm termination impedances.

SECTION II - DETAILED DESCRIPTION

1. AMPLITUDE MATCHING CIRCUIT

GENERAL

1.01 The purpose of the amplitude matching circuit is to adjust the level of the internally generated nominal 1000-Hz signal to be equal to the level of the incoming nominal 1000-Hz test signal. The amplitude matching circuit consists of two phase-locked loops (IC1 and IC2), a variolosser (IC3), a pair of low pass filters (IC4), two dc comparators (IC6 and IC7), two level shifters-inverters (Q5 and Q6), and an exclusive NOR gate (IC11A).

PHASE LOCKED LOOPS (PLLs)

1.02 The first phase-locked loop (IC1) locks onto the incoming nominal 1000-Hz test signal. The phase-locked loop produces a -90° phase shift between the input signal (pin 12) and its output signal (pin 15). The second phase-locked loop (IC2), locks onto the output of the first phase-locked loop. The second phase-locked loop produces a +90° phase shift between the two inputs of its phase detector (pins 10 and 12). The input to pin 12 of the second phase-locked loop is also the output signal of the control unit. Therefore, the input and output signals of the control unit are at the same frequency and in phase with each other.

1.03 The phase-locked loops used in the control unit are Western Electric 502EP integrated circuits. Each chip contains a phase comparator, unity gain amplifier, and voltage controlled oscillator (VCO). External components are added to the chips to:

(1) Provide biasing for the phase detectors (R1, R2, and R3);

(2) Control the gains of the phase dectors (R4 and R5);

(3) Low pass filter the outputs of the phase detectors (R4, C4 and R5, R6, C5);

(4) Provide biasing and offset nulling of the inputs to the VCOs (R7, R15 and R8, R17);

(5) Provide biasing for the output of the VCOs (R9 and R10, R12);

(6) Control the gains of the VCOs (R11 and R13);

(7) Control the free running frequency (1004 Hz) of the VCOs (R14, C8 and R16, C9).

1.04 The gain of the VCO in the first PLL (IC1) = 2360 radians/second/volt. The phase detector gain for PLL No. 1 = 38 volts/radian. The gain of the VCO in the second PLL (IC2) = 800 radians/volt. And the phase detector gain for PLL No. 2 = 35 volts/radian.

1.05 The capture range of the control unit is a function of the ac loop gain of each PLL. The approximate capture range of the control unit is from 800 Hz to 1200 Hz.

1.06 The lock-in range of the control unit is controlled by the dc loop gain of the PLLs. The approximate lock-in range of the control unit is from 550 Hz to 1475 Hz.

VARIOLOSSER CIRCUIT

1.07 The output of the second PLL is ac coupled through C7 to a Western Electric 502L variolosser (IC3). This variolosser controls the output level of the control unit. The variolosser nominally operates between 35 dB of loss, for a 0 dBm output signal, and 50 dB of loss, for a -15 dBm output signal.

1.08 The pinch-off voltage of the variolosser can vary between different chips from -2V to -4V. Therefore, the variolosser control voltage needed to produce a -15 dBm output signal will vary from -1.72V to -3.44V. R38 is selected at the time of manufacture to produce the proper variolosser control voltage which will produce approximately a -15 dBm output signal when the output of the exclusive NOR gate (IC11 pin 3) is a symetrical square wave. Under this condition the amplitude difference of the two signals at the input of IC6, pins 8 and 3, will be at a minimum.

LOW PASS FILTERS

1.09 Since the output of the PLL is a square wave, it must be low passed filtered to transform it into a sine wave. The first low pass filter (IC4B), has a pole at 1559 Hz and a zero at 81.14 KHz. The gain of the filter at 1004 Hz is 34 dB. The pole at 1559 Hz is controlled by the combination of R39 and C28. The zero at 81.14 KHz is controlled by the combination of R39, R47, and C28.

1.10 The second low pass filter (IC4A) has 7 dB of gain with a pair of complex poles, $\alpha = 0.4$, at 1004 Hz; and a pair of complex zeroes, $\alpha = 0.4$, at 3012 Hz. This pair of low pass filters attenuates the third harmonic of the 1004-Hz signal by 38 dB.

AMPLITUDE COMPARISON CIRCUIT

1.11 The input and output signals of the control unit are the same frequency and in phase with each other. They are continuously compared to each other with respect to amplitude by a dc comparator (IC6). The output of the comparator gives an indication of which signal is larger. If the input signal of the control unit is larger than the output signal, then during the positive half cycle of the input signal the output of IC6 will be at a high level. During the negative half cycle of the input signal the output of IC6 will be at a low level. IC7 detects the negative half cycle of input signal. The outputs of the two comparators (IC6 and IC7) are shifted in level and inverted by Q5, Q6, CR4, and CR5. These two transistors drive the inputs of an exclusive NOR gate. The exclusive NOR gate inverts the output of IC6 on the negative half cycle of the input signal, but not on the positive half cycle. Therefore, if the input signal to the control unit is larger than the output signal, the output of the exclusive NOR gate will be at its low level. The output of the exclusive NOR gate is a series of high and low level signals which represents the amplitude difference between the input and output signals. The output of the exclusive NOR gate is integrated by R27, R38, R45, and C27 to produce a dc voltage which controls the loss of the variolosser. The outputs of the two dc comparators in conjunction with the exclusive NOR gate, will adjust the loss of the variolosser until the input and output signals are equal in amplitude. The variolosser control voltage is continuously controlled by the dc comparators to maintain the output level equal to the input level.

1.12 The attenuator circuit at the input of IC6 (R19, R20, R22, R23, R32, R33, RT1) compensates for the initial loss of transformers (T1 and T2) plus the loss due to R18, and any variation in the transformer loss due to temperature changes. The variation of initial loss of the transformers is compensated for by selecting R20 at the time of manufacture. The variation in transformer loss due to a temperature change from 0°c to 50°c is compensated for by thermistor RT1 in the attenuator circuit.

1.13 The dc comparator (IC6) can have a maximum dc offset voltage equal to ±8 mV. A dc offset voltage in the comparator will produce an amplitude error between the input and output signals of the control unit. Therefore, the dc offset of this comparator is nulled out by selecting R35 at time of manufacture.

2. INPUT AND OUTPUT LINE SELECTOR

2.01 The nominal 1000-Hz input test signal may be applied to the control unit at either T1 or T2. It is therefore necessary to switch the input of the control unit to the trunk on which the nominal 1000-Hz test signal appears, and the output of the control unit to the other trunk. The input and output line switching is performed by relay K1.

2.02 Both input trunks are continuously monitored for an input signal above the threshold level by two dc comparators (IC5-A and IC5-B). The positive inputs to the comparators are dc biased by R57, R60, and R63, R69 below the VA supply voltage. When the input signal, which is attenuated 2.1 dB by R54, R56 or R59, R67, exceeds the level at the positive input of the comparators, the output of the comparator will change to its high state. The output of the comparator will drive either transistor Q3 or Q4 into saturation depending upon which trunk the input signal is on. The two transistors (Q3, Q4), plus the two capacitors (C31 and C33), and the two collector resistors (R51 and R65) convert the pulsating output of the comparators into a logic zero level for the inputs to IC8 and IC9.

2.03 IC8 is an 8-line-data-selector/multiplexer which is used to control relay K1. The data-selector is programmed by connecting the data inputs (D0 through D7) to either high levels, low levels, or to the Q output of the data-selector. The data-selector is addressed by controlling the logic levels of the data select inputs (A, B, C). IC8 will saturate Q1, which will operate relay K1, when the nominal 1000-Hz input signal appears on trunk B.

2.04 IC9 is also an 8-line-data-selector/multiplexer. The purpose of IC9 is to attenuate the output signal by placing the variolosser in its maximum attenuation state when there is no nominal 1000-Hz input signal. When the output of IC9 is high, transistors Q7 and Q8 are saturated. This cuts off transistors Q5 and Q6, thereby putting a logic "one" at the inputs of the exclusive NOR gate. The output of the exclusive NOR gate will therefore be a high level, which places the variolosser in its maximum attenuation state.

2.05 The RC combinations associated with Q2 provides a delay from the Q2 output of IC9 to its C input as well as an inversion of the Q2 output. When output Q2 goes high R67 and C36 delays the signal to the IC9 C input by 850 milliseconds. When output Q2 goes low R68 and C35 delays the signal to the IC9 C input by 375 milliseconds. The delay is needed in order to insure that the input level to the C input of IC9 does not change until after the variolosser has stabilized at its maximum attenuation state or at its free running state.

2.06 The one to zero transistion of the IC8 and IC9 B input signal is delayed by two exclusive NOR gates (IC11B and IC11C), R71 and C34. The delay is needed to insure that the relay will not chatter when the input signal is removed, if for some reason the delay produced by Q2 is not greater than the response time of the variolosser. The delay equals 100 milliseconds by the RC combination of R71 and C34. If the output of IC8 and IC9 are a "one" and a "zero" respectively, and the input signal on T2 is removed before the voltage across C35 has settled down to zero volts, the C input to IC9 could be a logic "zero" without being zero volts. Therefore, the delay produced by C35 and R68 for the positive transistion of the C input signal will be smaller than normal. Under these circumstances it is possible for the C input to IC9 to become a logic "one" signal before the variolosser has reduced the output signal of the control unit below -15 dBm. The input trunk selector circuit will then release the relay K1 and the threshold circuit for T2 will recognize the output signal of the control unit as an input signal. The delay produced by R71 and C34 prevents the B inputs to IC8 and IC9 from becoming a zero level immediately. The output signal of the control unit will drop below -15 dBm before the B inputs of IC8 and IC9 can become a zero level. Thus the B inputs to IC8 and IC9 will not become a zero level.

3. RADIO FREQUENCY INTERFERENCE (RFI) PROTECTION

3.01 The control unit is protected to 20 V/M of RFI from 0 to 900 MHz, by the addition of four resistors and 14 capacitors.

3.02 The most sensitive portion of the control unit to RFI was the low-pass filters when the RF is modulated with a nominal 1000-Hz signal. Resistor-capacitor networks R30-C16, R41-C23, C11-R28-C13, C24-R31-C22 were placed at the inputs to the op-amps to reduce the RF signal into the op-amp. The output of the op-amp is also loaded with 470 pico farads by C14. A capacitor is also placed across the power supply of the op-amp (C21).

3.03 Four RFI capacitors (C12, C17, C25, and C26) were placed on the inputs of the two voltage comparators IC6 and IC7. Without the RFI capacitors on the inputs of the comparators an RF signal will change the dc offset voltage of the comparator, thus causing an error in the output signal of the comparator.

3.04 Two RFI capacitors (C1 and C3) were added to the phase detector inputs of PLL No. 1. Without these two capacitors PLL No. 1 falls out of lock with a 20 V/M RF signal. The addition of all of these capacitors and resistors does not alter the normal operation of the control unit.

4. LIGHTNING PROTECTION

4.01 Zener surge protectors, CR1 and CR2, limit the voltage at the input circuitry of the control unit to 7V from lightning surges which may be present on the input and output trunks.

5. POWER SUPPLY

5.01 The control unit is designed to operate from a -48V supply. The typical current drain is 0.055A. When relay K1 is operated the typical current drain of the control unit increases to a 0.075A.

5.02 The power supply produces a plus and minus 6.2 volts to operate the control unit circuitry. The plus and minus 6.2 volts are generated by R53, CR8, and CR9. The supply voltages are ac bypassed by C30 and C32.

5.03 On the layout of the printed circuit board the supply voltage paths are separated into three different routs. The "A" subscript voltages power the analog circuitry. The "B" subscript voltages power the digital circuitry. And the "C" subscript voltage powers the relay. This prevents coupling through the power supply leads between the analog circuitry, digital circuitry, and the relay.

5.04 The 5-volt supply needed to power the logic circuitry is obtained by dropping the VB to -VB voltage by two diode drops through CR6 and CR7.

6. TESTING OF THE CONTROL UNIT IN ESS OFFICES

6.01 In ESS offices pins 17 and 18 of TB1 are connected to either the Remote Master Scanner Applique Circuit SD-1A210-01 or the Master Applique Circuit SD-1A133-01.

6.02 The test which was designed for issues 15B and earlier provides a low tone test signal at -24 dBm to the input of the control unit. Under this condition there should be no signal at the output of the control unit and contact 12 of the S relay should close.

6.03 In issue 16B there is no S relay. Therefore, a 3.83-kilohm 1W resistor (R73) is connected to terminals 17 and 18 of TB1. When the low tone test signal is applied to the control unit there will be no signal at the output of the control unit and the Remote Master Applique Circuit or Master Applique Circuit will recognize pins 17 and 18 of TB1 as being connected together.

SECTION III - REFERENCE DATA

1. WORKING LIMITS

1.01 Supply voltage must be between -42.75 volts and -52.5 volts.

1.02 Operating temperature is between 0°C and 50°C.

1.03 The input signal frequency should be between 990 Hz and 1030 Hz. The input signal level must be between -15 dBm and 0 dBm.

1.04 The input and output impedances of the control unit are either 600 ohms or 900 ohms. Printed circuit board ED99653-32 is 900 ohms ± 25 ohms. Printed circuit board ED99653-33 is 600 ohms ± 25 ohms.

2. FUNCTIONAL DESIGNATIONS

2.01 Circuit Package

Designation	Meaning
VCO	Voltage Controlled Oscillator

3. FUNCTIONS

3.01 The control unit will regenerate the nominal 1000-Hz input test signal at its output with less than 0.1 dB error in amplitude.

3.02 The control unit will not pass speech from one test line to the other.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed.

4.02 Transmission test line or test trunk circuit, SD-98100-01.

5. MANUFACTURING TESTING REQUIREMENTS

5.01 The testing requirements for this circuit are contained in L-182506.

SECTION IV - REASONS FOR REISSUE

D. Description of Changes

D.1 The control unit has been completely redesigned for the following reasons. The first reason is to overcome problems encountered when using the "Transmission Test Line or Test Trunk Circuit - SD-98100-01," with T1 carrier systems. D1 channel banks used on T1 carrier systems generate harmonics and noise of sufficient level to be detected as speech in the previous design of the control unit.

D.2 Secondly, this circuit provides improved terminations for the lines under test.

D.3 Thirdly, this design eliminates the need for field alignment of the control unit.

D.4 Fourthly, the control unit is available with 600-ohm or 900-ohm termination impedances.

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