SHEET INDEX		
ITEM	PAGE	ISSUE
SHEET INDEX		
RECORD OF CHANGES		
SUPPORTING INFORMATION		
SYSTEM USED ON	1	1
CURRENT DRAIN		
INPUT/OUTPUT INFORMATION	2	1
CIRCUIT DESCRIPTION		
SYMBOL	3	1

DWG ISS	CD ISS	DATE ISSD	DRN	APP
1		12-4-86		

CURRENT DRAIN	
+5V	650MA MAX

RECORD OF CHANGES

DWG ISS.	PREV FURN	STD	MFR DISC	SERIES NUMBER	SEE NOTE	CLEI CODE

SUPPORTING INFORMATION

SYSTEM USED ON	DESIGN CONTROL	CATEGORY	NO.
ADR	MV	CONNECTOR REQUIREMENTS ON PWB ON FRAME	

1N52

AMR110B CIRCUIT PACK
TERMINAL CONTROLLER
CIRCUIT

DWG SIZE	ISSUE
6S	1

AT&T BELL LABORATORIES	CPS-AMR110B	SHEET 1 OF 3

INPUT/OUTPUT DESCRIPTION

PIN#	DESIG	DESCRIPTION (BD FUNCTION)	I/O	SIGNAL
PRIMARY BUS				
002	EAD0	EXTERNAL DATA BUS	I/O	TTL
102	EAD1	EXTERNAL DATA BUS	I/O	TTL
003	EAD2	EXTERNAL DATA BUS	I/O	TTL
103	EAD3	EXTERNAL DATA BUS	I/O	TTL
004	EAD4	EXTERNAL DATA BUS	I/O	TTL
104	EAD5	EXTERNAL DATA BUS	I/O	TTL
005	EAD6	EXTERNAL DATA BUS	I/O	TTL
105	EAD7	EXTERNAL DATA BUS	I/O	TTL
008	ELA0	EXTERNAL LATCHED ADDR BUS	0	TTL
108	ELA1	EXTERNAL LATCHED ADDR BUS	0	TTL
009	ELA2	EXTERNAL LATCHED ADDR BUS	0	TTL
109	ELA3	EXTERNAL LATCHED ADDR BUS	0	TTL
007	ERES	EXTERNAL RESET SIGNAL ACTIVE-HIGH	0	TTL
006	ERD	EXTERNAL READ CONTROL LINE ACTIVE-LOW	0	TTL
106	EWR	EXTERNAL WRITE CONTROL LINE ACTIVE-LOW	0	TTL
107	EPCLK	EXTERNAL PERIPHERAL CLOCK 2.4576 MHZ	I	TTL
SECONDARY ADDR/CONTROL/CLOCK BUS				
010	ELA4	EXTERNAL LATCHED ADDR BUS	0	TTL
110	ELA5	EXTERNAL LATCHED ADDR BUS	0	TTL
011	ELA6	EXTERNAL LATCHED ADDR BUS	0	TTL
111	ELA7	EXTERNAL LATCHED ADDR BUS	0	TTL
012	ELA8	EXTERNAL LATCHED ADDR BUS	0	TTL
112	ELA9	EXTERNAL LATCHED ADDR BUS	0	TTL
013	ELA10	EXTERNAL LATCHED ADDR BUS	0	TTL
113	ELA11	EXTERNAL LATCHED ADDR BUS	0	TTL
014	ELA12	EXTERNAL LATCHED ADDR BUS	0	TTL
114	ELA13	EXTERNAL LATCHED ADDR BUS	0	TTL
015	ELA14	EXTERNAL LATCHED ADDR BUS	0	TTL
115	ELA15	EXTERNAL LATCHED ADDR BUS	0	TTL
016	ELA16	EXTERNAL LATCHED ADDR BUS	0	TTL
116	ELA17	EXTERNAL LATCHED ADDR BUS	0	TTL
017	ELA18	EXTERNAL LATCHED ADDR BUS	0	TTL
117	ELA19	EXTERNAL LATCHED ADDR BUS	0	TTL
151	ERESIN	RESET (CPU) IN ACTIVE LOW	I	TTL
124	ERDY	CPU READY	I	TTL

PIN#	DESIG	DESCRIPTION (BD FUNCTION)	I/O	SIGNAL
		ACTIVE HIGH		
054	ENMI	NON-MASKABLE INTR	I	TTL
		ACTIVE LOW		
024	EHOLD	CPU HOLD	I	TTL
		ACTIVE HIGH		
022	EIO/M	IO/MEMORY SELECT HIGH IO LOW MEMORY	0	TTL
123	EINTA	INTR ACKNOWLEDGE ACTIVE LOW	0	TTL
122	EALE	ADDR LATCH ENABLE ACTIVE HIGH	0	TTL
018	EDEN	DATA ENABLE ACTIVE LOW	0	TTL
118	EDT/R	DATA TRANSMIT/RECEIVE HIGH TRANSMIT LOW RECEIVE	0	TTL
137	EHALTN	HALT STATUS ACTIVE LOW	0	TTL
023	EHLDA	HOLD ACKNOWLEDGE ACTIVE HIGH	0	TTL
025	EOSC	OSCILLATOR 14.7456 MHZ	0	TTL
120	ECLK	PROCESSOR CLOCK 4.9152 MHZ	0	TTL
020	EBCLK	BAUD RATE 1 CLOCK 1.2288 MHZ	0	TTL
125	EB2CLK	BAUD RATE 2 CLOCK 153.600 KHZ	0	TTL
ADDRESS DECODING - ALL ACTIVE LOW				
138	EPS0	PAGE SELECT 0	0	TTL
128	EBS0	BANK SELECT 0 IO ADDR SPACE	0	TTL
038	TELMEN	TELM DPR ENABLE	0	TTL
139	FLEN	FAULT LOC DPR ENABLE	0	TTL
039	PMEN	PERF MON DPR ENABLE	0	TTL
044	EN3	ENABLE 3- SPARE	0	TTL
127	EBS08	BANK SELECT 0 LOW HALF	0	TTL
052	ECS80	CKT SELECT 8	0	TTL
027	ECS90	CKT SELECT 9	0	TTL
051	ECSA0	CKT SELECT A	0	TTL
150	ECSB0	CKT SELECT B	0	TTL
152	ECSC8F	CKT SELECT C HIGH HALF	0	TTL
050	ECSD0	CKT SELECT D	0	TTL
149	ECSE0	CKT SELECT E	0	TTL
049	ECSF0	CKT SELECT F	0	TTL
INTERRUPT/TIMER				
037	EIR0	INTR 0	I	TTL

INPUT/OUTPUT DESCRIPTION (CONT)

PIN#	DESIG	DESCRIPTION (BD FUNCTION)	I/O	SIGNAL
		ACTIVE HIGH		
136	EIR1	INTR 1 ACTIVE HIGH	I	TTL
134	EIR2	INTR 2 ACTIVE LOW	I	TTL
036	EIR3	INTR 3 ACTIVE LOW	I	TTL
135	EIR4	INTR 4 ACTIVE LOW	I	TTL
133	EIR6	INTR 6 ACTIVE LOW	I	TTL
033	EIR7	INTR 7 ACTIVE LOW	I	TTL
129	EGATE0	TIMER 0 END OF COUNT INDICATION, ACTIVE LOW	0	TTL
SANITY TIMER				
026	CPUF	CPU FAIL ACTIVE HIGH	0	TTL
028	CONTRF	CONTROLLER FAIL ACTIVE HIGH	I	TTL
053	RSTINH	RESET INHIBIT ACTIVE LOW	I	TTL
154	ERESTART	CPU RESTART ACTIVE LOW	0	TTL

CIRCUIT DESCRIPTION

FUNCTIONAL DESCRIPTION:

THE AMR110B TERMINAL CONTROLLER CIRCUIT PACK PROVIDES A CONTROLLER FUNCTION WHICH IS BASED ON THE 8088 MICROPROCESSOR. ADDITIONAL FUNCTIONS PROVIDED INCLUDE: BUFFERED DATA, ADDRESS AND CONTROL BUSES, INTERRUPT CONTROLLER, PROGRAMMABLE TIMERS, RAM DATA MEMORY, EPROM PROGRAM MEMORY, ADDRESS DECODING AND A SANITY TIMER. IT FORMS THE CENTRAL PART OF THE MULTI-BOARD TERMINAL STATION CONTROLLER FOR FREQUENCY DIVERSITY SYSTEMS AND BOTH THE TERMINAL AND REGENERATOR STATION CONTROLLERS FOR HOT STANDBY SYSTEMS.

BLOCK DIAGRAM DESCRIPTION:

1. MICROPROCESSOR
THE 8-BIT 8088 MICROPROCESSOR FORMS THE CENTRAL CORE OF THE CIRCUIT PACK. ITS NON-MASKABLE INTERRUPT (ENMI) IS EDGE BOARD AVAILABLE ALONG WITH THE HOLD SIGNAL (EHOLD). FOR ON BOARD PROGRAM MEMORY APPLICATIONS, SUCH AS HOT STANDBY, THE EHOLD LEAD MUST BE TIED LOW ON THE BACKPLANE. FOR OFF BOARD APPLICATIONS, IT IS DESIGNED TO BE OPERATED THROUGH THE ASSOCIATED MEMORY BOARD, EG., THE AMR111 IN FREQUENCY DIVERSITY.

2. CLOCK/RESET/WAIT STATE CONTROL
THE 8284A CLOCK GENERATOR AND DRIVER GENERATES THE PROCESSOR CLOCK FROM A 14.7456MHZ CRYSTAL. THIS DEVICE IN ASSOCIATION WITH A 4-BIT COUNTER PROVIDES THE FOLLOWING EDGE BOARD BUFFERED CLOCK SIGNALS FOR USE BY THE STATION CONTROLLER PERIPHERAL CIRCUIT PACKS.

DESIG	FREQ
EOSC	14.7456MHZ
ECLK (EOSC/3)	4.9152MHZ
EPCLK (ECLK/2)	2.4576MHZ
EBCLK (EPCLK/2)	1.2288MHZ
EB3CLK (EPCLK/8)	307.2KHZ
EB2CLK(EPCLK/16)	153.6KHZ

THE DEVICE GENERATES A SYNCHRONIZED SYSTEM RESET SIGNAL THROUGH ITS SCHMITT TRIGGER INPUT FROM THE FOLLOWING THREE SOURCES: 1) AN RC NETWORK FOR POWER ON RESET, 2) A FRONT PANEL RECESSED PUSHBUTTON FOR MANUAL RESET, AND 3) A BACKPLANE INPUT (ERESIN) FOR AUTOMATIC RESET FROM THE HARDWARE SANITY TIMER CIRCUIT.
THE WAIT STATE GENERATOR WILL INTRODUCE ONE MACHINE CYCLE OF DELAY FOR USE WHEN ACCESSING SLOW PERIPHERAL DEVICES. THE OUTPUT OF THE WAIT STATE GENERATOR FEEDS THE 8284 DEVICE WHICH PROVIDES A SYNCHRONIZED READY SIGNAL FOR THE MICROPROCESSOR. USE OF THE WAIT CYCLE IS CONTROLLED BY THE WAIT SIGNAL WHICH IS AN OUTPUT FROM THE PROGRAMMABLE ADDRESS DECODER CIRCUIT. THE BACKPLANE ERDY INPUT SIGNAL IS AVAILABLE FOR ANY ADDITIONAL OFF BOARD GENERATED WAIT STATE.

CIRCUIT DESCRIPTION (CONT)

3. SYSTEM PRIMARY BUS
THE PRIMARY BUS IS A RESERVED SECTION OF I/O BACKPLANE PINS WHICH GOES TO ALL STATION CONTROLLER PERIPHERAL CIRCUIT PACKS. IT CONSISTS OF THE FOLLOWING FUNCTIONS:
ADDRESS BUS: A 4-BIT (A0-A3) LATCHED AND BUFFERED ADDRESS BUS.
DATA BUS: AN 8-BIT BIDIRECTIONAL DATA BUS. TRI-STATE CONTROL OF THE BIDIRECTIONAL TRANSCEIVER IS BY MEANS OF THE ONBRD SIGNAL. THIS SIGNAL DISABLES THE TRANSCEIVER UNDER THE FOLLOWING CONDITIONS: THE INTERRUPT ACKNOWLEDGE (INTA) AND DATA ENABLE (DEN) SIGNALS FROM THE MICROPROCESSOR, THE DATA MEMORY SELECT SIGNAL (CSRAM) AND THE INTERRUPT CONTROLLER, PROGRAMMABLE TIMER AND SANITY TIMER PERIPHERAL CIRCUITS SELECT SIGNAL (CSC07) FROM THE ADDRESS DECODER. WHEN IN USE FOR OFF BOARD FUNCTIONS, ITS DIRECTION IS CONTROLLED BY THE MICROPROCESSORS DATA TRANSMIT/RECEIVE (DT/-R) SIGNAL.
CONTROL BUS: THREE BITS FROM THE 10-BIT BUFFERED CONTROL BUS ARE A PART OF THE PRIMARY BUS: READ (ERD), WRITE (EWR) AND RESET (ERES).
CLOCK BUS: THE PERIPHERAL CLOCK (EPCLK), ONE OF THE 6 CLOCK SIGNALS DESCRIBED ABOVE, IS A PART OF THE PRIMARY BUS.

4. SECONDARY ADDR/CONTROL/CLOCK BUS: THE REMAINING 16 LATCHED AND BUFFERED ADDRESS SIGNALS AND THE REMAINING CONTROL AND CLOCK SIGNALS ARE BACKPLANE AVAILABLE FOR USE BY THE PERIPHERAL CIRCUIT PACKS ON A AS NEEDED BASIS.

5. INTERRUPT CONTROLLER
AN 8-BIT PROGRAMMABLE INTERRUPT CONTROLLER (8259) IS USED TO INTERFACE INTERRUPT REQUESTS TO THE MICROPROCESSOR. TWO OF INTERRUPT INPUTS ARE ACTIVE HIGH SIGNALS, FIVE ARE ACTIVE LOW SIGNALS, AND ONE INPUT IS USED INTERNALLY BY THE SYSTEM CLOCK GENERATOR.

6. TIMERS
AN 8253 TIMER DEVICE, CONTAINING THREE 16-BIT PROGRAMMABLE TIMERS, PROVIDES USER TIMING CAPABILITY. ONE OF THE TIMERS IS DEDICATED AS A SOFTWARE SYSTEM CLOCK, VIA INTERRUPT 5. THE OTHER TWO ARE AVAILABLE FOR GENERAL USE BY THE APPLCATION SOFTWARE.

7. DATA MEMORY
8K BYTES OF RANDOM ACCESS MEMORY (RAM) IS AVAILABLE FOR USE BY THE APPLICATION SOFTWARE.

8. PROGRAM MEMORY
A SOCKET IS PROVIDED FOR OPTIONALLY EQUIPPING PROGRAMMABLE MEMORY OF THE FOLLOWING TYPES: 27128-16K BYTES, 27256-32K BYTES, OR 27512-64K BYTES. TWO OPTIONING TERMINAL FIELDS ARE USED TO CONNECT THE APPROPRIATE CONTROL SIGNALS TO PINS 1 AND 27 OF THE PROM SOCKET, AS FOLLOWS.

PROM	E9 (PIN 1)	E5 (PIN 27)
27128	E10	E4
27256	E10	E3
27512	E8	E3

9. ADDRESS DECODER
THE ADDRESS DECODING FOR ALL OF THE MICROPROCESSOR INTERFACED DEVICES, BOTH INTERNALLY ON THE AMR110B UNIT ITSELF AND EXTERNALLY ON THE PERIPHERAL CIRCUIT PACKS, IS ACCOMPLISHED IN THE FOLLOWING HIERARCHICAL FASHION.
HIGH LEVEL 20-BIT DECODING:
THE OVERALL 20-BIT ADDRESS SPACE IS INITIALLY BROKEN UP BY MEANS OF A PROGRAMMABLE 512 X 8 BIPOLAR PROM. THIS GIVES A MINIMUM BLOCK SIZE CAPABILITY OF 4K BYTES. THIS ALLOWS FOR FLEXIBILITY IN USING THE BASIC CIRCUIT FOR OTHER APPLICATIONS. THE SPECIFIC CONFIGURATION FOR THE AMR110B IS AS FOLLOWS:

SIGNAL	ADDRESS RANGE	SIZE
EPROM	F0000-FFFFF	64K
EPS0	00000-0FFFF	64K
CSRAM	00000-01FFF	8K
WAIT	0C000-0FFFF	16K
PMEN	0C000-0CFFF	4K
FLEN	0D000-0DFFF	4K
TELMEN	0E000-0EFFF	4K
EBS0	0FF00-0FFFF	256
EN3	NOT ASSIGNED	

SIGNAL	DESCRIPTION
EPROM	PROGRAM MEMORY SELECT
EPS0	PAGE 0 SELECT - 64K DATA MEMORY (RAM) AND ALL MEMORY MAPPED IO
CSRAM	DATA MEMORY SELECT
WAIT	MEMORY MAPPED IO WAIT STATE SELECT
EBS0	MEMORY MAPPED IO ADDRESS SPACE
TELMEN	AS&C TELEMETRY DUAL PORT RAM SELECT
FLEN	FAULT LOCATE DUAL PORT RAM SELECT
PMEN	PERFORMANCE MONITOR DUAL PORT RAM SELECT

CIRCUIT DESCRIPTION (CONT)

MEMORY MAPPED IO DECODING:
AN EIGHT-BIT EQUAL-TO COMPARATOR (25LS2521) IS USED TO DECODE THE UPPER 256 BYTE BLOCK FROM THE PAGE 0 SELECT. THIS SPACE IS DEFINED BY THE EBS0 SIGNAL AND IS USED FOR PERIPHERAL CIRCUIT SELECTION.
THE EBS0 BLOCK IS FURTHER DIVIDED IN HALF, VIA ADDRESS A7, INTO THE FOLLOWING TWO AREAS.
1) EBS00 IS THE BOTTOM 128 BYTES OF THIS BLOCK. IT IS USED IN FREQUENCY DIVERSITY TO DECODE THE CHANNEL STATUS CIRCUIT PACKS (AMR113-PROTECTION, AMR114-REGULARS). ADDRESSES A6-A3 ARE USED TO DECODE THE INDIVIDUAL STATUS SLOTS VIA FIXED BACKPLANE CODED WIRING, ALLOWING FOR A MAXIMUM OF 16 CHANNELS. ADDRESS A2 DECODES THE TWO HALVES OF THE DUAL REGULAR CHANNEL STATUS UNITS, LEAVING ADDRESSES A1-A0 FOR THE INDIVIDUAL PORT DECODING.
2) THE UPPER 128 BYTES ARE DIVIDED, VIA A 3 LINE TO 8 LINE DECODER (LS138), INTO 8 16-BYTE WIDE PERIPHERAL CIRCUIT PACK SELECT LEADS. ADDRESSES A3-A0 ARE THEN AVAILABLE FOR PORT DECODING ON A GIVEN PERIPHERAL UNIT.
FINALLY, CIRCUIT SELECT CSC0 SPACE IS DIVIDED IN HALF VIA ADDRESS A3 AND A DUAL 2 LINE TO 4 LINE DECODER (LS139). THE LOWER 8 BYTES, REPRESENTED BY SIGNAL CSC07, ARE USED FOR DECODING THE ON BOARD PERIPHERAL CHIPS. THE UPPER 8 BYTES, REPRESENTED BY SIGNAL ECS8F, IS AVAILABLE FOR OFF BOARD SELECTION.
THE 256 BYTE EBS0 SPACE CAN ALSO BE ACCESSED VIA IO MAPPING. FOR THIS MODE OF OPERATION THE IO PORT ADDRESSES ARE FROM 0 TO 255.

THE SPECIFIC CONFIGURATION IS AS FOLLOWS:

SIGNAL	ADDRESS RANGE	SIZE
EBS00	0FF00-0FF7F	128
(EBS01)	0FF80-0FFFF	128
ECS80	0FF00-0FF0F	16
ECS90	0FF90-0FF9F	16
ECSA0	0FFA0-0FFAF	16
ECSB0	0FFB0-0FFBF	16
ECSC0	0FFC0-0FFCF	16
CSC07	0FFC0-0FFC7	8
INTRPT_ENB	0FFC0-0FFC1	2
SNTY_TRG	0FFC2-0FFC3	2
TIMER_ENB	0FFC4-0FFC7	4
ECS8F	0FFC8-0FFCF	8
ECSD0	0FFD0-0FFDF	16
ECSE0	0FFE0-0FFEF	16
ECSF0	0FFF0-0FFFF	16

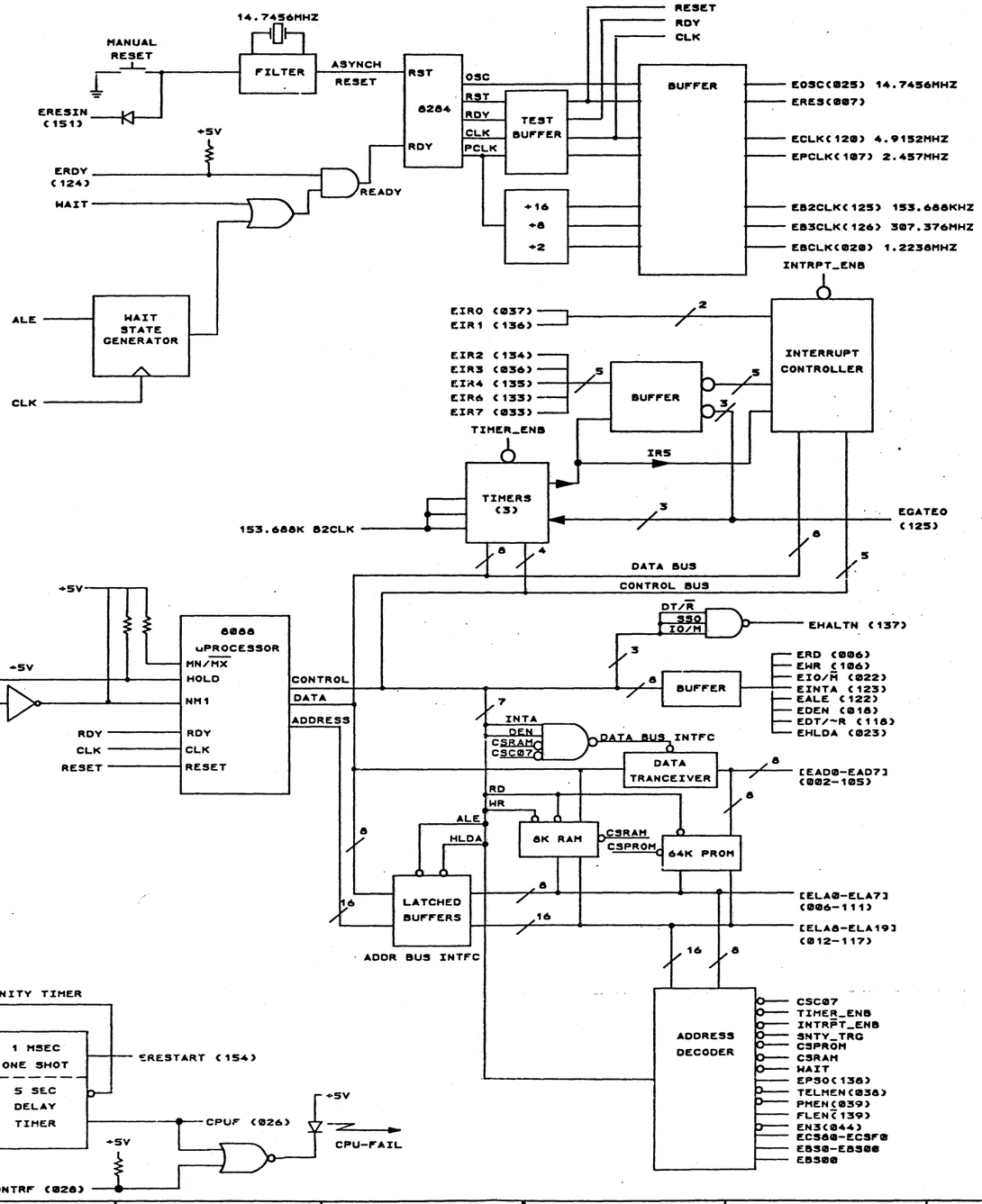
10. SANITY TIMER
A HARDWARE SANITY TIMER IS PROVIDED WHICH CAN BE USED TO AUTOMATICALLY RESET THE MICROPROCESSOR IF THE APPLICATION PROGRAM WERE TO BECOME LOST. IT CONSISTS OF TWO TIMERS.
THE FIRST STAGE IS A 5 SECOND DELAY TIMER WHICH MUST BE RETRIGGERED BY THE APPLICATION PROGRAM BY WRITING (ANY DATA VALUE) TO THE SANITY TIMER ADDRESS WITHIN THIS TIME FRAME. IF THE TIMER IS ALLOWED TO TIME OUT ITS TWO OUTPUTS WILL GO ACTIVE. ONE, CPUF, IS A LOGIC LEVEL ALARM SIGNAL (ACTIVE HIGH) AVAILABLE ON THE BACKPLANE AND WHICH ALSO DRIVES THE FACEPLATE CPU FAIL LED. THE OTHER OUTPUT DRIVES THE SECOND STAGE.
THE SECOND STAGE IS A 1-MSEC ONE SHOT WHOSE OUTPUT, ERESTART, IS AVAILABLE ON THE BACKPLANE AND IS NORMALLY CONNECTED TO THE ERESIN INPUT TO THE RESET CIRCUITRY. THE OUTPUT OF THIS STAGE CAN BE DISABLED BY PULLING THE RSTINH SIGNAL LOW.
THE FACEPLATE CPU FAIL INDICATOR MAY ALSO BE DRIVEN BY THE CONTRF INPUT. SINCE A LOGIC 0 REPRESENTS THE OFF (NO ALARM) STATE, IT MUST BE PULLED LOW ON THE BACKPLANE WHEN NOT USED.

AMR110B CIRCUIT PACK

DWG SIZE 6S | ISSUE 1

AT&T BELL LABORATORIES | CPS-AMR110B | 2

SYMBOL



AMR110B CIRCUIT PACK		
	DWG SIZE 6S	ISSUE 1
AT&T BELL LABORATORIES	CPS-AMR110B	3