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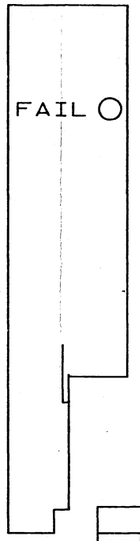
CIRCUIT DESCRIPTION

THE VMR PULSE INTERFACE CIRCUIT PACK (AMR118) MONITORS AND COUNTS THE PULSES GENERATED BY THE DS-3 PARITY VIOLATION MONITOR/RECEIVER CIRCUIT PACK (AMR72B) IN RESPONSE TO PARITY ERRORS AND DS-3 FRAME LOSS. THE DATA COLLECTED FOR A DEFINED MEASUREMENT INTERVAL IS USED TO ASCERTAIN THE PERFORMANCE OF THE DS-3 SIGNAL MONITORED BY THE AMR118.

CURRENT DRAIN	
+5V	1425 MA MAX 1215 MA TYP

DRAWING NOTES

101. FACEPLATE DIAGRAM FOR AMR118.



DWG ISS	CD ISS	DATE ISSD	DRN	APP
1		8-26 87		

RECORD OF CHANGES						
DWG ISSUE	PREV FURN	STD	MFR DISC	SERIES NUMBER	SEE NOTE	CLEI CODE

SUPPORTING INFORMATION

SYSTEM USED ON	DESIGN CONTROL	CATEGORY	NO.
ADR	MV		

AMR118 CIRCUIT PACK AN52
VMR INTERFACE
CIRCUIT

DWG SIZE	ISSUE
6S	1

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INPUT/OUTPUT INFORMATION

PIN#	DESIG	DESCRIPTON (BOARD FUNCTION)	I/O	SIGNAL
PRIMARY BUS				
002	EAD0	EXTERNAL LATCHED DATA BUS	IO	TTL
102	EAD1	EXTERNAL LATCHED DATA BUS	IO	TTL
003	EAD2	EXTERNAL LATCHED DATA BUS	IO	TTL
103	EAD3	EXTERNAL LATCHED DATA BUS	IO	TTL
004	EAD4	EXTERNAL LATCHED DATA BUS	IO	TTL
104	EAD5	EXTERNAL LATCHED DATA BUS	IO	TTL
005	EAD6	EXTERNAL LATCHED DATA BUS	IO	TTL
105	EAD7	EXTERNAL LATCHED DATA BUS	IO	TTL
013	EAD8	EXTERNAL LATCHED DATA BUS	IO	TTL
113	EAD9	EXTERNAL LATCHED DATA BUS	IO	TTL
014	EAD10	EXTERNAL LATCHED DATA BUS	IO	TTL
114	EAD11	EXTERNAL LATCHED DATA BUS	IO	TTL
015	EAD12	EXTERNAL LATCHED DATA BUS	IO	TTL
115	EAD13	EXTERNAL LATCHED DATA BUS	IO	TTL
016	EAD14	EXTERNAL LATCHED DATA BUS	IO	TTL
116	EAD15	EXTERNAL LATCHED DATA BUS	IO	TTL
008	ELA0	EXTERNAL LATCHED ADDRESS BUS	I	TTL
108	ELA1	EXTERNAL LATCHED ADDRESS BUS	I	TTL
009	ELA2	EXTERNAL LATCHED ADDRESS BUS	I	TTL
109	ELA3	EXTERNAL LATCHED ADDRESS BUS	I	TTL
010	ELA4	EXTERNAL LATCHED ADDRESS BUS	I	TTL
110	ELA5	EXTERNAL LATCHED ADDRESS BUS	I	TTL
011	ELA6	EXTERNAL LATCHED ADDRESS BUS	I	TTL
111	ELA7	EXTERNAL LATCHED ADDRESS BUS	I	TTL
012	ELA8	EXTERNAL LATCHED ADDRESS BUS	I	TTL
112	ELA9	EXTERNAL LATCHED ADDRESS BUS	I	TTL
048	XLA5	STRAPPED BOARD ADDRESS LEAD (LSB)	I	TTL
148	XLA6	STRAPPED BOARD ADDRESS LEAD	I	TTL
049	XLA7	STRAPPED BOARD ADDRESS LEAD	I	TTL
149	XLA8	STRAPPED SHELF ADDRESS LEAD (LSB)	I	TTL
050	XLA9	STRAPPED SHELF ADDRESS LEAD	I	TTL
006	-ERD	EXTERNAL READ CONTROL LINE ACTIVE LOW	I	TTL
106	-EWR	EXTERNAL WRITE CONTROL LINE ACTIVE LOW	I	TTL
007	ERES	EXTERNAL RESET SIGNAL ACTIVE HIGH	I	TTL
107	-FLEN	EXTERNAL BOARD SELECT SIGNAL ACTIVE LOW	I	TTL
020	EBCLK	EXTERNAL CLOCK 1.2288MHZ	I	TTL

PIN#	DESIG	DESCRIPTON (BOARD FUNCTION)	I/O	SIGNAL
VMR INTERFACE				
022	D3P1	RS422 VMR PARITY PULSE LINE #1	I	
122	D3PB1	COMPLEMENT OF D3P1	I	
023	CSRVS1	LINE #1 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
051	SUPRT1	D3P LINE #1 SUPPORT SIGNAL	I	TTL
024	D3P2	RS422 VMR PARITY PULSE LINE #2	I	
124	D3PB2	COMPLEMENT OF D3P2	I	
123	CSRVS2	LINE #2 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
151	SUPRT2	D3P LINE #2 SUPPORT SIGNAL	I	TTL
026	D3P3	RS422 VMR PARITY PULSE LINE #3	I	
126	D3PB3	COMPLEMENT OF D3P3	I	
027	CSRVS3	LINE #3 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
052	SUPRT3	D3P LINE #3 SUPPORT SIGNAL	I	TTL
028	D3P4	RS422 VMR PARITY PULSE LINE #4	I	
128	D3PB4	COMPLEMENT OF D3P4	I	
127	CSRVS4	LINE #4 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
152	SUPRT4	D3P LINE #4 SUPPORT SIGNAL	I	TTL
033	D3P5	RS422 VMR PARITY PULSE LINE #5	I	
133	D3PB5	COMPLEMENT OF D3P5	I	
034	CSRVS5	LINE #5 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
053	SUPRT5	D3P LINE #5 SUPPORT SIGNAL	I	TTL
035	D3P6	RS422 VMR PARITY PULSE LINE #6	I	
135	D3PB6	COMPLEMENT OF D3P6	I	
134	CSRVS6	LINE #6 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
153	SUPRT6	D3P LINE #6 SUPPORT SIGNAL	I	TTL
037	D3P7	RS422 VMR PARITY PULSE LINE #7	I	
137	D3PB7	COMPLEMENT OF D3P7	I	
038	CSRVS7	LINE #7 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
054	SUPRT7	D3P LINE #7 SUPPORT SIGNAL	I	TTL

INPUT/OUTPUT INFORMATION (CONT)

VMR INTERFACE (CONT)

039	D3P8	RS422 VMR PARITY PULSE LINE #8	I	
139	D3PB8	COMPLEMENT OF D3P8	I	
138	CSRVS8	LINE #8 SERVICE STATUS INPUT SERVICE PRESENT HIGH	I	TTL
154	SUPRT8	D3P LINE #8 SUPPORT SIGNAL	I	TTL
029	BCTHRSHLD	TYPE B/C ERROR THRESHOLD STRAPPING	I	TTL
129	AVAIL1	AVAILABLE INPUT FOR GROWTH	I	TTL
030	AVAIL2	AVAILABLE INPUT FOR GROWTH	I	TTL
017	EXTAL1	OPTIONAL EXTERNAL OSC SOURCE TO IC1	I	TTL
117	EXTAL2	OPTIONAL EXTERNAL OSC SOURCE TO IC2	I	TTL
018	EXTAL3	OPTIONAL EXTERNAL OSC SOURCE TO IC3	I	TTL
118	EXTAL4	OPTIONAL EXTERNAL OSC SOURCE TO IC4	I	TTL

PIN#	DESIG	DESCRIPTON (BOARD FUNCTION)	I/O	SIGNAL
POWER BUS AND RESERVED PINS				
000	GRD	GROUND BUS	G	
100	GRD	GROUND BUS	G	
001	GRD	GROUND BUS	G	
101	GRD	GROUND BUS	G	
055	GRD	GROUND BUS	G	
155	GRD	GROUND BUS	G	
056	GRD	GROUND BUS	G	
156	GRD	GROUND BUS	G	
045	+5VIN	VCC +5V SOURCE INPUT	P	
145	+5VIN	VCC +5V SOURCE INPUT	P	
046	+5VIN	VCC +5V SOURCE INPUT	P	
146	+5VIN	VCC +5V SOURCE INPUT	P	
047	+5VIN	VCC +5V SOURCE INPUT	P	
147	+5VIN	VCC +5V SOURCE INPUT	P	
021	VCC1	RESERVED +12V SOURCE INPUT	P	
121	VCC1	RESERVED +12V SOURCE INPUT	P	
040	VEE	RESERVED -5V SOURCE INPUT	P	
140	VEE	RESERVED -5V SOURCE INPUT	P	
041	VEE	RESERVED -5V SOURCE INPUT	P	
141	VEE	RESERVED -5V SOURCE INPUT	P	
042	VEE	RESERVED -5V SOURCE INPUT	P	
142	VEE	RESERVED -5V SOURCE INPUT	P	
043	VEE	RESERVED -5V SOURCE INPUT	P	
143	VEE	RESERVED -5V SOURCE INPUT	P	
019	VEE1	RESERVED -12V SOURCE INPUT	P	
119	VEE1	RESERVED -12V SOURCE INPUT	P	

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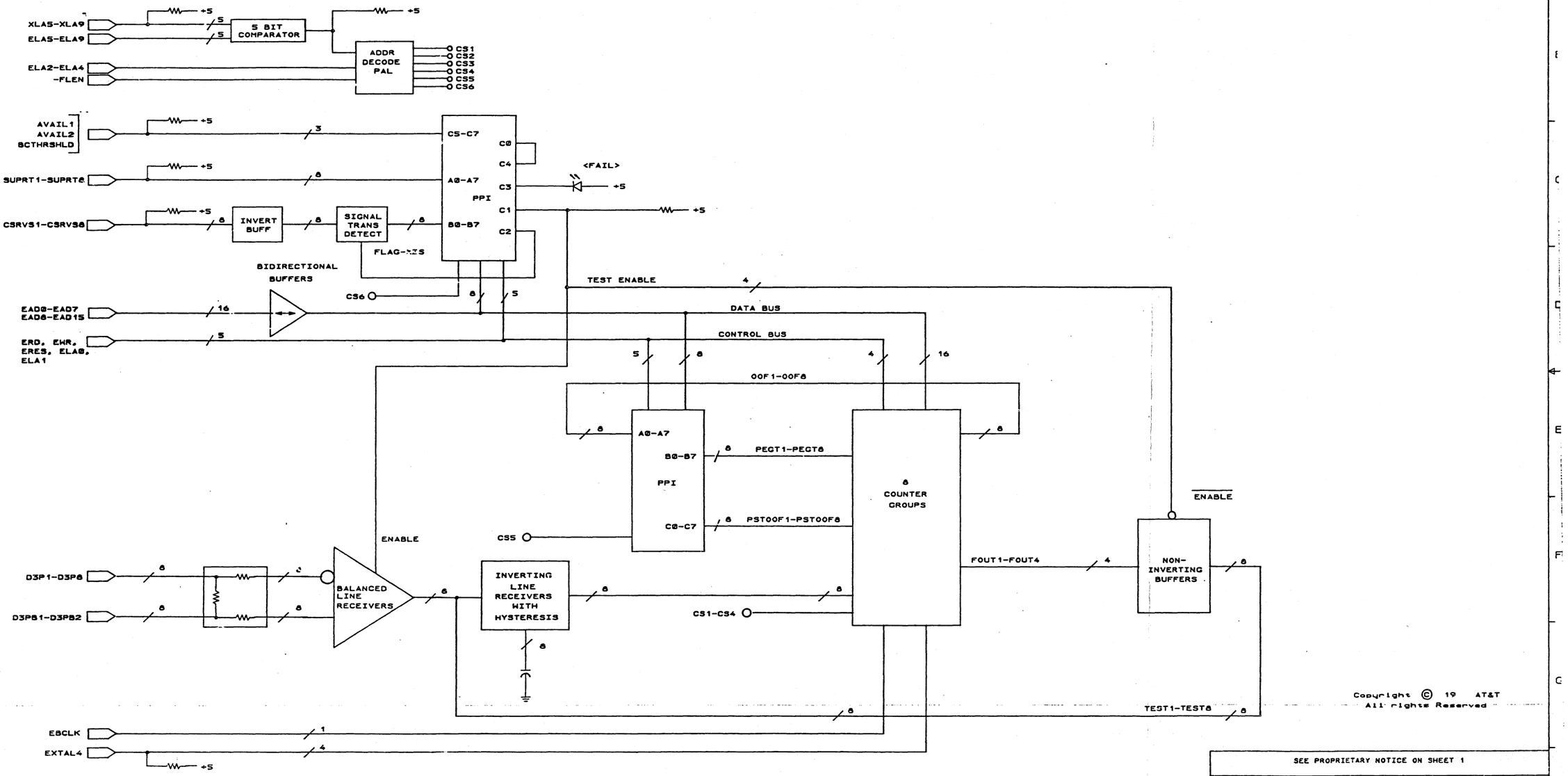
AMR118 CIRCUIT PACK		
	DWG SIZE 6S	ISSUE 1
AT&T BELL LABORATORIES	CPS-AMR118	2

SYMBOL



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AMR118 CIRCUIT PACK

DWG SIZE 6S | ISSUE 1

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