PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS

SHEET INDEX

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	FC20C
CONNECTOR ON FRAME	947A OR 947C
ACCEPTABLE SERIES	7

DWG. ISSUE	CD ISSUE	DATE ISSUED	DRAWN	APPD
1	—	7-17-74	P/S MCL	JJR MTS RFG
2A	—	9-19-75	P/S LRE	RAM LAW RFG
3A	—	4-19-77	[illegible] DKO	AAN LEG JBD

SYMBOL

CHANNEL INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

A

TERM. MOD.	FUNCT	TERM.	LOC
DION	I	303	2A1
DIOP	I	203	2A0
DI1N	I	002	2A2
DI1P	I	101	2A1
ENØBO	I	207	2A2
ENZØO	I	307	2A2
IDØVI1	I	306	2A2
IDPIO	I	103	2A5
INHØIO	I	209	2A2
INHZIO	I	208	2A1
ØDO	I	302	2A2
SINTO	I	102	2A4
DØON	Ø	305	2G1
DØOP	Ø	205	2G2
DØ1N	Ø	304	2G2
DØ1P	Ø	205	2G2
IDO	Ø	201	2G0
IDØV1	Ø	003	2G5
IDPO	Ø	202	2G0
ION	Ø	105	2G3
IOP	Ø	005	2G3
I1N	Ø	104	2G4
I1P	Ø	004	2G4
ØACTO	Ø	301	2G1
SHFTO	Ø	308	2G0
ZACTO	Ø	300	2G0

LINE INTERFACE CIRCUITS
ELEMENT IDENTIFICATION

B

TERM. MOD.	FUNCT	TERM.	LOC
ALAO	I	017	3A3
ALBO	I	116	3A4
ALCO	I	015	3A5
ALDO	I	014	3A5
RAO	I	016	3A3
RBO	I	115	3A4
RCO	I	114	3A5
RDO	I	113	3A6
TPAO	I	210	3A6
TPBO	I	213	3A7
TPCI	I	109	3A8
TPDO	I	110	3A8
FPAI1	Ø	214	3G3
FPBI1	Ø	215	3G4
PCI1	Ø	216	3G5
PDI1	Ø	217	3G6
SALMA1	Ø	009	3G3
SALMB1	Ø	011	3G4
SALMC1	Ø	315	3G5
SALMD1	Ø	316	3G5
SAO	Ø	310	3G6
SBO	Ø	309	3G7
SCO	Ø	108	3G8
SDO	Ø	008	3G9
+3	P	000	3G0
+24F	P	013,112	3G1
+24	P	019,118	3G2
-24	P	218,318	3G1
GRD	G	200,319	3G1
GRD	G	0GD	3G1

LINE TIMING CIRCUITS
ELEMENT IDENTIFICATION

C

TERM. MOD.	FUNCT.	TERM.	LOC.
LTIMØ1	Ø	204	2G7

NOTES:

1. ⏚ GROUND RETURN.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS.

IC CODE	BAT. TERM.	GRD TERM.
153A	14	1
41M	3,6,7,8	12
41AE	16	7,8
41DL	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
-24	218, 318
+3	000
+24	019,118
+24F	013,112
GRD	200,319,0GD

5. HORIZONTAL MOUNTING CENTERS AT 0.5 INCH.

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN:

+3V	300mA
+24V	150mA
-24V	50mA

ISSUE 3A

1N98

AT&TCO STANDARD

FC200 CIRCUIT PACK

TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS (2)

CPS-FC200
7 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

DRG. SIZE 6S

PRINTED IN U.S.A.

CPS-FC200

PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE AND
TIMING CIRCUITS

CHANNEL INTERFACE CIRCUIT
ELEMENT A

LINE TIMING CIRCUIT
ELEMENT C

CPS-FC200

3A

FC200 CIRCUIT PACK

CPS-FC200
SHEET 2

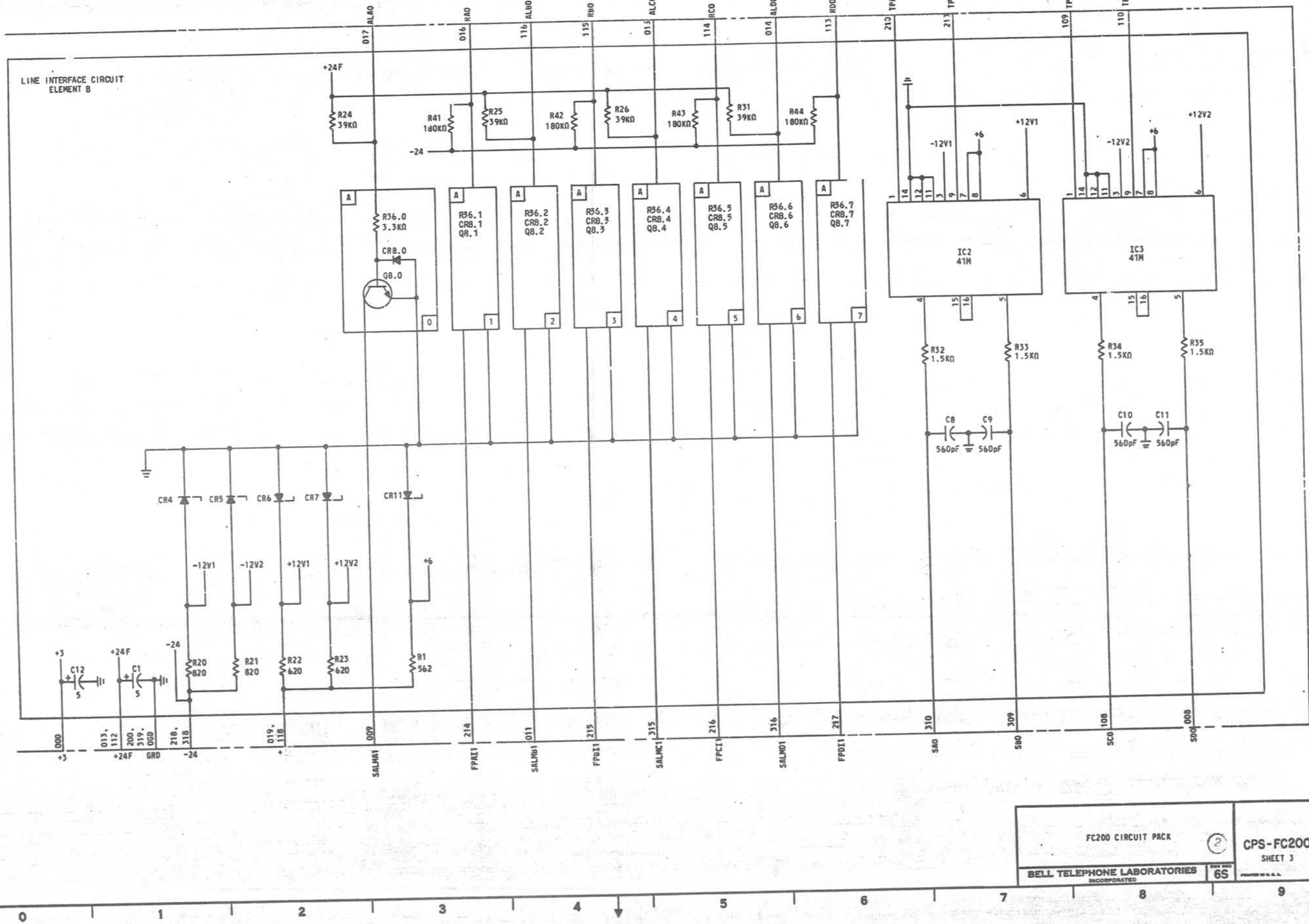
BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS

LINE INTERFACE CIRCUIT ELEMENT B



ISSUE 3A

FC200 CIRCUIT PACK (2)	CPS-FC200 SHEET 3
BELL TELEPHONE LABORATORIES INCORPORATED	6S

CPS-FC200

PART OF CPS FC200

TELETYPEWRITER CONTROLLER INTERFACE AND TIMING CIRCUITS

COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	601A, 5
[2] C2,C3	KS-19774 L5, 0.1
C5	KS-19774 L1, 510pF
C6	KS-19774 L1, 220pF
C7	KS-19774 L1, 220pF
C8	KS-19774 L1, 560pF
C9	KS-19774 L1, 560pF
C10	KS-19774 L1, 560pF
C11	KS-19774 L1, 560pF
C12	601A, 5

CIRCUIT MODULE

DESIG	CODE
CM1	153A

CRYSTAL

DESIG	CODE
Y0	100C 9.87136 MHZ

DIODE

DESIG	CODE
CR1	458C
CR2	458C
CR3	458C
CR4	808J
CR5	808J
CR6	808J
CR7	808J
[8] CR8.0-CR8.7	458C
CR9	459B
CR10	459B
CR11	459B

INTEGRATED CIRCUIT

DESIG	CODE
IC2	41M
IC3	41M
IC5	41DL
IC6	41AE

RESISTOR

DESIG	CODE
R1	KS-20289 L6C, 562
R2	KS-20810 L1A, 1KΩ
R3	KS-20616 L1A, 237
R4	KS-20616 L1A, 1KΩ
R5	KS-20616 L1A, 2.87KΩ
R6	KS-20616 L1A, 1KΩ
R7	KS-20289 L6A, 178
R8	KS-16645 L1, 1KΩ
R9	KS-16645 L1, 3KΩ
R10	KS-16645 L1, 560
R11	KS-16645 L1, 1KΩ
R12	KS-16645 L1, 1KΩ
R13	KS-16645 L1, 150
R14	KS-16645 L1, 150
R15	KS-16645 L1, 15
R16	KS-16645 L1, 1.2KΩ

RESISTOR (CONT)

DESIG	CODE
R17	KS-16645 L1, 2.4KΩ
R18	KS-16645 L1, 300
R19	KS-16645 L1, 3KΩ
R20	KS-19150 L1, 820
R21	KS-19150 L1, 820
R22	KS-19150 L1, 62C
R23	KS-19150 L1, 620
R24	KS-16645 L1, 39KΩ
R25	KS-16645 L1, 39KΩ
R26	KS-16645 L1, 39KΩ
R27	KS-16645 L1, 100
R28	KS-16645 L1, 100
R29	KS-16645 L1, 100
R30	KS-16645 L1, 100
R31	KS-16645 L1, 39KΩ
R32	KS-16645 L1, 1.5KΩ
R33	KS-16645 L1, 1.5KΩ
R34	KS-16645 L1, 1.5KΩ
R35	KS-16645 L1, 1.5KΩ
[8] R36.0-R36.7	KS-16645 L1, 3.3KΩ
R41	KS-16645 L1, 180KΩ
R42	KS-16645 L1, 180KΩ
R43	KS-16645 L1, 180KΩ
R44	KS-16645 L1, 180KΩ

TRANSFORMER

DESIG	CODE
T1	2664G
T2	↓
T3	↓
T4	↓
T5	↓
T6	2664G

TRANSISTOR

DESIG	CODE
Q1	92A
Q2	66S
Q3	↓
Q4	↓
Q5	↓
Q6	↓
Q7	↓
[8] Q8.0-Q8.7	66S

CIRCUIT DESCRIPTION

A. FUNCTION

CIRCUIT PACK (CP) FC200 IS USED IN THE TELETYPEWRITER CONTROLLER (TTYC) CIRCUIT TO INTERFACE THE TTYC LOGIC CIRCUITRY TO THE 3A CENTRAL CONTROL [3A CC] AND THE TELETYPEWRITER [TTY].

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATION THAT END IN 0 ARE LOW WHEN ACTIVE OR IN THE ONE STATE. LEADS HAVING DESIGNATION THAT END IN 1 ARE HIGH WHEN ACTIVE OR IN THE ONE STATE.

CHANNEL INTERFACE CIRCUIT - ELEMENT A

DATA IS PASSED BETWEEN THE 3A CC TO THE TTYC IN SERIAL BIPOLAR FORM. A COAXIAL LINE TO EACH OF TWO 3A CC'S IS TERMINATED BY TRANSFORMERS T3 AND T4 AND THEIR ASSOCIATED RESISTORS. CIRCUIT MODULE (CM) 1 CONVERTS THE BIPOLAR INPUT DATA TO LOGIC-LEVEL SIGNALS APPEARING ON LEAD IDO. A TIMING SIGNAL IS ALSO GENERATED BY CM1 ON LEAD SHFTO SO THAT THE TTYC LOGIC CIRCUITS WILL SAMPLE LEAD IDO WHEN IT IS STABLE. (REFER TO THE DESCRIPTION CMS 153A FOR THE RELATIONSHIP BETWEEN THE BIPOLAR INPUT AND LOGIC LEVEL TIMING AND DATA LEADS.) THE DATA INPUT FROM CC0 OR CC1 IS BLOCKED WHEN LEADS INHZIO OR INHØIO ARE ACTIVE. LEADS ZACTO OR ØACTO ARE ACTIVE WHEN DATA IS BEING RECEIVED FROM CC0 OR CC1. THESE LEADS CAN BE CONNECTED TO THE OPPOSITE CC INPUT CONTROL LEAD (IE, ZACTO CONNECTED TO INHØIO AND ØACTO CONNECTED TO INHZIO) TO LOCK OUT ONE CC WHILE AN INPUT IS BEING RECEIVED FROM THE OTHER.

IDPO IS ACTIVE WHILE INPUT DATA IS PRESENT. IT CAN BE CONNECTED TO IDPIO WHERE IT WILL TURN OFF Q6 AND ALLOW C7 TO CHARGE TO +3 VOLTS THROUGH R18. WHEN THE INPUT DATA STOPS, IDPO IS NO LONGER ACTIVE AND C6 CHARGES TO +3V THROUGH R16. WHEN IT REACHES APPROXIMATELY 1.5 VOLTS, Q6 WILL TURN ON AND DISCHARGE C7. Q7 WILL CUT OFF UNTIL C7 CAN CHANGE ITS CHARGE THROUGH R19 TO ABOUT 0.7 VOLTS IN THE OPPOSITE DIRECTION. THIS RESULTS IN A NOMINAL 450ns PULSE ON LEAD IDØV1. IDØV1 IS CONNECTED TO IDØVI1 WHERE IT INITIALIZES CIRCUITS IN CM1. THIS SIGNAL CAN ALSO INITIALIZE OTHER TTYC LOGIC CIRCUITS.

DATA IS SENT FROM THE TTYC TO THE 3A CC'S IN BIPOLAR FORM VIA COAXIAL CABLE CONNECTED TO DØOP/N AND DØ1P/N. THE LOGIC - LEVEL SIGNAL OF DATA TO BE OUTPUTTED IS SET ON LEAD ØDO. TIMING FOR THE OUTPUT DATA IS DERIVED FROM AN ALL - ZERO'S INPUT DATA STREAM THAT IS SUPPLIED BY THE 3A CC DURING THE TIME WHEN THE TTYC IS EXPECTED TO OUTPUT DATA TO IT. LEADS ENZØO AND ENØØO ENABLE THE OUTPUT DATA TO BE DIRECTED TO 3A CC0 OR 3A CC1.

LEAD SINTO IS ACTIVATED BY THE TTYC WHEN IT HAS COMPLETED A CHARACTER EXCHANGE WITH THE TTY. WHEN SINTO IS NOT ACTIVE, C5 IS CHARGED TO ABOUT +3 VOLTS THROUGH R8. WHEN SINTO GOES ACTIVE, C5 IS DISCHARGED AND CUTS OFF Q3 UNTIL C5 CAN CHANGE ITS CHARGE THROUGH R9. THIS RESULTS IN A NOMINAL 1μSEC PULSE OUT OF Q3 WHICH IS SENT TO BOTH 3A CC'S VIA DRIVERS Q4 AND Q5 AND TRANSFORMERS T5 AND T6. THIS SIGNAL IS CONNECTED TO THE 3A CC INTERRUPT CIRCUITS WHEN THE 3A CC IS USED IN A SYSTEM THAT SERVICES ITS TTY'S ON A DEMAND BASIS.

LINE TIMING CIRCUIT - ELEMENT C

Y0 IS A CRYSTAL CONTROLLED OSCILLATOR WITH A FREQUENCY OF 9.87136MHZ. IC5 IS A 4-STAGE RIPPLE COUNTER. IC6 IS A TOGGLE F/F. IC5 AND IC6 DIVIDE THE OSCILLATOR OUTPUT BY 32 TO PRODUCE A 308.48KHZ FREQUENCY (3.2417USEC PERIOD) OUTPUT AT TERMINAL 204. Q2 INTERFACES THIS SIGNAL TO THE TTYC LOGIC WHERE IT IS USED TO DETERMINE BIT TIMING FOR THE CHARACTER EXCHANGED WITH THE TTY. Q1 IS A 5 VOLT REGULATOR TO SUPPLY Y0, IC5 AND IC6.

LINE INTERFACE CIRCUIT - ELEMENT B

THIS CIRCUIT PROVIDES THE LEVEL CONVERSION FOR SIGNALS EXCHANGED BETWEEN THE TTYC AND THE TTY. THREE SIGNALS, RECEIVED DATA, TRANSMITTED DATA, AND TTY ALARM ARE PROVIDED BY THE TTYC FOR EACH OF FOUR TTY PORTS. THE PORTS ARE DESIGNATED A THROUGH D. THUS, LEADS RAO THROUGH RDO ARE THE EIA LEVEL RECEIVED - DATA SIGNALS FROM TTY PORTS A THROUGH D. THESE ARE CONVERTED TO LOGIC LEVEL ON LEADS FPAI1 THROUGH FPDI1, RESPECTIVELY. LIKEWISE, EIA LEVELS ON ALAO THROUGH ALDO ARE CONVERTED TO LOGIC LEVEL ON SALMA1 THROUGH SALMD1 TO MONITOR THE TTY ALARMS. IN THE OTHER DIRECTION, LOGIC SIGNALS TPAO THROUGH TPDO FROM THE TTYC ARE CONVERTED TO EIA LEVEL ON LEADS SAO THROUGH SDO BY THE 41M DEVICE, CM1 AND IC2. THE ALARM INPUT LEADS ARE BIASED IN THE NO-ALARM STATE BY R24, R25, R26 AND R31 TO PREVENT ERRONEOUS ALARMS FROM UNUSED PORTS. SIMILARLY THE RECEIVED DATA LINES ARE BIASED IN THE MARKING STATE FOR DISCONNECTED PORT BY R41 THROUGH R44. R20 THROUGH R23 AND CR4 THROUGH CR7 PROVIDE THE ±12 VOLT POTENTIALS REQUIRED BY THE 41MS. R32 THROUGH R35 AND C8 THROUGH C11 PROPERLY TERMINATE THE 41M OUTPUTS.

C. SYMBOL/LEAD MNEMONICS

MNEMONIC	DEFINITION
ALAO-DO	ETA LEVEL ALARM SIGNAL FROM TTY PORTS A THROUGH D
DION/P	DATA INPUT FROM CC0 NEGATIVE/POSITIVE
DI1N/P	DATA INPUT FROM CC1 NEGATIVE/POSITIVE
DØON/P	DATA OUTPUT TO CC0 NEGATIVE/POSITIVE
DØ1N/P	DATA OUTPUT TO CC1 NEGATIVE/POSITIVE
ENØØO	ENABLE OUTPUT DATA TO CC1
ENZOO	ENABLE OUTPUT DATA TO CC0
FPAI1-DI1	LOGIC LEVEL RECEIVED DATA SIGNAL FROM TTY PORTS A THROUGH D
IDØVI1	INCOMING DATA OVER-INPUT
IDØV1	INCOMING DATA OVER-OUTPUT
IDPIO	INCOMING DATA PRESENT-INPUT
IDPO	INCOMING DATA PRESENT-OUTPUT
IDO	INCOMING DATA
INHØIO	INHIBIT INPUT FROM CC1
INHZIO	INHIBIT INPUT FROM CC0
ION/P	INTERRUPT SIGNAL TO CC0 NEGATIVE/POSITIVE
I1N/P	INTERRUPT SIGNAL TO CC1 NEGATIVE/POSITIVE
LTIMØ1	LINE TIMING SIGNAL
ØACTO	CC1 IS ACTIVE WITH THE TTYC
ØDO	OUTGOING DATA
RAO-DO	EIA LEVEL RECEIVED DATA FROM TTY PORTS A THROUGH D
SALMA1-D1	LOGIC LEVEL ALARM SIGNAL FROM TTY PORTS A THROUGH D
SAO-DO	EIA LEVEL TRANSMITTED DATA TO TTY PORTS A THROUGH D
SHFTO	SHIFT
SINTO	SET INTERRUPT
TPAO-DO	LOGIC LEVEL TRANSMITTED DATA SIGNAL TO TTY PORTS A THROUGH D
ZACTO	CC0 IS ACTIVE WITH TTYC

CPS-FC200

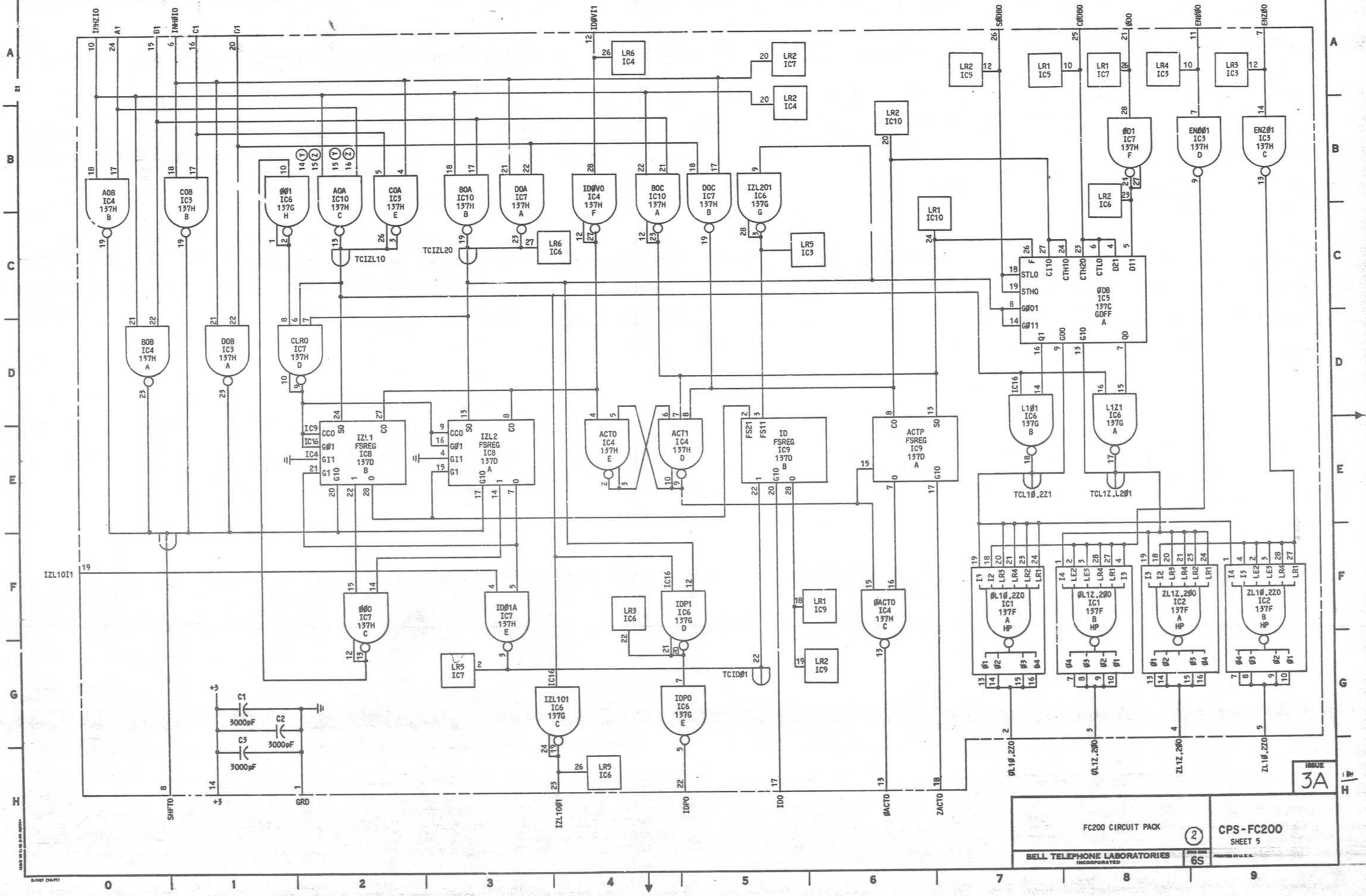
ISSUE 3A

FC200 CIRCUIT PACK

BELL TELEPHONE LABORATORIES INCORPORATED

CPS-FC200 SHEET 4

PART OF CMS 153A



ISSUE 3A

FC200 CIRCUIT PACK (2)	CPS-FC200 SHEET 5
BELL TELEPHONE LABORATORIES INCORPORATED	DRG SIZE 6S

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 137F (NOTE 1) DESIG	SH LOC	IC2 137F (NOTE 1) DESIG	SH LOC	IC3 137H DESIG	SH LOC	IC4 137H DESIG	SH LOC	IC5 137C DESIG	SH LOC	IC6 137G DESIG	SH LOC	IC7 137H DESIG	SH LOC	IC8 137D DESIG	SH LOC	IC9 137D DESIG	SH LOC	IC10 137H DESIG	SH LOC	LOC CODE ELEM ID
A	ØL1Ø.2ZO	5F7	ZL1Z.2ØO	5F8	DOB	5D1	BOB	5DO	ØOB	5C8	L1Z1	5E8	DOA	5B3	IZL2	5E3	ACTP	5E6	BOC	5B4	A
B	ØL1Z.2ØO	5F8	ZL1Ø.2ZO	5F9	COB	5B1	AOB	5BO			L1Ø1	5D7	DOC	5B5	IZL1	5E2	ID	5E5	BOA	5B3	B
C					ENZØ1	5B9	ØACTO	5F6			IZL101	5G4	ØØO	5F2					AOA	5B2	C
D					ENØØ1	5B9	ACT1	5E4			IDP1	5F4	CLRO	5D1							D
E					COA	5B2	ACTO	5E4			IDPO	5G5	ID Ø1A	5F3							F
F					ØACTO	5F5	IDØVO	5B4					ØD1	5B8							F
G											IZL201	5B5									G
H											ØØ1	5B1									H

CAPACITOR

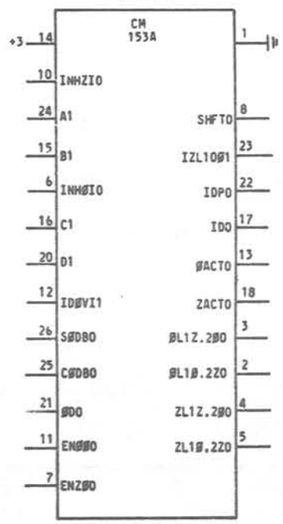
	DESIG	CODE	
[3]	C1-C3	801A	3000pF

NOTES:

1. CAPACITOR CHIP 801A, 3000$_{pF}$ IS BONDED ON EACH SIDE OF 137F SIC.

RECORD OF CHANGES				
DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE
3	Z	Y	Z	

SYMBOL



BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	BAT TERM	GRD TERM
137C	25	11
137D	25	11
137F	25,26	11,12
137G	25	11
137H	25	11

SUPPORTING INFORMATION

CATEGORY	NO
INTEGRATED CIRCUIT CODE	153A
ACCEPTABLE SERIES	3-4,4

153A IC

3A

FC200 CIRCUIT PACK

CPS-FC200
SHEET 6

BELL TELEPHONE LABORATORIES INCORPORATED

6S

CPS-FC200

TIMING DIAGRAM

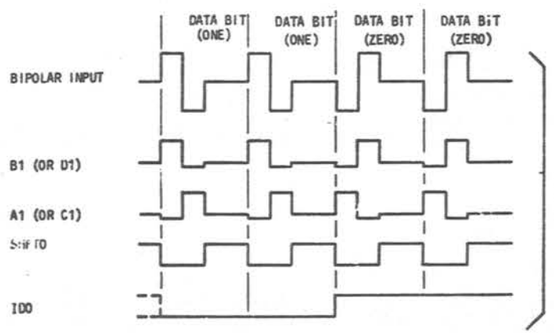


FIG. 1
BIPOLAR TO LOGIC LEVEL CONVERSION USING CM 153A

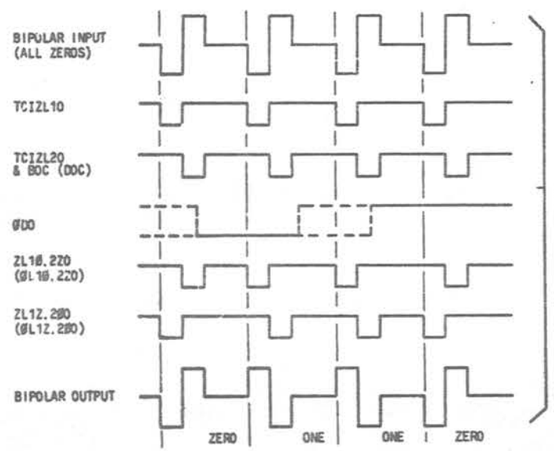


FIG. 2
LOGIC LEVEL TO BIPOLAR CONVERSION USING CM 153A

CIRCUIT DESCRIPTION

A. FUNCTION

CM 153A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC I/Ø DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN 0 ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CM 153A ON LEADS A1 AND B1 FROM CCO, AND C1 AND D1 FROM CC1. THE DATA IS OR'ED BY GATES AOA AND COA AT TCIZL10, AND BY GATES BOA AND DOA AT TCIZL20. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CM 153A, AND ITS LOGIC-LEVEL DATA (IDO) AND TIMING (SHFTO) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC STATE OF THE BIPOLAR DATA BIT IS DETERMINED BY THE ORDER OF ITS POSITIVE AND NEGATIVE EXCURSIONS. A LOGICAL ONE IS A POSITIVE LOBE FOLLOWED BY A NEGATIVE LOBE. A LOGICAL ZERO IS A NEGATIVE LOBE FOLLOWED BY A POSITIVE LOBE. CLIPPING CIRCUITS, WHICH ARE PART OF GATES TO WHICH THE A1, B1, C1, AND D1 INPUTS CONNECT, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE GATES.

THE INPUT DATA LEAD (IDO) IS SET AT THE LEADING EDGE OF THE FIRST LOBE. THE TIMING SIGNAL IS THE TRAILING EDGE OF SHFTO WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOBE. THUS, THE CONTROLLER IS SIGNALED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE IDO AND SHFTO LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THESE SIGNALS. NOMINAL TIMES FOR THE 3A CC SERIAL I/Ø DATA ARE A 150-NS BIT INTERVAL WITH 37.5-NS LOBES.

THE SHFTO LEAD IS CONTROLLED BY GATES AOB, BOB, COB, AND DOB, AND FLIP-FLOPS IZL1 AND IZ.2. INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT SHFTO IS HIGH. IF INHZIO AND INHØIO ARE NOT ACTIVE, THE FIRST LOBE OF THE INPUT DATA BIT WILL ACTIVATE ONE OF THE GATES (DEPENDING ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CCO OR CC1) AND PULL SHFTO LOW. THE FIRST LOBE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TCIZL10 OR TCIZL20 WHICH WILL SET ONE OF THE FLIP-FLOPS, IZL1 OR IZL2, DEPENDING ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD SHFTO LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOBES AND TO PREVENT THE SECOND LOBE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (ID).

WHEN THE SECOND LOBE OF THE INCOMING DATA BIT IS ACTIVE THE MATE OF THE GATE ACTIVATED BY THE FIRST LOBE WILL BE ACTIVE, AND IT WILL ALSO HOLD SHFTO LOW (AOB AND BOB ARE MATES AS ARE COB AND DOB). THIS LOBE WILL ALSO SET THE FLIP-FLOP (IZL1 OR IZL2) THAT WAS NOT SET BY THE FIRST LOBE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP HELD SHFTO TO GROUND. WHEN THE FIRST LOBE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOBE HOLDS SHFTO LOW.

WITH BOTH FLIP-FLOPS SET, THE INPUT TO CLRO FROM ØØ1 IS HIGH. THE OTHER INPUTS TO CLRO, TCIZL10, AND TCIZL20 ARE CONTROLLED BY THE DATA LOBES. WHEN THE FIRST LOBE IS GONE, ONLY THE SECOND LOBE CONTROLS CLRO. WHEN THE SECOND LOBE EXPIRES, THE GATE HOLDING SHFTO IS DISABLED AND SHFTO WILL GO HIGH. CLRO WILL GO LOW AT THIS TIME AND CLEAR BOTH FLIP-FLOPS. CLRO LOW ALSO BLOCKS THE IZL1 AND IZL2 CONNECTION TO SHFTO SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE 00 STATE.

LEAD IDO IS CONTROLLED BY THE ID FLIP-FLOP. ID RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOBE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TCIZL10 WILL BE ACTIVE FIRST AND DRIVE GATE IZL101 HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT IDO1A HAS BOTH INPUTS HIGH. IT SHOULD BE NOTED THAT IZL1 AND IZL2 ARE INITIATED FROM THE CLEARED STATE AND THAT TCIZL10 SETS IZL1 BUT DOES NOT AFFECT IZL2. IDO1A WILL PULL TCIDØ1 LOW, WHICH WILL CLEAR ID AND DRIVE IDO HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOBE IS ACTIVE FOR THE ZERO DATA BIT, TCIZL20 WILL DRIVE IZL201 HIGH. HOWEVER, IZL1 WAS SET BY THE FIRST LOBE, IN ORDER TO PREVENT IZL201 FROM CHANGING THE ID FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TCIZL20 WILL BE ACTIVE FIRST, IZL201 WILL BE HIGH WHILE IZL1 IS CLEARED, AND THE ID FLIP-FLOP WILL BE SET. IDO WILL THUS BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOBE IS ACTIVE FOR AN INCOMING ONE, TCIZL10 IS ACTIVE, AND WILL DRIVE IZL101 HIGH. TCIZL20, HOWEVER, WILL HAVE SET IZL2, WHICH PREVENTS IDØ1A FROM CHANGING ID.

LEADS ZACTO AND ØACTO INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTO AND ACT1, IS SET BY GATES BOC OR DOC TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACTP IS SET BY BOC WHEN CCO IS ACTIVE, AND IS CLEARED BY DOC WHEN CC1 IS ACTIVE. THE ACT AND ACTP FLIP-FLOPS ARE COMBINED TO ACTIVATE ZACTO WHEN CCO IS ACTIVE AND ØACTO WHEN CC1 IS ACTIVE. BOTH THE ZACTO AND ØACTO ARE HIGH WHEN NEITHER CC IS ACTIVE.

INHZIO AND INHØIO BLOCK INPUT DATA FROM CCO AND CC1 WHEN THEY ARE ACTIVE.

LEAD IDPO WILL BE ACTIVE WHEN EITHER LOBE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOBES.

INPUT IDØV1 IS USED TO INITIALIZE THE IZL1 AND IZL2 TO THE 00 STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC FOLLOWS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITH AN ALL-ZEROS BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SENT TO THE 3A CC. THE 3A CC MAINTAINS THE ALL-ZEROS BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE MAXIMUM INTERVAL IN WHICH IT SHOULD RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 (OR C1) IS ACTIVE FOLLOWED BY B1 (OR D1) ACTIVE. INPUTS ENZØ0 AND ENØ00 ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CCO OR CC1.

GATES ZL1Ø.22O AND ZL1Z.28O ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CCO. GATES ØL1O.22O AND ØL1Z.28O ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CC1. THESE GATES ARE HELD HIGH WHEN THERE IS NO INCOMING DATA OR WHEN THE ENABLE LEAD (ENZØ0, ENØØ0) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (ØDO) IS TOGGLED INTO ØDB PRIOR TO THE BIT PERIOD. THE OUTPUT OF ODB IS COMBINED WITH THE TIMING SIGNALS DERIVED FROM THE INCOMING DATA (TCIZL10 AND TCIZL20) TO DETERMINE THE ORDER IN WHICH TCL1Ø.2Z1 AND TCL1Z.2Ø1 WILL BE ACTIVE. IF A ONE IS TO BE SENT, TCL1Ø.2Z1 WILL BE ACTIVE DURING THE FIRST LOBE AND TCL1Z.2Ø1 WILL BE ACTIVE DURING THE SECOND LOBE. THE REVERSE WILL BE TRUE TO OUTPUT A ZERO. THESE SIGNALS WILL BE INVERTED BY THE ENABLED OUTPUT GATES ZL1O.22O AND ZL1Z.28O AND/OR ØL1O.22O AND ØL1Z.28O.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER; EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THUS, THE ORDER IN WHICH THE GATES ARE ACTIVE DETERMINES THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY WINDING. NOTE THAT THE STATE OF THE ØDO LEAD IS TOGGLED INTO ODB BY BOC (OR DOC) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TRANSMITTED. INPUTS SØDBO AND CØDBO ALLOW DIRECT SET AND CLEAR OPERATIONS ON ØDB.

SYMBOL/LEAD C. MNEMONICS

MNEMONIC	DEFINITION
ACTP	SET OR CLEARED TO DETERMINE WHICH INPUT PORT IS ACTIVE
ACTO,1	SET WHEN EITHER INPUT PORT IS ACTIVE
A1,B1	INPUTS FROM CCO
CØDBO	CLEAR ODB FF
C1,D1	INPUTS FROM CC1
ENØØ0	ENABLE OUTPUT TO CC1
ENZØ0	ENABLE OUTPUT TO CCO
ID	INCOMING DATA
IDØV11	INCOMING DATA OVER, INPUT
IDPO	INCOMING DATA PRESENT
IZL1	INCOMING ZERO LOBE ONE - SET BY FIRST LOBE WHEN INPUT IS ZERO
IZL2	INCOMING ZERO LOBE TWO - SET BY SECOND LOBE WHEN INPUT IS ZERO
IDO	INCOMING DATA
ØACTO	CC1 IS ACTIVE
ØDB	OUTGOING DATA BIT
ØDO	OUTGOING DATA
ØL1Ø.22O	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CC1
ØL1Z.28O	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC1
SHFTO	SHIFT
SØDBO	SET ODB FF
ZACTO	CCO IS ACTIVE
ZL1Ø.22O	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CCO
ZL1Z.28O	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CCO

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