SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SYMBOL MANUFACTURING REFERENCES NOTES USED-ON TABLE CURRENT DRAIN RECORD OF CHANGES	1	2
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CMS 144AJ	6	2
	7	2
	8	2
CMS 153A	9	2
	10	2
	11	2

SYMBOL

DIAGNOSTIC ACCESS
ELEMENT A

TERM. MOD.	FUNCT	TERM.	LOC
BUFBOIO	I	013	3B1
CLØINIC	I	003	3B0
DØUTIO	I	113	3B6
FCKIO	I	207	2B2
FSTPCKIO	I	10A	2B2
INITIO	I	30?	2B2
IØNI1	I	218	3B5
IØPI1	I	318	3B6
IZNI1	I	316	3B5
IZPI1	I	317	3B5
SHSTPIU	I	102	3B1
CLINIT1	Ø	010	3B2
DIND	Ø	014	3G5
ØØN1	Ø	213	3G7
ØØP1	Ø	313	3G7
ØZN1	Ø	214	3G7
ØZP1	Ø	314	3G6
RESETO	Ø	306	3G1
SHFTO	Ø	103	3G5
+3	P	000,119,	2E7
GRD	G	200	
GRD	G	319	
GRD	G	0GD,2GD	2E7

ADDRESS & DATA
ELEMENT B

TERM. MOD.	FUNCT	TERM.	LOC
SAD17IO	I	005	2B3
AD17Ø	Ø	304	2E3
AD171A	Ø	210	
AD171B	Ø	311	
SAD17Ø	Ø	203	2E3

ERROR DETECTION
ELEMENT C

TERM. MOD.	FUNCT	TERM.	LOC
ERIO	I	104	2B4
SERAIO	I	206	2B1
TSERAO	Ø	205	2E4

REFRESH CONTROL
ELEMENT D

TERM. MOD.	FUNCT	TERM.	LOC
REFIO	I	002	2B4

CONTROL AND TIMING
ELEMENT E

TERM. MOD.	FUNCT	TERM.	LOC
NLDIO	I	105	2B5
PINITI1	I	004	2B3
SREQIO	I	006	2B5
SREQO	Ø	302	2E5
PINITO	Ø	305	
TCKOA	Ø	204	
TCKOB	Ø	202	2E5

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
144AJ	1,38	19,20
153A	14	1

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+3V	000,119
GRD	200,319,0GD,2GD

5. HORIZONTAL MOUNTING CENTER AT [illegible] INCHES.
6. CMS 153A IS CONTROLLED BY CPS FC200.

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	Drawn	APPD
1		12-20-74	RDS LRG	ACT LEG RFG
2A		1-8-76	DAPP LRE	ACT LEG RFG

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	FC203
CONNECTOR ON FRAME	
SERIES FOR CLASS "A" CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE)	6

CURRENT DRAIN: 510mA

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

ISSUE 2A

IN98

FC203 CIRCUIT PACK

CLOCK CIRCUIT

(2)

AT&TCO STANDARD

CPS-FC203
11 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED
DWG SIZE 6S

PART OF CPS FC203

CLOCK CIRCUIT

COMPONENT LIST

CAPACITOR

DESIG	CODE
[2] C1,C2	KS-20813 L4, 42.2PF
[5] C3-C7	KS-19774 L2, .01
C8	KS-19774 L1, 1200pF
C9	KS-20813 L4, 316pF
C10	KS-20813 L4, 215pF
[3] C11-C13	KS-19774 L6, .1

CRYSTAL

DESIG	CODE
Y1	106AB 14.9254

DIODE

DESIG	CODE
[3] CR1-CR3	458A
CR4	458C

INDUCTOR

DESIG	CODE
L1	KS-13726 L76, 4.22μH
L2	KS-13726 L24, 33μH

INTEGRATED CIRCUIT

DESIG	CODE
CM1	144AJ
CM2	153A

RESISTOR

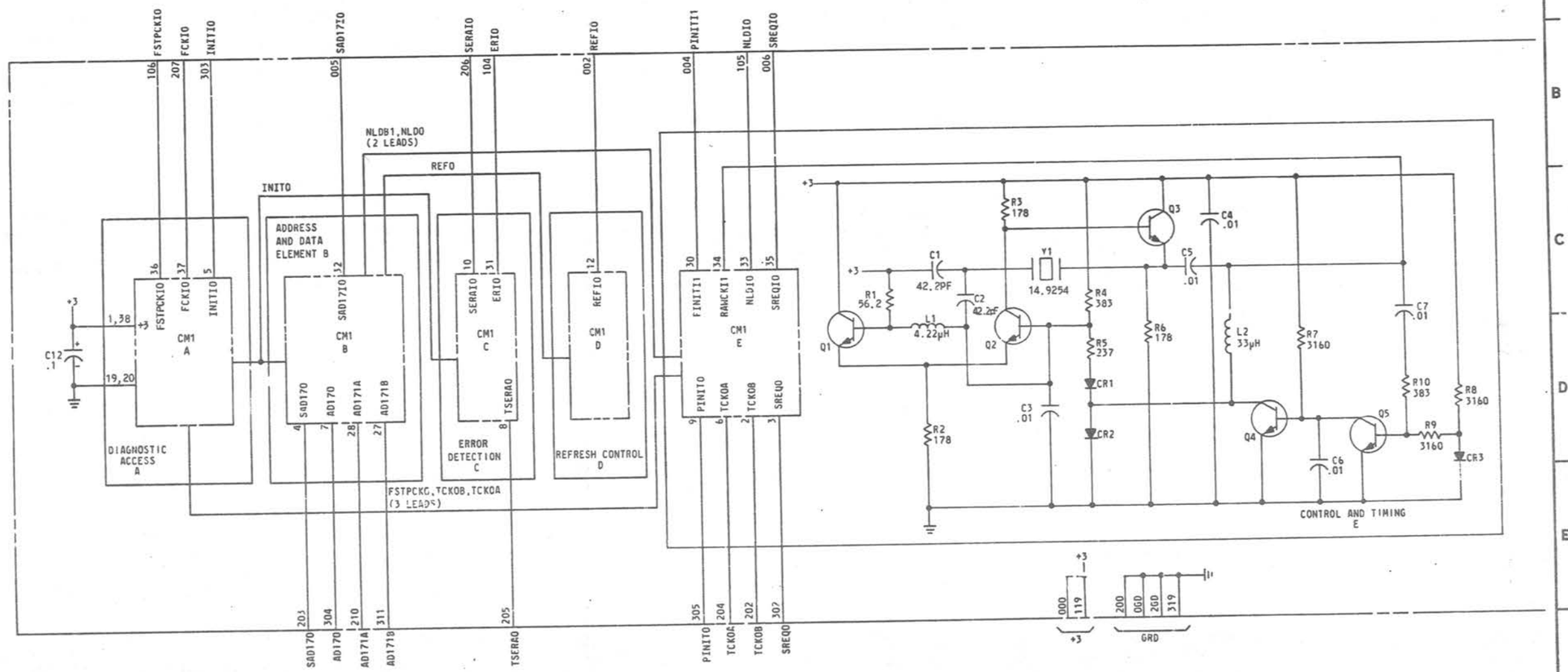
DESIG	CODE
R1	KS-20616 L1A, 56.2
[2] R2,R3	178
R4	383
R5	237
R6	178
[3] R7-R9	3160
R10	383
R11	511
R12	2150
R13	1210
R14	14.7
R15	2370
R16	237
R17	KS-20616 L1A, 2870

TRANSFORMER

DESIG	CODE
[4] T1-T4	2664G

TRANSISTOR

DESIG	CODE
[3] Q1-Q3	45A
[5] Q4-Q8	66J



FC203 CIRCUIT PACK (2)		CPS-FC203 SHEET 2
BELL TELEPHONE LABORATORIES INCORPORATED	6S	

ISSUE 2A

PART OF CPS FC203

CLOCK CIRCUIT

DIAGNOSTIC ACCESS
P/Ø A₂

CM1
P/Ø A

CM2

T1 T2 T3 T4

Q6 Q7 Q8

CR4

R11 R12 2150 R13 1210 R14 14.7 R15 2370 R16 237 R17 2870 R18 100 R19 100 R20 100 R21 100

C8 1200pF C9 316pF C10 215pF C11 .1 C13 0.1

NC

FC203 CIRCUIT PACK (2)

BELL TELEPHONE LABORATORIES INCORPORATED

CPS-FC203
SHEET 3

ISSUE 2A

CIRCUIT DESCRIPTION

A. FUNCTION

THE FC203 IS A CLOCK CIRCUIT PACK USED IN THE MAIN STORE CONTROLLER CIRCUIT (MASC). IT CONTAINS THE INTERFACE AND CONTROL CIRCUITS WHICH ENABLE COMMUNICATION WITH THE 3A CENTRAL CONTROL (3A CC) OVER THE SERIAL I/Ø CHANNEL (SIØC). IT ALSO CONTAINS THE MASC CLOCK OSCILLATOR AND ASSOCIATED CONTROLS, ONE BIT OF THE STORE ADDRESS REGISTER, AND AN ERROR REGISTER (ER) BIT.

B. DETAILED DESCRIPTION

NET NAME CONVENTIONS

A CONVENTION HAS BEEN CHOSEN AND USED FOR NET NAME MNEUMONICS:

1) THE LAST DIGIT OF A MNEUMONIC WILL BE EITHER 1 OR 0, INDICATING THE ACTIVE VOLTAGE LEVEL (HIGH OR LOW, RESPECTIVELY) OF THAT NET. E.G., NET SELIO IS ACTIVE WHEN VOLTAGE LOW.

2) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS AN I, THIS NET SERVES AS A SIGNAL INPUT TO THE CIRCUIT. E.G., SELIO IS AN INPUT, WHILE SELO IS NOT.

3) IF THE LAST CHARACTER OF A NET NAME IS A LETTER, THIS NET IS A MEMBER OF A PARALLEL GROUP OF NETS CARRYING THE SAME SIGNAL. E.G., SELOA, SELOB, AND SELOC WOULD BE THREE PARALLEL NETS, CARRYING THE SAME INFORMATION.

4) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS A B, THIS NET SERVES AS A SERIAL DUPLICATION OF THE NET WITHOUT THE B. E.G., SELBO IS THE SERIAL DUPLICATE OF SELO, SELBBO IS THE SERIAL DUPLICATE OF SELBO, ETC.

5) THE OUTPUTS OF A HIGH-LEVEL REGISTER; I.E., A 2-BIT REGISTER OR GATED DELAY FLIP-FLOP, UNLESS OTHERWISE RENAMED, WILL BE ACTIVE IF THE REGISTER IS SET. E.G., IF NET ERR.Q1 IS THE Q1 OUTPUT OF REGISTER ERR, THEN ERR.Q1 WILL BE ACTIVE IF REGISTER ERR IS SET. IF THIS NET IS RENAMED ERRØRO, THE NET WILL BE ACTIVE ONLY IF REGISTER ERR IS CLEARED.

6) IF THE FIRST CHARACTER OF A NET NAME IS THE LETTER T, THIS NET WILL BE A COLLECTOR-TIE (OUTPUTS FROM TWO OR MORE GATES TIED TO THE SAME NET). E.G., TSELO IS SUCH A NET.

WHILE THESE CONVENTIONS HAVE BEEN CONSCIENTIOUSLY FOLLOWED, THERE WERE CIRCUMSTANCES THAT PRECLUDED THEIR USE. IN SUCH CASES, THE NET WILL BE SPECIALLY NOTED.

C. SYMBOL/LEAD MNEMONICS

MNEMONIC	DEFINITION
AD17O	ADDRESS BIT 17 (OUTPUT)
AD171A	ADDRESS BIT 17 (OUTPUT TO BRANCH A)
AD171B	ADDRESS BIT 17 (OUTPUT TO BRANCH B)
BUFBOG	BUFFER BIT 0
CLINIT1	CLEAR INITIALIZE
CLØINIO	CLEAR THE CHANNEL ONE INHIBIT
DØUTIO	DATA OUT (TO SIØC FROM MASC)
ERIO	ERROR A REGISTER (INPUT)
FCKIO	FORCE CLOCK (DIAGNOSTIC INPUT)
FSTPCKIO	FORCE STOP CLOCK (DIAGNOSTIC INPUT)
GSAD17O	ADDRESS BUT BIT 17 (OUTPUT TO HIGHER ORDER STORES)
GSREQO	STORE REQUEST (OUTPUT TO HIGHER STORES)
IDO	INPUT DATA (FROM SIØC TO MASC)
INITIIO	INITIALIZE
IØNI1	INPUT ONE, NEGATIVE (SIØC INPUT TO MASC NEGATIVE FROM CHANNEL ONE)
IØPI1	INPUT ONE, POSITIVE (SIØC INPUT TO MASC POSITIVE FROM CHANNEL ONE)
IZNI1	INPUT ZERO, NEGATIVE (SIØC INPUT TO MASC NEGATIVE FROM CHANNEL ZERO)
IZPI1	INPUT ZERO, POSITIVE (SIØC INPUT TO MASC POSITIVE FROM CHANNEL ZERO)
NLDIO	NORMAL LOAD
ØØN1	OUTPUT ONE, NEGATIVE (SIØC OUTPUT FROM MASC NEGATIVE TO CHANNEL ONE)
ØØP1	OUTPUT ONE, POSITIVE (SIØC OUTPUT FROM MASC POSITIVE TO CHANNEL ONE)
ØZN1	OUTPUT ZERO, NEGATIVE (SIØC OUTPUT FROM MASC NEGATIVE TO CHANNEL ZERO)
ØZP1	OUTPUT ZERO, POSITIVE (SIØC OUTPUT FROM MASC POSITIVE TO CHANNEL ZERO)
PINITIO	POWER INITIALIZE INPUT
PINITO	POWER INITIALIZE OUTPUT
REFIO	REFRESH
REFO	REFRESH MODE
RESETO	RESET OF I/Ø FUNCTIONS
SAD17IO	ADDRESS BUS BIT 17 (INPUT)
SERAIO	STORE ERROR A (FROM HIGHER STORES)
SHFTIO	SHIFT
SHFTO	SHIFT (SIØC SHIFT SIGNAL)
SHSTPIO	SHIFT STOP
SREQIO	STORE REQUEST
TCKOA	CLOCK BRANCH A
TCKOB	CLOCK BRANCH B
TSERAO	STORE ERROR A OUTPUT

ISSUE 2A

FC203 CIRCUIT PACK (2)

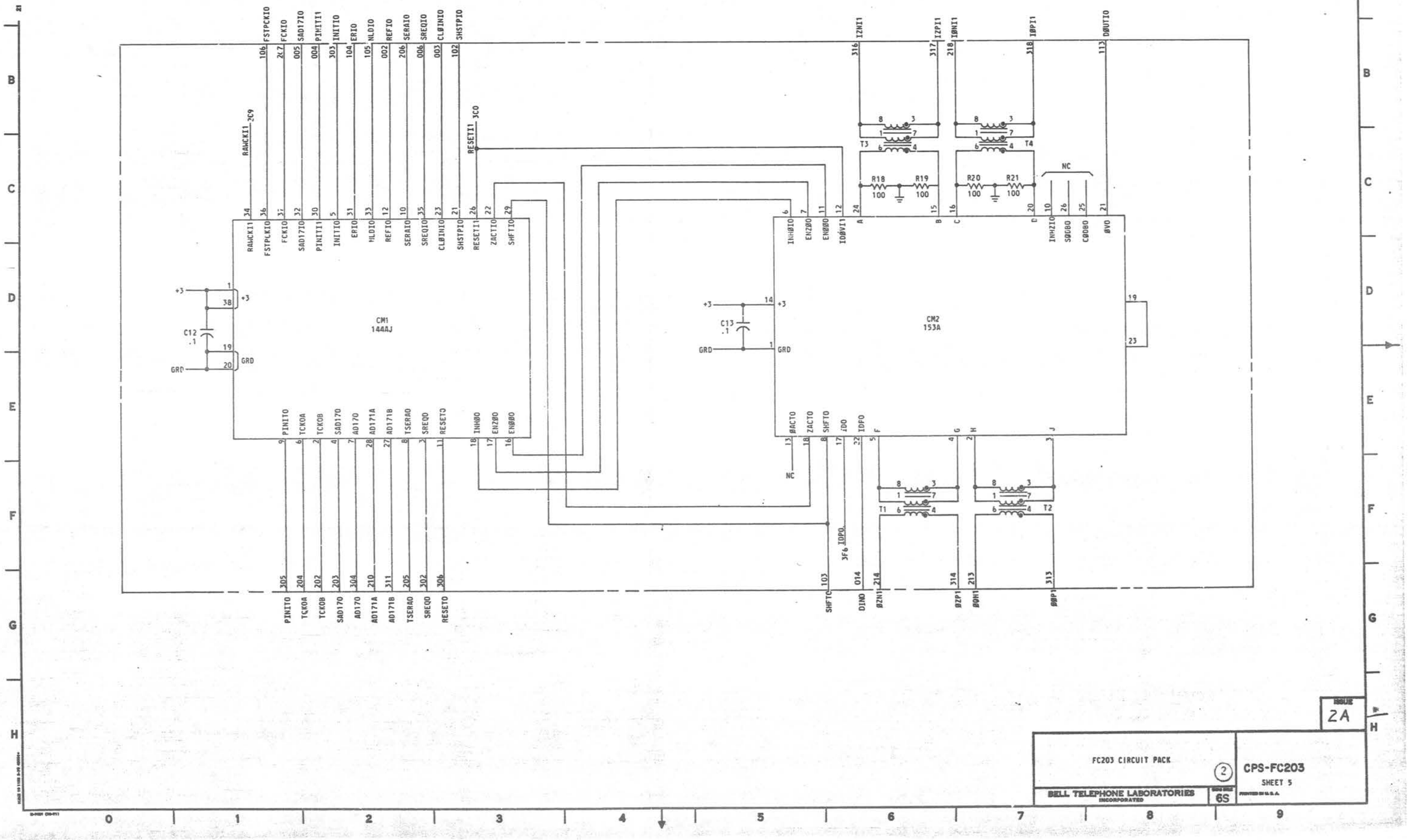
CPS-FC203
SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PART OF CPS FC 203

GENERAL BLOCK INTERCONNECTIONS



ISSUE
2A

FC203 CIRCUIT PACK (2)	CPS-FC203
BELL TELEPHONE LABORATORIES INCORPORATED	SHEET 5
	6S

PART OF CMS 144AJ

FSTPCKIO
FCKIO
INITIO
SAD171IO
ERIO
SERAIO
REFIO

FSTPCK1 IC9 137J E
FCK1 IC9 137J C
INIT IC9 137J G
SAD171A IC11 137J A
SAD171B IC11 137J B
SAD171C IC11 137J C
SAD171D IC11 137J D
SAD171E IC11 137J E
ER1 IC4 137J A
SERA1A IC4 137J C
SERA1B IC4 137J D
SERA1C IC4 137J E
SERA1D IC4 137J F
SERA1E IC4 137J G
REF1 IC5 137N B

NC

FSTPCKO IC1 137B B
TCKB0B IC1 137B A
TCKB0A IC1 137B F
INITO IC2 137N G

TCKOB
TCKOA

P/B A

FSTPCKO
TCKOB
TCKOA
INITO
6B1
AS

IC4 LR1
IC4 LR2
IC4 LR3

ERO IC2 137N F
TSERAO IC5 137N A
REFO IC5 137N D

FS REG AD17 IC3 1370 B
FS REG ER IC3 1370 A
AD171B IC12 137F B
AD171A IC12 137F A
SAD170 IC1 137B E
A170 IC5 137N H

NLDB1
NLDO
INITO
REFO
TSERAO

C1 3000pf
C2 3000pf
+3
GRD

SAD170
AD170
AD171B
AD171A
TSERAO

144AJ IC

ISSUE 2A

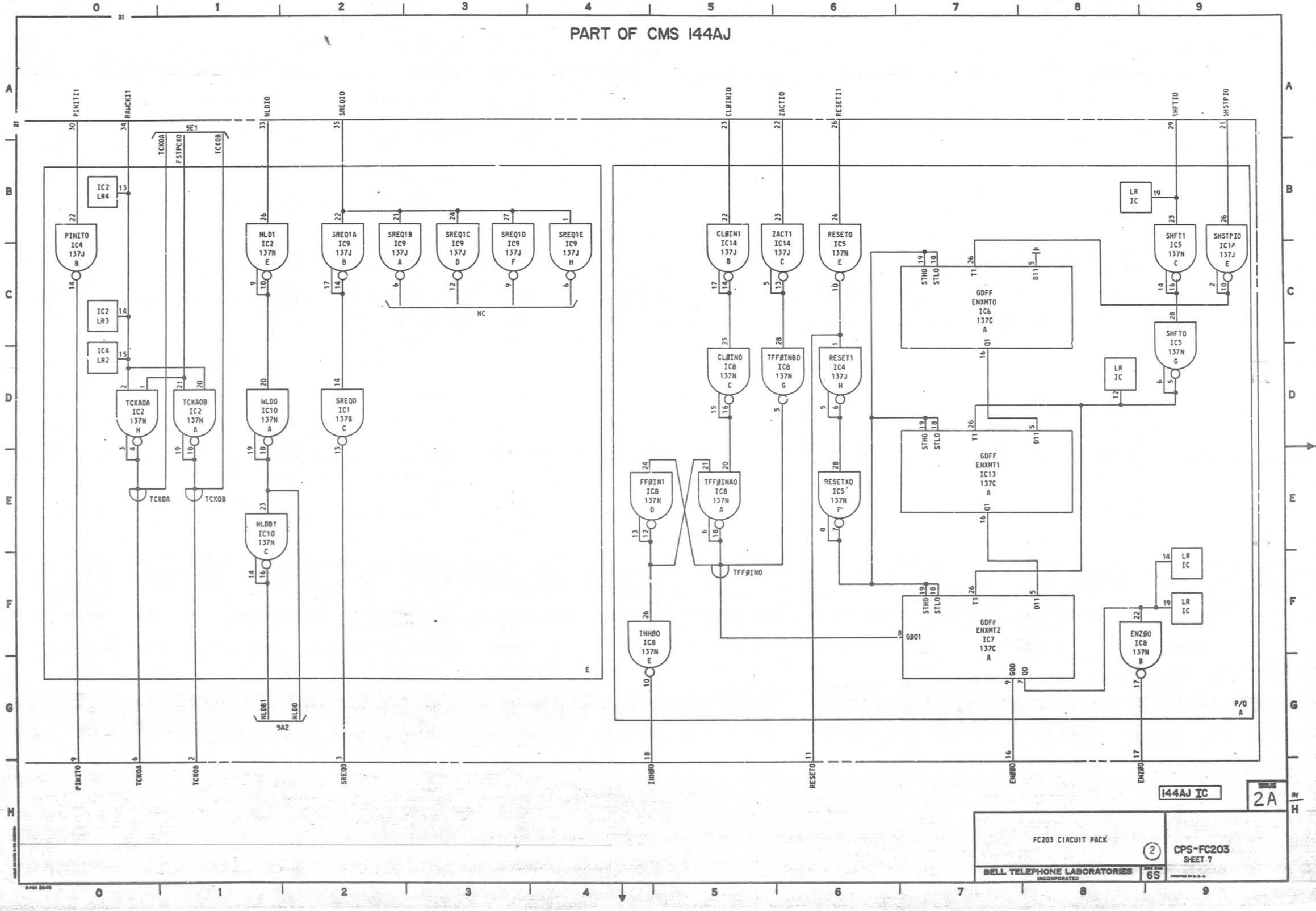
FC203 CIRCUIT PACK (2)

CPS-FC203 SHEET 6

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PART OF CMS 144AJ



PART OF CMS 144AJ

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 137B DESIG	SH LOC	IC2 137N DESIG	SH LOC	IC3 137D DESIG	SH LOC	IC4 137J DESIG	SH LOC	IC5 137N DESIG	SH LOC	IC6 137C DESIG	SH LOC	IC7 137C DESIG	SH LOC	LOC CODE ELEM ID
A	TCKBOB	5C1	TCKAOB	6D1	ERAD17	5D3	ER1	5B5	TSERAO	5D5	ENXMTO	6F7	ENXMT2	6C7	A
B	FSTPCKO	5CO					PINITO	6BO	REFi	5B8					B
C	SREQC	6D2					SERA1A	5B5	SHFT1	6B9					C
D							SERA1B	5B6	REFO	5D8					D
E	SAD17O	5F2	NLD1	6B2			SERA1C	5B6	RESETO	6B6					E
F	TCKBOA	5C1	ERO	5D5			SERA1D	5B7	RESETXO	6E6					F
G			INITO	5C2			SERA1E	5B7	SHFTO	6C9					G
H			TCKAOA	6DO			RESET1	6D6	A17O	5F3					H

LOC CODE ELEM ID	IC8 137N DESIG	SH LOC	IC9 137J DESIG	SH LOC	IC10 137N DESIG	SH LOC	IC11 137J DESIG	SH LOC	IC12 (NOTE 1) 137F DESIG	SH LOC	IC13 137C DESIG	SH LOC	IC14 137J DESIG	SH LOC	LOC CODE ELEM ID
A	TFFØINAO	6E5	SREQ1B	6B3	NLDO	6B1	SAD171A	5B2	AD171A	5G3	ENXMT1	6D7			A
B	ENZØO	6F8	SREQ1A	6B2			SAD171B	5B3	AD171B	5G3					B
C	CLØINO	6D5	FCK1	5B1	NLDB1	6E2	SAD171C	5B3					CLØIN1	6B5	C
D	FFEIN1	6E5	SREQ1C	6B3			SAD171D	5B4					ZACT1	6B6	D
E	INHØO	6F5	FSTPCK1	5BO			SAD171E	5B4							E
F			SREQ1D	6B4									SHSTPIC	6B9	F
G	TFFØINBO	6D6	INIT1	5B2											G
H			SREQ1E	6B4											H

CAPACITOR

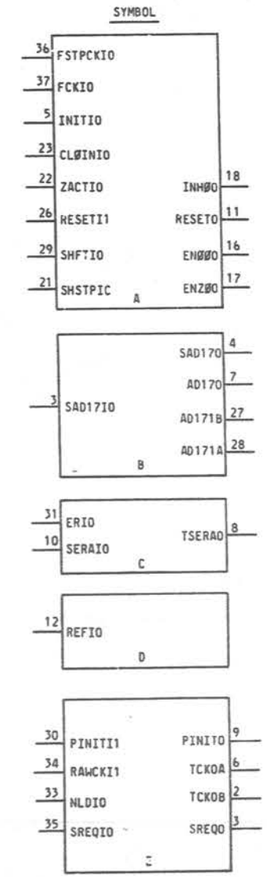
DESIG	CODE
[2] C1-C2	801A, 3000pf

NOTES:

1. A CAPACITOR CHIP (801A, 3000pf) IS BONDED ON EACH SIDE OF THE 137F SIC.

CIRCUIT DESCRIPTION

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE.

IC CODE	BAT TERM	GRD TERM
137B	25	11
137C	25	11
137D	25	11
137F	25	11
137J	25	11
137M	25	11
137N	25	11

144AJ IC

ISSUE 2A

SUPPORTING INFORMATION

CATEGORY	NO.
INTEGRATED CIRCUIT CODE	144AJ
ONLY ACCEPTABLE SERIES	6

FC203 CIRCUIT PACK (2)

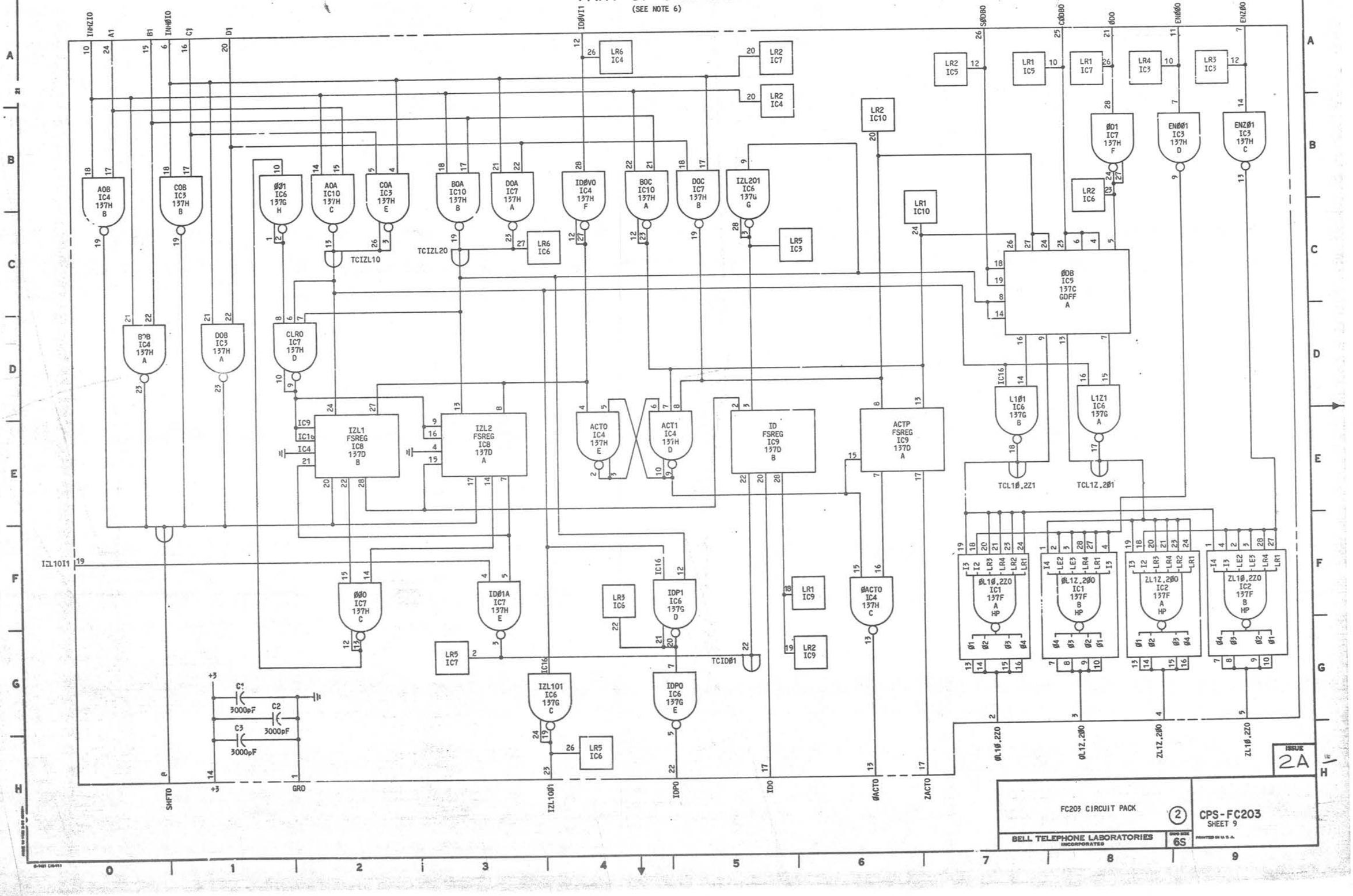
CPS-FC203 SHEET 8

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PART OF CMS 153A

(SEE NOTE 6)



ISSUE 2A

FC203 CIRCUIT PACK (2) CPS-FC203 SHEET 9

BELL TELEPHONE LABORATORIES INCORPORATED 6S

PRINTED IN U.S.A.

PART OF CMS 153A

(SEE NOTE 6)

COMPONENT LIST

INTEGRATED CIRCUIT

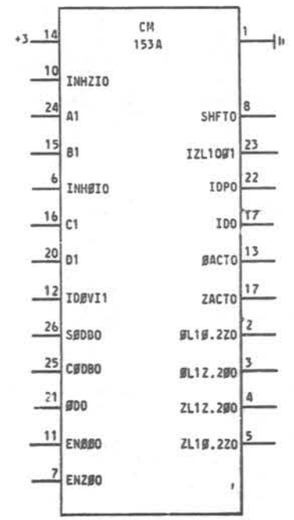
LOC CODE ELEM ID	IC1 137F (NOTE 1) DESIG	SH LOC	IC2 137F (NOTE 1) DESIG	SH LOC	IC3 137H DESIG	SH LOC	IC4 137H DESIG	SH LOC	IC5 137C DESIG	SH LOC	IC6 137G DESIG	SH LOC	IC7 137H DESIG	SH LOC	IC8 137D DESIG	SH LOC	IC9 137D DESIG	SH LOC	IC10 137H DESIG	SH LOC	LOC CODE ELEM ID
A	ØL1Ø.2ZO	8F7	ZL1Z.2Ø0	8F8	DOB	8D1	BOB	8DO	ØDB	8C8	L1Z1	8E8	DOA	8B3	IZL2	8E3	ACTP	8E6	BOC	8B4	A
B	ØL1Z.2Ø0	8F8	ZL1Ø.2ZO	8F9	COB	8B1	AOB	8BO			L1Ø1	8Ø7	DOC	8B5	IZL1	8E2	ID	8E5	BOA	8B3	B
C					ENZØ1	8B9	ØACTO	8F6			IZL101	8G4	ØØO	8F2					AOA	8B2	C
D					ENØØ1	8B9	ACT1	8E4			IDP1	8F4	CLRO	8D1							D
E					COA	8B2	ACTO	8E4			IDPO	8G5	IDØ1A	8F3							E
F					ØACTO	8F5	IDØVO	8B4					ØD1	8B8							F
G											IZL201	8B5									G
H											ØØ1	8B1									H

CAPACITOR

DESIG	CODE	
[3] C1-C3	801 A	3000 Pf

NOTES:
1. A CAPACITOR CHIP (801 A, 3000 Pf) IS BONDED ON EACH SIDE OF THE 137 F SIC.

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE:

IC CODE	BAT TERM	GRD TERM
137C	25	11
137D	25	11
137F	25	11
137H	25	11
137N	25	11

SPECIAL MANUFACTURING REFERENCES

CATEGORY	NO.
CONTROLLING DRAWING	FC200
CIRCUIT PACK CODE	FC200

SUPPORTING INFORMATION

CATEGORY	NO.
INTEGRATED CIRCUIT CODE	153A
(ANY HIGHER SERIES IS ACCEPTABLE)	3-4

153A IC

ISSUE 2A

FC203 CIRCUIT PACK

BELL TELEPHONE LABORATORIES INCORPORATED

DRAWING SIZE 6S

CPS-FC203
SHEET 10

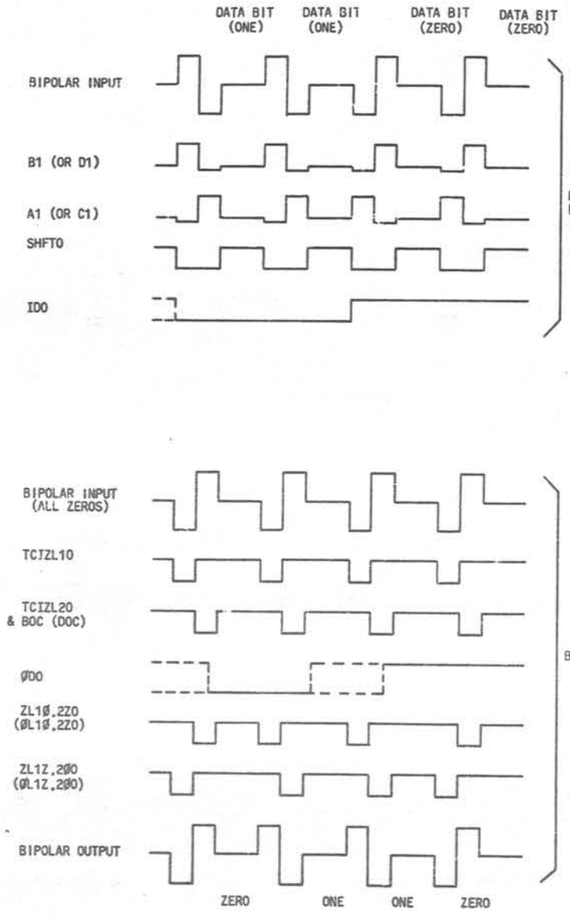


FIG. 1
BIPOLAR TO LOGIC LEVEL CONVERSION USING CM 153A

FIG. 2
LOGIC LEVEL TO BIPOLAR CONVERSION USING CM 153A

CIRCUIT DESCRIPTION

A. FUNCTION

CM 153A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC I/Ø DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN 0 ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER-RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CM 153A ON LEADS A1 AND B1 FROM CC0, AND C1 AND D1 FROM CC1. THE DATA IS OR'ED BY GATES AOA AND COA AT TCIZL10, AND BY GATES BOA AND DON AT TCIZL20. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CM 153A, AND ITS LOGIC-LEVEL DATA (IDO) AND TIMING (SHFTO) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC STATE OF THE BIPOLAR DATA BIT IS DETERMINED BY THE ORDER OF ITS POSITIVE AND NEGATIVE EXCURSIONS. A LOGICAL ONE IS A POSITIVE LOBE FOLLOWED BY A NEGATIVE LOBE. A LOGICAL ZERO IS A NEGATIVE LOBE FOLLOWED BY A POSITIVE LOBE. CLIPPING CIRCUITS, WHICH ARE PART OF GATES TO WHICH THE A1, B1, C1, AND D1 INPUTS CONNECT, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE GATES.

THE INPUT DATA LEAD (IDO) IS SET AT THE LEADING EDGE OF THE FIRST LOBE. THE TIMING SIGNAL IS THE TRAILING EDGE OF SHFTO WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOBE. THUS, THE CONTROLLER IS SIGNALED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE IDO AND SHFTO LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THESE SIGNALS. NOMINAL TIMES FOR THE 3A CC SERIAL I/Ø DATA ARE A 150-NS BIT INTERVAL WITH 37.5-NS LOBES.

THE SHFTO LEAD IS CONTROLLED BY GATES AOB, BOB, COB, AND DOB, AND FLIP-FLOPS IZL1 AND IZL2. INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT SHFTO IS HIGH. IF INH2IO AND INHØIO ARE NOT ACTIVE, THE FIRST LOBE OF THE INPUT DATA BIT WILL ACTIVATE ONE OF THE GATES (DEPENDING ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CC0 OR CC1) AND PULL SHFTO LOW. THE FIRST LOBE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TCIZL10 OR TCIZL20 WHICH WILL SET ONE OF THE FLIP-FLOPS, IZL1 OR IZL2, DEPENDING ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD SHFTO LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOBES AND TO PREVENT THE SECOND LOBE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (ID).

WHEN THE SECOND LOBE OF THE INCOMING DATA BIT IS ACTIVE THE MATE OF THE GATE ACTIVATED BY THE FIRST LOBE WILL BE ACTIVE, AND IT WILL ALSO HOLD SHFTO LOW (AOB AND BOB ARE MATES AS ARE COB AND DOB). THIS LOBE WILL ALSO SET THE FLIP-FLOP (IZL1 OR IZL2) THAT WAS NOT SET BY THE FIRST LOBE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP HELD SHFTO TO GROUND. WHEN THE FIRST LOBE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOBE HOLDS SHFTO LOW.

WITH BOTH FLIP-FLOPS SET, THE INPUT TO CLRO FROM ØØ1 IS HIGH. THE OTHER INPUTS TO CLRO, TCIZL10, AND TCIZL20 ARE CONTROLLED BY THE DATA LOBES. WHEN THE FIRST LOBE IS GONE, ONLY THE SECOND LOBE CONTROLS CLRO. WHEN THE SECOND LOBE EXPIRES, THE GATE HOLDING SHFTO IS DISABLED AND SHFTO WILL GO HIGH. CLRO WILL GO LOW AT THIS TIME AND CLEAR BOTH FLOP-FLOPS. CLRO LOW ALSO BLOCKS THE IZL1 AND IZL2 CONNECTION TO SHFTO SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE 00 STATE.

LEAD IDO IS CONTROLLED BY THE ID FLIP-FLOP. ID RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOBE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TCIZL10 WILL BE ACTIVE FIRST AND DRIVE GATE IZL101 HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT IDO1A HAS BOTH INPUTS HIGH. IT SHOULD BE NOTED THAT IZL1 AND IZL2 ARE INITIATED FROM THE CLEARED STATE AND THAT TCIZL10 SETS IZL1 BUT DOES NOT AFFECT IZL2. IDO1A WILL PULL TCIDØ1 LOW, WHICH WILL CLEAR ID AND DRIVE IDO HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOBE IS ACTIVE FOR THE ZERO DATA BIT, TCIZL20 WILL DRIVE IZL201 HIGH. HOWEVER, IZL1 WAS SET BY THE FIRST LOBE, IN ORDER TO PREVENT IZL201 FROM CHANGING THE ID FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TCIZL20 WILL BE ACTIVE FIRST, IZL201 WILL BE HIGH WHILE IZL1 IS CLEARED, AND THE ID FLIP-FLOP WILL BE SET. IDO WILL THUS BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOBE IS ACTIVE FOR AN INCOMING ONE, TCIZL10 IS ACTIVE, AND WILL DRIVE IZL101 HIGH. TCIZL20, HOWEVER, WILL HAVE SET IZL2, WHICH PREVENTS ID01A FROM CHANGING ID.

LEADS ZACTO AND ØACTO INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTO AND ACT1, IS SET BY GATES BOC ON DOC TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACTP IS SET BY BOC WHEN CC0 IS ACTIVE, A IS CLEARED BY DOC WHEN CC1 IS ACTIVE. THE ACT AND ACTP FLIP-FLOPS ARE COMBINED TO ACTIVATE ZACTO WHEN CC0 IS ACTIVE AND ØACTO WHEN CC1 IS ACTIVE. BOTH THE ZACTO AND ØACTO ARE HIGH WHEN NEITHER CC IS ACTIVE.

INHZIO AND INHØIO BLOCK INPUT DATA FROM CC0 AND CC1 WHEN THEY ARE ACTIVE.

LEAD IDPO WILL BE ACTIVE WHEN EITHER LOBE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOBES.

INPUT IDØU1 IS USED TO INITIALIZE THE IZL1 AND IZL2 TO THE 00 STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC FOLLOWS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITH AN ALL-ZEROS BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SENT TO THE 3A CC. THE 3A CC MAINTAINS THE ALL-ZEROS BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE MAXIMUM INTERVAL IN WHICH IT SHOULD RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 IS ACTIVE FOLLOWED BY B1 ACTIVE. INPUTS ENZØ0 AND ENØØ0 ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CC0 OR CC1.

GATES ZL1Ø,2Z0 AND ZL1Z,2Ø0 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CC0. GATES ØL1Ø,2Z0 AND ØL1Z,2Ø0 ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CC1. THESE GATES ARE HELD HIGH WHEN THERE IS NO INCOMING DATA OR WHEN THE ENABLE LEAD (EN2Ø0, ENØDO) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (ØDO) IS TOGGLED INTO ØDB PRIOR TO THE BIT PERIOD. THE OUTPUT OF ODB IS COMBINED WITH THE TIMING SIGNALS DERIVED FROM THE INCOMING DATA (TCIZL10 AND TCIZL20) TO DETERMINE THE ORDER IN WHICH TCL1Ø,2Z1 AND TCL1Z,2Ø1 WILL BE ACTIVE. IF A ONE IS TO BE SENT, TCL1Ø,2Z1 WILL BE ACTIVE DURING THE FIRST LOBE AND TCL1Z,2Ø1 WILL BE ACTIVE DURING THE SECOND LOBE. THE REVERSE WILL BE TRUE TO OUTPUT A ZERO. THESE SIGNALS WILL BE INVERTED BY THE ENABLED OUTPUT GATES ZL10,2Z0 AND ZL1Z,2Ø0 AND/OR ØL10,2Z0 AND ØL1Z,2Ø0.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER; EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THUS, THE ORDER IN WHICH THE GATES ARE ACTIVE DETERMINES THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY WINDING. NOTE THAT THE STATE OF THE ØDO LEAD IS TOGGLED INTO ODB BY BOC (OR DOC) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TRANSMITTED. INPUTS SØDBO AND CØDBO ALLOW DIRECT SET AND CLEAR OPERATIONS ON ØDB.

SYMBOL/LEAD

C. MNEMONICS

MNEMONIC	DEFINITION
ACTP	SET OR CLEARED TO DETERMINE WHICH INPUT PORT IS ACTIVE
ACTO,1	SET WHEN EITHER INPUT PORT IS ACTIVE
A1,B1	INPUTS FROM CC0
CØDBO	CLEAR ODB FF
C1,D1	INPUTS FROM CC1
ENØØ0	ENABLE OUTPUT TO CC1
ENZØ0	ENABLE OUTPUT TO CC0
ID	INCOMING DATA
IDØVI1	INCOMING DATA OVER, INPUT
IDPO	INCOMING DATA PRESENT
IZL1	INCOMING ZERO LOBE ONE - SET BY FIRST LOBE WHEN INPUT IS ZERO
IZL2	INCOMING ZERO LOBE TWO - SET BY SECOND LOBE WHEN INPUT IS ZERO
IDO	INCOMING DATA
ØACTO	CC1 IS ACTIVE
ØDB	OUTGOING DATA
ØDO	OUTGOING DATA BIT
ØL1Ø,2Z0	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CC1
ØL1Z,2Ø0	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC1
SHFTO	SHIFT
SØDBO	SET ODB FF
ZACTO	CC0 IS ACTIVE
ZL1Ø,2Z0	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CC0
ZL1Z,2Ø0	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC0

ISSUE 2A

FC203 CIRCUIT PACK (2)

CPS - FC203
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