CPS-FC207

SHEET INDEX

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SYMBOL
LEVEL CONTROL BOARD
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM.	LOC
COM	I	311	2F0
LRA	I	316	2G0
LRB	I	214	2G0
LRC	I	213	2G0
LRD	I	312	2H0
MARGIO	I	212	2G0
ØFCPDIO	I	205	2E0
SENS	I	310	2F0
TCCPDIO	I	210	2E0
IS1	Ø	303	2D9
LREN	Ø	206	2H4
LREP	Ø	305	2H3
MS1	Ø	204	2C9
NS1	Ø	304	2F9
+3	P	000	2H5
+24	P	018,118	2B0
GRD1	G	200,319	2H5
GRD2	G	0GD,2GD	2H4

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	PWR TERM.	GRD TERM.
5028G	15	11
5020E	13	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+3V	00G
+24V	018,118
GRD1	200,319
GRD2	0GD,2GD

5. HORIZONTAL MOUNTING CENTERS ARE 1.0 INCH.
6. CURRENT DRAIN: +3 AT 10 mA
   +24 AT 130 mA

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	Drawn	Appd
1		9-26-73	AS/SS WPM	RWF MTS RFG
2D1		1-24-74	PJS NGL	RWF MTS RFG
3D1		3-18-74	BTL NGL	RWF MTS RFG
4D1		4-8-74	BTL NGL	RWF MTS RFG
5A		11-8-74	AS LRE	JJR MTS RFG
6A		1-4-78	MA DKO	JLU LEG JBD

SUPPORTING INFORMATION

CATEGORY	NO.
CONNECTOR ON FRAME	947A OR 947C
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE).	4

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEM	TH

ISSUE 6A

1N98

FC207 CIRCUIT PACK

LEVEL CONTROL BOARD CIRCUIT

(2)

AT&TCO STANDARD

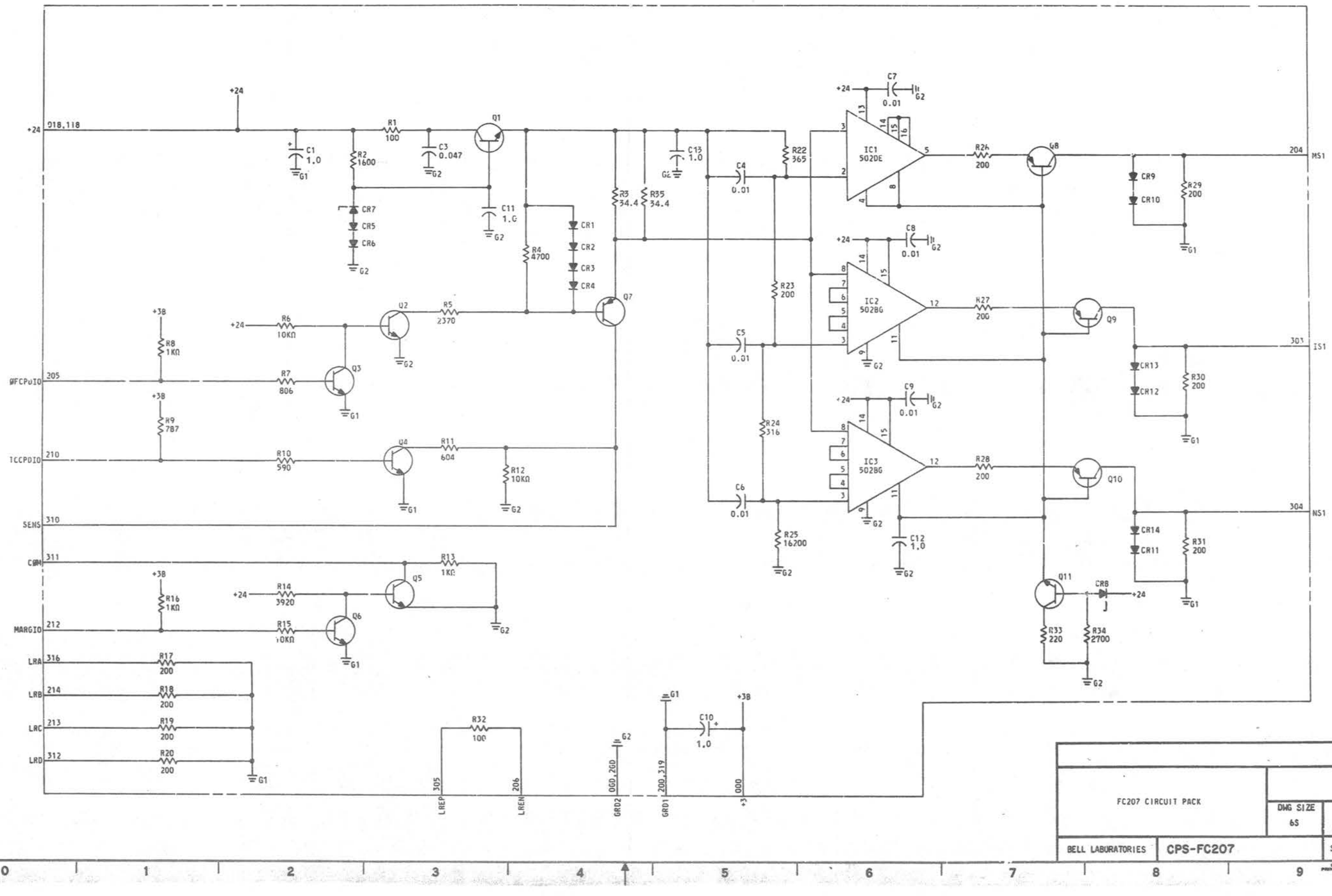
CPS-FC207
4 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED
6S
PRINTED IN U.S.A.

CPS-FC207

PART OF CPS FC207

LEVEL CONTROL BOARD CIRCUIT



FC207 CIRCUIT PACK		DWG SIZE 6S	ISSUE 6A
BELL LABORATORIES	CPS-FC207		SHEET 2

PART OF CPS FC207

LEVEL CONTROL BOARD CIRCUIT

COMPONENT LIST

CAPACITOR

	DESIG	CODE	
	C1	600A,	1.0
	C3	KS-19774 L5,	0.047
[6]	C4-C9	KS-19774 L1,	0.01
	C10	600A,	1.0
[3]	C11-C13	KS-20736 L1,	1.0

DIODE

	DESIG	CODE
[6]	CR1-CR6	458C
	CR7	459AC
	CR8	459AA
[6]	CR9-CR14	458C

INTEGRATED CIRCUIT

	DESIG	CODE
	IC1	502DE
[2]	IC2,IC3	502BG

RESISTOR

	DESIG	CODE	
	R1	KS-20289 L1A,	100
	R2	257A,	1600
	R3	257A,	34.4
	R4	KS-16645 L2,	4700
	R5	KS-20616 L1A,	2370
	R6	257A,	10KΩ
	R7		806
	R8		1KΩ
	R9		787
	R10		590
	R11		604
	R12		10KΩ
	R13		1KΩ
	R14		3920
	R15		10KΩ
	R16		1KΩ
[4]	R17-R20		200
	R22		365
	R23		200
	R24		316
	R25		16200
[6]	R26 R31	257A,	200
	R32		100
	R33	KS-19150 L1,	220
	R34	KS-16645 L2,	2700
	R35	257A,	34.4

TRANSISTOR

	DESIG	LOC
[4]	Q1-Q4	66W
[2]	Q5,Q6	66S
	Q7	58A
[4]	Q8-Q11	51A

FC207 CIRCUIT DESCRIPTION

THIS CIRCUIT PACK CONTROLS THE VOLTAGE POTENTIAL FOR A CPD PULSE, AS WELL AS MONITORS THE CURRENT PROVIDED TO THE CPD MATRIX. THE INPUTS HAVE A CONFIGURATION SIMILAR TO THAT OF AN INPUT BUFFER, SO THAT THESE INPUTS CAN BE DRIVEN BY 1A LOW-POWERED GATES. THE OUTPUTS NS1,IS1, AND MS1 HAVE BEEN DESIGNED TO DRIVE A LOAD PROVIDED BY AN INPUT BUFFER GATE. THE VOLTAGE POTENTIAL BETWEEN THE SENS AND THE COM LEADS IS APPROXIMATELY 17 VOLTS, WHICH IS USED TO DRIVE THE CPD MATRIX FOR THE PRODUCTION OF CPD PULSES.

THE THREE INPUTS OFCPDIO, TCCPDIO, AND MARGIO ARE USEL IN MAINTENANCE TESTING, SO THAT FOR NORMAL OPERATION (PRODUCTION OF NORMAL CURRENT LEVEL CPD PULSES), THESE INPUTS ARE HELD LOW (AT GROUND POTENTIAL). THE VOLTAGE FOR A CPD PULSE IS PRODUCED BY THE COMBINATION OF THE ZENER DIODE CR7, LOGIC DIODES CR5 AND CR6, AND THE EMITTER FOLLOWER CONFIGURATION OF TRANSISTOR Q1. THUS, THE BASE OF Q1 IS HELD AT 16.2 TO 18.4 VOLTS. THE NORMAL LOAD IMPEDANCE PROVIDED BY THE CPD MATRIX BETWEEN THE SENS (THE COLLECTER OF Q7) AND THE COM (WHICH USUALLY GOES TO GROUND THROUGH SATURATED TRANSISTOR Q5) LEADS IS 200 TO 268 OHMS. IN CASE OF A SHORT BETWEEN THE SENS AND COM LEADS, OR THE SENS LEAD AND GROUND, TRANSISTOR Q7, DIODES CR1 THRU CR4, AND RESISTORS R3 AND R35 WILL LIMIT THE SENSE CURRENT TO A MAXIMUM OF 120mA.

FOR MAINTENANCE PURPOSES THE INPUTS OFCPDIO, TCCPDIO, OR MARGIO CAN BE ACTIVATED (INPUT GOES HIGH TO APPROXIMATELY 1.05 VOLTS) DEPENDING UPON WHETHER NO CPD CURRENT, AN INTERMEDIATE LEVEL OF CURRENT OR A MARGINAL LEVEL OF CPD CURRENT IS TO BE GENERATED, RESPECTIVELY. IF THE OFCPDIO LEAD GOES HIGH TRANSISTOR Q3 SATURATES AND Q2 AND Q7 TURN OFF. WITH Q7 OFF NO CURRENT CAN FLOW INTO THE CPD MATRIX. THE TCCPDIO LEAD CAN BE USED TO GENERATE A REDUCED CURRENT LEVEL TO CHECK THE INTEGRITY OF THE MONITORING CIRCUITRY ON THIS PACK AND THE CURRENT LEVEL ERROR LOGIC (1A LOGIC ON FA1094). BY SWITCHING THIS INPUT HIGH, TRANSISTOR Q4 SATURATES, PLACING A 604 OHM RESISTOR R11 IN PARALLEL WITH THE 10 KILOHM RESISTOR R12, THUS PRODUCING ABOUT 30 TO 36 MILLIAMPERES OF CURRENT IN THE COLLECTOR OF Q7. THIS CIRCUIT STATE IS USED ONLY FOR MAINTENANCE TESTING THE CURRENT LEVEL DETECTING CIRCUITRY. IT SHOULD NOT BE ACTIVATED WHEN A CPD SELECTION PROVIDES A CURRENT PATH THROUGH THE CPD MATRIX, (SENS TO COM). THE MARGIO INPUT CAN BE USED TO GENERATE CPD PULSES WITH A CURRENT LEVEL OF 9.5 TO 12.5 MILLIAMPERES BY SWITCHING THIS INPUT HIGH, TRANSISTOR Q6 IS TURNED ON AND TRANSISTOR Q5 IS TURNED OFF PLACING A 1K RESISTOR IN SERIES WITH THE COM LEAD. THUS, INSTEAD OF CONNECTING 200 TO 268 OHMS, (THE LOAD DUE TO THE SELECTED CPD OUTPUT CIRCUITRY CONNECTED BETWEEN THE SENS AND COM LEADS), TO GROUND VIA THE COM LEAD, A 1.2 TO 1.268 KILOHM LOAD TO GROUND IS CONNECTED TO THE SENS LEAD. THE INCREASED RESISTANCE LOWERS THE PRIMARY CURRENT IN THE SELECTED CPD OUTPUT TRANSFORMER AND REDUCES THE AMPLITUDE OF THE OUTPUT PULSE.

MONITORING OF THE CURRENT IN THE SENSE LEAD IS ACCOMPLISHED BY THE 502DE, (IC1), AND THE TWO 502BG, (IC2 AND IC3), INTEGRATED COMPARATORS. THE SENSE LEAD CURRENT TO THE CPD MATRIX PLUS THE BASE CURRENT OF Q7 FLOWS THROUGH THE PARALLEL COMBINATION OF R3 AND R35. THE VOLTAGE DEVELOPED ACROSS R3 AND R35 WILL BE PROPORTIONAL TO THE SENSE CURRENT WHICH FLOWS TO THE CPD MATRIX TO GENERATE THE CPD OUTPUT PULSES. THE VOLTAGE ACROSS R3 AND R35 IS USED AS A COMMON INPUT TO ALL THREE COMPARATORS, EACH COMPARATOR HAS A DIFFERENT REFERENCE VOLTAGE TO WHICH IT COMPARES THE SENSE VOLTAGE INPUT. THUS, EACH OF THE COMPARATORS OUTPUTS WILL GO POSITIVE AT A DIFFERENT SENSE CURRENT LEVEL.

THE REFERENCE VOLTAGES USED BY THE THREE COMPARATORS HAVE BEEN SET SO AS TO DISTINGUISH THREE DIFFERENT CPD PULSE CURRENT LEVELS. THE OUTPUTS NS1, IS1, AND MS1, THEREFORE, REPRESENT MONITORED CURRENT LEVELS ABOVE THREE THRESHOLDS. THE NS1 CURRENT THRESHOLD LEVEL IS ABOUT 43 MILLIAMPERES. THE IS1 THRESHOLD LEVEL IS ABOUT 25 MILLIAMPERES, AND THE MS1 CURRENT THRESHOLD LEVEL IS ABOUT 14 MILLIAMPERES. THE ACTUAL OPERATION OF MONITORING THE CURRENT IS ACCOMPLISHED BY COMPARING THE EMITTER VOLTAGE OF Q7 TO THE VARIOUS REFERENCE VOLTAGES OF THE COMPARATORS. THE THREE REFERENCE VOLTAGES ARE PRODUCED BY THE VOLTAGE DIVIDER MADE UP OF RESISTORS R22, R23, R24 AND R25.. THE VOLTAGE APPLIED TO THE DIVIDER IS THE REGULATED VOLTAGE AT THE EMITTER OF Q1 TO GROUND.

CURRENT FLOWING IN THE SENS LEAD WILL CAUSE A PROPORTIONAL VOLTAGE ACROSS THE PARALLEL COMBINATION OF R3 AND R35 (AT THE EMITTER OF Q7). IF THIS VOLTAGE IS MORE POSITIVE THAN THE REFERENCE LEVEL OF A PARTICULAR COMPARATOR, THE OUTPUT OF THAT COMPARATOR WILL BE HELD "LOW" (A Vce SAT ABOVE THE REGULATED VOLTAGE AT THE BASE OF LEVEL SHIFTING TRANSISTORS Q8, Q9, OR Q10). UNDER THESE CONDITIONS THE LEVEL SHIFTING TRANSISTOR ASSOCIATED WITH THE COMPARATOR WILL BE TURNED "OFF" AND THE MS1, IS1, AND NS1 OUTPUTS HELD LOW BY RESISTORS R29, R30 AND R31, RESPECTIVELY.

FC207 CIRCUIT DESCRIPTION (CONT)

WHEN THE CURRENT FLOWING IN THE SENSE LEAD EXCEEDS THE THRESHOLD OF A COMPARATOR, THE VOLTAGE AT THE EMITTER OF Q7 BECOMES NEGATIVE WITH RESPECT TO THE REFERENCE VOLTAGE OF THE COMPARATOR. UNDER THESE CONDITIONS THE OUTPUT OF THE COMPARATOR WILL GO POSITIVE. (RELATIVE TO THE REFERENCE VOLTAGE AT THE EMITTER OF Q11). THE ASSOCIATED LEVEL SHIFTING TRANSISTOR, (Q8, Q9 OR Q10), WILL BE TURNED ON BY THE POSITIVE COMPARATOR OUTPUT AND CAUSE A "HIGH" GOING SIGNAL ON THE ASSOCIATED OUTPUT LEAD (MS1, IS1 OR NS1, RESPECTIVELY). THE DIODES CR9-CR14 ACROSS RESISTORS R29, R30 AND R31 ARE USED TO LIMIT THE "HIGH" GOING OUTPUT SIGNALS TO ABOUT 1.2V WHEN TRANSISTORS Q8, Q9 OR Q10 ARE TURNED "ON".

CR8, R34, R35 AND Q11 PROVIDE A REFERENCE VOLTAGE FOR THE COMPARATOR OUTPUTS AND OUTPUT LEVEL CONVERTING TRANSISTORS OF APPROXIMATELY 13V.

CAPACITORS C1 AND C10 PERFORM A FILTERING FUNCTION FOR THE +24 VOLT AND +3 VOLT POWER SUPPLIES. THE 100 OHM RESISTOR (R16) IS USED AS A TERMINATION FOR TESTING OF CPD POINTS. THE FOUR INPUTS LRA, LRB, LRC, AND LRD ARE USED TO TERMINATE THE BACKPLANE LEADS WHICH CONTAIN THE 3A CC CLOCK PHASES.

FC207 CIRCUIT PACK		DWG SIZE 6S	ISSUE 6A
BELL LABORATORIES	CPS-FC207		SHEET 3

PART OF CPS FC207
LEVEL CONTROL BOARD CIRCUIT

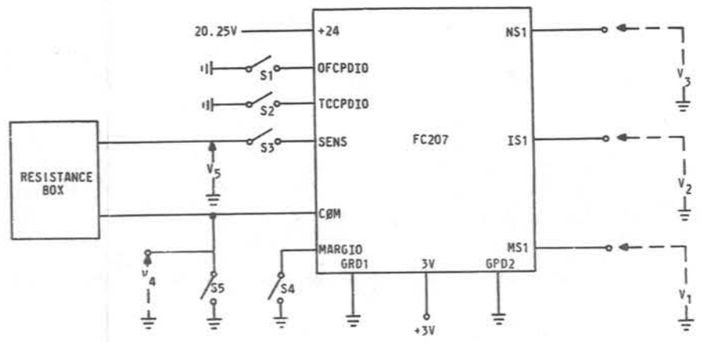
ALL FC207 CIRCUIT PACKS SHALL BE CAPABLE OF PASSING THE FOLLOWING TESTS.

1.0 DC TESTS

FC207 SHALL BE CONNECTED AS SHOWN. POWER SUPPLY VOLTAGES MUST BE CAPABLE OF MAINTAINING INDICATED VOLTAGE ±5%. RESISTANCE BOX MUST HAVE A RANGE OF 1 TO 1505 OHMS AND A TOLERANCE OF ±1% OR LOWER.

S1	S2	S3	S4	S5	RES BOX SETTING	V1	V2	V3	V4	V5
X	X	X	X	X	7Ω	≥1.2V	≥1.2V	≥1 ↵		<1.0V
X	X	X	X	X	1505Ω	≤0.1V	≤0.1V	≤0.1V		15 TO 17V
X	X	X	X	X	1081Ω	≥1.2V	≤0.1V	↓		↓
X	X	X	X	X	718Ω	↓	≤0.1V	↓		↓
X	X	X	X	X	605Ω	↓	≥1.2V	↓		↓
X	X	X	X	X	403Ω	↓	↓	≤0.1V		↓
X	X	X	X	X	346Ω	↓	↓	≥1.2V		↓
X	X	X	X	-	200Ω	≥1.2V	≥1.2V	≥1.2V	≤1V	15 TO 17V
-	X	X	X	-	200Ω	≤0.1V	≤0.1V	≤0.1V		≤1V
X	X	X	-	-	200Ω	≥1.2V	≤0.1V	≤0.1V		15 TO 17V
X	-	-	X	-		≥1.2V	≥1.2V	≤0.1V		15 TO 17V

X SWITCH CLOSED
\- SWITCH OPEN
☐ (BLANK) DON'T CARE



2.0 AC TESTS

AC OPERATION OF THE FC207 CAN BE CHECKED BY PERFORMING THE FOLLOWING TESTS. THE FC207 SHOULD BE CONNECTED AS SHOWN. THE POWER SUPPLIES MUST BE CAPABLE OF MAINTAINING THE INDICATED VOLTAGES ±1%. THE PULSE GENERATOR USED SHOULD BE CAPABLE OF GENERATING A NEGATIVE OUTPUT PULSE OF 450ns WIDTH AT A 6μSEC REPETITION RATE. THE RISE TIME OF THE 450ns PULSE SHOULD BE 5ns OR LESS, AND THE PULSE AMPLITUDE SHOULD BE ADJUSTABLE FROM -.5V TO -10V WHEN TERMINATED IN 50Ω (DATA PULSE 101 OR EQUIVALENT).

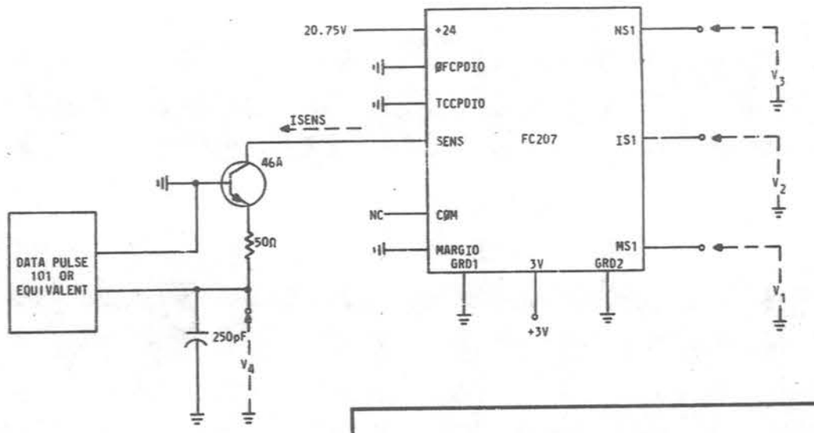
THE VOLTAGE WAVEFORMS AT V1-V4 SHOULD BE MONITORED WITH AN OSCILLOSCOPE CAPABLE OF RELIABLE TRIGGERING, AND ABLE TO VIEW AT LEAST TWO OF THE OUTPUT WAVEFORMS FOR TIMING COMPARISONS. FOR TEST ACCURACY IN TIMING CHECKS, THE OSCILLOSCOPE TIME BASE SHOULD ALLOW VIEWING THE OUTPUTS ON A 10ns/CM DISPLAY (TEKTRONIX 7000 SERIES OSCILLOSCOPE OR EQUIVALENT).

THE CURRENT PULSE IN THE SENSE LEAD, (ISENS), SHOULD BE MONITORED USING A CURRENT PROBE ATTATCHED TO THE OSCILLOSCOPE. THE PROBE SHOULD BE OF SUFFICIENT SENSITIVITY TO ACCURATELY DETERMINE THE AMPLITUDE OF CURRENT PULSES OF 15mA TO 200 mA (TEKTRONIX P6042 OR EQUIVALENT).

2.1 ADJUST THE PULSE GENEFATOR FOR A NEGATIVE OUTPUT PULSE 450ns WIDE WITH A REPETITION RATE OF 6μSEC.

TEST NO.	ADJUST ISENS CURRENT LEVEL	MONITOR OUTPUT	MONITOR FOR:	OUTPUT TIMING	WAVEFORMS AND TIMING DIAGRAMS	PURPOSE OF THE TEST
1.	ADJUST V4 UNTIL THE ISENS CURRENT PULSE IS 16mA.	V1	AN OUTPUT PULSE ≥1.2V AND WIDER THAN 300ns.	THE OUTPUT AT V1 SHOULD BE ≥1V WITHIN 50ns AFTER ISENS CROSSES THE 15mA LEVEL.	15mA, 0, ISENS, <50ns, 0, *, V1	THIS TEST MEASURES THE DELAY IN THE RESPONSE OF THE MARGINAL CURRENT LEVEL DETECTOR WHEN A MARGINAL CURRENT IS FLOWING IN THE SENSE LEAD.
2.	ADJUST V4 UNTIL THE ISENS CURRENT PULSE IS 60mA.	V1 V2 V3	AN OUTPUT PULSE ≥1.2V AND WIDER THAN 350ns. AN OUTPUT PULSE ≥1.2V AND WIDER THAN 250ns. AN OUTPUT PULSE ≥1.2V AND WIDER THAN 250ns.	THE OUTPUT AT V1 SHOULD BE ≥1V WITHIN 30ns AFTER ISENS CROSSES THE 15mA LEVEL. THE OUTPUT AT V2 SHOULD BE ≥1V WITHIN 200ns AFTER ISENS CROSSES THE 25mA LEVEL. THE OUTPUT AT V3 SHOULD BE ≥1V WITHIN 200ns AFTER ISENS CROSSES THE 45mA LEVEL.	45mA, 25mA, 15mA, 0, ISENS, <30ns, 0, *, V1, <200ns, 0, V2, <200ns, 0, *, V3	THIS TEST MEASURES THE DELAY IN THE RESPONSE OF THE MARGINAL, (V1), INTERMEDIATE, (V2), AND NORMAL (V3), CURRENT LEVEL DETECTORS WHEN A NORMAL CURRENT IS FLOWING IN THE SENSE LEAD.

* V1, V2 AND V3 TIMES MEASURED AT THE 1V CROSSING



FC207 CIRCUIT PACK		DWG SIZE 6S	ISSUE 6A
BELL LABORATORIES	CPS-FC207		SHEET 4