CPS-FC210

PART OF CPS FC210

POWER ALARM AND CONTROL CIRCUIT

SHEET INDEX

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SYMBOL

CONTROL
ELEMENT IDENT
A

TERM. MOD	FUNCT	TERM.	LOC
APØNO	I	205	2A5
BPØNO	I	101	7A6
DBPØNI1	I	201	2A2
LØFF1	I	001	2A3
LØFF1G	I	100	2A4
PØFF0	I	203	2A4
PØFF0G	I	303	2A4
DBPØNØ1	Ø	102	2G5
ØBRLY0	Ø	002	2G3
PWRØN1	Ø	301	2G6
PWRØN1G	Ø	202	2G6

ALARMS
ELEMENT IDENT
B

+AA01	I	117	3A2
+AA11	I	215	3A5
+AA21	I	316	3A7
+AB01	I	018	3A2
+AB11	I	315	3A5
+AB21	I	217	3A8
-AA00	I	116	3A3
-AA10	I	016	3A6
-AA20	I	210	3A8
CLR00	I	017	3A2
CLR10	I	314	3A5
CLR20	I	216	3A7
ØRLY00	Ø	208	3G1
ØRLY10	Ø	302	3G4
ØRLY20	Ø	307	3G7
+24A	P	019,118	3G2
+24B	P	015,114	3G2
+24C	P	218,318	3G2
GRD	G	200,260	3G2

TEST
ELEMENT IDENT
C

NPAI0	I	308	4A3
NPA1	I	003	4A2
ØPATR1	I	305	4A5
RNPARI0	I	013	4A4
NPAØ0	Ø	012	4G2
ØNPARO	Ø	211	4G4
ØPATR0	Ø	206	4G5
PAR1	Ø	113	4G6
RNPARØ0	Ø	209	4G3

NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT TERM.	GRD TERM.
502AJ		3
502BK		3

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+24A	019,118
+24B	015,114
+24C	218,318
	060,200

5. +24D IS INTERNALLY DERIVED FROM +24VA.
6. HORIZONTAL MOUNTING CENTERS AT 1.0 INCH.

CURRENT DRAIN

50mA AT +24V

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

MANUFACTURING REFERENCES

CATEGORY	NO.
CIRCUIT PACK CODE	FC210
CONNECTOR ON FRAME	947A OR 947C
SERIES NO. IDENT	FOR LATEST CLASS "A" CHANGE ACCEPTABLE SERIES 2

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	DESIGNED	APPD
1		3-11-74	NCL	RLP MTG RFG
2D1		3-26-74	BTL NCL	RLP MTG RFG
3A		5-7-75	P/S LDD	JJR MTG RFG
4D1		6-23-78	RLN RJR	RAW JOB MTG

ISSUE 4D1

1N98

FC210 CIRCUIT PACK

POWER ALARM AND CONTROL CIRCUIT

AT&TCO STANDARD

(2)

CPS-FC210
5 SHEETS

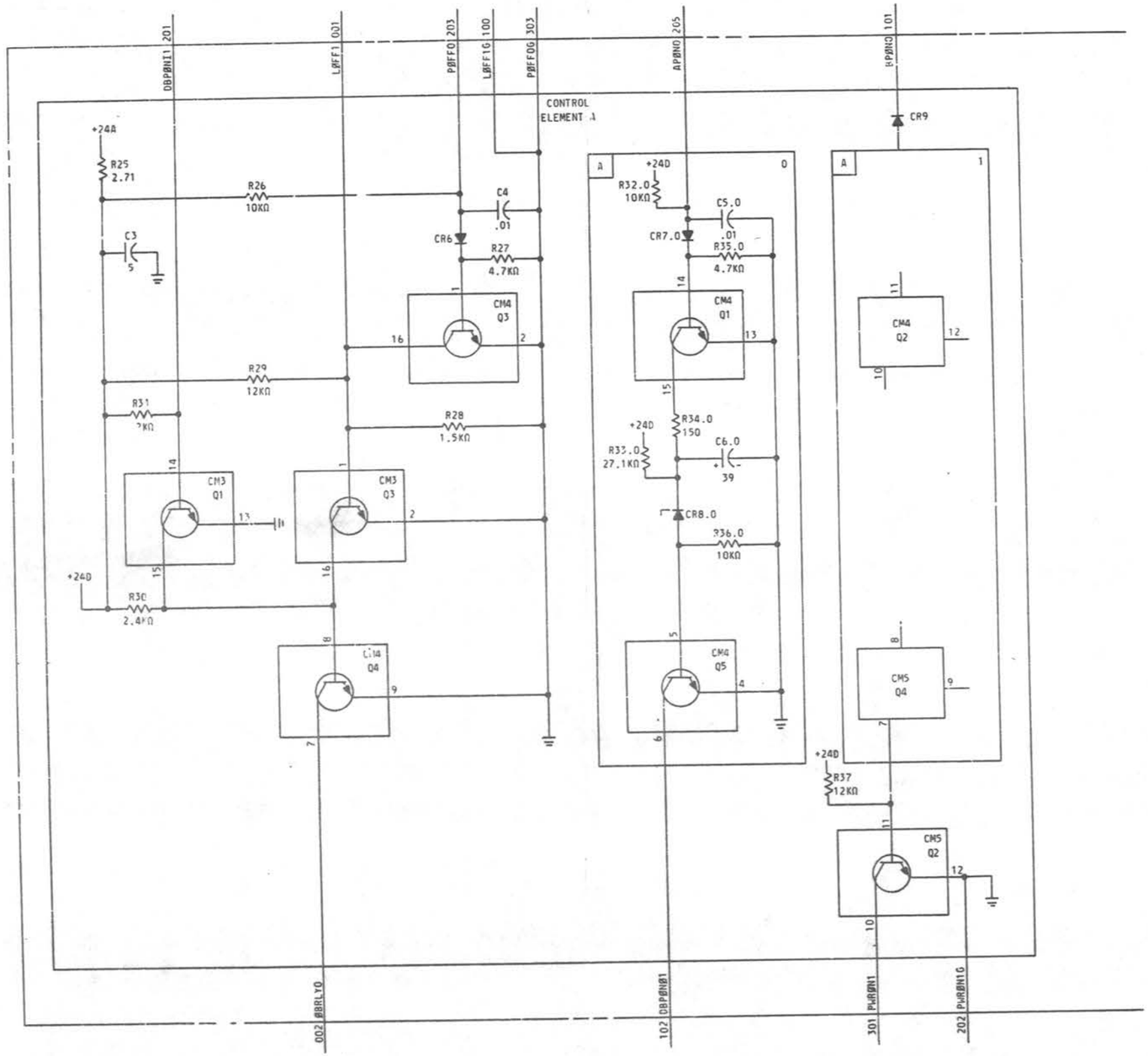
BELL TELEPHONE LABORATORIES INCORPORATED

SIZE 6S

CPS-FC210

PART OF CPS FC210

POWER ALARM AND CONTROL CIRCUIT



CPS-FC210

ISSUE	3A
FC210 CIRCUIT PACK (2)	CPS-FC210 SHEET 2
BELL TELEPHONE LABORATORIES INCORPORATED	SIZE 6S

PART OF CPS FC210

POWER ALARM AND CONTROL CIRCUIT

ALARMS ELEMENT B

CLR00 017 | +AA01 117 | +AB01 018 | -AA00 116 | CLR10 314 | +AA11 215 | +AB11 315 | -AA10 016 | CLR20 216 | +AA21 316 | +AB21 217 | -AA20 210

+24A

CR2.0

R15.0 12KΩ

CM1 Q4

R14.0 4.7KΩ

R1.0 20KΩ

C.0 .01

CR1.0

R7.0 20KΩ

R8.0 20KΩ

R3.0 20KΩ

R13.0 8.25KΩ

CR3.0

C2.0 .01

R12.0 4.7KΩ

R11.0 47KΩ

R6.0 10KΩ

R5.0 10KΩ

R4.0 1KΩ

CM1 Q1

CM1 Q5

R10.0 4.7KΩ

CM2 Q5

+24B

CM5 Q1

CM5 Q3

CM1 Q2

CM5 Q5

+24C

CM2 Q1

CM2 Q2

CM1 Q3

CM2 Q4

200 @RLY00 | 019 118 +24A | 200 200 GRD | 015 114 +24B | 218 318 +24C

302 @RLY10

307 @RLY20

CPS-FC210

3A

FC210 CIRCUIT PACK (2)

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CPS-FC210 SHEET 3

PART OF CPS FC210

POWER ALARM AND CONTROL CIRCUIT

COMPONENT LIST

CAPACITOR

	DESIG	CODE
[3]	C1.0-C1.2	KS-19774 L1,.01
[3]	C2.0-C2.2	KS-19774 L1,.01
	C3	601A,5
	C4	KS-19774 L1,.01
[2]	C5.0,C5.1	KS-19774 L1,.01
[2]	C6.0,C6.1	614C, 39

DIODE

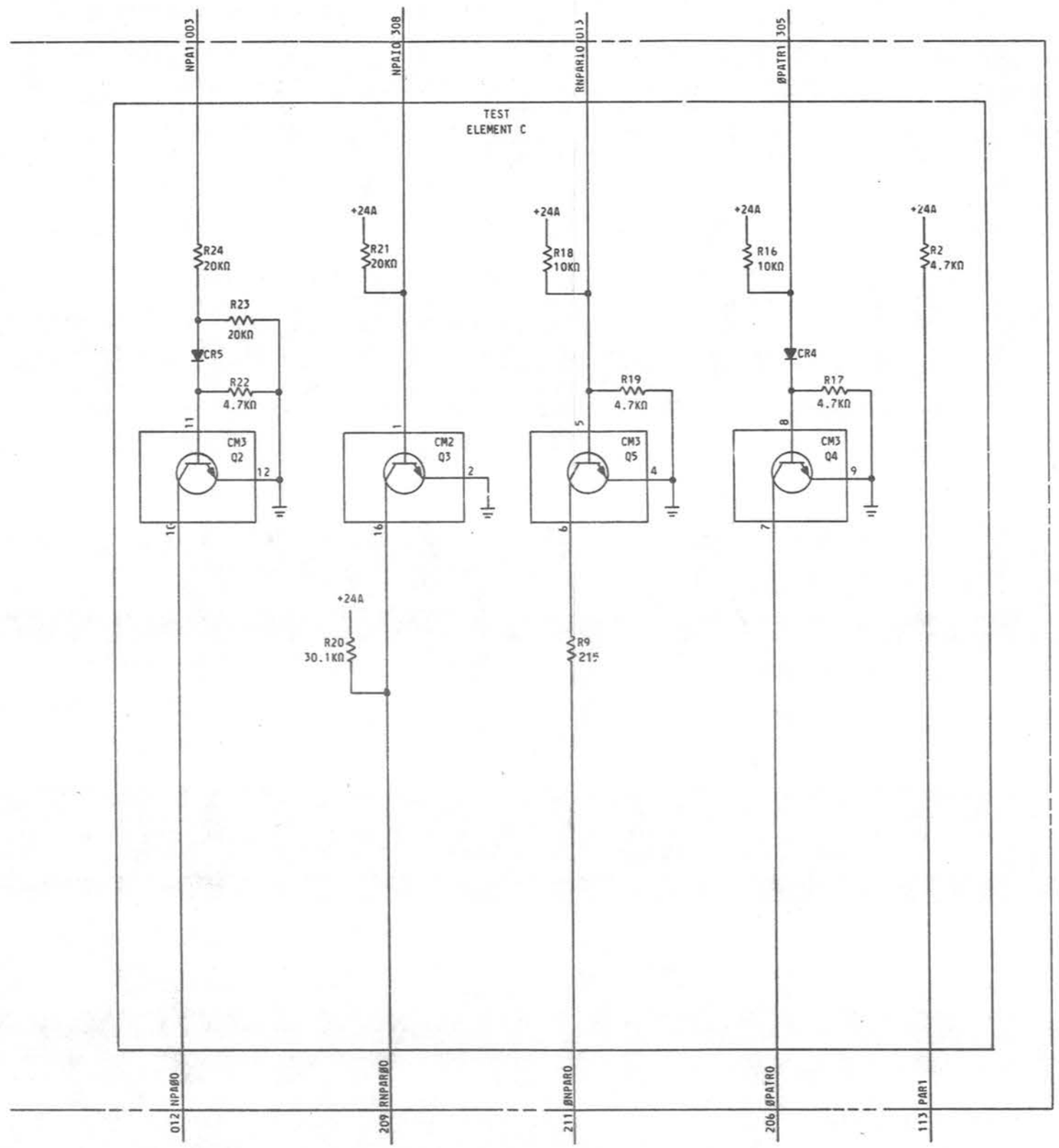
	DESIG	CODE
[3]	CR1.0-CR1.2	458A
[3]	CR2.0-CR2.2	458A
[3]	CR3.0-CR3.2	458A
[3]	CR4-CR6	449A
[2]	CR7.0,CR7.1	449A
[2]	CR8.0,CR8.1	459J
	CR9	458A

INTEGRATED CIRCUIT

	DESIG	CODE
	CM1	502AJ
[4]	CM2-CM5	502BK

RESISTOR

	DESIG	CODE
[3]	R1.0-R1.2	257A, 20KΩ
	R2	KS-20616, L1A,4.7KΩ
[3]	R3.0-R3.2	257A,20KΩ
[3]	R4.0-R4.2	1KΩ
[3]	R5.0-R5.2	10KΩ
[3]	R6.0-R6.2	10KΩ
[3]	R7.0-R7.2	20KΩ
[3]	R8.0-R8.2	257A,20KΩ
	R9	KS-14603 L3A, 21[illegible]
[3]	R10.0-R10.2	257A,4.7KΩ
[3]	R11.0-R11.2	KS-20616, L1A,4.7KΩ
[3]	R12.0-R12.2	257A,4.7KΩ
[3]	R13.0-R13.2	8.25KΩ
[3]	R14.0-R14.2	4.7KΩ
[3]	R15.0-R15.2	12KΩ
	R16	10KΩ
	R17	4.7KΩ
	R18	10KΩ
	R19	4.7KΩ
	R20	30.1KΩ
	R21	20KΩ
	R22	4.7KΩ
	R23	20KΩ
	R24	257A,20KΩ
	R25	KS-20616, L1A 2.7[illegible]
	R26	257A,10KΩ
	R27	4.7KΩ
	R28	1.5KΩ
	R29	257A,12KΩ
	R30	KS-19150 L1,2.4KΩ
	R31	257A,12KΩ
[2]	R32.0,R32.1	10KΩ
[2]	R33.0,R33.1	27.1KΩ
[2]	R34.0,R34.1	150
[2]	R35.0,R35.1	4.7KΩ
[2]	R36.0,R36.1	10KΩ
	R37	257A,12KΩ



CPS-FC210

4D1

FC210 CIRCUIT PACK (2)

CPS-FC210 SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CIRCUIT DESCRIPTION

A. FUNCTION

THE FC210 CIRCUIT PACK CONTAINS LOGIC AND TIMING CIRCUITS USED TO CONTROL, TEST AND ALARM POWER IN THE MAINTENANCE AND PROCESSOR FRAMES.

B. DETAILED DESCRIPTION

LEADS WITH MNEMONICS THAT END IN 1 ARE GENERALLY HIGH WHEN ACTIVE OR IN THE ONE STATE. THOSE THAT END IN 0 ARE GENERALLY LOW WHEN ACTIVE OR IN THE ONE STATE.

CONTROL - ELEMENT A

OUTPUT ØBRLYO CAN SINK UP TO 50 MILLIAMPERES FROM A SOURCE LESS THAN 30 VOLTS. IT IS CONTROLLED BY INPUTS DBPØNI1, LØFF1 AND PØFFO IN ACCORDANCE WITH THE FOLLOWING TABLE:

TABLE A

DBPØNI1	LØFF1	PØFFO	ØBRLYO
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

VOLTAGE DIVIDER R29 AND R28 LIMITS THE POTENTIAL AT LØFF1 TO LESS THAN 3 VOLTS IN THE EVENT THAT Q3 OF CM3 FAILS IN ORDER TO PROTECT THE CP LOGIC GATE THAT DRIVES LØFF1. C4,CR6, AND R27 PROVIDE NOISE IMMUNITY ON THE PØFFO INPUT. LØFF1G AND PØFF1G ARE TERMINATIONS FOR GROUND LEADS PAIRED WITH LØFF1 AND PØFF1 TO ALLOW THE SOURCE FOR THESE SIGNAL LEADS TO BE IN A DIFFERENT UNIT FROM THE FC210 CIRCUIT PACK.

DPBØNØ1 IS CONTROLLED BY APØNO THROUGH A DELAY CIRCUIT. WHEN APØNO IS OPEN, R32.0 TURNS ON Q1 OF CM4 WHICH CUTS OFF Q5 OF CM4 AND ALLOWS DBPØNØ1 TO GO HIGH. DBPØNØ1 CAN SINK 2.5 MILLIAMPERES FROM A 30-VOLT SOURCE. WHEN APØNO IS GROUNDED Q1 CUTS OFF AND C6.0 CHARGES TO +24 VOLTS THROUGH R33.0. WHEN C6.0 HAS CHARGED TO APPROXIMATELY 12.8 VOLTS, CR8.0 TURNS ON Q5 AND DBPØNØ1 FALLS TO GROUND. THE DELAY BETWEEN THE CHANGE IN APØNO AND DPBØNØ1 IN THIS DIRECTION IS NOMINALLY 800 MILLISECONDS, BUT WITH CIRCUIT TOLERANCES, IT CAN RANGE BETWEEN 500 MILLISECONDS AND 2 SECONDS. DPBØNØ1 IMMEDIATELY FOLLOWS APØNO WHEN THE LATTER GOES OPEN.

PWRØN1 IS CONTROLLED BY BPØNO IN THE SAME MANNER DESCRIBED FOR DBPØNO1 AND APØNO EXCEPT THAT AN INVERTER, Q5 OF CM2, CAUSES PWRØN1 TO BE LOW WHEN BPØNO IS HIGH AND VICE VERSA.

THE DIODE INPUT FROM BPØNO TO THE DELAY CIRCUIT PROVIDES ISOLATION SO THE SOURCE THAT CONTROLS BPØNO CAN CONTROL ANOTHER CIRCUIT. PWRØN1G PROVIDES A GROUND CONNECTION FOR A LEAD PAIRED WITH THE PWRØN1 SIGNAL LEAD WHEN IT IS SENT TO A REMOTE CIRCUIT.

ALARMS - ELEMENT B

THREE IDENTICAL CIRCUITS DESIGNATED 0, 1 AND 2 ARE PROVIDED TO MONITOR THE FRAME FUSE ALARM AND POWER ALARM BUSES. THE FOLLOWING DESCRIPTION FOR CIRCUIT 0 IS APPLICABLE TO CIRCUITS 1 AND 2. Q1 AND Q4 OF CM1 FORM A FLIP-FLOP TO LATCH THE ALARM SIGNALS. INPUTS +AAG1,+ABG1, AND -AAGO ARE OPEN IN THE ABSENCE OF AN ALARM. THE FLIP-FLOP IS INITIALIZED BY GROUNDING CLRGO, WHICH CUTS OFF Q1 BY DIVERTING ITS BASE CURRENT TO GROUND THROUGH CR2.0. Q2 SATURATES AND HOLDS Q1 OFF WHEN THE CLRO SIGNAL IS REMOVED. IN THIS STATE, Q5 OF CM1 CAN SINK 30 MILLIAMPERES FROM A SOURCE LESS THAN 30 VOLTS. INPUTS +AEG1 AND +ABG1 CONNECT TO ALARM BUSES THAT ARE AT +20 VOLTS IN THE ALARM STATE. EITHER INPUT IN THIS STATE SETS THE FLIP-FLOP CAUSING Q5 OF CM2 TO CUT OFF. INPUT -AAGO CONNECTS TO THE FRAME NEGATIVE FUSE ALARM BUS. IN THE ALARM CONDITION, A NEGATIVE POTENTIAL IS PRESENT ON THIS BUS. Q5 OF CM1 CUTS OFF IN THIS CONDITION AND SETS THE FLIP-FLOP VIA R5 AND R6.

C2.0, CR3.0 AND R12.0 SET THE INPUT LEVEL OF THE FLIP-FLOPS AND PROVIDE FILTERING SO THAT NOISE SPIKES WILL NOT ERRONEOUSLY CHANGE THE STATE OF THE FLIP-FLOP.

TEST - ELEMENT C

FOUR INVERTERS USED IN THE FRAME POWER ALARM TEST ARE PROVIDED. Q4 AND Q5 OF CM3 CONTROL THE NPA AND PAT RELAYS OF THE POWER UNIT. CR4 AND CR5 RAISE THE THRESHOLD OF THEIR RESPECTIVE INPUTS TO PROVIDE NOISE PROTECTION. PAR1 SUPPLIES A 24-VOLT SIGNAL FOR THE POWER ALARM TEST FUNCTION.

C. SYMBOL/LEAD MNEMONICS

DESIGNATION	MEANING
APØNO	"A" POWER ON SIGNAL
+AAO1,+AA11,+AA21 +AB01,+AB11,+AB21	POSITIVE FUSE ALARM INPUTS
-AAOC,-AA10,-AA20	NEGATIVE FUSE ALARM INPUTS
BPLNO	"B" POWER ON SIGNAL
CLR00,CLR10,CLR20	CLEAR ALARM FLIP-FLOP 0,1 AND 2
DBPØNI1	DELAY "B" POWER ON, INPUT SIGNAL
DBPØNØ1	DELAY "B" POWER ON, OUTPUT SIGNAL
LØFF1/LØFF1G	LOCKED OFF LINE SIGNAL/GROUND
NPAIO	NPA INVERTED INPUT SIGNAL
NPAØO	NPA INVERTED OUTPUT SIGNAL
NPA1	NPA NET CONNECTION
ØBRLYO	OPERATE "B" RELAYS
ØNPARO	OPERATE NPA RELAY
ØPATRO	OPERATE PAT RELAY
ØPATR1	OPERATE PAT RELAY
PAR1	POWER ALARM TEST SIGNAL
PØFFO/PØFFOG	POWER OFF SIGNAL/GROUND
PWRØN1/PWRØN1G	POWER ON SIGNAL/GROUND
RNPARIO	RELEASE NPA RELAY