SHEET INDEX

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SYMBOL

BUFFER C
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM.	LOC
CLKITRO	I	015	2A3
ENDTO	I	104	2A0
LDITR1	I	004	2A6
LØADO	I	106	2A7
SDITRO	I	002	2A0
SHIFT1	I	014	2A3
PN4S	I	217,317	2A9
LDDO	Ø	017	2G9
LDD1	Ø	115	2G9
PPEHO	Ø	103	2H3
PPELO	Ø	114	2H7
-17.20V	Ø	018,118	2G9
INFPHO	ØI	101	2H3
INFPLO	ØI	005	2H6
INFOOO	ØI	116	2H6
INFO10	ØI	216	2H6
INFO20	ØI	016	2H5
INFO30	ØI	315	2H5
INFO40	ØI	113	2H4
INFO50	ØI	215	2H4
INFO60	ØI	013	2H4
INFO70	ØI	214	2H4
INFO80	ØI	006	2H2
INFO90	ØI	207	2H2
INF100	ØI	105	2H2
INF110	ØI	305	2H2
INF120	ØI	003	2H1
INF130	ØI	203	2H1
INF140	ØI	102	2H1
INF150	ØI	301	2HØ
+5	P	000,119	2G7
GRD	G	200,319	2G8

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: +5V SUPPLY = 325mA
-48V SUPPLY = 50mA

NOTES:

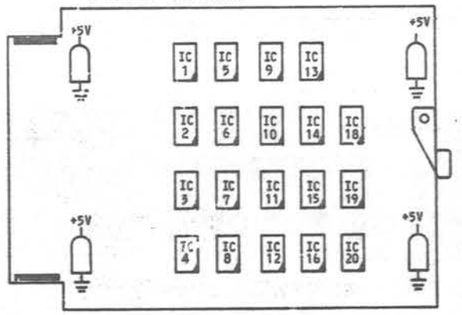
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AE	16	7,8
41BP	16	8
41CA	16	8
41CF	16	7,8
41DA	16	7,8
41EF	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK12
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	DRAWN	APPD
1	—	10-8-74	LRE LRE	RWF MTS RFG
2D1	—	1-5-76	MPPL LRE	JLT LEG RFG

ISSUE 2D1

IN98

JK12 CIRCUIT PACK

BUFFER C
CIRCUIT

(2)

AT&TCO STANDARD

CPS-JK12
3 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PART OF CPS JK12

BUFFER C

0	1	2	3	4	5	6	7	8	9

ENDTO SDITRO CLKITRO SHIFT1 LDITR1 LØAD0 PH48

G1 G3 G5 G6 H3 H7

SDITR1 IC20 41BP A
INF151 IC16 41EF A
INF131 IC16 41EF F
INF141 IC16 41EF G
INF121 IC16 41EF E
INF111 IC11 41EF A
INF091 IC11 41EF F
INF101 IC11 41EF G
INF081 IC11 41EF E
CLKITR1 IC18 41BP E
SHFTO IC18 41BP F
INF071 IC14 41EF A
INF051 IC14 41EF F
INF061 IC14 41EF G
INF041 IC14 41EF E
INF031 IC9 41EF A
INF011 IC9 41EF F
INF021 IC9 41EF G
INF001 IC9 41EF E
LDITRC IC20 41BP F
LDITR1A IC20 41BP E
INFPH1 IC16 41EF B
LØAD1 IC18 41BP G
HIGHA1 IC20 41BP C
INFPL1 IC11 41EF B
R1 681
CR1 CR2 CR3 CR4

ITR1512 IC12 41CF A
ITR1100 IC7 41CF A
ITR0704 IC10 41CF A
ITR0300 IC5 41CF A
MODE CLKP CLKS C NC DS QA QB QC QD DA DB DC DD

ITRPH IC15 41AE A
ITRPL IC15 41AE B
LDD IC13 41AE A

GPH IC8 41DA A
GPL IC6 41DA A
DATA SUM

ENDT1A IC19 41CA C
ENDT1B IC19 41CA A
INF150 IC4 41CA D
INF140 IC4 41CA A
INF130 IC4 41CA C
INF120 IC4 41CA B
INF110 IC3 41CA D
INF100 IC3 41CA A
INF090 IC3 41CA C
INF080 IC3 41CA B
INF070 IC2 41CA D
INF060 IC2 41CA A
INF050 IC2 41CA C
INF040 IC2 41CA B
INF030 IC1 41CA D
INF020 IC1 41CA A
INF010 IC1 41CA C
INF000 IC1 41CA B
INFPHO IC19 41CA D
PPEHO IC20 41BP D
INFPLO IC19 41CA B
PPELO IC18 41BP A

R2 392 +5
R3 392 +5

C1 5 C2 5 C3 5 C4 5
C5 0.1 C6 0.1 C7 0.1 C8 0.1 (C9-C22) 0.1 C23 0.1

LDD1 IC18 41BP D
LDDO IC18 41BP C

INF120 INF130 INF140 INF150 A1
INF080 INF090 INF100 INF110 A2
INFPHO A7
INF040 INF050 INF060 INF070 A4
INF000 INF010 INF020 INF030 A5
INFPLO A8

+5 GRD -17.20V LDD1 LDDO

INF150 INF140 INF130 INF120 INF110 INF100 INF090 INF080 INFPHO PPEHO INF070 INF060 INF050 INF040 INF030 INF020 INF010 INF000 INFPLO PPELO

CPS-JK12

2D1

JK12 CIRCUIT PACK (2)

BELL TELEPHONE LABORATORIES INCORPORATED

CPS-JK12 SHEET 2

PART OF CPS JK12

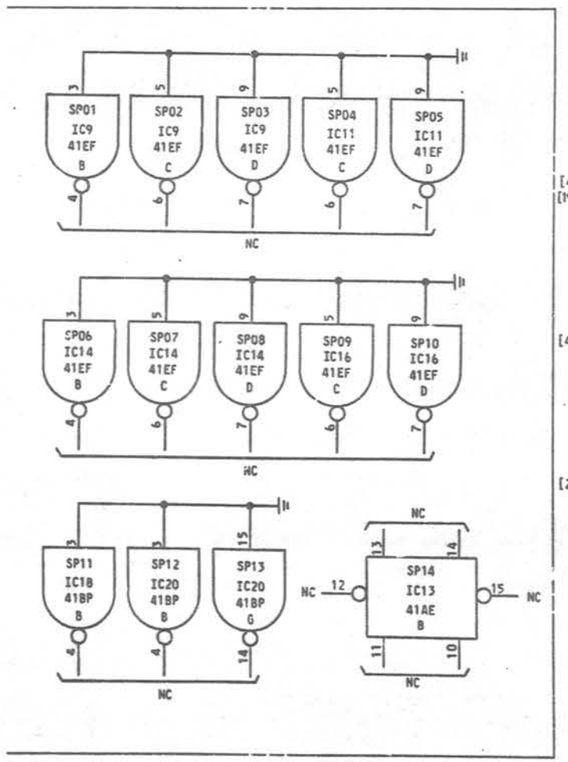
BUFFER C

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA DESIG	SH LOC	IC2 41CA DESIG	SH LOC	IC3 41CA DESIG	SH LOC	IC4 41CA DESIG	SH LOC	IC5 41CF DESIG	SH LOC	IC6 41DA DESIG	SH LOC	IC7 41CF DESIG	SH LOC	IC8 41DA DESIG	SH LOC	IC9 41EF DESIG	SH LOC	IC10 41CF DESIG	SH LOC	IC11 41EF DESIG	SH LOC
A	INF020	2G5	INF060	2G4	INF100	2G2	INF140	2G1	ITR0300	2D6	GPL	2E6	ITR1108	2D2	GPH	2E3	INF031	2B5	ITR0704	2D4	INF111	2B2
B	INF000	2G6	INF040	2G4	INF080	2G2	INF120	2G1									SP01	3E0			INFPL1	2B8
C	INF010	2F6	INF050	2F4	INF090	2F2	INF130	2F1									SP02	3E0			SP04	3E1
D	INF030	2F5	INF070	2F4	INF110	2F2	INF150	2F0									SP03	3E1			SP05	3E1
E																	INF001	2C6			INF081	2C3
F																	INF011	2B6			INF091	2B2
G																	INF021	2C5			INF101	2C2

LOC CODE ELEM ID	IC12 41CF DESIG	SH LOC	IC13 41AE DESIG	SH LOC	IC14 41EF DESIG	SH LOC	IC15 41AE DESIG	SH LOC	IC16 41EF DESIG	SH LOC	IC18 41BP DESIG	SH LOC	IC19 41CA DESIG	SH LOC	IC20 41BP DESIG	SH LOC
A	ITR1512	2D1	LDD	2C9	INF071	2B4	ITRPH	2C7	INF151	2B0	PPELO	2G7	ENDT1B	2G0	SDITR1	2B0
B			SP14	3G1	SP06	3F0	ITRPL	2C8	INFPH1	2B7	SP11	3G0	INFPL0	2G6	SP12	3G0
C					SP07	3F0			SP09	3F1	LDDO	2E9	ENDT1A	2F0	HIGHA1	2B8
D					SP08	3F1			SP10	3F1	LDD1	2E9	INFPH0	2G3	PPEH0	2G3
E					INF041	2C4			INF121	2C1	CLKITR1	2B3			LDITR1A	2C6
F					INF051	2B4			INF131	2B1	SHFT0	2B3			LDITR0	2B6
G					INF061	2C4			INF141	2C1	LØAD1	2B7			SP13	3G1



CAPACITOR

DESIGN	CODE
[4]C1-C4	601A,5
[19]C5-C23	KS-19774 L5,0.1

DIODE

DESIG	CODE
[4]CR1-CR4	4488

RESISTOR

DESIG	CODE
R1	KS-14603 L6,681
[2]R2,R3	KS-20616 L1A,392

CIRCUIT DESCRIPTIØN:

THIS CIRCUIT PACK IS PART ØF THE BUFFER UNIT. IT CØNTAINS A 16-BIT SHIFT REGISTER FØR PARALLEL-TØ-SERIAL AND SERIAL-TØ-PARALLEL CØNVERSIØN. TWØ 8-BIT PARITY TREES ARE USED TØ CHECK AND GENERATE PARITY. THE SERIAL INPUT/ØUTPUT LEADS CØNNECT TØ THE ØFF-LINE SERIAL BUFFER ØN JK13. PARALLEL INPUT AND ØUTPUTS ARE CØNNECTED TØ THE BIDIRECTIØNAL INFØRMATIØN LEADS.

THE REGISTER IS NØRMALLY IN THE PARALLEL LØAD MØDE. THE MØDE INPUT ØF THE 41CFs ARE HELD HIGH BY THE SHFT1 INPUT BEING LØW. THE LØADØ IS HIGH WHENEVER THE BUFFER UNIT IS NØT IN THE LØAD STATE. IN THIS MØDE, THE PARITY F/F ITRPL AND ITRPH ARE HELD IN THE CLEARED STATE. THIS FØRCES THE EVEN INPUTS ØF THE PARITY TREES GPL AND GPH TØ A LØW LEVEL AND THE ØDD INPUTS TØ A HIGH LEVEL. IN THIS PARITY GENERATIØN MØDE, THE ØUTPUTS ØF THE PARITY TREES ARE HIGH FØR AN EVEN NUMBER ØF ØNE INPUTS ØR ARE LØW FØR AN ØDD NUMBER ØF ØNE INPUTS. THE TRUTH TABLE BELOW SHØWS THE ØPERATIØN.

Σ ØF INPUTS	INPUT EVEN	INPUT ØDD	ØDD ØUT
ODD	0	1	0
EVEN	0	1	1

AN UNLØAD ØPERATIØN IS DEFINED BY A 16-BIT DATA TRANSFER FRØM THE ØFF-LINE BUFFER TØ THE 3A CC. THE FØLLØWING SEQUENCE IS PERFØRMED ØN JK12.

THE SERIAL DATA FRØM THE ØFF-LINE BUFFER APPEARS ØN SDITRO. LEAD SHIFT1 IS SET HIGH TØ PLACE THE 16-BIT REGISTER INTØ THE SERIAL SHIFT MØDE. SIXTEEN GRØUND LEVEL PULSES ARE APPLIED TØ LEAD CLKITRO. THE DATA IS SHIFTED INTØ THE REGISTER AT THE TRAILING EDGE ØF THE CLØCK PULSES. LEAD LDDO IS HELD AT A HIGH LEVEL. THIS MEANS THAT ZERØ DATA IS SHIFTED INTØ THE ØFF-LINE BUFFER DURING UNLØAD ØPERATIØNS. THE 16-DATA BITS CØNTAINED IN THE REGISTER ARE FED INTØ THE PARITY TREES. THE PARITY TREES ARE ALLØWED TØ SETTLE. THE SHFT1 LEAD IS SET LØW AGAIN TØ PLACE THE REGISTER INTØ THE PARALLEL LØAD MØDE. THE CØNTENTS ØF THE REGISTER AND THE TWØ PARITY BITS ARE THEN GATED ØNTØ THE INFØRMATIØN BUS LEADS BY SETTING LEAD ENDTO TØ A LØW LEVEL.

CIRCUIT DESCRIPTIØN (CONT):

LØAD

A LØAD ØPERATIØN IS DEFINED BY A 16-BIT DATA TRANSFER FRØM THE CC TØ THE ØFF-LINE BUFFER. THE FØLLØWING SEQUENCE IS PERFØRMED ØN JK12. WHEN THE LØAD STATE IS SET, LEAD LØADO IS AT GRØUND LEVEL REMØVING THE CLEAR INPUT FRØM ITRPH, ITRPL, AND LDD1 F/Fs. SIXTEEN BITS ØF INFØRMATIØN AND THE TWØ PARITY BITS APPEAR IN PARALLEL ØN THE INFØRMATIØN BUS LEADS. A SINGLE HIGH LEVEL PULSE APPEARS ØN LEAD LDITR1. THE STATE ØF THE INFØRMATIØN LEADS IS CLØCKED INTØ THE REGISTER AND THE TWØ PARITY F/F AT THE TRAILING EDGE ØF THE PULSE. IN THE LØAD MØDE, THE TWØ PARITY TREES AND THE TWØ PARITY F/F CHECK FØR PRØPER PARITY ØF THE JUST RECEIVED DATA WØRD. AN ERRØR CØNDITIØN IS INDICATED WHENEVER PPELO ØR PPEHO IS AT GRØUND LEVEL. THE FØLLØWING TRUTH TABLE SHØWS THE CHECKING ØPERATIØN.

Σ ØF INPUTS	PARITY BITS	INPUT ØDD	INPUT EVEN	ØDD ØUTPUT	
EVEN	1	0	1	0	NØ ERRØR
ØDD	0	1	0	0	NØ ERRØR
ØDD	1	0	1	1	ERRØR
EVEN	0	1	0	1	ERRØR

IF AN ERRØR CØNDITIØN EXISTS, NØ SERIAL SHIFTING INTØ THE ØFF-LINE BUFFER TAKES PLACE. IF NØ ERRØR CØNDITIØN EXISTS LEAD SHFT1 IS SET HIGH TØ PLACE THE REGISTER INTØ THE SERIAL SHIFT MØDE. SIXTEEN CLØCK PULSES ØN LEAD CLKITRO SHIFT THE 16-BIT WØRD INTØ THE ØFF-LINE BUFFER VIA LEAD LDDO. F/F LDD1 IS CLØCKED ØN THE LEADING EDGE ØF CLKITRO AND THE REGISTER IS SHIFTED ØN THE TRAILING EDGE. THE LDDO F/F KEEPS THE DATA STEADY ØVER THE TRAILING EDGE ØF THE ØFF-LINE SHIFT PULSE ØN JK13.

ISSUE 2D1

JK12 CIRCUIT PACK

2

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CPS-JK12 SHEET 3

CPS-JK12