

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SYMBOL SUPPORTING INFORMATION NOTES USED-ON TABLE CURRENT DRAIN RECORD OF CHANGES	1	4
CIRCUIT SCHEMATIC	2	4
COMPONENT LIST	3	3
CIRCUIT DESCRIPTION	4	3
	5	3
	6	3
	7	3

SYMBOL  
TAPE UNIT CONTROLLER,  
BOARD B

TERM. MOD.	FUNCT	TERM.	LOC
CLK011	I	114	3A0
CLRCRC0	I	206	2A2
ENRD1	I	013	3A1
ERENIN1	I	014	2A9
INITB0	I	210	2A4
MAINT0	I	305	7A3
MAINT1	I	207	2A2
MDD0	I	015	3A8
RDADJ1	I	115	3A0
RDCLK0	I	218	3A7
RDCLC0	I	306	2A2
RDDATA0	I	318	3A2
SCRCC0	I	103	2A3
ST0PP0	I	008	2A1
WDATA1	I	116	3A2
W011	I	316	3A1
CRCER0	Ø	113	2H7
ERENOUT1	Ø	003	3H6
FILENB1	Ø	201	3H8
RDCLKP0	Ø	301	3H7
RD0JT1	Ø	002	2H5
SHCRC1	Ø	102	3H5
ERDET1	ØI	112	2H6
HILEV1	ØI	300	3A3
MDDNP1	ØI	202	3H6
RDC0TA	ØI	107	2H0
LDATA1	ØI	118	3H6
RSP1	ØI	017	3H4
RSTPN1	ØI	108	3H6
RSTP0	ØI	009	3H4
+5	P	000	3H0
+5	P	119	3H0
GRD	G	200	3H2
GRD	G	319	3H2

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

- GROUND RETURN
- UNLESS OTHERWISE SPECIFIED:  
RESISTANCE VALUES ARE IN OHMS  
CAPACITANCE VALUES ARE IN MICROFARADS  
VALUES PRECEDED BY THE SYMBOL + (PLUS)  
OR - (MINUS) ARE IN VOLTS
- BATTERY AND GROUND TERMINALS FOR  
INTEGRATED CIRCUITS

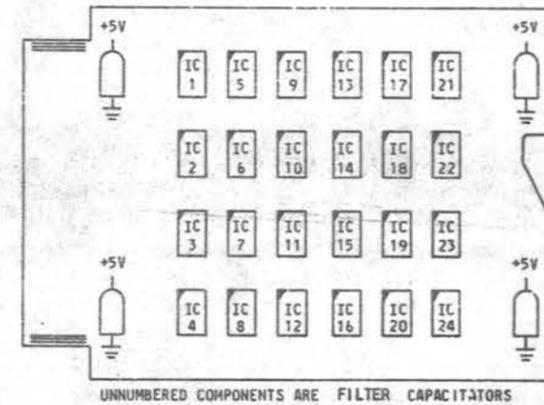
IC CODE	BAT. TERM.	GRD. TERM.
41AA	16	8
41AE	16	7,8
41BL	16	8
41BP	14	8
41BR	16	7,8
41CC	16	8
41CF	16	7,8
41CJ	16	8
41T	16	8
41U	16	8
41W	16	8

- BATTERY AND GROUND TERMINALS FOR  
THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

- HORIZONTAL MOUNTING CENTERS AT  
0.50 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE:  
(COMPONENT SIDE SHOWN).



SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK17
CONNECTOR ON FRAME	947A OR 947C
ACCEPTABLE SERIES	2-3,3

CURRENT DRAIN: 350ma

SHEET INDEX NOTES

- WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
- THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
- THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
- SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
- THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE  
4B1

JK17 CIRCUIT PACK  
CARTRIDGE TAPE TRANSPORT, BOARD B  
CONTROLLER  
CIRCUIT

1N98

2

AT&TCO  
STANDARD

CPS-JK17  
7 SHEETS

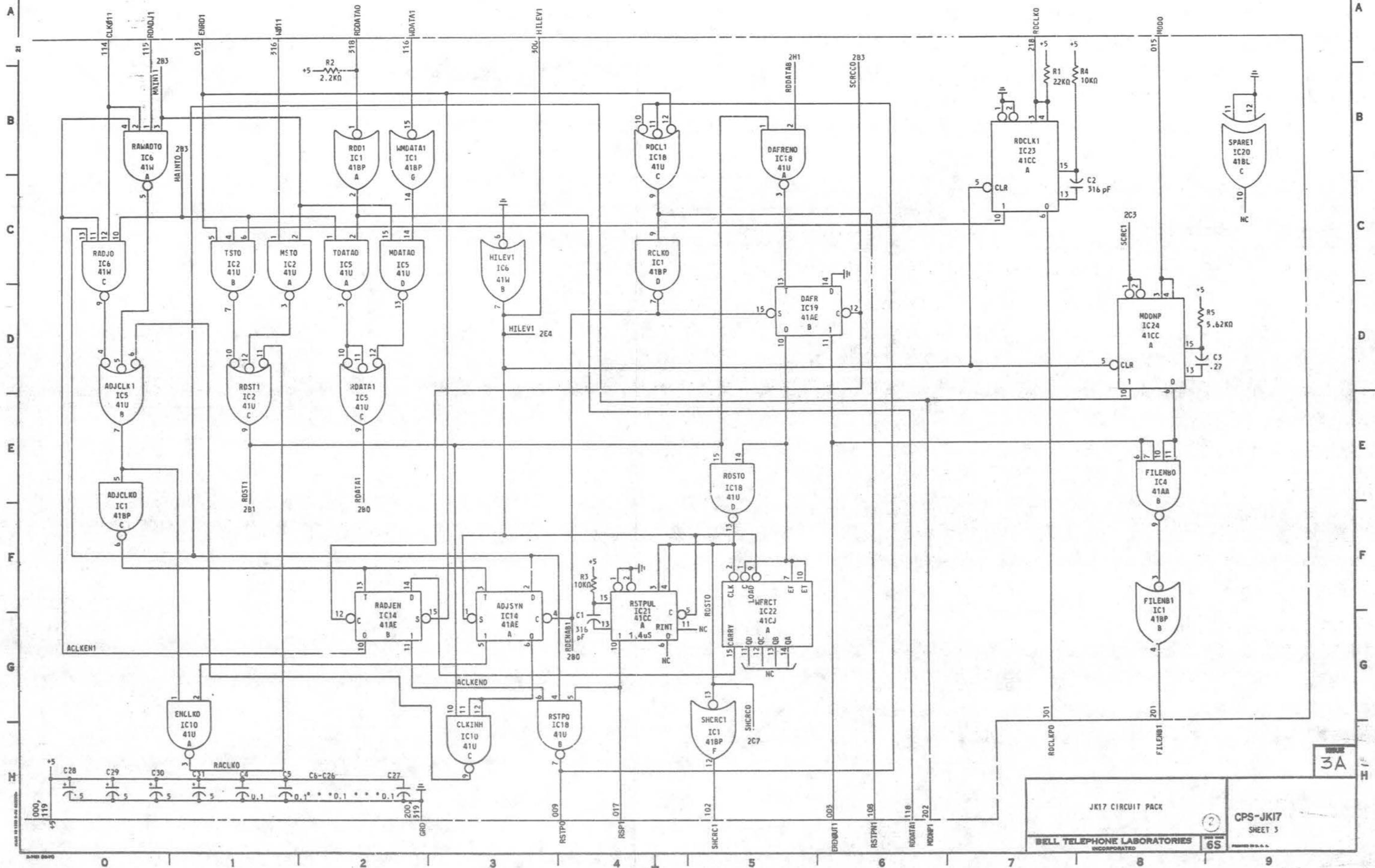
BELL TELEPHONE LABORATORIES  
INCORPORATED

6S

PRINTED IN U.S.A.



CARTRIDGE TAPE TRANSPORT  
CONTROLLER, BOARD B



COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41BP		IC2 41U		IC3 41BR		IC4 41AA		IC5 41U		IC6 41H		IC7 41BR		IC8 41BR		IC9 41T		IC10 41U		IC11 41T		IC12 41T	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	RDD1	3B2	HSTO	3C1	CRLRCL1	2B2	ERDET1	2G7	TDATA0	3C2	RAWADT0	3B0	ER1B0	2F5	ER1F0	2F7	PSTREG1B	2E0	ENCLK0	3H1	CRCRGC	2C8	CRCRGC	2C6
B	FILENB1	3F8	TSTO	3C1	CLCRC1	2B2	FILENB0	3E8	ADJCLK1	3D0	HILEV1	3C3	ER1H0	2F8	ER1D0	2F6			INCR1	2C3				
C	ADJCLK0	3E0	RDST1	3D1	SRRC1	2B3			RDATA1	3D2	RADJO	3C0	ER1G0	2F8	ER1C0	2F6			CLKINH0	3H3				
D	RCLK0	3C4	CRCERO	2H7	CRCELO	2C2			MDATA0	3C2	INCRCC	2C3	ER1A0	2E4	ER1E0	2F7			CRC01	2D2				
E	RDDAT0	2G1																						
F	SHCRC1																							
G	WMDATA1	3B2																						
H																								

LOC CODE ELEM ID	IC13 41T		IC14 41AE		IC15 41U		IC16 41CF		IC17 41T		IC18 41U		IC19 41AE		IC20 41BL		IC21 41CC		IC22 41CJ		IC23 41CC		IC24 41CC	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	PSTREG1A	2D0	ADJSYN	3F3	TDOUTO	2E2	CRCRGA	2C5	#FLREG	2C0	DAFRENO	3B5	SHEN	2D3	CRC3D1	2E5	RSTPUL	3F4	WFRCT	3G5	RDCLK1	3B7	MDDNP	3D8
B			RADJEN	3F2	DOUT1	2F3					RSTPO	3G3	DAFR	3D5	CRC1D1	2B1								
C					CRCDENO	2C2					RDCL1	3B4			SPARE1	3B9								
D					CDOUT0	2E3					RDSTO	3E5			CRC15D1	2B5								
E																								
F																								
G																								
H																								

CAPACITOR

DESIG	CODE
C1, C2	KS-20813 L2, 116pF
C3	YS-1977A L5, .27
[24]C4-C27	KS-1977A L5, 0.1
[4]C28-C31	601A, 5

RESISTOR

DESIG	CODE
R1, R2	KS-20616 L1A, 2.2KΩ
R3, R4	KS-20616 L1A, 10KΩ
R5	KS-20616 L1A, 5.62KΩ

3A

JK17 CIRCUIT PACK		2	CPS-JK17 SHEET 4
BELL TELEPHONE LABORATORIES INCORPORATED			

MADE IN THE U.S.A.

## CIRCUIT DESCRIPTION

## A. FUNCTIONAL DESCRIPTION

THIS CIRCUIT PACK IS ONE OF THE FOUR THAT MAKE UP THE CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC). IT CONTAINS THE READ CIRCUIT WHICH INCLUDES PREAMBLE/POSTAMBLE STRIPPING CIRCUITRY, WORD FRAMING CIRCUITRY, CYCLIC REDUNDANCY CHECK (CRC) CIRCUITRY, AND THE BUFFER FILL ENABLE CIRCUITRY. IT PERFORMS THE FUNCTION OF SHIFTING THE CONTENTS OF THE CRC REGISTER TO THE BUFFER CIRCUITS.

THE READ CIRCUIT CAN OPERATE IN EITHER OF TWO MODES, NORMAL DATA TRANSFER OR MAINTENANCE DATA TRANSFER. IN THE NORMAL MODE DATA IS TRANSFERRED FROM THE CARTRIDGE TAPE TRANSPORT (CTT). IN THE MAINTENANCE MODE, THE READ AND WRITE CIRCUITS CAN BE EXERCISED WITHOUT OPERATING THE CTT. DATA WILL ENTER DIRECTLY FROM THE OUTPUT OF THE WRITE CIRCUIT LOCATED ON JK18 (SEE FIG. 1). THE DATA AND ITS ASSOCIATED CLOCK ENTERS THE READ CIRCUIT THROUGH THE DATA SELECTOR AND THE CLOCK SELECTOR CIRCUITS, RESPECTIVELY. THE DATA CLOCKING CONTROL CIRCUIT WHICH RECEIVES CLOCK PULSES FROM BOTH THE CLOCK SELECTOR CIRCUIT AND A FREE RUNNING CLOCK (OPERATING AT THE NORMAL DATA FREQUENCY) HAS TWO BASIC CLOCK OUTPUTS. THE OUTPUT LABELED SHIFT PULSES BEGINS CLOCKING THE 24-BIT DATA REGISTER AND THE DATA FRAME CIRCUITRY (THE DATA FRAME CIRCUITRY INCLUDES LOGIC FOR STRIPPING THE PREAMBLE AND POSTAMBLE) AS DATA INITIALLY ENTERS THE READ CIRCUIT. AS THE PREAMBLE (FIFTEEN ZEROS FOLLOWED BY A SINGLE ONE) IS SHIFTED THROUGH THE 24-BIT REGISTER, THE OUTPUT OF THE DATA FRAME CIRCUIT INHIBITS CLOCK PULSES TO BOTH THE CRC CHECK CIRCUIT AND THE BUFFER CIRCUITS (THE BUFFERS ARE CLOCKED BY THE LEAD LABELED CLOCK OUT). BY MONITORING THE OUTPUT OF THE 24-BIT REGISTER, THE DATA FRAME CIRCUIT DETECTS THE FIRST ONE (LAST BIT OF THE PREAMBLE) AND THEN ENABLES THE CRC CHECK CIRCUIT AND THE CLOCK OUT LEAD. THIS ALLOWS THE FOLLOWING DATA TO BE CLOCKED INTO THE CRC CHECK CIRCUIT AND TO THE BUFFER CIRCUITS. THIS IN EFFECT, STRIPS THE PREAMBLE FROM THE DATA BY SIMPLY IGNORING IT AS IT FALLS OUT THE END OF THE 24-BIT REGISTER.

THE OUTPUT DATA WHICH GOES TO THE BUFFER CIRCUIT PROPAGATES FROM THE 24-BIT REGISTER THROUGH THE DATA OUT SELECTOR CIRCUIT. THE DATA OUT SELECTOR NORMALLY ALLOWS DATA FROM THE 24-BIT REGISTER TO PROPAGATE OVER THE DATA OUT LEAD TO THE BUFFER CIRCUITS. WHEN IT IS DESIRED TO EXAMINE THE CONTENTS OF THE CRC REGISTER, THE NORMAL INPUT TO THE SELECTOR IS INHIBITED AND THE DATA FROM THE CRC REGISTER IS CLOCKED THROUGH THE SELECTOR TO THE BUFFER CIRCUITS. THE CTTC MUST BE IN THE MAINTENANCE MODE TO SHIFT THE CONTENTS OF THE CRC REGISTER TO THE BUFFER CIRCUIT.

NOTICE THE OUTPUT DATA IS DELAYED BY 24 BITS FROM THE INPUT DATA. IN NORMAL OPERATION THE CTT MAY PROVIDE ONE OR TWO ERRONEOUS DATA CLOCK PULSES FOLLOWING THE END OF DATA READ FROM THE TAPE. THIS MEANS THAT THE 24-BIT REGISTER WILL CONTAIN UP TO EIGHT DATA BITS, THE POSTAMBLE AND POSSIBLY ONE OR TWO ERRONEOUS BITS AT THE END OF THE CLOCK STREAM FROM THE CTT. THE DATA FRAME CIRCUITRY CONTAINS A 4-BIT COUNTER WHICH RECYCLES ITSELF EVERY 16 CLOCK PULSES BEGINNING AT THE FIRST DATA BIT AFTER THE PREAMBLE. THIS COUNTER WILL BE AT A COUNT LESS THAN 16 AT THE END OF THE DATA STREAM. THE DIFFERENCE BETWEEN THE DATA-FRAME COUNTER AND 16 IS THE NUMBER OF DATA BITS LEFT IN THE 24-BIT REGISTER. ASSUMING THAT DATA WAS BEING READ FROM TAPE, THE DATA-DETECT LEAD WILL GO TO A FALSE STATE AT THE END OF THE DATA STREAM (IT IS FORCED TO A FALSE STATE AT THIS POINT IF THE INPUT DATA IS FROM THE WRITE CIRCUITS). THE DATA-DETECT LEAD IS TRUE WHEN THE READ HEAD OF THE CTT IS CROSSING DATA AND FALSE WHEN IT IS OVER AN INTERRECORD GAP. THE COMBINATION OF DATA DETECT BEING FALSE, THE DATA FRAME CIRCUIT BEING ENABLED, AND THE COUNTER NOT EQUAL TO 16 (READ ADJUST MODE), ENABLES THE FREE RUNNING CLOCK TO PROPAGATE THROUGH THE DATA CLOCKING CONTROL CIRCUIT UNTIL THE DATA FRAME COUNTER REACHES A COUNT OF 16, AT WHICH TIME ALL CLOCKS ARE INHIBITED. THE POSTAMBLE WILL REMAIN IN THE 24-BIT REGISTER EFFECTIVELY STRIPPING IT FROM THE DATA AND THE BUFFER FILL LEAD (BUF FILL) IS ENABLED. THE BUFFER FILL LEAD ALLOWS CIRCUITRY LOCATED ON JK19 TO REQUEST A FILL OPERATION IN THE BUFFER CIRCUITS IF NECESSARY. COMPLETION OF THE READ ADJUST SEQUENCE ALSO ENABLES THE CRC ERROR LEAD WHICH WILL BE TRUE IF THE CONTENTS OF THE CRC REGISTER IS NOT ALL ZEROS.

IN THE MAINTENANCE MODE THE CONTENTS OF THE CRC REGISTER MAY BE SHIFTED TO THE BUFFER CIRCUIT. THE INITIALIZATION OF THIS SEQUENCE ENABLES THE DATA FRAME CIRCUITRY AND SELECTS THE CRC INPUT AT THE DATA OUT SELECTOR CIRCUIT MAINTAINING A FALSE STATE ON THE DATA-DETECT LEAD. THIS EFFECTIVELY PUTS THE READ CIRCUIT IN THE READ ADJUST MODE WHICH ALLOWS EXACTLY 16 CLOCK PULSES ENTERING FROM THE FREE RUNNING CLOCK INPUT TO PROPAGATE THROUGH THE READ CIRCUIT.

AS IN A NORMAL READ OPERATION, WHEN THE DATA FRAME COUNTER REACHES A COUNT OF 16, ALL OPERATIONS WILL BE TERMINATED, LEAVING THE BUF FILL LEAD ENABLED.

## B. DETAILED DESCRIPTION

THE READ DATA CLOCK LEAD (RDCLKO) WHICH COMES FROM THE CTT, FEEDS THE  $\mu$ S MONOPULSER RDLK1. THIS MONOPULSER PROVIDES A DELAY T. ENSURE THAT THE DATA LEAD (RDATO) FROM THE CTT IS STABLE BEFORE CLOCKING INFORMATION INTO THE OVERFLOW REGISTER #FLREG. THE ZERO OUTPUT OF RDLK1 SERVES AS A TEST POINT WHICH IS BROUGHT OUT TO A CONNECTOR TERMINAL. THE ONE OUTPUT OF RDLK1 FEEDS THE NAND GATE TSTO WHICH IS ENABLED BY BOTH MAINTO AND ENRD1. MAINTO IS AN OUTPUT OF THE MAINTENANCE FLIP-FLOP ON JK16. IT IS AT A HIGH LEVEL WHEN THE CTTC IS NOT IN A MAINTENANCE MODE. ENRD1 IS AN OUTPUT OF THE READ FLIP-FLOP ON JK16. IT IS AT A HIGH LEVEL WHENEVER THE CTTC IS HANDLING DATA (READ, WRITE AND CRC SHIFT OPERATIONS). TSTO FEEDS ROST1 WHICH CLOCKS THE DATA THROUGH THE THREE 8-BIT REGISTERS #FLREG, PSTREG1A, AND PSTREG1B. THE DATA IS FED INTO #FLREG BY RDATA1 WHICH PASSES DATA FROM EITHER THE CTT OR FROM THE WRITE CIRCUIT (JK18) DEPENDING UPON THE ENABLING OF EITHER WDATA OR MDATA BY MAINTO OR MAINT1, RESPECTIVELY. MAINT1 IS THE SECOND OUTPUT OF THE MAINTENANCE FLIP-FLOP ON JK16.

IN THE MAINTENANCE MODE THE READ AND WRITE CIRCUITS CAN BE EXERCISED WITHOUT OPERATING THE CTT. MAINTO WILL BE AT A LOW LEVEL AND MAINT1 WILL BE AT A HIGH LEVEL. THIS ENABLES A DATA PATH FROM WDATA1 AND A CLOCK PATH FROM W#11 THROUGH M#10. THIS STATE DISABLES THE DATA AND CLOCK PATHS FROM THE CTT. WDATA1 AND W#11 ARE DATA AND ASSOCIATED CLOCK LEADS FROM THE OUTPUT OF THE WRITE CIRCUIT.

INPUT DATA WHETHER CLOCKED FROM THE WRITE CIRCUIT OR FROM THE CTT IS CLOCKED THROUGH THE THREE REGISTERS #FLREG, PSTREG1A, AND PSTREG1B. THESE ARE 41T 8-BIT SHIFT REGISTERS WHICH MAKE UP A 24-BIT SERIAL SHIFT REGISTER. THE OUTPUT OF THIS REGISTER RDATA1B IS AND'ed WITH ROST1 BY DAFRENO. DAFRENO WILL PROVIDE A TOGGLE PULSE WHICH CLEARS DAFR ON THE FIRST READ-CLOCK PULSE AFTER RDATA1B GOES TO THE ONE STATE. THE FIRST WORD OF A DATA BLOCK IS THE PREAMBLE (15 "ZEROS" FOLLOWED BY A SINGLE "ONE"). THEREFORE, THE CLEARING OF DAFR IMPLIES THAT THE FIRST DATA BIT FOLLOWING THE PREAMBLE IS AT THE OUTPUT OF THE 24-BIT REGISTER. WHEN THE CTTC IS IN THE MAINTENANCE MODE, THE FIRST WORD FROM THE WRITE CIRCUIT IS ALSO THE PREAMBLE. ALL DATA-CLOCK PULSES WHICH FEED EITHER THE CRC CIRCUIT OR THE BUFFER CIRCUITS MUST PROPAGATE THROUGH THE NAND GATE, ROSTO. ROSTO HAD BEEN INHIBITED BY THE SET STATE ON DAFR UNTIL AFTER THE LAST BIT OF THE PREAMBLE. SINCE NO CLOCK PULSES ARE PERMITTED THROUGH ROSTO, UNTIL AFTER THE PREAMBLE HAS BEEN SHIFTED FROM THE 24-BIT REGISTER, THE PREAMBLE IS STRIPPED FROM THE DATA STREAM. THE CLEARED STATE OF DAFR ENABLES ROSTO. THE OUTPUT OF ROSTO PROVIDES DATA CLOCK PULSES TO THE 16-STATE WORD FRAMING COUNTER (WFRCT), THE READ SHIFT PULSE MONOPULSER (RSTPUL), THE CLOCK INPUTS TO THE CRC REGISTER, AND SHCRC1.

IN THE NORMAL DATA TRANSMISSION MODE, DATA WHICH APPEARS AT THE Q8 OUTPUT OF PSTREG1B PROPAGATES THROUGH RDATA1, TDATA1, AND DOUT1 TO THE D CELL OF CCRGCA. IT IS LOADED ONTO THIS FLIP-FLOP BY SHCRC0. THE OUTPUT OF THIS CELL (RDATA1) IS THE DATA OUTPUT SIGNAL FROM THE CTTC'S READ CIRCUITRY. SHCRC0 ALSO CLOCKS THE Q8 OUTPUT OF PSTREG1B THROUGH THE CRC ERROR DETECTION CIRCUIT.

AS DATA IS BEING SHIFTED THROUGH THE CRC CIRCUITS AND THE OUTPUT FLIP-FLOP, ROSTO IS ALSO PROVIDING CLOCK PULSES TO THE  $\mu$ S MONOPULSER, RSTPUL AND THE 16-STATE WORD FRAME COUNTER, WFRCT. THE OUTPUT OF RSTPUL (RSP1) SERVES AS THE READ-DATA CLOCK TO THE BUFFER CIRCUIT. DATA IS CLOCKED INTO THE BUFFERS ON THE TRAILING EDGE OF RSP1. THIS ALLOWS DATA FROM PSTREG1B TO BE SETTLED IN THE D CELL OF CCRG1 BEFORE THE BUFFER IS CLEARED.

WHEN THE READ CIRCUIT IS IN THE IDLE STATE (NO DATA IS BEING TRANSFERRED THROUGH IT), ENRD1 THE ONE OUTPUT OF THE READ FLIP-FLOP ON JK16 IS AT A LOW LEVEL. THIS LOW LEVEL MAINTAINS A SET STATE ON THE D-TYPE FLIP-FLOP RADJEN AND BY DRIVING THE OUTPUT OF RDLK1 HIGH, IT MAINTAINS A LOW LEVEL AT THE OUTPUT OF RDLK0. THE LOW LEVEL AT THE OUTPUT OF RDLK0 RETAINS A CLEARED STATE ON THE OUTPUT OF THE D-TYPE FLIP-FLOP ADJSYN AND A SET STATE AT THE OUTPUT OF DAFR. THE LOW LEVEL AT THE ZERO OUTPUT OF DAFR HOLDS WFRCT IN ITS CLEARED OR INITIAL STATE. THIS ENSURES THAT THE COUNTER WILL BEGIN COUNTING AT THE ZERO STATE ON THE FIRST CLOCK PULSE AFTER THE PREAMBLE HAS FALLEN FROM PSTREG1B. AS A READ OPERATION BEGINS THE CLEARED STATE OF ADJSYN ENABLES CLKINH AND DISABLES ENCLKO. THE ENABLED CLKINH ALLOWS READ-CLOCK PULSES FROM ROST1 TO PROPAGATE THROUGH ADJCLK1 TO THE INPUT OF ENCLKO WHICH IS DISABLED, AND TO ADJCLK0. THE

OUTPUT OF ADJCLK0 PROVIDES CLOCK PULSES TO RADJEN AND ADJSYN. SINCE THE CARRY OUTPUT OF WFRCT FEEDS THE DATA INPUT TO RADJEN, EACH CLOCK PULSE APPEARING AT RADJEN WILL ATTEMPT TO CLEAR IT, EXCEPT WHEN THE CARRY OUTPUT OF WFRCT IS HIGH. A READ-CLOCK PULSE OCCURRING WHILE THE CARRY OUTPUT OF WFRCT IS IN THE HIGH STATE WILL SET RADJEN. THIS OCCURS EVERY SIXTEENTH CLOCK PULSE AFTER THE PREAMBLE HAS BEEN STRIPPED. WHEN RADJEN IS IN ITS CLEARED STATE THE "ZERO" OUTPUT ACKEN1 WILL ENABLE RADJO IF THE "ONE" OUTPUT OF THE MONOPULSER MDDNP IS IN A HIGH STATE. WHEN DATA IS BEING TRANSMITTED FROM THE CTT THE "ONE" OUTPUT OF MDDNP WILL BE AT A LOW LEVEL, MAINTAINING A LOW LEVEL AT THE DATA INPUT TO ADJSYN. THIS LOW INPUT WILL RETAIN THE CLEARED OUTPUT ON ADJSYN AS IT IS CLOCKED BY ADJCLK0. THE "ONE" OUTPUT OF MDDNP IS TRIGGERED TO A LOW LEVEL BY A LOW-TO-HIGH TRANSITION ON MDDO, WHICH ONLY OCCURS AT THE TRAILING EDGE OF A DATA STREAM FROM THE CTT. WHEN ALL DATA OF A GIVEN BLOCK HAS BEEN CLOCKED FROM THE CTT AND THE READ HEAD IS OVER AN INTERBLOCK GAP (IBG), MDDO GOES HIGH. THIS CAUSES THE "ONE" OUTPUT OF MDDNP TO GO TO A HIGH STATE FOR APPROXIMATELY 400 $\mu$ s. THE DATA BEING SHIFTED TO THE BUFFER CIRCUIT IS DELAYED BY 24 BITS BY THE 24-BIT DATA DELAY REGISTER. WFRCT SHOULD BE AT A COUNT OF EIGHT WHEN THE LAST INFORMATION BIT IS CLOCKED FROM THE CTT. (THIS COUNT MAY BE NINE OR TEN, DEPENDING UPON RINGING OF THE PREAMPLIFIERS OF THE CTT. THE DIFFERENCE BETWEEN THE COUNTER OUTPUT AND 16 IS THE NUMBER OF DATA BITS LEFT IN THE REGISTER.) SINCE WFRCT IS NOT AT A FULL COUNT OF 16, PART OF THE LAST DATA WORD AND THE POSTAMBLE ARE STORED IN THE 24-BIT REGISTER AND RADJEN IS LEFT IN THE CLEARED STATE AFTER THE LAST DATA-CLOCK PULSE. THE READ HEAD OF THE CTT HAS NOW MOVED TO AN IBG. MDDO GOES HIGH CAUSING THE "ONE" OUTPUT OF MDDNP TO GO TO A HIGH STATE ENABLING RADJO. THE FREE-RUNNING CLOCK PULSES ON CLK#11 (48KHZ) WILL BEGIN PROPAGATING THROUGH RADJO. THE FIRST CLOCK PULSE WILL SET ADJSYN WHICH HAD BEEN IN THE CLEAR STATE PREVIOUSLY. SETTING ADJSYN ENABLES ENCLKO AND DISABLES CLKINH SO THAT CLOCK PULSES, WHICH APPEAR ON CLK#11, CAN PROPAGATE THROUGH ROST1. DISABLES CLKINH PREVENTS ITS LOW OUTPUT (OUTPUT FROM THE FIRST CLOCK PULSE ON CLK#11) FROM INHIBITING ADJCLK1. THE CLOCK INPUT TO ROST1 WILL CONTINUE UNTIL WFRCT REACHES A FULL COUNT OF 16. AT THE SIXTEENTH CLOCK PULSE THE CARRY OUTPUT OF WFRCT IS HIGH AND RADJEN IS CLOCKED TO THE SET STATE. ACKEN1 IS NOW LOW DISABLES THE CLOCK INPUT AT RADJO. AT THIS POINT THE REMAINING DATA WHICH WAS STORED IN THE 24-BIT REGISTER HAS BEEN CLOCKED INTO THE BUFFER CIRCUIT AND INTO THE CRC CIRCUIT. THE POSTAMBLE WILL REMAIN IN THE LAST 16 CELLS OF THE REGISTER, EFFECTIVELY STRIPPING IT FROM THE DATA. THE READ-ADJUST OPERATION DESCRIBED ABOVE REQUIRES A MAXIMUM OF NINE CLOCK PULSES FROM THE CLK#11 INPUT, LESS THAN 200 $\mu$ s. THIS MEANS THAT THE "ONE" OUTPUT OF MDDNP REMAINS HIGH AFTER THE LAST CLOCK PULSE FROM ROSTO. THE LAST CLOCK PULSE HAD ALSO SET RADJEN LEAVING ACKEN0 HIGH. THE COMBINATION OF THESE TWO HIGH LEVELS ENABLES RSTPO ALLOWING THE LAST CLOCK PULSE APPEARING ON RSP1 TO PROPAGATE THROUGH RDLK1 AND RDLK0 TO SET THE FLIP-FLOP DAFR, ENDING THE READ CYCLE. (NOTE CLOCK PULSES ON RSP1 ARE INITIATED AT THE TRAILING EDGE OF CLOCK PULSES FROM ROSTO.) WHEN MDDNP TIMES OUT AND RETURNS TO ITS STABLE STATE, FILEN1 GOES TO A HIGH STATE WHICH WILL ENABLE THE FILL SIGNAL ON JK18. THE HIGH-LEVEL ON THE "ONE" OUTPUT OF DAFR (EREN#1) APPEARS ON ERENIN1 ENABLING CCRERO. ERENUT1 AND ERENIN1 ARE CONNECTED ON THE BACKPLANE. A HIGH-LEVEL AT THE OUTPUT OF ERDET1 WILL DRIVE THE ENABLED OUTPUT OF CCRERO TO A LOW LEVEL, INDICATING THAT THERE WAS A CRC ERROR IN THE DATA THAT HAS BEEN READ. THE OUTPUT OF ERDET1 IS HIGH WHENEVER THE CONTENTS OF THE CRC REGISTER IS NOT AN ALL ZEROS WORD.

IN THE MAINTENANCE STATE THE READ CIRCUIT OPERATES IN A VERY SIMILAR MANNER. MAINTO WILL BE LOW AND MAINT1 WILL BE HIGH. DATA THAT COMES DIRECTLY FROM THE WRITE CIRCUIT (JK18) WILL APPEAR ON WDATA1. THE CLOCK WILL APPEAR ON W#11 (ALSO FROM JK18). AT THE END OF THE INPUT DATA RADJEN1 WILL BE DRIVEN HIGH BY THE WRITE CIRCUIT. THIS ALLOWS THE READ ADJUST CLOCK CLK#11 TO PROPAGATE THROUGH RAMADJO.

THE CRC CIRCUIT MONITORS ALL DATA READ INTO THE READ CIRCUIT. WHEN THE CTTC IS IN THE NORMAL OPERATING MODE, THE CRC REGISTER IS CLEARED BY A PULSE ON THE RDCLK (OUTPUT FROM JK16) INPUT LEAD AT THE BEGINNING OF ANY DATA TRANSFER OPERATION. WHEN THE CTTC IS IN THE MAINTENANCE MODE THE CRC REGISTER IS CLEARED BY ISSUING A CLEAR CRC ORDER WHICH APPEARS AS A PULSE ON THE CLRRC00 INPUT LEAD. CLRRC00 IS AN OUTPUT FROM THE CTTC'S COMMAND DECODER LOCATED ON JK16. THE CRC REGISTER IS MADE UP OF: CELLS A, B, AND C OF CCRGCA, ALL OF CCRG1B AND CELLS 1, 2, 3, 4, AND 5 OF CCRG1C. CCRGCA IS OPERATED IN A PARALLEL MODE WHERE THE OTHER TWO REGISTERS ARE OPERATED IN THE SERIAL MODE. THE 16 BITS OF THE CRC REGISTER ARE ORGANIZED IN FOLLOWING MANNER: BITS 0, 1, AND 15 ARE CELLS A, B, AND C OF CCRGCA, RESPECTIVELY. BITS 2, 3, 4, 5, 6, 7, 8, AND 9 ARE CELLS 1, 2, 3, 4, 5, 6, 7, AND 8 OF CCRG1B, RESPECTIVELY.

BITS 10, 11, 12, 13, AND 14 ARE CELLS 1, 2, 3, 4, AND 5 OF CCRG1C, RESPECTIVELY. CCR101 PERFORMS AN EXCLUSIVE OR FUNCTION ON RDATA1B (INPUT DATA TO THE CRC CIRCUIT) AND BIT 15 OF THE CHECK REGISTER. THE OUTPUT OF CCR101 IS ENABLED THROUGH GATES CCRDNO AND CCRD1 BY SHEN. THE OUTPUT OF CCRD1 FEEDS BIT 0 OF THE CHECK REGISTER, AND IS EXCLUSIVELY AND'ed WITH BIT 1 BY CCR301 TO FEED BIT 3, AND BIT 14 BY CR1501 WHICH FEEDS BIT 15 OF THE CHECK REGISTER. THIS CIRCUIT IS A CYCLIC-REDUNDANCY CHECKER FOR THE GENERATOR POLYNOMIAL  $1 + x^2 + x^{15} + x^{16}$ . ER1A0, ER1B0, ER1C0, ER1D0, ER1E0, ER1F0, ER1G0, ER1H0, AND ERDET1 OR THE 16-OUTPUT BITS OF THE REGISTER TOGETHER AND INDICATE IF ANY OF THE 16 CELLS CONTAIN A "ONE." (THIS INDICATES AN ERROR CONDITION AFTER AN ENTIRE BLOCK OF DATA HAS PASSED THROUGH THE CIRCUIT.) THE OUTPUT OF ERDET1 IS ENABLED THROUGH CCRERO BY ERENIN1. ERENIN1 IS HIGH WHENEVER THE CTTC IS NOT IN A READ OR READ-AFTER-WRITE MODE (THE READ CIRCUIT IS NOT TRANSFERRING DATA).

IN THE MAINTENANCE MODE THE CTTC NOT ONLY HAS THE CAPABILITY OF EXERCISING THE READ AND WRITE CIRCUITS WITHOUT UTILIZING THE CTT, BUT ALSO THE CAPABILITY OF SHIFTING THE CONTENTS OF THE CRC REGISTER TO THE BUFFER CIRCUITS. WITH THE CTTC IN THE MAINTENANCE MODE, IF A COMMAND TO SHIFT THE CRC REGISTER CONTENTS IS ISSUED, A PULSE WILL APPEAR ON THE INPUT SCRCO. SCRCO IS AN OUTPUT FROM THE CTTC'S COMMAND DECODER LOCATED ON JK16. THIS PULSE WILL IMMEDIATELY CLEAR DAFR AND RADJEN. IT CREATES A PULSE AT THE OUTPUT OF SCRC1 WHICH TOGGLES SHEN TO A CLEARED STATE AND TRIGGERS MDDNP. CLEARING DAFR ENABLES ROSTO AND REMOVES THE CLEAR SIGNAL FROM WFRCT, ALLOWING IT TO COUNT FROM AN INITIAL STATE OF ZERO. THE WRITE CIRCUIT WHICH IS IN AN IDLE STATE, MAINTAINS A HIGH LEVEL ON RDATA1 AND THE CLEARED STATE OF RADJEN MAINTAINS A HIGH LEVEL ON ACKEN1, ENABLING THE FREE RUNNING CLOCK CLK#11 THROUGH RAMADTO. THE FIRST CLOCK PULSE FROM RAMADTO WILL PROPAGATE THROUGH ADJCLK1 AND ADJCLK0 TO SET ADJSYN, ENABLING ENCLKO. NOTICE THAT THE READ ADJUST CIRCUIT IS AS IT WOULD BE JUST AFTER DATA DETECT GOES INACTIVE AT THE END OF A READ SEQUENCE. FROM THIS POINT, THE READ FRAMING CIRCUITRY WILL ALLOW EXACTLY 16 CLOCK PULSES TO PROPAGATE THROUGH TO THE CRC CIRCUIT AND THEN END THE SEQUENCE. LEAVING FILEN1 AT A HIGH LEVEL. THE SEQUENCE IS ENDED AS WFRCT REACHES A COUNT OF 16 (SEE FIG. 3 FOR TIMING DIAGRAM). WHEN SHEN IS CLEARED AT THE BEGINNING OF THE SHIFT CRC SEQUENCE, IT DISABLES CCRDNO WHICH INHIBITS NEW DATA FROM ENTERING THE CRC CIRCUIT. IT ALSO DISABLES THE NORMAL OUTPUT DATA PATH (FROM THE Q8 OUTPUT OF PSTREG1B) AND ENABLES CCRATO. THIS ALLOWS DATA FROM THE CRC REGISTER TO APPEAR ON RDATA1B.

3A

JK17 CIRCUIT PACK

2

CPS - JK17  
SHEET 5BELL TELEPHONE LABORATORIES  
INCORPORATED

6S

F/O CIRCUIT DESCRIPTION

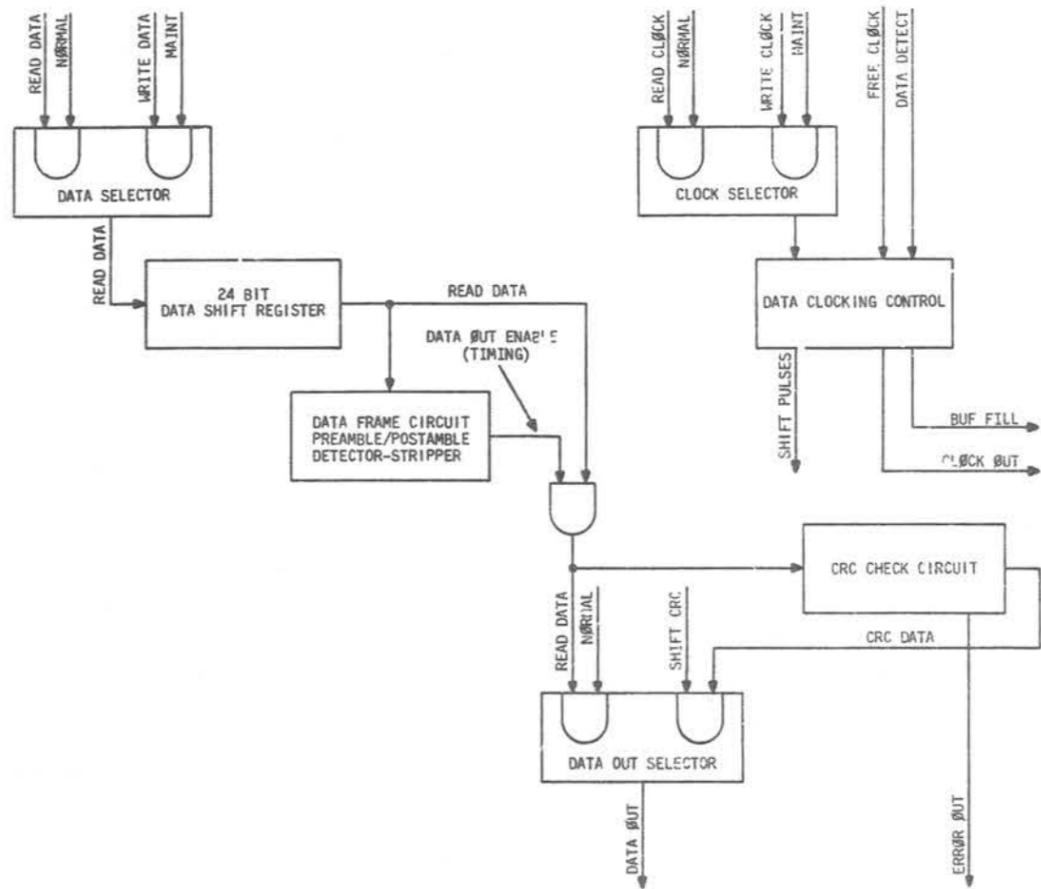


FIGURE 1 - BLOCK DIAGRAM

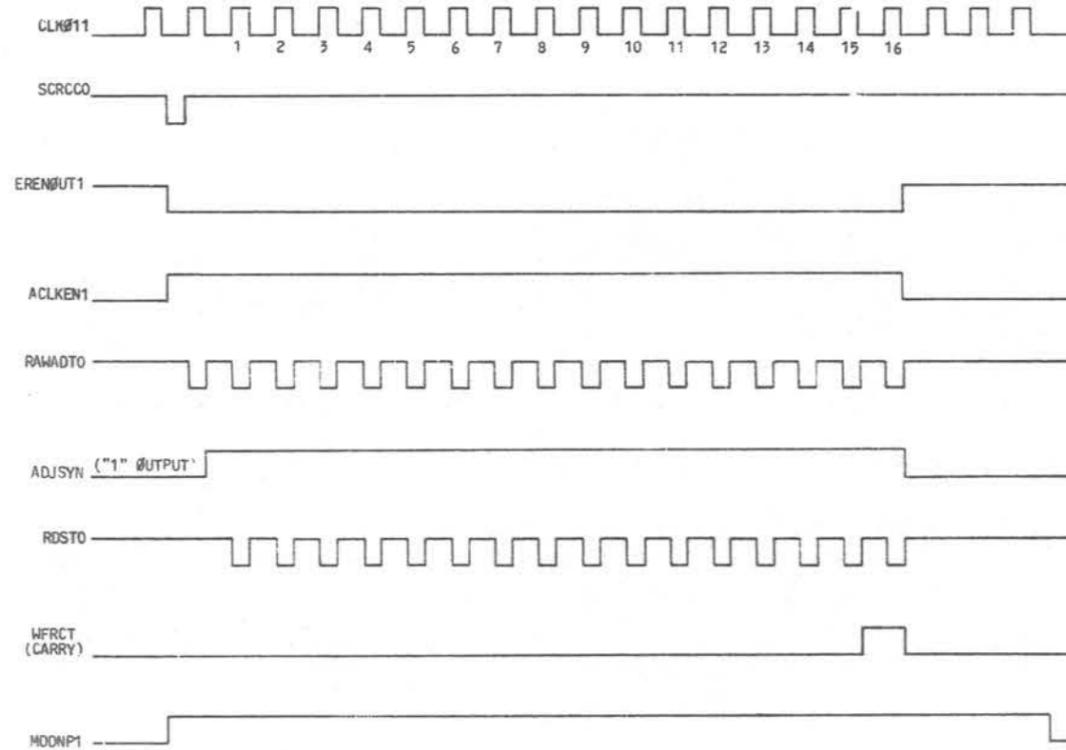


FIGURE 3 - SHIFT CRC

P/O CIRCUIT DESCRIPTION

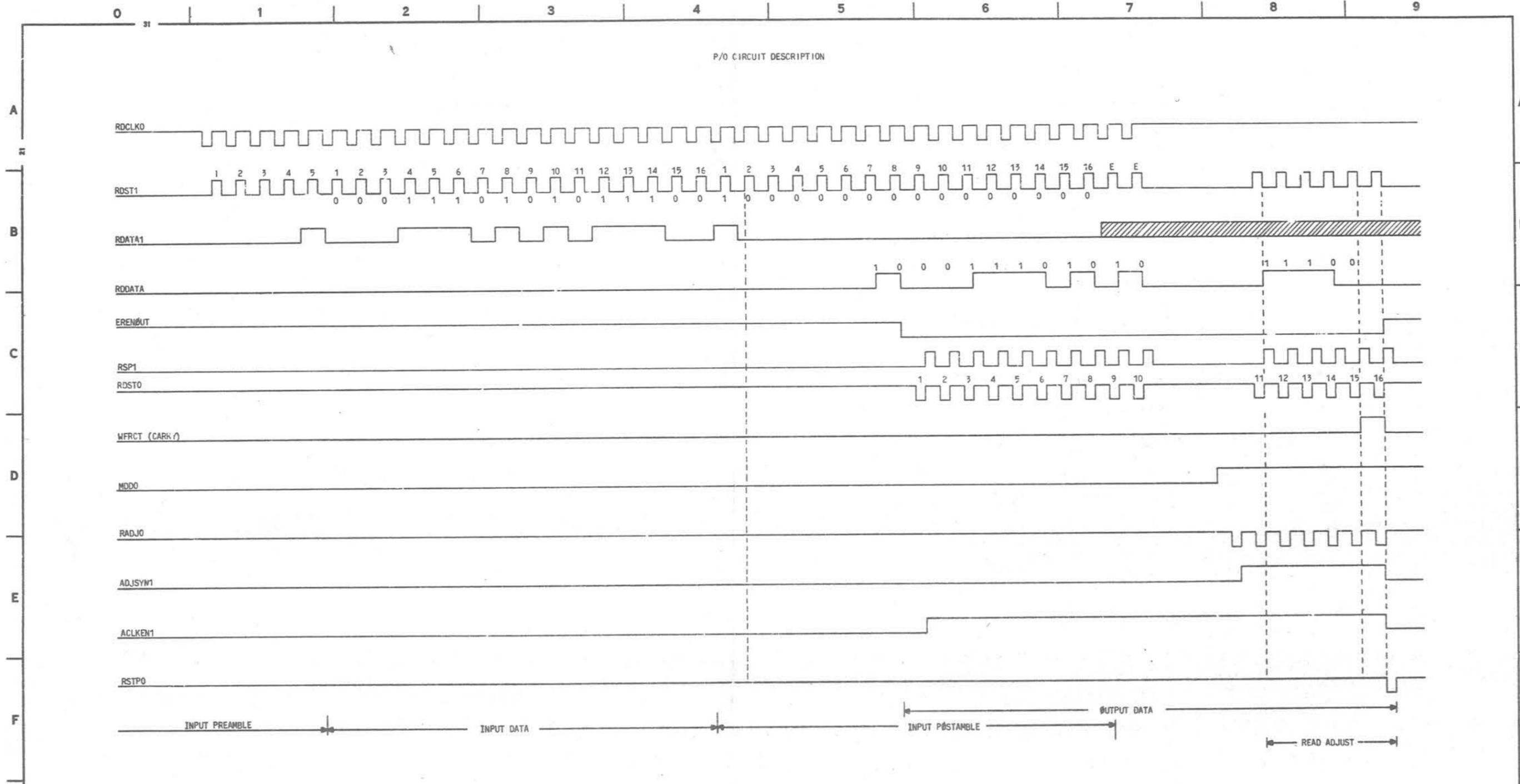


FIGURE 2  
READ TIMING FOR CTTC