SHEET INDEX

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SYMBOL

TAPE UNIT CONTROLLER
BOARD C

TERM. MOD.	FUNCT	TERM.	LOC
BACRO	I	315	3A2
BKSPACO	I	017	4A6
BØFLO	I	317	4A0
CLKØ11	I	018	2A1
CLKØ21	I	118	2A0
CRCERO	I	300	4A0
ENRD1	I	207	3A6
FILENB1	I	003	3A6
FWDO	I	316	4A1
HILVL1	I	104	4A0
INITBO	I	009	4A0
MAINT1	I	108	4A3
MDDO	I	103	4A5
RDBLKCO	I	016	4A6
RDØUT1	I	208	3A6
REVO	I	219	4A1
RSP1	I	101	2A4
RWDINGBO	I	013	4A0
RWTSTPCO	I	117	3A3
SDØTO	I	214	2A5
SHCRC1	I	106	3A5
STØPCO	I	012	4A3
SWTSTPCO	I	318	3A3
TTBØTO	I	302	4A2
TTEØTAO	I	113	4A2
WENAAO	I	107	3A5
WRITEPO	I	019	2A0
WRITEO	I	211	4A6
BLØCKO	Ø	001	4H6
BLØCK1	Ø	201	4H5
BSHPO	Ø	006	2H4
DDINHO	Ø	002	4H6
FILLAO	Ø	303	3H6
FILLO	Ø	004	3H5
RDADJO	Ø	310	2H9
SDINO	Ø	306	3H6
STØPPO	Ø	301	4H3
WRDATA	Ø	312	2H3
HILVEL1	ØI	218	3H2
RDADJ1	ØI	109	2H7
STØPPAO	ØI	209	3H4
WDATA1	ØI	102	2H4
WØ11	ØI	010	2H1
+5	P	000	2H4
+5	P	119	2H4
GRD	G	200	2H7
GRD	G	319	2H7

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

NOTES:

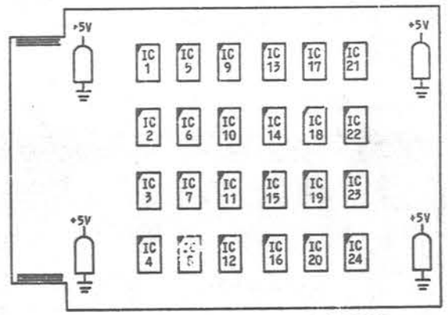
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AA	16	8
41AE	16	7,8
41BP	16	8
41CA	16	8
41CC	16	8
41CJ	16	8
41U	16	8
41W	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN).



UNNUMBERED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK18
CONNECTOR ON FRAME	947A OR 947C
ACCEPTABLE SERIES	3

CURRENT DRAIN: 305ma

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	DSN-ER	APPD
1	–	11-4-74	BP LRE	RWF MTS RFG
2A	–	11-24-75	AS LRE	LEM LEG RFG

ISSUE 2A

IN98

JK18 CIRCUIT PACK

CARTRIDGE TAPE TRANSPORT CONTROLLER BOARD C CIRCUIT

(2)

AT&TCO STANDARD

CPS-JK18
8 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED

6S

PRINTED IN U.S.A.

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD C

WRITEP0 (G19) · CLKØ21 (118) · CLKØ11 (G18) · RSP1 (101) · SDØT0 (214) · WENAA0 (385) · HILVELTB (3F1)

STØPPA0 3F3,4G5 · STPWRT0 4E4 · WDØNE1 3F2 · WSTP0 4B3

CLKSYN IC5 41AE A (NC) · CLKEN IC5 41AE B · SYNC0 IC9 41U A · EN Ø2 IC9 41U D · EN Ø1 IC9 41U C · WØ21 IC19 41BP F · WØ11 IC10 41BP G

CLKSTP1 IC9 41U B · CLKSTP0 IC10 41BP A · GAPSET0 IC24 41AA B · 1STAT1 IC13 41U D · 1STATE1 IC13 41U B · 1STATE0 IC19 41BP B · PHCØDE IC22 41AE B (NC)

WDATAJ IC11 41W D · OSTATE0 IC13 41U A · WCLK0 IC8 41W C · WDATA1 IC12 41U C · SDØT1 IC2 41BP E · R/WCLK1 IC12 41U A · WRDATAØ IC2 41BP D · BSHPØ0 IC3 41CA D

ENRSP0 IC1 41U D · ENSCØT0 IC12 41U D · SDØT0 IC2 41EP C · ENSTP0 IC15 41U A · DSTØP IC16 41AE B · DSTP1 IC12 41U B · PØSTP0 IC18 41U B · DSTP0 IC19 41BP D · ENDATA IC16 41AE A (NC) · STPCLK IC22 41AE A (NC) · STPCLK1 IC13 41U C

CARRY0 IC15 41U C · ENCRY1 IC19 41BP E · XCARRY0 IC15 41U D · ENWCLK1 IC15 41U B · WSTP0 IC18 41U C

ENWCLK0 IC19 41BP A · CØUNT0 IC18 41U A · CØUNT1 IC18 41U D · CØCLK0 IC19 41BP G

SPARE1 IC6 41U B (NC) · SPARE2 IC10 41BP B

LOAD EP ET · CLK CLR · PRPØCT IC23 41CJ A · CA

XCØUNT IC14 41AE B

C3 5 · C4 5 · C5 5 · C6 5 · C7 0.1 · C8 0.1 · C9–C29 0.1 · C30 0.1

+5 (000, 119) · WØ11 (010) · WRDATA (312) · BSHP0 (006) · WDATA1 (102) · GRD (200, 319) · RDADJ1 (109) · RDADJ0 (310)

ISSUE 2A

JK18 CIRCUIT PACK (2)

CPS-JK18
SHEET 2

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD C

BACR0 315
SWTSTPC0 318
RWTSTPC0 117
SWCRC1 106
WENAA0 107
FILENB1 003
ROMBit1 208
ENDR1 207

BACR1 IC2 41BP B
WENAA0 2A3
BACR0 IC10 41BP F
ENFILL0 IC7 41U D
HILVEL1B IC19 41BP C
HILVEL1A IC11 41W B
WSTØP1 IC1 41U B
WSTØP0 IC1 41U C
STØPC0 484
INITB0 4F0
FILLST0 IC11 41W C
FILLST1 IC11 41W A
WDØNE IC14 41AE A
FILL0 IC3 41CA C
FILLA0 IC3 41CA B
SDIN0 IC3 41CA A
NC
HILVEL1B 2A0
HILVEL1A 4C6, 4D4, 4F4
WDØNE1 2A5
STØPPA0 2A1, 4G5
HILVEL1 218
STØPPA0 209
FILL0 004
FILLA0 303
SDIN0 306

ISSUE 2A

JK18 CIRCUIT PACK (2)
BELL TELEPHONE LABORATORIES INCORPORATED
DRG SIZE 6S
CPS-JK18 SHEET 3
PRINTED IN U.S.A.

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD C

INITBO HILVLT BØFLO CRCERO RADINGBO FWDO REVO TTEØTAO TTEØTO MAINT1 STØPCO WDDO RDBLKCO BKSPACO WRITEO

009 104 317 300 013 316 219 113 302 108 012 105 016 017 211

+5 R3 2.2KΩ +5 R4 2.2KΩ

MSTPO 2B8 STØPCO 3D4

FRCØND1 IC7 41U B
MØTIØN1 IC1 41U A
FWD1 IC10 41BP D
TTEØTB1 IC10 41BP C
TTBØT1 IC2 41BP F
REV1 IC2 41BP G
MTSTP1 IC6 41U D
STCMD1 IC7 41U C
STCMDO IC7 41U A
BLOCK IC4 41AE A
SBLØCK1 IC6 41U C
DDINH IC17 41CC A
R1 23.7KΩ
C1
NC
D4, F3, 3F2, HILVEL1A

ERSTØPO IC21 41U A
EØTSTØPO IC21 41U B
BØTSTØPO IC21 41U C
MTCSTØPO IC21 41U D
CMDSTPO IC8 41W A

C6, F2, 3F2 HILVEL1A
BLKSTP IC4 41AE B
NC
BLØCK1 IC8 41W B
BLØCKO IC8 41W D

STPTRIG1 IC24 41AA A
STPTRIGO IC6 41U A
STPARTO IC10 41BP E
STPARTO 2A1

INITBO 304
R2 31.6KΩ C6,D4,3F2 HILVEL1A C2
STØPP IC20 41CC A
STØPPO IC2 41BP A
STØPPAO 2A1, 3F3

STØPPO 301
BLØCK1 201
BLØCKO 001
DDINHO 002

ISSUE 2A

JK18 CIRCUIT PACK (2)
CPS-JK18 SHEET 4
BELL TELEPHONE LABORATORIES INCORPORATED
DRAWING SIZE 6S
PRINTED IN U.S.A.

COMPONENT LIST

INTERGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41U DESIG	SH LOC	IC2 41BP DESIG	SH LOC	IC3 41CA DESIG	SH LOC	IC4 41AE DESIG	SH LOC	IC5 41AE DESIG	SH LOC	IC6 41U DESIG	SH LOC	IC7 41U DESIG	SH LOC	IC8 41W DESIG	SH LOC	IC9 41U DESIG	SH LOC	IC10 41BP DESIG	SH LOC	IC11 41W DESIG	SH LOC	IC12 41U DESIG	SH LOC
A	MØTIØN1	4B1	STØPPO	4F7	SDINO	3E6	BLØCK	4B5	CLKSIN	2B0	STPTRIGO	4E3	STCMDO	4B4	CMDSTPO	4C4	SYNCO	2C0	CLKSTPO	2C1	FILLST1	3D5	R/WCLK1	2F4
B	WST@P1	3D3	BACR1	3B2	SDØTO	2B5	BLKSTP	4D4	CLKEN	2D0	SPARE1		ERCØND1	4B0	BLØCK1	4D5	CLKSTP1	2B1	SPARE2		HILVEL1A	3D2	DSTP1	2E4
C	WST@PO	3D3	WRDATAO	2G3	FILLO	3E5					SBLØCK1	4B6	STCMD1	4B4	WCLKO	2D4	EN@1	2E1	TTE@TB1	4B2	FILLSTO	3D4	WDATA1	2D4
D	ENRSPO	2B4	SDWT1	2D5	BSHP@O	2G4					MTSTP1	4B5	ENFILLO	3C5	BLØCKO	4E5	EN@2	2E0	FWD1	4B1	WDATAO	2C3	ENSC@TO	2B4
E			TTB@T1	4B2															STPWRTO	4D4				
F			REV1	4B3															BACRO	3C4				
G																			W@11	2F1				

LOC CODE ELEM ID	IC13 41U DESIG	SH LOC	IC14 41A3 DESIG	SH LOC	IC15 41U DESIG	SH LOC	IC16 41AE DESIG	SH LOC	IC17 41CC DESIG	SH LOC	IC18 41U DESIG	SH LOC	IC19 41BP DESIG	SH LOC	IC20 41CC DESIG	SH LOC	IC21 41U DESIG	SH LOC	IC22 41AE DESIG	SH LOC	IC23 41CJ DESIG	SH LOC	IC24 41AA DESIG	SH LOC
A	OSTATEO	2D3	WD@NE	3E3	ENSTPO	2B5	ENSATA	2G5	DDINH	4C6	C@UNTO	2C8	EN@CKLO	2B8	ST@PP	4F3	ERST@PO	4C1	STPCLK	2F7	PRP@CT	2F9	STPTRIG1	4D3
B	1STATE1	2D1	XC@UNT	2F9	EN@CLK1	2D7	DST@P	2C5			P@STPO	2E5	1STATEO	2E1			E@TST@PO	4C2	PHC@DE	2E2			GAPSETO	2B1
C	STPCLK1	2G6			CARRYO	2B6					WSTPO	2E7	HILVEL1B	3D2			B@TST@PO	4C3						
D	STAT1	2C2			XCARRYO	2C7					C@UNT1	2D8	DSTPO	2F5			MTCST@PO	4C3						
E													ENCRY1	2B7										
F													W@21	2F0										
G													C@CLKO	2E8										

CAPACITOR

DESIG	CODE
[6]C1-C6	601A,5
[24]C7-C30	KS-19774 L5,0.1

RESISTOR

DESIG	CODE
R1	KS-20616 L1A,23.7KΩ
R2	KS-20616 L1A,31.6KΩ
R3	KS-20616 L1A,2.2KΩ
R4	KS-20616 L1A,2.2KΩ

ISSUE 2A

JK18 CIRCUIT PACK (2)

CPS-JK18 SHEET 5

BELL TELEPHONE LABORATORIES INCORPORATED

6S

CIRCUIT DESCRIPTION

A. FUNCTIONAL DESCRIPTION

JK18 IS ONE OF THE FOUR CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC) BOARDS. IT CONTAINS THE WRITE CIRCUITRY, CONDITION STOP LOGIC, AND BUFFER FILL REQUEST CIRCUITRY. THE WRITE CIRCUITRY INCLUDES A PREAMBLE GENERATOR, A POSTAMBLE GENERATOR, AND A DATA PHASE ENCODER CIRCUIT.

FIGURE 1 IS A BLOCK DIAGRAM OF JK18. AS A WRITE OPERATION BEGINS, A 42ms PULSE OCCURS ON THE WRITE START PULSE INPUT LEAD. THIS PULSE, WHICH COMES FROM THE WRITE DELAY CIRCUIT LOCATED ON JK19, IS INITIATED BY A WRITE COMMAND TO THE CTTC. THE CARTRIDGE TAPE TRANSPORT (CTT) BEGINS TO MOVE FORWARD AT READ/WRITE SPEED AS THE COMMAND IS ISSUED. THE CLOCK SYNC CIRCUIT, WHICH WAS LEFT IN A DISABLED STATE FROM THE PREVIOUS WRITE OPERATION OR INITIALIZATION SEQUENCE, WILL MAINTAIN AN INTERBLOCK GAP (IBG) STATE AT THE OUTPUT OF THE PHASE ENCODER CIRCUIT UNTIL THE TRAILING EDGE OF THE WRITE-START PULSE. THIS STATE MAINTAINS A CONSTANT LOW LEVEL AT THE OUTPUT OF THE PHASE ENCODER CIRCUIT, WHILE THE CTT IS WRITE ENABLED AND MOVING FORWARD AT READ/WRITE SPEED, IT WILL EFFECTIVELY WRITE AN IBG ONTO THAT PORTION OF TAPE WHICH PASSES THE WRITE WINDING OF THE CTTs HEAD. THE TRAILING EDGE OF THE WRITE START PULSE ENABLES THE CLOCK SYNC CIRCUIT. THIS CIRCUIT WILL THEN SYNC IN ON THE TWO CLOCK SIGNALS APPEARING ON THE CLØCKØ1 AND CLØCKØ2 INPUTS. CLØCKØ1 AND CLØCKØ2 MAKE UP A SINGLE 2-PHASE CLOCK OPERATING AT 48 KHZ. THEY ARE GENERATED BY A CRYSTAL OSCILLATOR CIRCUIT LOCATED ON JK19. BOTH CLOCK SIGNALS PROVIDE 1μs PULSES THAT ARE 180° OUT OF PHASE WITH EACH OTHER. THE SYNC CIRCUIT ALSO ENSURES THAT THE FIRST CLOCK PULSE AT ITS OUTPUT WILL APPEAR ON Ø1.

THE 2-PHASE CLOCK AT THE OUTPUT OF THE SYNC CIRCUIT FEEDS THE PHASE ENCODER CIRCUIT AND THE PREAMBLE/POSTAMBLE GENERATOR CIRCUIT. THE PHASE ENCODER CIRCUIT RECEIVES DATA FROM THE DATA SELECTOR CIRCUIT, AND BY UTILIZING THE 2-PHASE CLOCK, IT WILL TRANSLATE ANY NONRETURN TO ZERO (NRZ) DATA, APPEARING AT THE OUTPUT DATA SELECTOR, TO PHASE ENCODED (PE) DATA. THE PE DATA LEAD IS FED DIRECTLY TO THE CTT'S WRITE CIRCUITS.

THE PREAMBLE/POSTAMBLE GENERATOR PROVIDES DATA TO THE DATA SELECTOR CIRCUIT FOR WRITING THE PREAMBLE (15 ZEROS FOLLOWED BY A SINGLE ONE) AND THE POSTAMBLE (A SINGLE ONE FOLLOWED BY 15 ZEROS). IT ALSO PROVIDES CONTROL FOR THE DATA SELECTOR AND THE BUFFER CLOCK LEAD (DATA IN CLOCK). WHEN THE CLOCK SYNC CIRCUIT IS INITIALLY ENABLED, THE DATA ENABLE LEAD WILL BE IN A STATE SUCH THAT, DATA AT THE OUTPUT OF THE PREAMBLE/POSTAMBLE GENERATOR WILL BE GATED THROUGH THE DATA SELECTOR. THE CLOCK OUTPUT OF THE PREAMBLE/POSTAMBLE GENERATOR CIRCUIT IS DISABLED. FOR THE FIRST 15 CYCLES OF THE 2-PHASE CLOCK, THE DATA OUTPUT OF THE PREAMBLE/POSTAMBLE GENERATOR WILL REMAIN IN THE "ZERO" STATE. THIS OUTPUT GOES TO A "ONE" STATE FOR THE 16TH CYCLE OF THE CLOCK. THIS ACCOMPLISHES WRITING OF THE PREAMBLE ONTO TAPE. THE BUFFER CLOCK LEAD (DATA IN CLOCK) IS ENABLED PRIOR TO THE SIXTEENTH CYCLE OF THE 2-PHASE CLOCK; ALLOWING THE FIRST DATA BIT FROM THE BUFFER CIRCUITS TO BE LOADED ONTO THE INPUT DATA LEAD (INPUT DATA), AS THE LAST BIT OF THE PREAMBLE IS WRITTEN ONTO TAPE. AT THIS POINT, THE DATA-ENABLE LEAD CHANGES STATES, ALLOWING DATA FROM THE BUFFER CIRCUITS TO BE GATED THROUGH THE DATA SELECTOR TO THE PHASE ENCODER CIRCUITS.

A WRITE CYCLE CAN ONLY BE ENDED AS THE LAST DATA BIT FROM A GIVEN BUFFER IS CLOCKED FROM THE BUFFER CIRCUIT. THE BUFFER CIRCUIT WILL GENERATE A CARRY PULSE, APPEARING ON THE BUFFER CARRY PULSE LEAD AT THE END OF EACH BUFFER OF DATA. THIS PULSE WILL OCCUR EVERY 1024 BITS UNLESS THE REGISTER WAS STUFFED, THEREFORE, PRESETTING THE BUFFER COUNTER. TO END A WRITE CYCLE, A SET WRITE STOP COMMAND IS ISSUED TO THE CTTC. THIS COMMAND INITIATES A PULSE AT THE OUPUT OF THE CTTC'S COMMAND DECODER LOCATED ON JK16, WHICH APPEARS ON THE WRITE STOP LEAD. THIS PULSE SETS THE WRITE-STOP LATCH, ALLOWING THE NEXT PULSE OCCURRING ON THE BUFFER CARRY PULSE LEAD TO APPEAR AT THE INPUT TO THE PREAMBLE/POSTAMBLE GENERATOR CIRCUIT. AT THIS POINT, ALL DATA HAS BEEN WRITTEN AND THE BUFFER-CLOCK LEAD IS DISABLED. THE DATA ENABLE LEAD SWITCHES BACK TO ITS ORIGINAL STATE, ENABLING A DATA PATH FROM THE PREAMBLE/POSTAMBLE GENERATOR THROUGH THE DATA SELECTOR. THE DATA LEAD OF THE PREAMBLE/POSTAMBLE GENERATOR HAS REMAINED IN THE "ONE" STATE FROM THE LAST BIT OF THE PREAMBLE.

IT STAYS IN THAT STATE THROUGH THE NEXT CYCLE OF THE 2-PHASE CLOCK, WHILE WRITING THE FIRST BIT OF THE POSTAMBLE, A "ONE". THIS DATA LEAD THEN GOES TO THE "ZERO" STATE ALLOWING THE 15 "ZEROS" OF THE POSTAMBLE TO BE WRITTEN. THE CLOCK SYNC CIRCUIT IS THEN DISABLED, LATCHING THE PHASE ENCODER CIRCUIT IN THE IBG STATE. THE ACTUAL STOP SIGNAL TO THE CTT IS INITIATED BY THE READ CIRCUIT, AFTER THE READ WINDING OF THE CTT'S HEAD HAS REACHED THE IBG.

THE WRITE DATA OUTPUT (WRITE DATA) FROM THE DATA SELECTOR AND Ø1 (WRITE CLOCK OUTPUT LEAD) IS CONNECTED TO THE READ CIRCUIT LOCATED ON JK17. THE WRITE DATA LEAD IS THE NRZ FORM OF THE DATA BEING WRITTEN ONTO TAPE. A PULSE APPEARS ON THE WRITE CLOCK LEAD AT THE CENTER OF EACH BIT. WHEN THE CTTC IS IN THE MAINTENANCE MODE, AND THE READ AND WRITE CIRCUITS ARE EXERCISED WITHOUT OPERATING THE CTT, THE WRITE DATA AND WRITE CLOCK SIGNALS ARE GATED THROUGH THE READ CIRCUITS, THEREBY, TESTING ALL OF THE WRITE CIRCUITS EXCEPT THE PHASE ENCODER BY UTILIZING THE CRC CIRCUIT LOCATED ON JK17.

THE STOP CIRCUIT GENERATES A 40ms STOP PULSE WHENEVER THE TAPE DATA CONTROLLER (TDC) UNIT EXPERIENCES ANY ONE OF SEVERAL CONDITIONS. THIS PULSE, WHICH APPEARS ON THE STOP PULSE LEAD, RESETS ALL CIRCUITS OF THE CTTC TO THEIR KNOWN STOP OR INITIAL STATE. THIS STOP PULSE IS GENERATED UNDER THE FOLLOWING CONDITIONS.

(A) BUFFER OVERFLOW

THE BUFFER CIRCUITS WERE NOT PROPERLY SERVICED BY THE CENTRAL PROCESSOR (ERROR CONDITION).

(B) CRC ERRØR

A CRC ERRØR WAS DETECTED DURING THE PREVIOUS READ OR READ-AFTER-WRITE OPERATION.

(C) REWINDING

THE CTT STARTS A REWIND SEQUENCE.

(D) BEGINNING OR END OF TAPE

THE CTT SENSES THE PHYSICAL BEGINNING OF TAPE OR THE PHYSICAL END OF TAPE MARKERS.

(E) STØP

A STØP COMMAND IS ISSUED TO THE CTTC.

(F) THE COMPLETION OF A BACKSPACE, WRITE, OR READ-A-BLOCK OPERATION

EITHER OF THESE COMMANDS ISSUED TO THE CTTC WILL SET THE IBG STOP CIRCUIT. THIS CIRCUIT MONITORS THE DATA DETECT INPUT. AFTER OBSERVING DATA DETECT GO ACTIVE, THEN INACTIVE (INDICATING THAT THE CTTC HAS CROSSED A BLOCK OF DATA) IT TRIGGERS THE STOP CIRCUIT.

(G) TDC INITIALIZE

A TDC INTIALIZE COMMAND IS ISSUED TO THE TDC.

ALL READ OR SHIFT CRC (SHIFT THE CONTENTS OF THE CRC REGISTER, LOCATED ON JK17, TO THE BUFFER CIRCUITS) OPERATIONS MUST LEAVE THE ON-LINE BUFFER IN A FULL STATE. THE BUFFER CIRCUITS (ON JK13) CONTAIN TWO 1024-BIT SHIFT REGISTERS. THE ON-LINE BUFFER IS THE 1024-BIT SHIFT REGISTER WHICH IS ACTIVELY ACCEPTING DATA FROM (OR TRANSMITTING DATA TO) THE CTTC. IF THE DATA TRANFERRED TO THE BUFFER CIRCUITS IS NOT AN INCREMENT OF 1024 BITS, A FILL REQUEST MUST BE ISSUED TO THE BUFFER CIRCUITS. THE FILL CIRCUIT INDICATES IF A FILL REQUEST SHOULD BE SENT TO THE BUFFER CIRCUITS AT THE COMPLETION OF A DATA TRANSFER SEQUENCE. THE READ-DATA CLOCK LEAD IS THE BUFFER CLOCK OUTPUT FROM THE READ CIRCUIT (JK17). EACH PULSE ON THIS LEAD ATTEMPTS TO SET THE FILL REQUEST CIRCUIT. EACH PULSE ON THE BUFFER-CARRY LEAD CLEARS THE FILL REQUEST CIRCUIT. NOTE THAT THE BUFFER-CARRY PULSE OCCURS AT THE TRAILING EDGE OF READ-DATA CLOCK PULSES. IT OCCURS ONCE EVERY 1024 CLOCK PULSES TO INDICATE THAT A COMPLETE BUFFER HAS BEEN FILLED. THE FILL REQUEST CIRCUIT WILL BE LEFT IN ITS CLEARED STATE, ONLY IF THE ON-LINE BUFFER IS FULL WHEN THE LAST DATA BIT IS LOADED ONTO IT. IF THE ON-LINE BUFFER IS NOT FULL AFTER THE LAST DATA BIT HAS BEEN TRANSFERED, THE FILL REQUEST CIRCUIT WILL BE LEFT IN THE ENABLED STATE. THIS CAUSES THE FILL LEAD (FILL) TO GO ACTIVE, REQUESTING THE BUFFER FILL OPERATION WHEN IT IS ENABLED BY THE FILL-ENABLE LEAD. THE FILL-ENABLE LEAD IS DRIVEN ACTIVE BY THE READ CIRCUIT AS IT COMPLETES ITS OPERATION FOR A GIVEN DATA TRANSFER FUNCTION.

THE READ DATA INPUT LEAD (THE DATA OUTPUT FROM THE READ CIRCUIT), IS ENABLED BY THE READ-DATA ENABLE LEAD TO DRIVE THE READ OUTPUT DATA LEAD. THE READ OUTPUT DATA LEAD TRANSMITS READ DATA TO THE BUFFER CIRCUITS. THE READ DATA LEAD IS ENABLED BY JK16 WHENEVER DATA IS BEING TRANFERRED THROUGH THE READ CIRCUITS OR FROM THE CRC REGISTER TO THE BUFFER CIRCUIT.

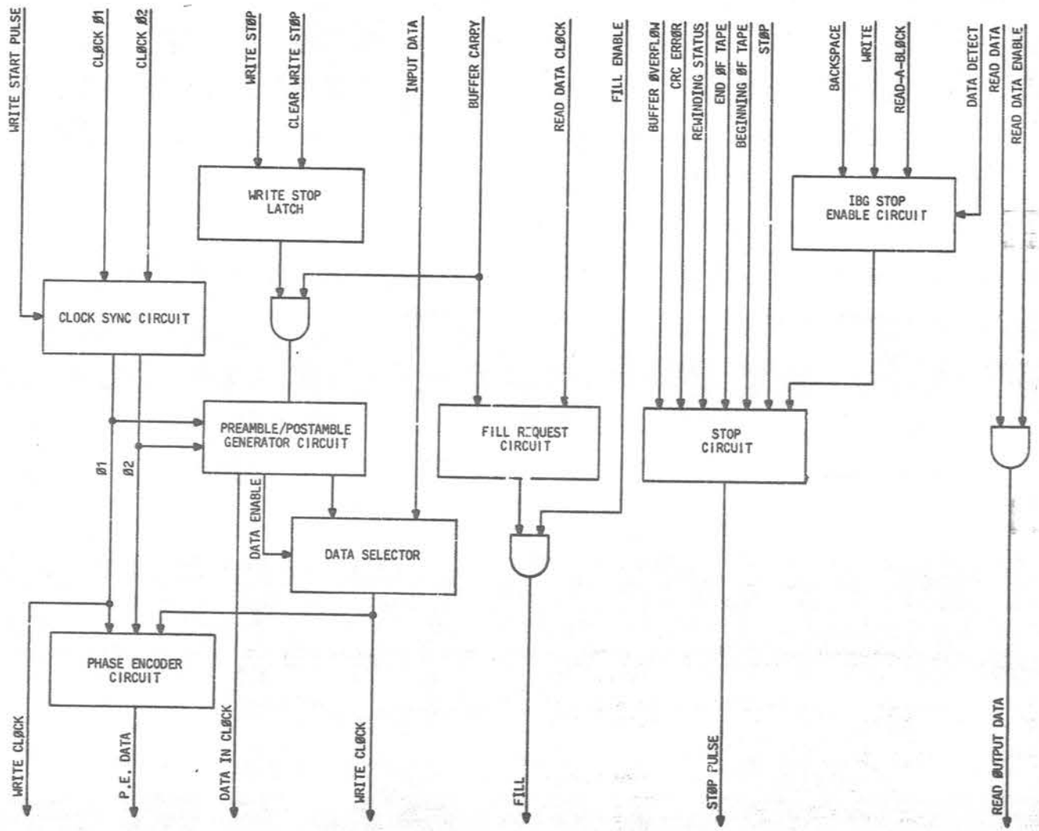


FIGURE 1 - BLOCK DIAGRAM

CIRCUIT DESCRIPTION (CONT)

B. DETAILED DESCRIPTION

WHEN A WRITE OPERATION IS PERFORMED, THE CLOCK SYNC CIRCUIT PERFORMS THE FUNCTIONS OF LATCHING THE PHASE ENCODER CIRCUIT IN ITS INTERRECORD GAP STATE AND SYNCHRONIZING THE 2-PHASE INPUT CLOCK. THE WRITE OPERATION IS INITIALIZED BY A 42ms PULSE ON THE INPUT LEAD, WRITEPO. THIS PULSE IS GENERATED BY THE WRITE DELAY CIRCUIT LOCATED ON JK19. THE D-TYPE FLIP-FLOPS, CLKSYN AND CLKEN, HAD BEEN LEFT IN THEIR SET STATES FROM THE PREVIOUS WRITE OPERATION OR INITIALIZATION SEQUENCE. INITIALLY, THE LOW LEVEL AT THE "ZERO" OUTPUT OF CLKEN, DISABLES ENØ2 AND ENØ1, PREVENTING CLOCK PULSES WHICH APPEAR ON CLKØ21 AND CLKØ11, FROM PROPAGATING THROUGH THE WRITE CIRCUIT. THE HIGH LEVEL AT CLKEN'S "ONE" OUTPUT ENABLES GAPSETO, ALLOWING CLOCK PULSES APPEARING AT THE CLKØ11 INPUT TO PROPAGATE THROUGH 1STATE1 AND 1STATEO. THESE CLOCK PULSES MAINTAIN A CLEARED STATE AT THE OUTPUT OF THE D-TYPE FLIP-FLOP PHCØDE. THE CLEARED STATE OF PHCØDE ENSURES A HIGH LEVEL AT THE OUTPUT OF WRDATAO (INPUT TO THE CTTs WRITE CIRCUIT). THIS HIGH LEVEL CAUSES THE CTT TO WRITE AN INTERRECORD GAP ONTO THAT PORTION OF TAPE WHICH PASSES UNDER THE WRITE WINDING OF THE CTTs HEAD, WHILE THE CTT IS WRITE ENABLED.

THE HIGH-GOING TRAILING EDGE OF THE PULSE ON WRITEPO TOGGLES CLKSYN TO THE CLEARED STATE, ENABLING SYNCO. THIS ALLOWS CLKEN TO BE TOGGLED TO THE CLEARED STATE AT THE TRAILING EDGE OF THE NEXT PULSE OCCURING ON CLKØ21. CLEARING CLKEN DISABLES GAPSETO AND ENABLES ENØ2 AND ENØ1. NOTE THAT THE CLOCK PULSES ON CLKØ21 AND CLKØ11 ALTERNATE (FIG. 2). THE FIRST CLOCK PULSE TO PROPAGATE THROUGH THE CLOCK SYNC CIRCUIT WILL APPEAR AT THE OUTPUT OF WØ11. THE OUTPUT PULSES FROM WØ21 WILL ALTERNATE WITH THOSE FROM WØ11, UNTIL CLKEN AND CLKSYN ARE SET AT THE END OF THE WRITE OPERATION.

AFTER GAPSETO HAS BEEN DISABLED BY CLEARING CLKEN, THE PHASE ENCODER CIRCUIT WILL ACCEPT ITS 2-PHASE CLOCK INPUT FROM WØ11 AND WØ21, AND ITS DATA INPUT FROM THE OUTPUT OF WDATA1. ALL DATA IS TO BE WRITTEN ONTO TAPE, INCLUDING THE PREAMBLE AND POSTAMBLE WILL APPEAR AT THE OUTPUT OF WDATA1. THE OUTPUT OF WDATA1 IS FED DIRECTLY INTO 1STAT1 AND INVERTED BY WDATAO TO FEED OSTATEO. FOR THE TIMING DIAGRAM OF THE PHASE ENCODER CIRCUIT SEE FIG. 2. NOTICE THAT A "ZERO" IS A LOW-TO-HIGH TRANSITION AT THE WRDATA OUTPUT, AND A "ONE" IS A HIGH-TO-LOW TRANSITION. WRDATA FEEDS THE WRITE DATA INPUT TO THE CTT. TWO CONSECUTIVE "ONES" OR TWO CONSECUTIVE "ZEROS" REQUIRE A PHASE TRANSITION.

AS CAN BE SEEN IN THE TIMING DIAGRAM, THE PHASE ENCODER PERFORMS A LOOK-AHEAD FUNCTION BY GENERATING A PHASE TRANSITION, IF NECESSARY, ON THE PHASE 1 CLOCK PULSE AND A DATA TRANSITION ON THE PHASE 2 CLOCK PULSE FOR EVERY BIT. FOR EXAMPLE, IF THE OUTPUT OF WDATA1 IS HIGH ("ZERO" DATA OUTPUT) 1STAT1 IS ENABLED, AND OSTATEO IS DISABLED. THE PHASE 1 CLOCK PULSE FOR THAT BIT WOULD APPEAR AT THE OUTPUT OF WØ11. THIS CLOCK PULSE WOULD PROPAGATE THROUGH 1STAT1, 1STATE1, AND 1STATEO TO CLEAR PHCØDE IF IT IS NOT ALREADY CLEARED. THE CLEARING OF PHCØDE DRIVES THE OUTPUT OF WRDATAO LOW, CREATING A PHASE TRANSITION ON TAPE (ASSUMING THAT PHCØDE WAS IN THE SET STATE, OTHERWISE THERE WOULD BE NO CHANGE AT THE OUTPUT OF WRDATAO, INDICATING THAT NO PHASE TRANSITION WAS NECESSARY). THE FOLLOWING PHASE 2 CLOCK PULSE APPEARING AT THE OUTPUT OF WØ21 WOULD TOGGLE PHCØDE TO ITS SET STATE CREATING A LOW-TO-HIGH TRANSITION AT THE OUTPUT OF WRDATA. PHCØDE'S "ZERO" OUTPUT IS TIED TO ITS DATA INPUT, SO THAT ANY PULSE FROM WØ21 WILL ALWAYS TOGGLE IT. IF A "ONE" IS TO BE WRITTEN THE OUTPUT OF WDATA WILL BE AT A LOW LEVEL, ENABLING OSTATEO AND DISABLING 1STAT1. THE PHASE 1 CLOCK PULSE WOULD PROPAGATE THROUGH OSTATEO, TO SET PHCØDE IF IT IS NOT ALREADY SET (CREATING A PHASE TRANSITION IF IT IS NECESSARY). THE FOLLOWING PHASE 2 CLOCK PULSE WILL CLEAR PHCØDE CREATING A HIGH-TO-LOW TRANSITION AT THE OUTPUT OF WRDATAO. THIS TRANSITION WRITES THE "ONE" ONTO TAPE.

THE PREAMBLE/POSTAMBLE GENERATOR CIRCUIT SUPPLIES DATA FOR WRITING THE PREAMBLE AND POSTAMBLE AND PROVIDES CONTROL FOR THE OUTPUT CLOCK TO THE BUFFER CIRCUITS. WHEN A WRITE OPERATION IS INITIATED, THE 42ms PULSE ON THE WRITEPO LEAD MAINTAINS A CLEARED STATE ON THE 4-BIT COUNTER PRPØCT, AND THE TWO D-TYPE FLIP-FLOPS, XCØUNT AND STPCLK. THE LOW LEVEL AT THE "1" OUTPUT OF XCØUNT DISABLES XCARRYO, AND THE LOW LEVEL ON THE CARRY OUTPUT OF PRPØCT DISABLES CARRYO. THE HIGH OUTPUTS FROM CARRYO AND XCARRYO LEAVE THE OUTPUT OF ENWCLK1 AT A LOW LEVEL. THIS LOW LEVEL DISABLES CLOCK PULSES WHICH WOULD PASS THROUGH WSTPO, PØSTPO, AND WCLKO. IT MAINTAINS A SET STATE AT THE OUTPUT OF THE D-TYPE FLIP-FLOP DSTØP AND IT DRIVES THE OUTPUT OF ENWCLKO HIGH ENABLING CØUNTO. THIS LOW LEVEL ALSO DRIVES THE OUTPUT OF DSTP1 HIGH, HOLDING DSTPO AT A LOW LEVEL. THE LOW LEVEL FROM DSTPO MAINTAINS A SET STATE AT THE OUTPUT OF THE D-TYPE FLIP-FLOP ENDATA. THE LOW "ZERO" OUTPUT OF ENDATA DISABLES ENSCØTO. WITH ENSCØTO DISABLED, THE LOW OUTPUT FROM ENWCLK1 WILL MAINTAIN A HIGH LEVEL ("ZERO" DATA STATE) AT THE OUTPUT OF WDATA1. AS WRITEPO RETURNS TO A HIGH LEVEL AND CLOCK PULSES BEGIN TO APPEAR AT THE OUTPUT OF WØ11 AND WØ21, THE CARRY OUTPUT OF PRPØCT WILL REMAIN AT A LOW LEVEL THROUGH THE FIRST 15 CLOCK PULSES FROM WØ11. SEE FIG. 3 FOR ALL WRITE TIMING. THE CLOCK PULSES FROM WØ11 WILL PROPAGATE THROUGH THE ENABLED CØUNTO, CØUNT1, AND CØCLKO TO CLOCK PRPØCT. THE CARRY OUTPUT OF PRPØCT DOES NOT GO HIGH UNTIL THE TRAILING EDGE OF THE FIFTEENTH CLOCK PULSE. THIS LOW LEVEL AT THE CARRY OUTPUT OF PRPØCT HAS HELD THE OUTPUT OF WDATA1, THE DATA INPUT TO THE PHASE ENCODER CIRCUIT, AT A HIGH LEVEL THROUGH THE 15 CLOCK PULSES, ALLOWING THE PHASE ENCODER TO TRANSMIT 14 "ZEROS" TO THE CTTs WRITE CIRCUITS. THE PHASE TRANSITION FOR THE FIFTEENTH "ZERO" WAS TRANSMITTED ON THE LAST CLOCK PULSE. THIS LEAVES PHCØDE IN ITS CLEARED STATE WHICH WILL ALLOW THE FOLLOWING CLOCK PULSE FROM WØ21 TO WRITE THE FIFTEENTH "ZERO" ONTO TAPE.

THE TRAILING EDGE OF THE FIFTEENTH CLOCK PULSE FROM WØ11 DRIVES THE CARRY OUTPUT OF PRPØCT HIGH. THE LOW LEVEL WHICH HAD REMAINED AT THE "ONE" OUTPUT OF STPCLK HAS HELD THE OUTPUT OF STPCLK1 HIGH. THE HIGH LEVEL AT THE OUTPUT OF STPCLK1 AND AT THE CARRY OUTPUT OF PRPØCT WILL CREATE A LOW LEVEL AT THE OUTPUT OF CARRYO DRIVING ENWCLK1 TO A HIGH LEVEL. THE HIGH LEVEL AT THE OUTPUT OF ENWCLK1 DRIVES ENWCLKO LOW, DISABLING CLOCK PULSES TO PRPØCT. IT REMOVES THE LOW LEVEL AT THE SET INPUT TO ENDATA AND DSTØP.

THIS HIGH LEVEL ALSO REMOVES ONE INHIBIT TO WCLKO AND ALLOWS THE OUTPUT OF WDATA1 TO GO LOW ("ONE" DATA STATE). THE SIXTEENTH CLOCK PULSE FROM WØ11 LOADS THE "ONE" INTO THE PHASE ENCODER CIRCUIT AND ITS TRAILING EDGE CLEARS ENDATA. THE HIGH LEVEL AT THE "ZERO" OUTPUT OF ENDATA ENABLES ENSCØTO. THIS ALLOWS DATA FROM THE BUFFER CIRCUITS, APPEARING ON THE SDØTO INPUT LEAD, TO FLOW THROUGH SDØTO, SDØT1 AND ENSCØTO TO THE INPUT OF WDATA1. THE "ONE", THE LAST BIT OF THE PREAMBLE, HAS ALREADY BEEN LOADED INTO THE PHASE ENCODER CIRCUIT. THE STATE OF SDØTO, WHICH IS UNKNOWN, IS NOT OBSERVED UNTIL THE NEXT CLOCK PULSE FROM WØ11. THE SIXTEENTH CLOCK PULSE FROM WØ21 TOGGLES PHCODE TO COMPLETE THE WRITING OF THE PREAMBLE (15 "ZEROS" FOLLOWED BY A SINGLE "ONE") ONTO TAPE. THE READER SHOULD NOTE THAT THE D-TYPE FLIP-FLOP WDØNE WAS LEFT IN THE CLEARED STATE AFTER THE PREVIOUS WRITE OPERATION OR INITIALIZATION SEQUENCE. THE LOW LEVEL AT ITS "ONE" OUTPUT KEEPS ENSTPO DISABLED. INHIBITING THE CLEARING OF DSTØP. THIS MEANS THAT WCLKO IS ENABLED AT THE SIXTEENTH CLOCK PULSE FROM WØ21 ALLOWING THAT TO BE THE FIRST WRITE CLOCK PULSE TO PROPAGATE THROUGH R/WCLK1 AND BSHPØO. THE OUTPUT OF BSHPØO (BSHPO) IS THE CLOCK LEAD TO THE BUFFER CIRCUITS. (THE BUFFER CIRCUITS MUST BE CLOCKED BEFORE THE FIRST DATA BIT APPEARS ON THE SDØTO INPUT LEAD.) FROM THIS POINT, DATA THAT IS CLOCKED FROM THE BUFFER CIRCUITS BY THE BSHPO OUTPUT WILL BE WRITTEN ONTO TAPE.

WHEN A READ OPERATION IS BEING PERFORMED, THE WENAAO INPUT WILL BE AT A HIGH-LEVEL ENABLING ENRSPO. WENAAO IS THE ZERO OUTPUT OF THE WRITE FLIP-FLOP LOCATED ON JK16. READ-CLOCK PULSES, GENERATED BY THE READ CIRCUIT, WILL APPEAR ON THE RSP1 INPUT LEAD. THESE CLOCK PULSES WOULD ALSO PROPAGATE THROUGH R/WCLK1 AND BSHPØO TO SHIFT DATA TO THE BUFFER CIRCUITS.

A WRITE OPERATION CAN ONLY BE ENDED JUST AFTER A GIVEN BUFFER OF THE BUFFER CIRCUITS HAS BEEN EMPTIED. THIS IS ACCOMPLISHED BY ISSUING A SET WRITE-STOP COMMAND TO THE CTTC. ISSUING THIS COMMAND GENERATES A PULSE AT THE OUTPUT OF THE CTTCs COMMAND DECODER, LOCATED ON JK16. THIS PULSE WILL APPEAR ON THE SWTSTPCO INPUT LEAD, SETTING THE OUTPUT OF WSTØP1 TO A HIGH LEVEL. WSTØP1 AND WSTØPO MAKE UP A S-R FLIP-FLOP WHICH CAN BE RESET BY ISSUING A RESET WRITE-STOP COMMAND WHICH ALSO GENERATES A PULSE AT THE OUTPUT OF THE COMMAND DECODER. THIS PULSE WOULD APPEAR AT THE RWTSTPCO INPUT AND RESET THE OUTPUT OF WSTØP1 TO A LOW STATE. A PULSE WILL APPEAR ON THE BACRO LEAD AT THE END OF EACH BUFFER OF DATA (NORMALLY 1024 BITS) FROM THE BUFFER CIRCUITS. THIS PULSE, WHICH APPEARS AT THE TRAILING EDGE OF THE PULSE TRANSMITTED OVER THE BSHPO LEAD, WILL SET WDØNE IF WSTØP1 IS AT A HIGH LEVEL. THE HIGH LEVEL AT THE "ONE" OUTPUT OF WDØNE WILL ENABLE ENSTPO. AT THIS POINT, THE LAST BIT OF DATA FROM THE BUFFER CIRCUITS IS AT THE OUTPUT OF WDATA1 WHICH HAS NOT BEEN LOADED ONTO THE PHASE ENCODER CIRCUIT. THE FOLLOWING CLOCK PULSE FROM WØ11 LOADS THE LAST DATA BIT INTO THE PHASE ENCODER AND TOGGLES DSTØP TO ITS CLEARED STATE. THE CLEARED STATE OF DSTØP ENABLES PØSTPO, DISABLES WCLKO, AND FORCES A LOW STATE AT THE OUTPUT OF DSTPO TO SET ENDATAO. DISABLING WCLKO INHIBITS ALL CLOCK PULSES TO THE BUFFER CIRCUITS AND SETTING ENDATA DISABLES ENSCØTO, INHIBITING THE BUFFER DATA INPUT FROM SDØTO. BY DISABLING THE BUFFER DATA INPUT, THE OUTPUT OF WDATA1 GOES LOW SINCE ENWCLK1 IS HIGH. THE NEXT CLOCK PULSE FROM WØ21 CLOCKS THE LAST DATA BIT, WHICH WAS STORED IN THE PHASE ENCODER ONTO TAPE. THE LOW LEVEL ("ONE" DATA STATE) AT THE OUTPUT OF WDATA1, IS NOW CLOCKED INTO THE PHASE ENCODER BY THE NEXT PULSE FROM WØ11. THIS IS THE FIRST BIT OF THE POSTAMBLE (A "ONE" FOLLOWED BY 15 ZEROES). THIS CLOCK PULSE PROPAGATES THROUGH PØSTPO TO SET STPCLK, WHICH DRIVES THE OUTPUT OF STPCLK1 LOW AT THE TRAILING EDGE OF THE PULSE. NOTICE THAT THE LOW GOING PULSE AT THE OUTPUT OF PØSTPO IS ALSO AN INPUT TO STPCLK1. THIS WAS DONE SO THAT THE LOW LEVEL WOULD REMAIN AT THE OUTPUT OF WDATA1 UNTIL THE PULSE FROM WØ11 WAS COMPLETED, ALLOWING PROPER LOADING OF THE PHASE ENCODER CIRCUIT.

THE PULSE AT THE OUTPUT OF PØSTPO ALSO PROPAGATES THROUGH CØUNT1 AND CØCLKO TO TOGGLE PRPØCT TO ITS "ZERO" STATE, REMOVING THE HIGH LEVEL OF ITS CARRY OUTPUT. THE LOW CARRY OUTPUT OF PRPØCT CREATES A HIGH OUTPUT FROM CARRYO ALLOWING THE OUTPUT OF ENWCLK1 TO GO TO A LOW STATE. THE LOW OUTPUT OF ENWCLK1 DRIVES THE OUTPUT OF ENWCLKO HIGH, ENABLING CØUNTO. IT SETS DSTØP WHILE MAINTAINING A DISABLED STATE AT THE INPUT TO WCLKO AND THE SET STATE AT THE OUTPUT OF ENDATA. IT ALSO DRIVES THE OUTPUT OF WDATA1 TO A HIGH-LEVEL ("ZERO" DATA OUTPUT). THE LOW LEVEL AT THE OUTPUT OF STPCLK1 DISABLES CARRYO AND DRIVES THE OUTPUT OF ENCRY1 TO A HIGH-LEVEL ENABLING XCARRYO. THE NEXT CLOCK PULSE FROM WØ21 CLOCKS THE "ONE" FROM THE PHASE ENCODER ONTO TAPE (FIRST BIT OF THE POSTAMBLE). THE OUTPUT OF WDATA1 REMAINS HIGH ("ZERO" DATA STATE) THROUGH THE NEXT 15-CLOCK PULSES FROM WØ11. THIS EFFECTIVELY ALLOWS THE WRITING OF 14 "ZEROS" ONTO TAPE AND LEAVES THE LAST "ZERO" OF THE POSTAMBLE STORED IN THE PHASE ENCODER CIRCUIT. NOTICE THAT DURING THIS PERIOD CØUNTO WAS ENABLED, ALLOWING CLOCK PULSES FROM WØ11 TO PROPAGATE TO THE CLOCK INPUT OF PRPØCT. THE CARRY OUTPUT OF PRPØCT WENT HIGH 2 CLOCK PULSES EARLIER, ALLOWING THE LAST CLOCK PULSE FROM WØ11 TO TOGGLE XCØUNT TO ITS SET STATE. THE HIGH LEVEL AT THE "ONE" OUTPUT OF XCØUNT DRIVES THE OUTPUT OF XCARRYO LOW, FORCING THE OUTPUT OF ENWCLK1 HIGH. THE HIGH OUTPUT OF ENWCLK1 ENABLES WSTPO SO THAT THE NEXT CLOCK PULSE FROM WØ21, WHICH WRITES THE 15TH "ZERO" OF THE POSTAMBLE ONTO TAPE, WILL PROPAGATE THROUGH IT. THIS PULSE PROPAGATES THROUGH CLKSTP1 AND CLKSTPO TO SET CLKEN AND CLKSYN, THEREBY, ENDING THE CLOCK INPUT TO THE WRITE CIRCUIT. IT TOGGLES STPCLK BACK TO ITS CLEARED OR INITIAL STATE AND IS FED INTO THE STOP CIRCUIT DESCRIBED BELOW. WHEN THE READ WINDING OF THE CTT REACHES THE END OF THE DATA JUST WRITTEN, THE STOP CIRCUIT WILL GENERATE A PULSE WHICH WILL CLEAR WDØNE.

THE STOP CIRCUIT WILL GENERATE A 40ms LOW GOING PULSE ON THE STØPPAO AND STØPPO LEADS, IF ANY OF THE INPUTS TO STPTRIG1 ARE DRIVEN LOW. A LOW INPUT TO STPTRIG1 DRIVES THE OUTPUT OF STPTRIGO LOW TRIGGERING THE MONOPULSER, STØPP. THE "ZERO" OUTPUT OF STØPP PULSES LOW FOR 40ms AND ITS "ONE" OUTPUT FORCES THE OUTPUT OF STØPPO LOW FOR 40ms. THE OUTPUT ON THE STØPPAO LEAD INITIALIZES ALL CIRCUITS LOCATED ON JK18 TO THEIR STOP STATE. IT CLEARS THE D-TYPE FLIP-FLOPS, BLØCK AND WDØNE, RESETS THE SR FLIP-FLOP WSTØP1/WSTØPO TO A LOW OUTPUT FROM WSTØP1, SETS THE D-TYPE FLIP-FLOP, BLKSTP, AND PROPAGATES THROUGH CLKSTP1 AND CLKSTPO TO SET CLKSYN AND CLKEN. THE PULSE ON STØPPAO ALSO DISABLES THE INPUTS TO STØPP WHILE IT IS ACTIVE. THE PULSE ON THE STØPPO LEAD IS USED TO INITIALIZE ALL OTHER CIRCUITS OF THE CTTC TO THEIR STOP STATES. STØPP IS ALSO TRIGGERED WHEN A TDC INITIALIZE COMMAND IS ISSUED. THIS COMMAND CAUSES CIRCUITS, WHICH ARE LOCATED ON JK16, TO PULSE THE INITBO LEAD.

IF THE CTTC IS IN ANY MOTION STATE OTHER THAN REWIND, EITHER THE FWDO OR THE REVO LEAD WILL BE HELD AT A LOW LEVEL BY CIRCUITS ON JK16. A LOW LEVEL ON FWDO OR REVO WILL CREATE A HIGH OUTPUT FROM MØTØN1 ENABLING ERSTØPO. A LOW SIGNAL ON BØFLO, CRCERO, OR RWDINGBO WILL DRIVE THE OUTPUT OF ENCØND1 HIGH, CREATING A LOW OUTPUT FROM ERSTØP WHEN IT IS ENABLED. THE LOW OUTPUT FROM ERSTØPO DRIVES AN INPUT TO STPTRIG1 LOW, CREATING A TRIGGER INPUT TO STØPP. BØFLO GOES LOW WHENEVER THERE IS AN OVERFLOW (ERROR) CONDITION IN THE BUFFER CIRCUITS. CRCERO IS DRIVEN LOW BY THE CRC CIRCUIT (LOCATED ON JK17) WHENEVER A CRC ERROR IS DETECTED. RWDINGBO IS DRIVEN LOW BY THE CTT WHENEVER THE CTT ENTERS A REWIND SEQUENCE. A LOW LEVEL ON THE FWDO LEAD WILL DRIVE THE OUTPUT OF FWD1 HIGH, ENABLING EØTSTØPO. WHILE EØTSTØPO IS ENABLED, A LOW LEVEL ON THE TTEØTAO LEAD WILL DRIVE THE OUTPUT OF EØTB1 HIGH, FORCING THE OUTPUT OF EØTSTØPO LOW. THIS LOW OUTPUT IS FED INTO STPTRIG1 TO TRIGGER STØPP. TTEØTAO IS DRIVEN LOW BY THE CTT WHEN THE PHYSICAL END OF TAPE IS DETECTED. A LOW ON REVO DRIVES THE OUTPUT OF REV1 HIGH, ENABLING BØTSTØPO. A LOW LEVEL ON THE TTBØTAO LEAD WILL PRODUCE A HIGH-OUTPUT FROM TTBØT1 DRIVING THE OUTPUT OF BØTSTØPO LOW WHEN IT IS ENABLED. THIS LOW IS FED INTO STPTRIG1 TO TRIGGER STØPP. TTEØTAO IS DRIVEN LOW BY THE CTT WHEN THE PHYSICAL BEGINNING OF TAPE IS DETECTED. THE ISSUING OF A STOP-COMMAND TO THE CTTC WILL GENERATE A LOW-GOING PULSE AT THE OUTPUT OF THE CTTCs COMMAND DECODER LOCATED ON JK16. THIS PULSE, WHICH WILL APPEAR ON THE STØPCO INPUT LEAD, WILL CREATE A HIGH-GOING PULSE AT THE OUTPUT OF MTSTP1. THE PULSE AT THE OUTPUT OF MTSTP1 WILL PROPAGATE THROUGH STPWRTO, CLKSTP1, AND CLKSTPO TO SET CLKSYN AND CLKEN. IF THE CTTC IS IN THE MAINTENANCE MODE, MAINT1 WILL BE AT A HIGH LEVEL ALLOWING THE PULSE FROM MTSTP1 TO PROPAGATE THROUGH MTCSTØPO. THE LOW-GOING PULSE, WHICH WILL APPEAR AT THE OUTPUT OF MTCSTØPO, IS FED INTO STPTRIG1 TO TRIGGER STØPP. A PULSE ON THE STØPCO LEAD WILL ALSO SET THE OUTPUT OF STCMD1 TO A HIGH STATE. STCMD1 AND STCMDO MAKE UP A SR FLIP-FLOP. THE HIGH OUTPUT FROM STCMD1 IS FED INTO CMDSTPO WHOSE OUTPUT WILL GO LOW WHEN IT IS ENABLED BY A HIGH LEVEL ON BOTH, MDDO AND THE "ZERO" OUTPUT OF THE D-TYPE FLIP-FLOP, BLØCK. THIS LOW OUTPUT FROM CMDSTPO IS FED INTO STPTRIG1 TO TRIGGER STØPP. BLØCK, WHICH IS PART OF THE IBG STOP ENABLE CIRCUIT, IS IN A CLEARED STATE (HIGH LEVEL AT ITS "ZERO" OUTPUT) UNLESS THE CTTC IS IN A READ, WRITE, OR READ-A-BLOCK MODE. THE PULSE ON WSTPO, WHICH OCCURS AT THE END OF A WRITE OPERATION HAS THE SAME EFFECT AS A PULSE ON THE STØPCO LEAD.

IF A COMMAND IS ISSUED TO THE CTTC TO WRITE, READ-A-BLOCK, OR BACK-SPACE, A LOW GOING PULSE WILL APPEAR ON THE WRITEO, THE RDBLKCO, OR THE BKSPACO INPUT LEAD, RESPECTIVELY. THIS PULSE WHICH IS GENERATED AT THE OUTPUT OF THE CTTC COMMAND DECODER, WILL PROPAGATE THROUGH SBLØCK1 AND TRIGGER DDINH A 90ms LOW GOING PULSE WILL APPEAR AT THE "ZERO" OUTPUT OF DDINH. THIS PULSE WILL SET BLØCK, WHICH IS ALWAYS LEFT IN THE CLEARED STATE AT THE END OF A CTTC OPERATION. THE SET STATE OF BLØCK CREATES A LOW LEVEL AT THE OUTPUT OF BLØCKO AND A HIGH LEVEL AT THE OUTPUT OF BLØCK1. THESE TWO OUTPUTS DRIVE THE STATUS CIRCUITRY LOCATED ON JK16. THE HIGH LEVEL AT THE "ZERO" OUTPUT OF BLØCK, DISABLES CMDSTPO. THE ISSUING OF ANY ONE OF THE THREE COMMANDS MENTIONED ABOVE CAUSES THE CTT TO MOVE TAPE IN EITHER THE FORWARD OR REVERSE DIRECTION AT READ/WRITE SPEED. AS DATA BEGINS TO CROSS THE READ WINDING OF THE CTTs HEAD, THE DATA DETECT LEAD MDDO WILL BE DRIVEN TO A LOW LEVEL BY THE CTT. WHEN THE READ WINDING REACHES THE NEXT IBG, MDDO WILL GO TO A HIGH LEVEL, TOGGLING BLØCK TO ITS CLEARED STATE. THE CLEARING OF BLØCK, WHICH CREATES A LOW-TO-HIGH TRANSITION ON ITS "ZERO" OUTPUT, WILL ENABLE CMDSTPO AND TOGGLE THE D-TYPE FLIP-FLOP BLKSTP TO ITS CLEARED STATE. THE LOW LEVEL AT THE "ONE" OUTPUT OF BLKSTP IS FED INTO STPTRIG1 CAUSING STØPP TO BE TRIGGERED.

FILLST1 AND FILLSTO MAKE UP A SR FLIP-FLOP. THIS FLIP-FLOP INDICATES WHETHER A FILL OPERATION IS REQUIRED AFTER DATA IS TRANSFERED FROM THE READ CIRCUITS TO THE BUFFER CIRCUITS. THE READER SHOULD REFER TO THE GENERAL DESCRIPTION FOR MORE DETAILS ON THE REQUIREMENT OF A FILL OPERATION. AS DATA IS SHIFTED TO THE BUFFER CIRCUITS, THE SHIFT PULSES WILL APPEAR ON THE SHCRC1 INPUT LEAD. WENAAO IS ALWAYS AT A HIGH LEVEL WHEN THE CTTC IS NOT IN THE WRITE MODE. THIS HIGH LEVEL ENABLES ENFILLO ALLOWING THE CLOCK PULSES ON SHCRC1 TO APPEAR AT THE INPUT OF FILLST1. EACH OF THESE CLOCK PULSES WILL LEAVE THE OUTPUT OF FILLST1 IN A HIGH-STATE. FILLST1 IS TOGGLED TO A LOW-STATE EACH TIME A PULSE OCCURS ON THE BACRO LEAD. A PULSE OCCURS ON THE BACRO LEAD EACH TIME A 1024-BIT BUFFER (ON JK13) HAS BEEN FILLED. IF THE LAST CLOCK PULSE ON THE SHCRC LEAD IS NOT FOLLOWED BY A PULSE ON THE BACRO LEAD, THE OUTPUT OF FILLST1 WILL BE LEFT IN A HIGH STATE AT THE END OF THE DATA TRANSFER SEQUENCE, INDICATING THE ON-LINE BUFFER IS NOT FULL. AS THE READ CIRCUITS COMPLETE THEIR OVERHEAD TASKS, THEY WILL DRIVE THE FILENB1 LEAD HIGH, ENABLING FILLO. THE HIGH LEVEL AT THE OUTPUT OF FILLST1 WILL THEN MAINTAIN A LOW LEVEL AT THE OUTPUT OF FILLO AND FILLAO UNTIL A PULSE OCCURS ON THE BACRO LEAD. THE LOW LEVEL ON THE FILLO LEAD IS A FILL REQUEST TO THE BUFFER CIRCUITS. WHEN THE ON-LINE BUFFER IS FULL, THE BACRO LEAD WILL BE PULSED LOW, SETTING FILLST1 TO A LOW STATE. THIS REMOVES THE LOW LEVEL AT THE OUTPUT OF FILLO AND FILLAO. FILLST1 CAN ALSO BE SET TO A HIGH STATE BY ISSUING A STOP OR TDC INITIALIZE COMMAND TO THE CTTC, CREATING A PULSE ON THE STØPCO OR INITBO LEAD, RESPECTIVELY.

THE NAND GATE, SDINO BUFFERS DATA FROM THE READ CIRCUITS. THE DATA APPEARS ON THE RDØUT1 LEAD AND IS ENABLED THROUGH SDINO BY A HIGH LEVEL ON THE ENRD1 LEAD. ENRD1 IS DRIVEN TO A HIGH LEVEL BY THE READ FLIP-FLOP, LOCATED ON JK16, WHEN THE CTTC IS IN A DATA TRANSFER MODE. THE OUTPUT OF SDINO IS THE DATA TRANSFER LEAD TO THE BUFFER CIRCUITS.

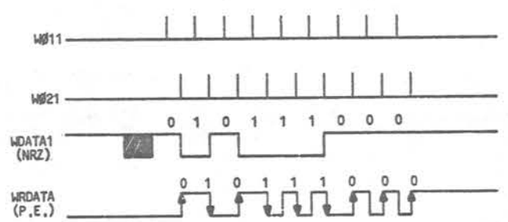


FIGURE 2 - PHASE ENCODING

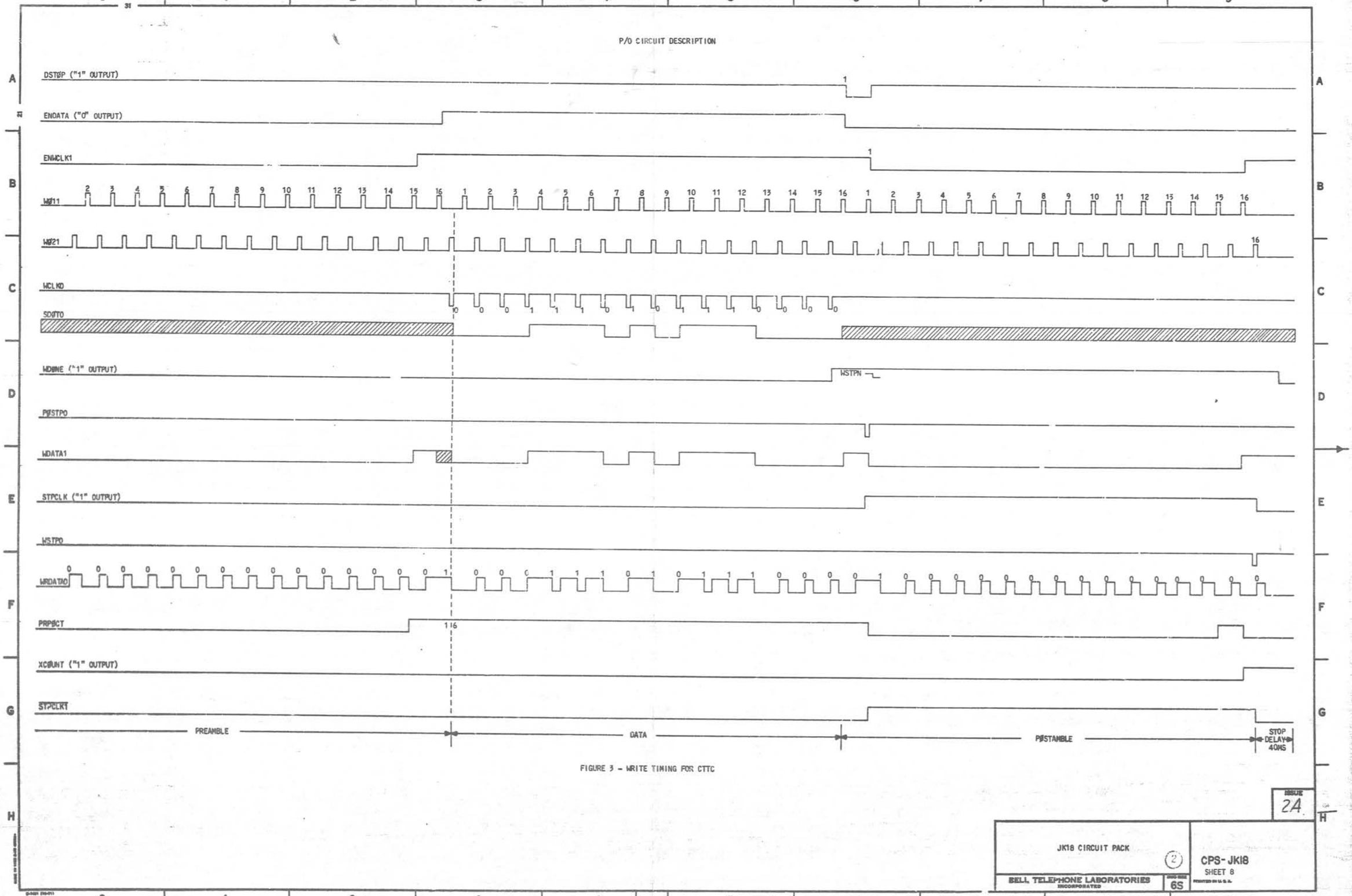


FIGURE 3 – WRITE TIMING FOR CTTC