PART OF CPS JK25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
SHEET INDEX SUPPORTING INFORMATION CURRENT DRAIN USED ON NOTES SYMBOL RECORD OF CHANGES	1	1
CIRCUIT PACK SCHEMATIC	2	1
	3	1
COMPONENT LIST	4	1
CIRCUIT DESCRIPTION TIMING	5	1

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
2. POWER AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	GRD TERM.	BAT. TERM		
41U	8	16		
41BP	8	16		
41BW	8	16		
41CA	8	16		
KS-21285,L24	8	16		
KS-21285,L45	7	14		
KS-21286,L3	8	16		
KS-21688,L3	7	14		
KS-21827,L15	7	14		
KS-22038,L1	7	14		

3. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

4. TERMINALS 203 AND 304 ARE RESERVED AND SHALL NOT BE USED.
5. (SEE SKETCH AT LEFT).
6. CURRENT DRAIN: 680 mA

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	3-2-78	AS TLB	MM JOB MG

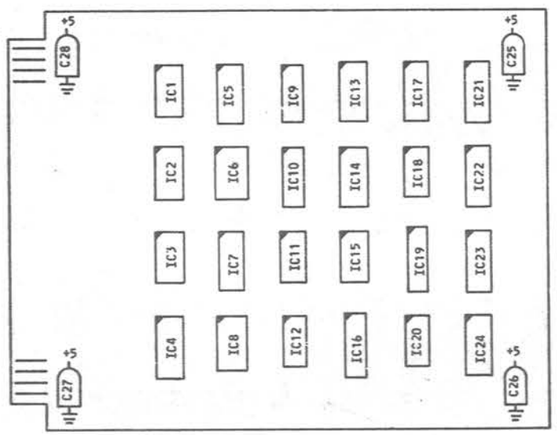
SYMPOL

FANOUT BOARD
ELEMENT A

TERM.MOD	FUNCT	TERM.	LOC	TERM.MOD	FUNCT	TERM.	LOC
AP17,8I1	I	303	2A8	RSEL1	Ø	013	2H3
AP7,0I1	I	204	3A9	SELRCO	Ø	210	2H5
AOCI1	I	010	3A7	SELRWO	Ø	205	2H1
A01I1	I	112	3A7	TAPERO	Ø	212	3H3
A02I1	I	011	3A6	UNSELERO	Ø	211	2H5
A03I1	I	111	3A9	+5	P	000	2H2
A04I1	I	207	3A6	+5	P	119	2H2
A05I1	I	012	3A6	GRD	G	004	2G8
A06I1	I	306	3A5	GRD	G	005	2G8
A07I1	I	208	3A5	GRD	G	008	2G8
A08I1	I	309	3A2	GRD	G	104	2G8
A09I1	I	307	3A0	GRD	G	107	2G8
A10I1	I	305	3A1	GRD	G	200	2H2
A11I1	I	206	3A5	GRD	G	319	2H2
A12I1	I	110	3A4				
A13I1	I	308	3A4				
A14I1	I	209	3A4				
A15I1	I	016	3A1				
A16I1	I	117	3A1				
A17I1	I	019	3A3				
RASIO	I	201	2A4				
REFIO	I	214	2A3				
RWIO	I	300	2A0				
SELOI1	I	113	2A2				
TS1I1	I	216	2A6				
CEA01	I/O	102	3G8				
CEA11	I/O	009	3H7				
CEA21	I/O	109	3H7				
GCAS0	I/O	310	2H6				
GRAS0	I/O	003	2H4				
GRCA00	I/O	007	3H4				
GRCA10	I/O	105	3H5				
GRCA20	I/O	006	3H5				
GRCA30	I/O	103	3H4				
GRCA40	I/O	101	3H1				
GRCA50	I/O	002	3H1				
GRCA60	I/O	106	3H0				
GRM0	I/O	001	2H0				
MSELO	O	311	2H1				
MSEL00	I/O	115	3H2				
REFCK1	I/O	218	2H4				
REF0	I/O	108	2H3				

NOTES: (CONT)

5. DIPS TO BE NUMBERED IN THE MANNER SHOWN BELOW (BOARD SHOWN FROM COMPONENT SIDE).



SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

SUPPORTING INFORMATION

CATEGORY	NUMBER
CONNECTOR ON FRAME	
CIRCUIT PACK INFORMATION DRAWING	
SERIES FOR LATEST CLASS "A" CHANGE	
ACCEPTABLE SERIES	

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

INSB

JK25 CIRCUIT PACK

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)
CIRCUIT

AT&TCO STANDARD

DWG SIZE 6S | ISSUE 1

BELL LABORATORIES | CPS-JK25 | 5 SHEETS

8262-070476

PART OF CPS JK25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

SHEET NOTES:

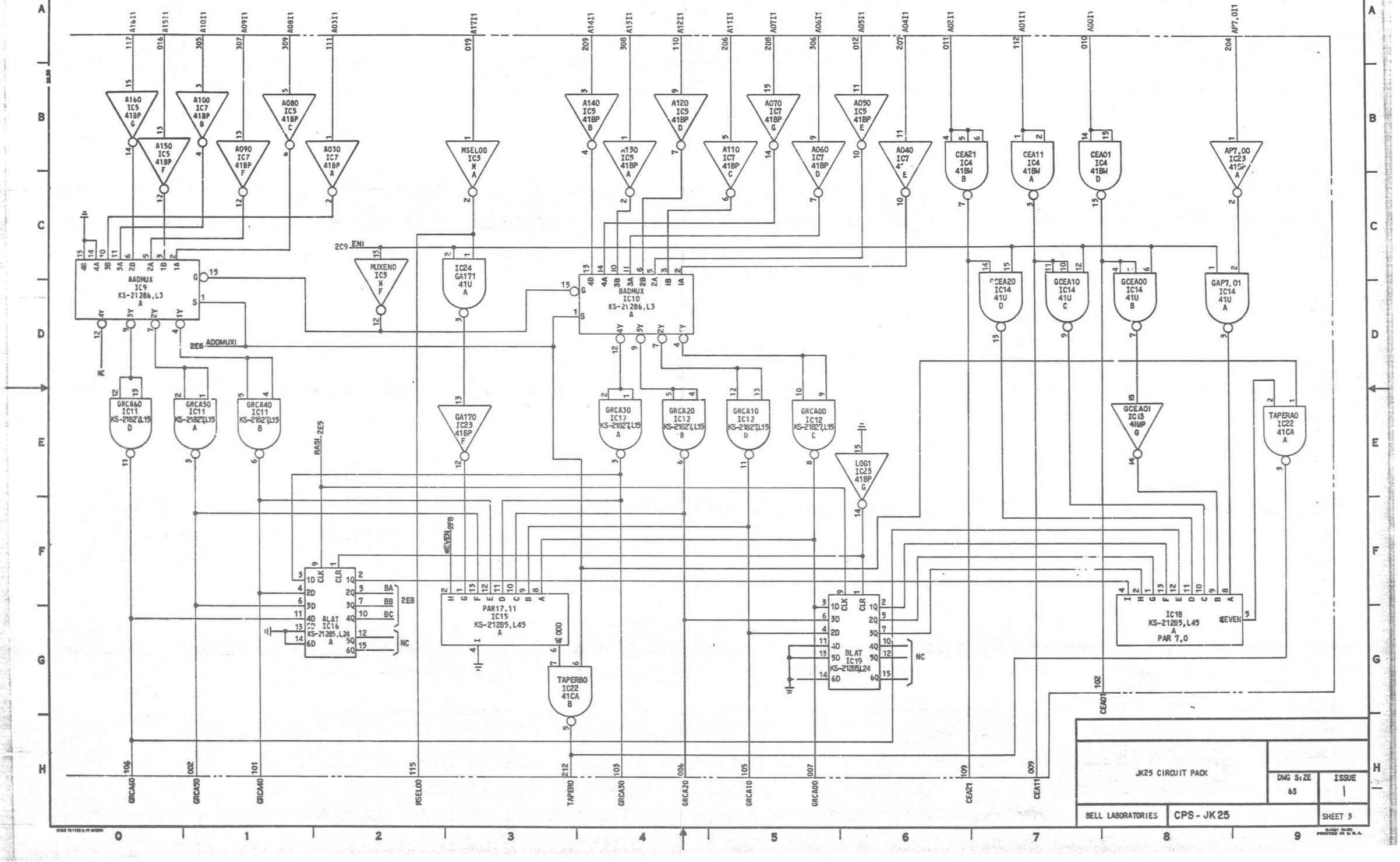
1. % DENOTES KS-21688,L3.

JK25 CIRCUIT PACK	DWG SIZE 65 / ISSUE —
BELL LABORATORIES	CPS-JK25 / SHEET 2

PART OF CPS JK 25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

NOTES:
1. * DENOTES KS-21688,L3.



JK25 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS - JK25		SHEET 3

PART OF CPS JK25

FAN OUT BOARD
(16K MEM DEV/MUX/DELAY)

COMPONENT LIST

INTEGRATED CIRCUIT

LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7		IC8		IC9		IC10		IC11		IC12		IC13		LOC
CODE	KS-21827,L15		KS-21827,L15		KS-21686,L3		41BW		41BP		KS-22038,L1		41BP		KS-22038,L1		KS-21286,L3		KS-21286,L3		KS-21827,L15		KS-21827,L15		41BP		CODE
ELEM																											ELEM
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	ID
A	REFO	2C4		2B7	MSELO0	3B3	CEA11	3B7	A130	3B4			A030	3B2			AADMUX1	2D5	BADMUX	3D4	GRCA50	3E1	GRCA30	3E4	GRW1	2E1	A
B	GRWO	2D0		2B7	RAS1	2C4	CEA21	3B7	A140	3B4			A100	3B1			AADMUX	3D0			GRCA40	3E1	GRCA20	3E4	GRAS1	2F5	B
C		2B8	EN1	2C2	RW1	2B0		2B1	A080	3B1			A110	3B5								2B9	GRCA00	3E5	REFCK1	2C4	C
D	GCAS0	2E6	GRAS0	2E4	REF1	2B3	CEA01	3B8	A120	3B4			A060	3B5							GRCA60	3D0	GRCA10	3E5		2B6	D
E					MENO	2B2			A050	3B6			A040	3B6												2B6	E
F					MUXEN0	3C2			A150	3B0			A090	3B1											CLKEN1	2E2	F
G									A160	3B0			A070	3B5											GCEA01	3E8	G

LOC	IC14		IC15		IC16		IC17		IC18		IC19		IC20		IC21		IC22		IC23		IC24		LOC
CODE	41U		KS-21285,L45		KS-21285,L24		41U		KS-21285,L45		KS-21285,L24		KS-21285,L45		41CA		41CA		41BP		41U		CODE
ELEM																							ELEM
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	ID
A	GAP7.01	3E9	PAR17.11	3G3	ALAT	3F2	CLKEN0	2D2	PAR7.0	3G8	BLAT	3G6	PAR10.8	2E7	MSELO	2D1	TAPERA0	3E9	AP7.00	3B9	GA171	3D9	A
B	GCEA00	3E8					RSEL0	2F3							RSEL1	2G3	TAPERB0	3G3	AP17.80	2C8	GP17.81	2D8	B
C	GCEA10	3E7					GRC1	2F5							SELRW0	2F1	UNSELER0	2G5	TS10	2C7		2B8	C
D	GCEA20	3E7					GCAS1	2F5								2B8	SELRC0	2G5		2B5	TSORME	2D7	D
E																				2B5			E
F																			GA170	3E3			F
G																			LOG1	3E6			G

CAPACITOR

DESIG	CODE
[24] C1-C24	KS-21901,L1 .1
[4] C25-C28	601A 5

TABLE 1

WIRE FANOUT BOARD TERMINAL

MODULE	H5 TO
0	115
1	019

JK25 CIRCUIT PACK	DWG SIZE 6S	ISSUE
BELL LABORATORIES	CPS-JK25	SHEET 4

PART OF CPS JK25

CIRCUIT DESCRIPTION/TIMING

CIRCUIT DESCRIPTION

THE JK25 FAN-OUT-BOARD (FOB) IS USED AS AN ADDRESS AND CONTROL SIGNAL BUFFER BETWEEN A MEMORY CONTROLLER AND A MODULE OF MEMORY PLANES. A MODULE OF MEMORY PLANES THAT USE 16K RAMS IS DEFINED AS 128K WORDS. IN ADDITION, CONTROL MONITOR OUTPUTS ARE PROVIDED TO PERMIT VERIFICATION OF CIRCUIT OPERATION. ALL INPUTS AND OUTPUTS ARE +5 VOLT TTL COMPATIBLE.

THE 16K DYNAMIC MEMORY DEVICE REQUIRES A 14-BIT MULTIPLEXED ADDRESS AND TWO CLOCK PULSES TO ACHIEVE PROPER OPERATION. THE TIMING RELATIONSHIPS BETWEEN THE CLOCKS AND ADDRESSES CAN BE FOUND ON SHEET 5. THE JK25 CIRCUITRY MULTIPLEXES ADDRESS BITS A03I1 THROUGH A16I1 AND DRIVES THIS MULTIPLEXED INFORMATION TO THE MEMORY PLANES ON NETS GRCA00 THROUGH GRCA60. THE FIRST SEVEN ADDRESS BITS THAT ARE GATED THROUGH THE FOB ARE THE ROW ADDRESS BITS AND THE SECOND SEVEN ADDRESS BITS ARE THE COLUMN ADDRESS BITS. SINCE THE ADDRESSES ARE VALID ONLY FOR CERTAIN PORTIONS OF THE CYCLE, REGISTERS ARE PROVIDED TO LATCH THE ADDRESSES THAT ARE SENT TO THE MEMORY PLANES UNTIL A PARITY CHECK CAN BE PERFORMED ON THEM.

THE JK25 ADDRESS BUFFER CIRCUITRY IS CHECKED FOR ODD PARITY OVER A00I1 THROUGH A07I1 AND AP7.0I1, AND FOR ODD PARITY OVER A08I1 THROUGH A17I1 AND A17.8I1. AN ADDRESS PARITY ERROR IS INDICATED BY A LOW LEVEL ON OUTPUT TAPER0.

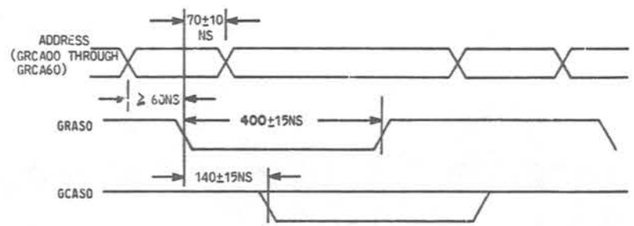
AS SHOWN IN TABLE 1, THE JK25 IS ENABLED BY HARDWIRING EITHER SIGNAL MSEL00 OR A17I1 TO DECODING GATE MEN0. THE PRESENCE OF THE MODULE ENABLE SIGNAL, GATE EN1 HIGH, FORCES OPEN COLLECTOR OUTPUT MSEL0 TO THE LOW STATE. ALL INPUT ADDRESS BITS EXCEPT THE THREE LEAST SIGNIFICANT BITS (A00I1 THROUGH A02I1) ARE GATED THROUGH THE JK25 BY ENABLE GATE EN1. IN THE SELECTED STATE GATE MUXEN0 ENABLES THE MULTIPLEXORS AND ALLOWS ADDRESS BITS A03I1 THROUGH A16I1 TO BE MULTIPLEXED. THESE ADDRESS BITS ARE INVERTED AND APPEAR AT OUTPUTS GRCA00 THROUGH GRCA60. IN THE UNSELECTED CONDITION, THE GATED ADDRESS OUTPUTS ARE FORCED TO THE LOW STATE. THE UNGATED ADDRESS BITS, A00I1 THROUGH A02I1 ARE INVERTED AND APPEAR AT OUTPUTS CEA01 THROUGH CEA21, RESPECTIVELY, REGARDLESS OF THE STATE OF EN1.

TWO 70ns DELAY LINES PROVIDE THE TIMING RELATIONSHIPS BETWEEN THE ADDRESS MULTIPLEXING AND THE SECOND CLOCK PULSE (GCAS0) AND ALSO PROVIDES A GATING INPUT TO THE ADDRESS PARITY ERROR GATES (TAPERA0, TAPERB0).

SEVERAL MEMORY CONTROL SIGNALS ARE BUFFERED AND GATED THROUGH THE JK25. WHEN SELECTED, OUTPUT GRW0 FOLLOWS INPUT RW10. IN THE UNSELECTED CONDITION, GRW0 IS FORCED TO A HIGH-LEVEL STATE. OPEN COLLECTOR OUTPUT SELRW0 IS PROVIDED TO MONITOR THE STATE OF OUTPUT GRW0. INPUT RAS10 AND THE MODULE ENABLE SIGNAL CONTROL GRASC. GCAS0 IS CONTROLLED BY THE MODULE ENABLE SIGNAL, EN1, THE REFRESH ENABLE GATE, REF0, AND THE INPUT PULSE FROM THE DELAY LINE, CASDEL1. GCAS0 IS INACTIVE DURING ALL REFRESH CYCLES. OPEN COLLECTOR OUTPUT SELRC0 IS PROVIDED TO MONITOR THE STATES OF OUTPUTS GRAS0 AND CCAS0. IN ADDITION, OUTPUT UNSELER0 IS PROVIDED AND ASSUMES A LOW STATE IF EITHER GRAS0 OR GCAS0 BECOMES ACTIVE (LOW) WHILE THE JK25 IS IN THE UNSELECTED STATE, THUS INDICATING AN ERROR. MAINTENANCE INPUT TS1I1 IS PROVIDED TO TEST THE INTEGRITY OF THIS GATING PATH.

REFRESH CONTROL INPUT RFFI0 IS PROVIDED TO FORCE JK25 TO THE ENABLED STATE INDEPENDENT OF ADDRESS BIT A17I1. A NONINVERTED REPLICA OF REFI0 APPEARS AT OUTPUT REF0. A HIGH LEVEL AT OPEN COLLECTOR OUTPUT RSEL1 INDICATES THE PRESENCE OF THE REFRESH STATE, THE REF0 OUTPUT ACTIVE (LOW), AND THE GCAS0 OUTPUT INACTIVE (HIGH).

JK25 TIMING EXAMPLE



JK25 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-JK25		SHEET 5