SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISSUE
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SYMBOL

SERIAL PERIPHERAL INTERFACE A CLEMENT IDENT. A

TERM. MOD	FUNCT	TERM.	LOC
B000	I	004	2A9
B010	I	009	2A8
B020	I	105	2A7
B030	I	007	2A6
B040	I	309	2A6
B050	I	300	2A5
B060	I	107	2A5
B070	I	008	2A5
B080	I	014	2A3
B090	I	005	2A3
B100	I	201	2A2
B110	I	308	2A2
B120	I	003	2A1
B130	I	103	2A1
B140	I	102	2A1
B150	I	002	2A0
BPH0	I	104	2A0
BPL0	I	108	2A4
GINF0	I	106	2A4
GP0	I	202	3A6
GPR0	I	101	3A5
INTP0	I	302	3A4
RSHP0A	I	100	3A1
SPER1	I	006	2A9
BSD1	B	001	3G2
INF000	B	215	2G9
INF010	B	314	2G8
INF020	B	211	2G7
INF030	B	310	2G6
INF040	B	116	2G6
INF050	B	214	2G5
INF060	B	205	2G5
INF070	B	304	2G5
INF080	B	206	2G3
INF090	B	305	2G3
INF100	B	010	2G2
INF110	B	109	2G2
INF120	B	207	2G1
INF130	B	307	2G1
INF140	B	312	2G1
INF150	B	212	2G0
INFPH0	B	203	2G0
INFPL0	B	301	2G4
MYINTAN	B	219	3G5
MYINTAP	B	318	3G4
MYINTBN	B	218	3G6
MYINTBP	B	317	3G5
PTOR0	B	019	3G1
RSETD1	B	217	3G2
+5	P	000,019	3G6
GRD	G	200,319	3G6

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 405mA

NOTES:

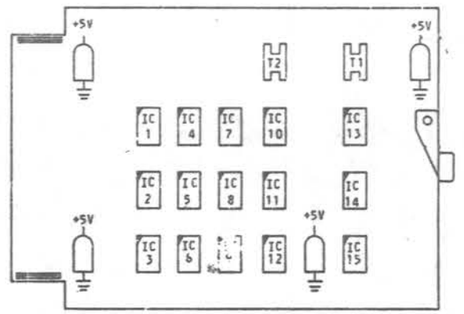
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41BP	16	8
41CA	16	8
41CC	16	7,8
41DE	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.5 INCH.
6. INTEGRATED CIRCUIT AND TRANSFORMER LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

DWG ISSUE	EE OR CD ISSUED	DATE ISSUE	DRAWN	APPD
1	—	10-7-74	LRE	RWF
			LRE	MTS
			PJS	RFG
2D1	—	12-8-75		CE
			LRE	LEG
				RFG
3D1	—	7-20-77	TJW	WJZ
			DKO	RKE
				JBD

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK5
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE)	1
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

ISSUE 3D1

1N98

JK5 CIRCUIT PACK

SERIAL PERIPHERAL INTERFACE A CIRCUIT

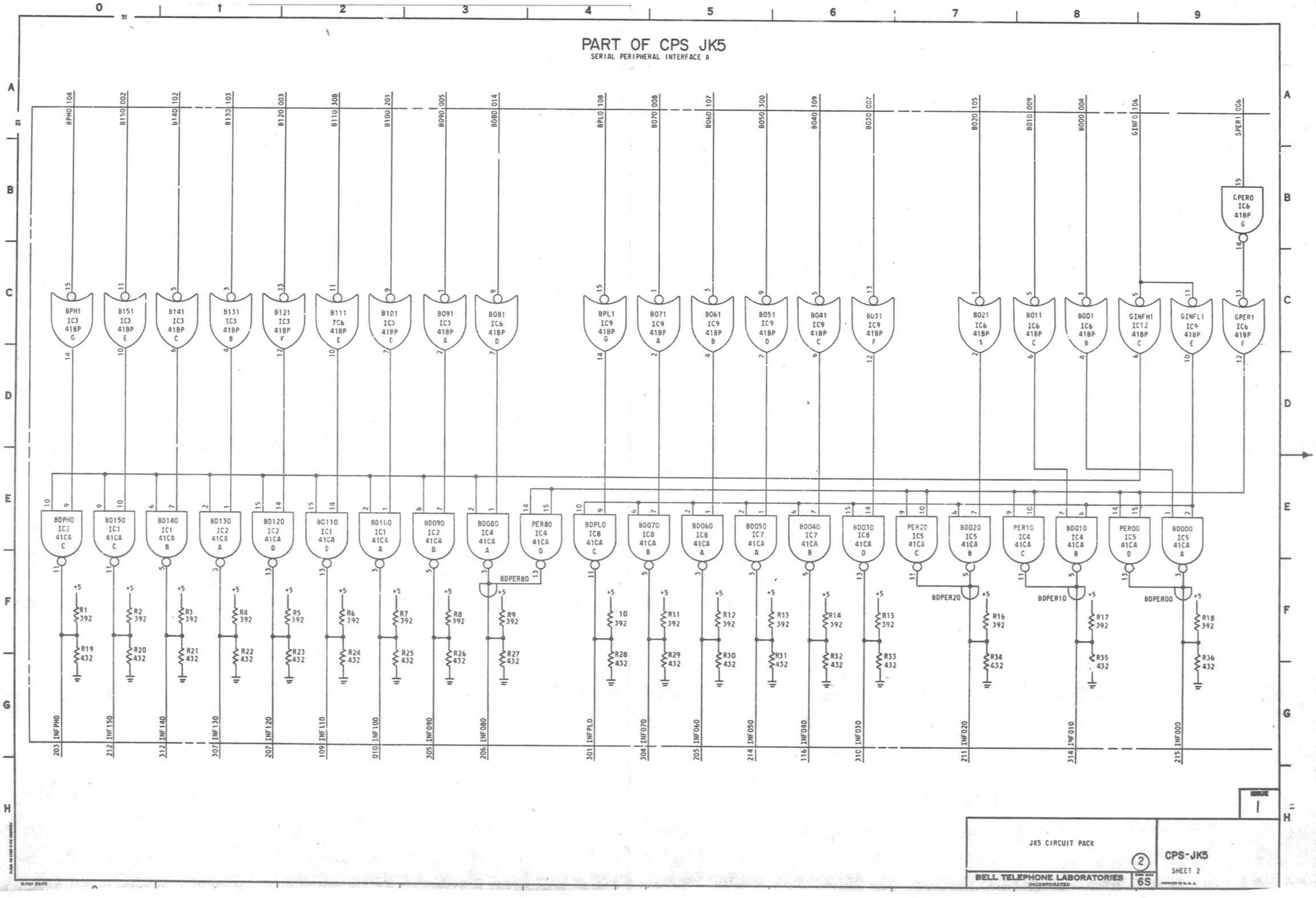
AT&TCO STANDARD

(2) CPS-JK5 4 SHEETS

BELL TELEPHONE LABORATORIES INCORPORATED 6S

PART OF CPS JK5

SERIAL PERIPHERAL INTERFACE A



ISSUE 1

JK5 CIRCUIT PACK

(2)

BELL TELEPHONE LABORATORIES INCORPORATED

6S

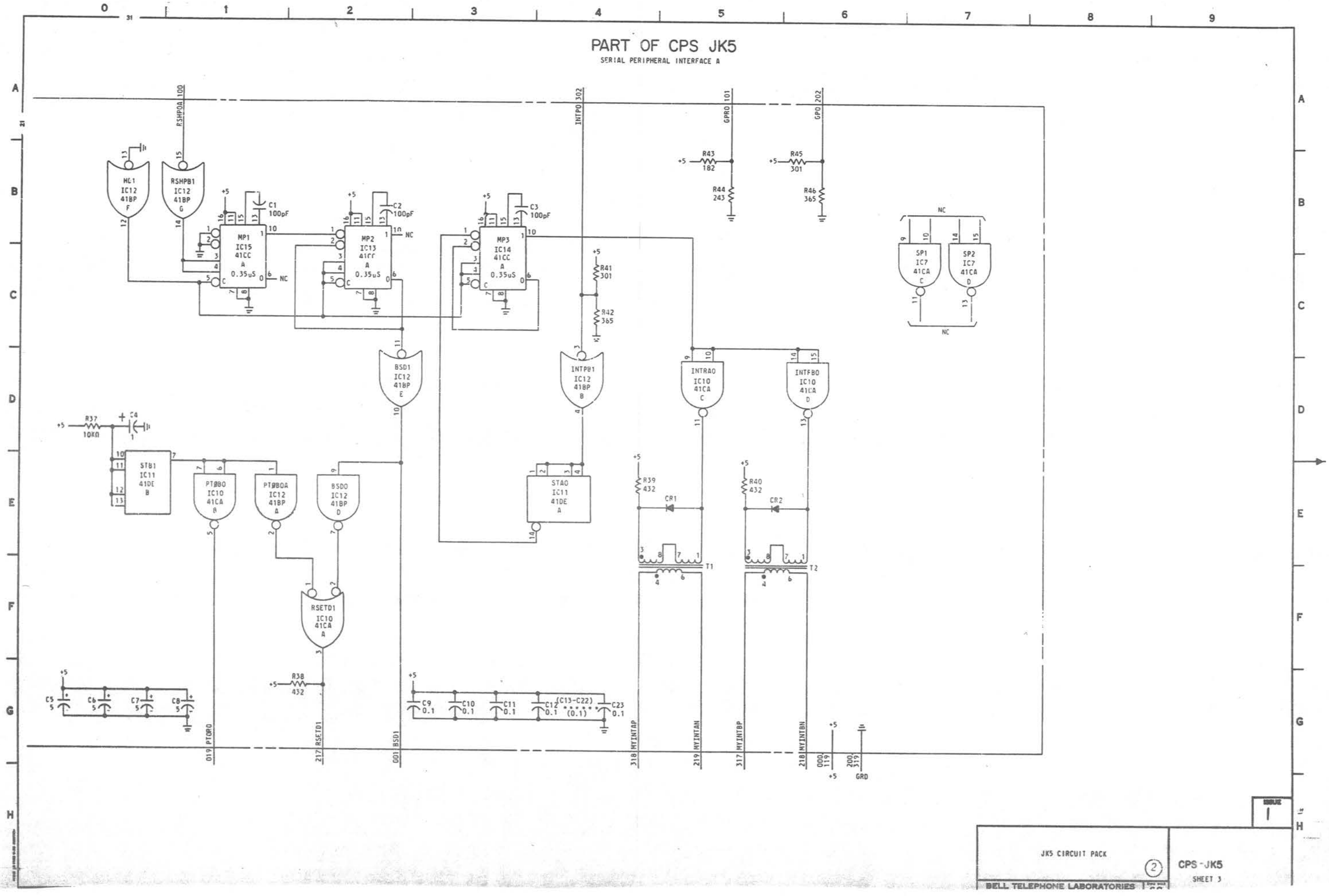
CPS-JK5

SHEET 2

CPS-JK5

PART OF CPS JK5

SERIAL PERIPHERAL INTERFACE A



JK5 CIRCUIT PACK	(2)	CPS-JK5	ISSUE 1
BELL TELEPHONE LABORATORIES		SHEET 3	

CPS-JK5

PART OF CPS JK5

SERIAL PERIPHERAL INTEPFACE A

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41CA DESIG	SH LOC	IC2 41CA DESIG	SH LOC	IC3 41BF DESIG	SH LOC	IC4 41CA DESIG	SH LOC	IC5 41CA DESIG	SH LOC	IC6 41BP DESIG	SH LOC	IC7 41CA DESIG	SH LOC	IC8 41CA DESIG	SH LOC	IC9 41BP DESIG	SH LOC	IC10 41CA DESIG	SH LOC	IC11 41DE DESIG	SH LOC
A	BD100	2E2	BD130	2E1	B091	2C3	BD080	2E3	BD000	2E9	B021	2C7	BD050	2E5	BD060	2E5	B071	2C5	RSETD1	3F2	STA0	3E4
B	BD140	2E1	BD090	2E3	B131	2C1	BD010	2E8	BD020	2E7	B001	2C8	BD040	2E6	BD070	2E4	B061	2C5	PTØB0	3E1	STB1	3E0
C	BD150	2E0	BDPH0	2E0	B141	2C1	PER10	2E7	PER20	2E7	B011	2C8	SP1	3C7	BDPL0	2E4	B041	2C6	INTRA0	3D5		
D	BD110	2E2	BD120	2E1	B101	2C2	PER80	2E4	PER00	2E8	B081	2C3	SP2	3C7	BD030	2E6	B051	2C5	INTRB0	3D6		
E					B151	2C0					B111	2C2					GINFL1	2C9				
F					B121	2C1					GPER1	2C9					B031	2C6				
G					BPH1	2C0					GPER0	2B9					BPL1	2C4				

LOC CODE ELEM ID	IC12 41BP DESIG	SH LOC	IC13 41CC DESIG	SH LOC	IC14 41CC DESIG	SH LOC	IC15 41CC DESIG	SH LOC
A	PTØB0A	3E1	MP2	3C2	MP3	3C3	MP1	3C1
B	INTPB1	3D4						
C	GINFH1	2C8						
D	BSD0	3E2						
E	BSD1	3D2						
F	HD1	3B0						
G	RSHPB1	3B1						

CAPACITOR

DESIG	CODE
C1-C3	~~KS-19256 L32~~, 100PF KS-20640 L3
C4	600A, 1
C5-C8	601A, 5
C9-C23	KS-19774 L5, 0.1

DIODE

DESIG	CODE
CR1, CR2	458C

RESISTOR

DESIG	CODE
R1-R18	KS-20616 L1A, 392
R19-R36	,432
R37	,10KΩ
R38-R40	,432
R41	,301
R42	,365
R43	,182
R44	,243
R45	,301
R46	KS-20616 L1A, 365

TRANSFORMER

DESIG	CODE
[2] T*, T2	2664G

CIRCUIT DESCRIPTIØN:

THIS CIRCUIT PACK CØNTAINS 18 BUFFER RECEIVERS AND 18 ØPEN CØLLECTØR BUS DRIVERS FØR THE 18 INFØRMATIØN LEADS. TRANSMISSIØN LINE TERMINATIØNS ARE PRØVIDED BY RESISTIVE VØLTAGE DIVIDERS FØR EACH ØF THE INFØRMATIØN LEADS. LEAD GINFO BEING LØW GATES THE BUS DRIVERS ØN.

LEAD SPER1 BEING HIGH GATES LEADS INF000, INF010, INF020, AND INF080 TØ GRØUND LEVEL. THIS BIT CØNFIGURATIØN IS THE PARITY ERRØR REPLY MESSAGE.

THE 50% DUTY CYCLE PULSE TRAIN ØN LEAD RSHPOA DRIVES THE RETRIGGERABLE MØNØPULSER MP1. THE LEADING EDGE ØF THE FIRST PULSE SETS THE "1" ØUTPUT ØF MP1 HIGH. WHEN THE INCØMING PULSE TRAIN IS INTEPRUPTED BY ABØUT 350 MSEC THE ØUTPUT ØF MP1 RETURNS TØ GRØUND LEVEL. THIS GRØUND GØING TRANSITIØN TRIGGERS MP2 TØ GENERATE A 350 MSEC WIDE RESET PULSE ØN LEADS BSD1 AND RSETD1.

TWØ CABLE DRIVERS CAN BE USED TØ TRANSMIT DEMAND INTERRUPT PULSES TØ BØTH CC'S. THESE PULSES ARE GENERATED BY HIGH TØ LØW TRANSITIØNS ØN LEAD INTPO.

THE RC NETWØRK (R37,C4) AT THE INPUT ØF SCHMITT TRIGGER STB1 CREATES AN EXPØNENTIAL VØLTAGE RISE AS THE +5V PØWER IS APPLIED TØ THE CIRCUIT. AS LØNG AS THE CAPACITØR VØLTAGE IS BELØW THE INPUT THRESHØLD LEVEL ØF STB1, THE ØUTPUT ØF STB1 IS HIGH. THIS HIGH LEVEL KEEPS THE RSETD1 LINE ACTIVE. THE SPI CØNTRØL LØGIC IS INITIALIZED BY THIS HIGH LEVEL.

ISSUE 3D1

JK5 CIRCUIT PACK (2) CPS-JK5 SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED 6S

CPS-JK5