

DWG NO.	DATE ISSUED	ISSUED BY	APPROVED BY
1	10-2-74	LRE	RWF
2B1	7-19-76	P/S	CE
3D1	2-24-78	LRE	LEG
4B1	2-24-78	TJW	CE
		DKO	JBC
		GC	TLB
			M6

SHEET INDEX		
CONTENTS	SHEET NO.	SHEET ISSUE
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- NOTES:
- GROUND RETURN
 - UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE 1/4 VOLTS

RECORD OF CHANGES				
DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE
3D1	NONE	Z		

IC CODE	BAT. TERM.	GRD TERM.
41AA	16	8
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41CF	16	7,8
41CG	16	8
41U	16	8

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

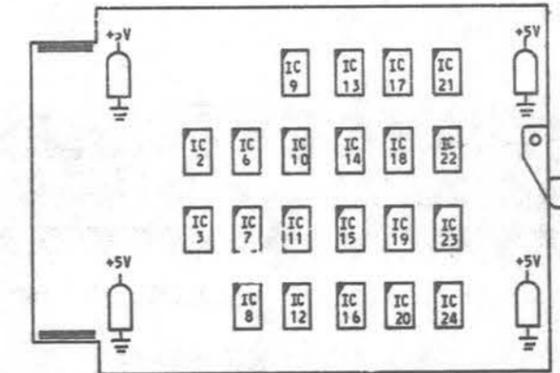
CURRENT DRAIN: 325mA

- BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:
- | FUNCTION | TERMINAL |
|----------|----------|
| +5 | 000,119 |
| GRD | 200,319 |
- HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

SYMBOL
SERIAL PERIPHERAL
INTERFACE C
ELEMENT IDENT

TERM. MOD.	FUNCT	TERM.	LOC
B000	I	202	2A3
B010	I	201	2A3
B020	I	300	2A2
B030	I	002	2A4
B040	I	101	2A3
B050	I	100	2A3
B120	I	301	2A1
B130	I	302	2A1
B140	I	001	2A1
B150	I	203	2A0
ERO	I	117	3A7
RSET1	I	014	3A8
RSETD1	I	113	3A5
RSHPOA	I	111	2A5
SCB10	I	010	2A5
SCB20	I	102	2A4
SPE1	I	018	2A7
STPBO	I	118	2A8
SYNCO	I	303	2A5
WA10	I	104	2A7
101ST0	Ø	019	2H8
ACK10	Ø	003	2H1
CLK	Ø	103	2H6
GINFO	Ø	013	3H3
HDA1	Ø	204	2H6
HDB1	Ø	304	2H5
INIT0	Ø	318	2H1
PLIØØ0	Ø	112	3H2
RC0	Ø	216	2H4
RDO	Ø	007	2H5
SD0	Ø	011	2H0
SPER1	Ø	114	2H9
SST0	Ø	217	2H1
STRTR1	Ø	110	3H6
+5	P	000,119	3H3
GRD	G	200,319	3H3

6. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



SUPPORTING INFORMATION	
CATEGORY	NO.
CIRCUIT PACK CODE	JK7
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.)	
ACCEPTABLE SERIES	1,2

- SHEET INDEX NOTES
- WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
 - THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
 - THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
 - SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
 - THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

ISSUE 4B1

1W98

AT&TCO STANDARD

JK7 CIRCUIT PACK
SERIAL PERIPHERAL INTERFACE C CIRCUIT

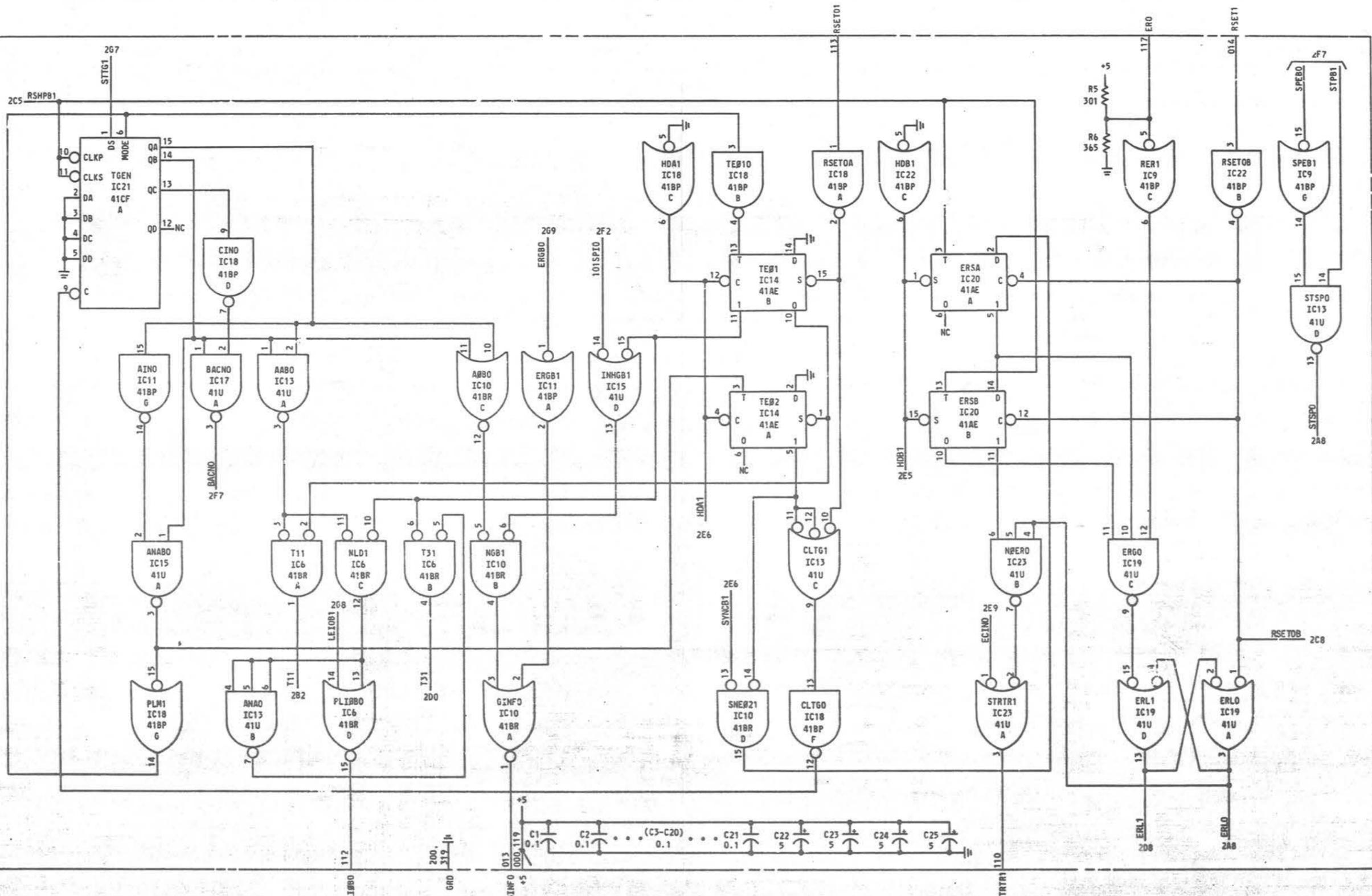
2

CPS-JK7
4 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF CPS JK7
SERIAL PERIPHERAL INTERFACE C



CPS-JK7

2B1

PART OF CPS JK7
SERIAL PERIPHERAL INTERFACE C

COMPONENT LIST
INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC2 41CA		IC3 41CA		IC6 41BR		IC7 41CG		IC8 41BP		IC9 41BP		IC10 41BR		IC11 41BP		IC12 41AA		IC13 41U		IC14 41AE	
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC										
A	RDO	2G5	SSTO	2D1	T11	3E2	C0MR	2C1	B14B1	2B0	SYNCO1	2B6	GINFO	3F3	ERGB1	3D3	7DVO	2C3	AABO	3D2	TE02	3D5
B	RCO	2G4	INITO	2C1	T31	3E3			B13B1	2B1	WTB1	2B7	NGB1	3E3	SCBB11	2B5	7NA20	2D4	ANAO	3F1	TE01	3C5
C	SPI5Y0	2G3	S00	2D0	NLD1	3E2			B12B1	2B1	RER1	3B7	ABO0	3D3	7DV1	2D3			CLTG1	3L5		
D	CLKD	2G6	ACKIO	2D1	PL10B0	3F2			B02B1	2B3	WTB0	2C7	SNE021	3F5	101SPI1	2F3			STSP0	3C9		
E									B01B1	2B3	SPEB0	2C7			SCBB21	2C4						
F									B00B1	2B3	STPB1	2C8			7NA21	2F4						
G									B15B1	2B0	SPEB1	3B8			A1NO	3D1						

LOC CODE ELEM ID	IC15 41U		IC16 41AE		IC17 41U		IC18 41BP		IC19 41U		IC20 41AE		IC21 41CF		IC22 41BP		IC23 41U		IC24 41CF			
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC		
A	ANABO	3E1	CHD4	2E6	BACND	3D1	RSET0A	3B5	ERL0	3F8	ERSA	3C6	TGEN	3B1	ESPER1	2F9	STRTR1	3F6	ERTCH	2C9		
B	SCBB10	2D5	CHD2	2F6	WTB01	2D7	TEB10	3B5	ERGB	2E9	ERSB	3D6			RSET0B	3B8	NB0RO	3E6				
C	101SPI0	2E3			STTGO	2E7	HDA1	3B4	ERGO	3E7					HDB1	3B6	EERT1	2B8				
D	INHGB1	3D4			STTG1	2F7	C1NO	3C1	ERL1	3F7					LEI0B1	2F8	ANBNO	2E8				
E							RSHPB1	2B5							B1NO	2D8						
F							CLTGO	3F5							EC1NO	2D9						
G							PLM1	3F1							101CT0	2E8						

CAPACITOR

DESIG	CODE
[21] C1-C21	KS-21901 L2
[4] C22-C25	601A,5

RESISTOR

DESIG	CODE
[2] R1,R2	KS-20616 L11,301
[2] R3,R4	.365
R5	.301
R6	KS-20616 L1A,365

CIRCUIT DESCRIPTION:

THE JK7 CIRCUIT PACK PROVIDES MOST OF THE CONTROL FUNCTIONS OF THE SERIAL PERIPHERAL INTERFACE (SPI) UNIT. THESE FUNCTIONS INCLUDE THE SUPERVISION OF THE I0B SHIFT REGISTER (ON JK6) WHICH RECEIVES OR TRANSMITS 21-BIT MESSAGES ON A SERIAL CHANNEL OF THE 3A CC. JK7 ALSO CONTROLS HANDSHAKING WITH PERIPHERAL UNITS RESIDING ON THE COMMON PARALLEL BUS DERIVED FROM THE I0B PARALLEL OUTPUTS.

COMMAND INFORMATION FROM THE 3A CC IS BROUGHT TO JK7 IN PARALLEL ON THREE GROUPS OF I0B OUTPUT LEADS: THE START CODE GROUP (SCB10, SCB20), THE DEVICE CODE GROUP (B000 THROUGH B050), AND THE COMMAND GROUP (B120 THROUGH B150). THE APPEARANCE OF A 011 START CODE IN THE I0B OF JK6 ASSERTS PARALLEL BUS COMMAND LEAD RDO DURING PERIOD T1 OF THE JK7 TIMING SEQUENCE. IF THE SPI IS NOT ADDRESSED A 101 START CODE SIMILARLY ASSERTS RCO DURING T1. THE SPI IS ADDRESSED WHEN AN 000111 DEVICE CODE ACCOMPANIES A 101 START CODE DURING T1. THE 000111 DEVICE CODE IS DECODED BY 7DVO WHICH INHIBITS RCO. AN ADDRESSED SPI ASSERTS SYNCO DURING T1 AND CLOCKS THE COMMAND GROUP INFORMATION INTO THE COMMAND REGISTER (C0MR) ON THE TRAILING EDGE OF T1. A SET BIT IN C0MR ASSERTS THE CORRESPONDING COMMAND LEAD (S00, INITO, ACKIO, OR SSTO) DURING PERIOD T3. THE C0MR SST BIT IS NORMALLY IN THE SET STATE WHEN THE SPI IS NOT ADDRESSED.

THE SEQUENCING PERFORMED ON JK7 CAN BE PARTITIONED INTO THREE MAJOR SEGMENTS, NAMELY THE SEND ORDER (T1), GET REPLY (T3), AND ERROR SEQUENCES. T1 AND T3 ARE CONTROLLED BY TIMING GENERATOR TGEN WHILE ERTCH CONTROLS THE ERROR SEQUENCE. TGEN IS CLOCKED BY THE PULSE TRAIN APPEARING ON RSHPOA. RSHPOA IS DIVIDED BY TWO TO CLOCK ERTCH AND BY FOUR TO PRODUCE BUS CLOCK SIGNALS ON THE CLK LEAD. TGEN AND ERTCH NORMALLY IDLE IN THE CLEARED STATE AS DO F/Fs ERSB AND ERSB. THE TE01 AND TE02 F/Fs IDLE IN THE SET STATE.

CIRCUIT DESCRIPTION (CONT):

THE REGISTRATION OF A 21-BIT CC MESSAGE IN THE I0B ACTIVATES LEAD ST0PB0. IF SPE1 IS FALSE AT THIS TIME, NO SERIAL PARITY ERRORS ARE INDICATED AND STTGO DRIVES THE TGEN SERIAL INPUT HIGH TO BEGIN THE SEND ORDER SEQUENCE. TGEN STATE QcQbQa = 001 ASSERTS GINFO WHICH GATES THE I0B ONTO THE BUS. TGEN 011 ASSERTS T11 WHICH GATES RCO OR RDO ONTO THE BUS, DEPENDING ON THE RECEIVED START CODE. A 101 START CODE ACCOMPANIED BY THE SPI DEVICE CODE INHIBITS RCO AND GINFO, ASSERTS SYNCO VIA SPI5Y0, AND ENABLES THE COMMAND GROUP INPUTS OF C0MR. TGEN 111 CAUSES THE SEQUENCER TO SUSPEND FURTHER ACTION UNTIL SYNCO IS RETURNED IN RESPONSE TO THE COMMAND AND WAITO IS INACTIVE. BACND INSURES THAT TGEN REACHES 111 EVEN IF THE SYNC-WAIT CONDITION IS QUICKLY SATISFIED IN T1. WHEN SYNC-WAIT IS SATISFIED, STTGO IS FALSE AND THE TGEN SERIAL INPUT GOES LOW. THE TGEN 111 TO 110 TRANSITION CUTS OFF T11 AND LOADS C0MR. THE NEXT CLOCK PULSE CLEARS TGEN, CLEARS THE TE01 F/F, AND INHIBITS GINFO. TGEN MARKS TIME IN THE 000 STATE UNTIL SYNCO IS REMOVED.

THE NEGATION OF SYNCO DRIVES THE TGEN SERIAL INPUT HIGH ONCE MORE AND BEGINS THE GET REPLY SEQUENCE. TGEN 011 ASSERTS PLI0B0 AND T31, GATING C0MR ONTO THE BUS. TGEN HANGS UP IN STATE 111 UNTIL THE SYNC-WAIT CONDITION IS AGAIN SATISFIED. THE 111 TO 110 TRANSITION CUTS OFF T31 AND NEGATES PLI0B0, CLOCKING THE BUS INTO THE I0B. THE FOLLOWING CLOCK PULSE CLEARS TGEN AND THE TE02 F/F. THE SEQUENCER MARKS TIME UNTIL SYNCO IS REMOVED. THE NEGATION OF SYNCO CAUSES ERSB TO BECOME SET ON THE NEXT DOWNWARD TRANSITION OF RSHPOA. THE BUS DEVICE ERROR LEAD IS CHECKED AT THIS TIME AND THE ERROR F/F LATCHES IF ERO IS TRUE. THE NEXT DOWNWARD TRANSITION OF RSHPOA SETS ERSB. THE ABSENCE OF DEVICE ERRORS RESULTS IN THE ASSERTION OF STRTR1 WHICH STARTS THE RETURN OF A SERIAL MESSAGE TO THE PROCESSOR.

CIRCUIT DESCRIPTION (CONT):

THE ERROR SEQUENCE IS CALLED IN WHEN EITHER A SERIAL PARITY ERROR OR DEVICE ERROR OCCURS, BUT THE ACTION TAKEN IN EACH CASE DIFFERS SOMEWHAT. DEVICE ERRORS LATCH THE ERL F/F FOLLOWING THE GET REPLY SEQUENCE. STRTR1 IS TEMPORARILY INHIBITED WHILE EERT1 ASSERTS 101STO AND FORCES THE ERTCH SERIAL INPUT HIGH. ERTCH FIRST ACTIVATES PLI0B0 AND GINFO WHICH GATES THE I0B ONTO THE BUS. 101STO FORCES A 101 START CODE AS THE TRAILING EDGE OF PLI0B0 LOADS THE BUS BACK INTO THE I0B. ERTCH THEN ASSERTS STRTR1 TO COMPLETE THE SEQUENCE.

SERIAL PARITY ERRORS OCCUR JUST AS THE SERIAL MESSAGE FROM THE CC IS REGISTERED IN THE I0B. A SERIAL PARITY ERROR (SPE1-ST0PB0 TRUE) ASSERTS SPEA1 AND 101STO, STARTS THE ERROR SEQUENCE, AND 101STO PULSES PLI0B0 WHICH LOADS THE I0B WITH THE PARITY ERROR REPLY MESSAGE AND A 101 START CODE. ERTCH THEN ASSERTS STRTR1 TO COMPLETE THE SEQUENCE.

RSETD1 AND RSET1 ARE PULSED TO RETURN THE SEQUENCING ELEMENTS TO THEIR IDLE STATES ONCE THE CC RECEIVES THE REPLY MESSAGE.

CPS-JK7

ISSUE 4B1

JK7 CIRCUIT PACK		2	CPS-JK7 SHEET 4
BELL TELEPHONE LABORATORIES INCORPORATED			
		65	PRINTED IN U.S.A.