

PART OF CPS JK8
BUS TERMINATOR A CIRCUIT

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM	IC2 41BR		IC4 41BP		IC6 41AA		IC7 41CA		IC8 41AE		IC10 41U		IC11 41W		IC12 41AE		IC13 41BP		IC14 41BP		IC15 41U	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC												
A	SPO1	2C9	GPB1	2B5	NVC10	2B1	BTER0	2G0	DA	2C7	G0B1	2F9	CLKR1	2F3	DB	2E7	RCB1	2B2	AIO	2E4	A11	2D4
B	0A11	2B1	CLKB0	2B6	DVCO0	2C0	BTSYNO	2G3	AIDA	2D6	I001	2D0	SPO4	2E9	AIDR	2E6	R0B1	2B2	ACKB0	2C4	BTR00	2D2
C	2A31	2B0	GP61	2D9			SPO2	2B9			BTER1	2F0	BTSYN1	2F2			INTB1	2B4	INTB0	2C4	ENG01	2D3
D	5A41	2B0	GP60	2E9			SPO3	2C9			BTRC0	2C2	CLKR0	2G3			ACKB1	2B4	SSTB0	2C3	BTSST0	2D3
E			STRD0	2B8													SSTB1	2B3	SDB0	2C3		
F			CLKB1	2C6													SDB1	2B3	AIER0	2F2		
G			GP80	2C5													SPO5	2F9	SPO6	2E9		

LOC CODE ELEM	IC16 41U		IC18 41AE		IC19 41CA		IC20 41AE	
ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	AICLK0	2F6	BTAD	2E0	GPRO	2F6	STD	2C8
B	ETO	2E4	SPO7	2F9	BTWTO	2F7	SPI0	2G9
C	ET1	2E5			SPO8	2D9		
D	ETCH1	2G4			SPO9	2D9		
E								
F								
G								

CAPACITOR

DESIG	CODE
[15] C1-C15	KS-19774 L5.0.1
[4] C16-C19	601A,5

RESISTOR

DESIG	CODE
[6] R1-R6	KS-20616 L1A,182
R7	301
R8	182
[11] R9-R19	392
[6] R20-R25	243
R26	365
R27	243
[11] R28-R38	432
R39	1K0
[6] R40-R45	301
[6] R46-R51	365

CIRCUIT DESCRIPTION

THIS CIRCUIT PACK IS PART OF THE BUS TERMINATOR DEVICE. HANDSHAKING AND CONTROL LOGIC FOR THE PARALLEL HOLDING REGISTER ON JK9 IS PROVIDED. FAR-END TERMINATING RESISTORS FOR THE PARALLEL BUS COMMAND LEADS AND THE SERIAL BUS LEADS ARE ALSO PROVIDED.

THE BUS TERMINATOR ADDRESS FF (BTAD) BECOMES SET AT THE LEADING EDGE OF RCO AND IF I001 THROUGH I0051 ARE ALL ONE'S OR ALL ZERO'S. RCB1 AND I001 ASSERT SYNC0 AND CLKR0. SYNC0 AND CLKR0 REMAIN LOW UNTIL RCO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RCO, THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER ON JK9.

A LOW LEVEL ON RDO AND FF BTAD BEING SET ASSERTS SYNC0 AND CLKR0. SYNC0 REMAINS LOW UNTIL RDO RETURNS TO A HIGH LEVEL. AT THE TRAILING EDGE OF RDO, THE STATE OF THE INFORMATION LEADS IS CLOCKED INTO THE REGISTER ON JK9.

A LOW LEVEL ON SST0 AND FF BTAD BEING SET ASSERTS SYNC0 AND G0B1. G0B1 GATES THE OUTPUTS OF THE REGISTER ON JK9 ON THE INFORMATION LEADS.

COMMAND INPUTS INIT0 OR ACKI0 ASSERT SYNC0. WAIT0 IS ASSERTED BY ETCH1. FFS AIDA, AND GATE AICLK0 GENERATE A CLOCK PULSE ON CLKR0. THE TRAILING EDGE OF THIS PULSE CLOCKS THE STATE OF THE INFORMATION LEADS INTO THE REGISTER ON JK9. THE TRAILING EDGE OF CLKR1 TOGGLES FF STD ENABLING THE TIMING CHAIN, FFS DA AND DB TO ASSERT GPRO AND G0B1. WHEN FF DB BECOMES SET WAIT0 IS NEGATED. GPRO, G0B1, AND SYNC0 REMAIN TRUE UNTIL INIT0 OR ACKI0 RETURN TO A HIGH LEVEL.

A PULSE ON THE GPO LEAD, WHILE SST0 OR SDO IS LOW, ENABLES THE TIMING CHAIN STD, DA, AND DB. THE LEADING EDGE OF GPO ASSERTS WAIT0. AT THE TRAILING EDGE OF GPO, THE PARALLEL REGISTER ON JK9 IS CLOCKED VIA CLKR0 AND FF STD IS TOGGLED. THE NEXT TRANSITION OF THE CLOCK TOGGLES FF DA. THE ONE OUT-PUT OF FF DA ASSERTS GPRO AND ENABLES THE OUTPUTS OF THE REGISTER ON JK9 VIA G0B1. THE NEXT TRANSITION OF THE INVERTED CLOCK (CLKB1) TOGGLES FF DB AND WAIT0 IS NEGATED. G0B1 AND GPRO REMAIN TRUE UNTIL SST0 OR SDO RETURN TO A HIGH LEVEL.

CPS-JK8

2D1

JK8 CIRCUIT PACK		2	CPS-JK8 SHEET 3
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