SHEET INDEX

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SYMBOL
SERIAL PERIPHERAL INTERFACE
B CIRCUIT
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM	LOC
CLKRO	I	009	2A2
G0B1	I	102	2A1
INF PHO	0	203	2H2
INF PLO	0	301	2H6
I6001	0	117	2C9
I6011	0	017	2C9
I6021	0	018	2C9
I6031	0	118	2C9
I6041	0	013	2C9
I6051	0	113	2C9
INF 000	0I	315	2H9
INF 010	0I	314	2H8
INF 020	0I	211	2H8
INF 030	0I	310	2H8
INF 040	0I	116	2H7
INF 050	0I	214	2H7
INF 060	0I	205	2H7
INF 070	0I	304	2H6
INF 080	0I	206	2H6
INF 090	0I	305	2H4
INF 100	0I	010	2H4
INF 110	0I	109	2H3
INF 120	0I	207	2H3
INF 130	0I	307	2H3
INF 140	0I	312	2H2
INF 150	0I	212	2H2
+5	P	000,119	2H0
GRD	G	200,319	2H0

RECORD OF CHANGES

DWG ISS	PREV FORM	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 470mA

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK9
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE (ANY HIGHER SERIES IS ACCEPTABLE)	
ACCEPTABLE SERIES	1

NOTES:

1. ⏚ GROUND RETURN

2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS)
   OR −(MINUS) ARE IN VOLTS

3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT TERM.	GRD TERM.
41BP	16	8
41CA	16	8
41CG	16	8
41DA	16	7,8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN)

UNMARKED COMPONENTS ARE FILTER CAPACITORS

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.

2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.

3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.

4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.

5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

DWG. ISSUE	CD ISSUE	DATE ISSUED		
1	—	10-2-74	LRE LRE	RWF MTS RFG
2DI	—	12-8-75	P/S LRE	AAN LEG RFG

ISSUE 2DI

IH98

JK9 CIRCUIT PACK

BUS TERMINATOR B CIRCUIT

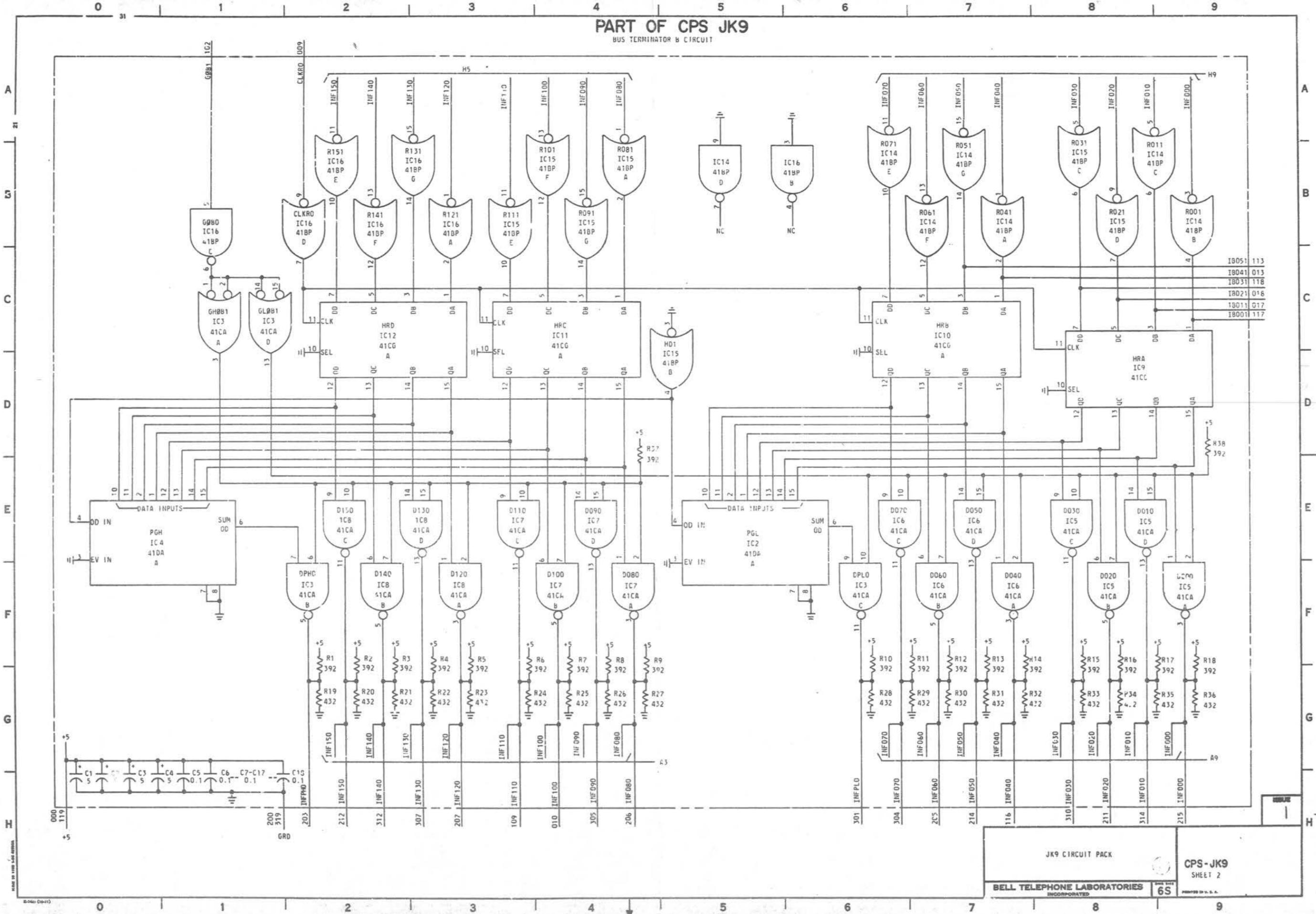AT&TCO STANDARD

② CPS-JK9
3 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

PART OF CPS JK9
BUS TERMINATOR B CIRCUIT

CPS-JK9

JK9 CIRCUIT PACK

CPS-JK9
SHEET 2

BELL TELEPHONE LABORATORIES
INCORPORATED

ISSUE
1

COMPONENT LIST
INTEGRATED CIRCUIT

LOC	IC2 41DA		IC3 41CA		IC4 41DA		IC5 41CA		IC6 41CA		IC7 41CA		IC8 41CA	
CODE														
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	PGL	2E5	GH0B1	2C1	FGH	2E1	D00	2F9	D040	2F7	D080	2F4	D120	2F3
B			0PH0	2F2			D020	2F8	D060	2F7	D100	2F4	D140	2F2
C			0PL0	2F6			D030	2E8	D070	2E6	D110	2E3	D150	2F2
D			GL0B1	2C1			D010	2E8	D050	2E7	D090	2F4	D130	2F3
E														
F														
G														

LOC	IC9 41CG		IC10 41CG		IC11 41CG		IC12 41CG		IC14 41BP		IC15 41BP		IC16 41BP	
CODE														
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	HRA	2C8	HRB	2C7	HRC	2C4	HRD	2C2	RO41	2B7	RO81	2B4	R121	2B3
B									RO01	2B9	HD1	2D5	SPARE	2B6
C									RO11	2B8	RO31	2B8	G0B0	2B1
D									SPARE	2B5	RO21	2B8	CLKRO	2B2
E									RO71	2B6	R111	2B3	R151	2B2
F									RO61	2B7	R101	2B4	R141	2B2
G									RO51	2B7	RO91	2B4	R131	2B3

CAPACITOR

DESIG	CODE
C1-C4	601A,5
C5-C18	KS-19774 L5, 0.1

RESISTOR

DESIG	CODE
R1-R18	KS-20616 L1A, 392
R19-R36	KS-20616 L1A, 432
R37	KS-20616 L1A, 392
R38	K-20616 L1A, 392

CIRCUIT DESCRIPTION

BUS TERMINATOR 8 CIRCUIT

THIS CIRCUIT PACK CONTAINS A 16 BIT HOLDING REGISTER. THE 16 OUTPUTS OF THE REGISTER FEED INTO TWO 8-BIT PARITY TREES. THE OUTPUT OF EACH OF THE PARITY TREES IS A ONE WHENEVER THERE ARE AN ODD NUMBER OF ONES PRESENT AT THE INPUTS. THE STATES OF THE 16 INFORMATION LEADS INFO00 INF15C ARE CLOCKED INTO THE HOLDING REGISTER AT THE TRAILING EDGE OF A GROUND GOING PULSE ON CLOCKLINE CLKRO. THE CONTENTS OF THE REGISTER AND THE ASSOCIATED PARITY BITS CAN BE GATED ONTO THE INFORMATION LEADS BY SETTING LEAD G0B1 TO A LOGICAL ONE.

TRANSMISSION LINE TERMINATIONS ARE PROVIDED BY THE RESISTIVE VOLTAGE DEVIDERS FOR EACH OF THE 18 INFORMATION BUS LEADS. THE 41CA'S ARE OPEN COLLECTOR BUS DRIVERS. THE 6 LEAST SIGNIFICANT BITS OF THE INFORMATION LEADS ARE INVERTED AND CONNECT TO JK8 FOR THE PURPOSE OF DEVICE DECODING.

ISSUE 1

JK9 CIRCUIT PACK

CPS-JK9
SHEET 3

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