SHEET INDEX

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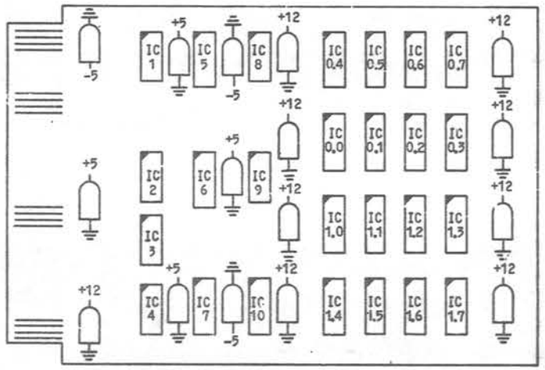
SYMBOL

TERM.MOD.	FUNCT	TERM	LOC
CASIO	I	014	2F0
CEAOI1	I	202	2D0
CEA1I1	I	009	2C0
CEA2I1	I	209	2B0
RASIO	I	003	2E0
RCA0IO	I	007	2H0
RCA1IO	I	205	2G0
RCA2IO	I	006	2G0
RCA3IO	I	203	2G0
RCA4IO	I	201	2C0
RCA5IO	I	002	2F0
RCA6IG	I	206	2F0
RFFIO	I	208	2E0
RWIO	I	001	2H0
WRTD0IO	I	218	2A8
WRTD1IO	I	216	2A9
RDDOO	O	217	2G9
RDD1O	O	212	2G9
-5	P	019	3A0
+5	P	011	3D0
+5	P	211	3B0
+12	P	000	3G0
GRD	G	00D	3C0
GRD	G	004	2F6
GRD	G	005	2F6
GRD	G	008	2F6
GRD	G	2GD	3C0
GRD	G	200	3G0
GRD	G	204	2F6
GRD	G	207	2F6
GRD	G	213	3B0
GRD	G	215	3B0
GRD	G	217	3B0
GRD	G	219	3B0

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

4. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.

2. POWER AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	GRD TERM.	-5 TERM.	+5 TERM.	+12 TERM.
28A	16	1	9	8
41BP	8		16	
41CD	8		16	
41U	8		16	
KS-21814,L1	7		14	
KS-21827,L14	7		14	

3. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
-5	019
+5	011,211
+12	000
GRD	00D, 2GD, 004, 005, 008, 200, 204, 207, 213, 215, 217, 219

4. CURRENT DRAINS ASSUMING TIMING SHOWN ON SHEET 5:

SUPPLY	VOLTAGE	CURRENT
VDD	+12V±0.1	70mA
VBB	-5V±0.1	2mA
VCC	+5V±0.1	230mA

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	3-2-78	NA-TAB TLB	MM JOB MG

SUPPORTING INFORMATION

CATEGORY	NUMBER
CONNECTOR ON FRAME CIRCUIT PACK INFORMATION DRAWING	947A OR 947C
SERIES FOR LATEST CLASS "A" CHANGE	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

IN98

JL16 CIRCUIT PACK

128K X 2 BIT MEMORY PLANE CIRCUIT

AT&TCO STANDARD

DWG SIZE	ISSUE
6S	1

BELL LABORATORIES | CPS-JL16 | 5 SHEETS

8282-070476

PRINTED IN U.S.A.

PART OF CPS JL16

128K X 2 BIT MEMORY PLANE

RASDC0D IC7 41CD

R9 14.7KΩ — CEA2I1 209 — pin 13 C
R10 14.7KΩ — CEA1I1 009 — pin 14 B
R12 14.7KΩ — CEA0I1 202 — pin 15 A
R11 14.7KΩ — REFI0 208 — REFEN1 IC10 41BP E — REFEN0 IC10 41BP D

"9" NC
"8" NC
"7" RAS71 IC5 41U B — RAS70 IC8 X B
"6" RAS61 IC5 41U C — RAS60 IC8 X C
"5" RAS51 IC5 41U D — RAS50 IC8 X D
"4" RAS41 IC5 41U A — RAS40 IC8 X A
"3" RAS31 IC6 41U D — RAS30 IC9 X D
"2" RAS21 IC6 41U A — RAS20 IC9 X A
"1" RAS11 IC6 41U B — RAS10 IC9 X B
"0" RAS01 IC6 41U C — RAS00 IC9 X C

RAS0 ICO.4 28A — W CAS A6 A5 A4 A3 A2 A1 A0 — 3 15 13 10 11 12 6 7 5 — F3 (SEE NOTE 1)
ICO.5 28A
ICO.6 28A
ICO.7 28A
ICO.0 28A
ICO.1 28A
ICO.2 28A
ICO.3 28A
IC1.0 28A
IC1.1 28A
IC1.2 28A
IC1.3 28A
IC1.4 28A
IC1.5 28A
IC1.6 28A
IC1.7 28A

WRTD10 — WRTD00 IC10 41BP G — WRTD10 IC10 41BS A — +5 — R4 2.15 KΩ — R3 5KΩ

CASEN1 F3 — RDD00 IC1 KS 21814, L1 D — RDD10 IC1 KS 21814, L1 A — R1 2.15KΩ — R2 5KΩ — RDD0C 214 — RDD10 212

RASI0 003 — R9 10KΩ — R6 1KΩ — RASEN1 IC2 X B
CASI0 014 — R13 10KΩ — R8 20.5KΩ — R7 20.5KΩ — CASEN1 IC2 X A — (SEE NOTE 4) — CASEN1 D9

(SEE NOTE 3)
CAS00 IC2 X C — TO PIN 15 ICO.0-ICO.7
CAS10 IC2 X D — TO PIN 15 IC1.0-IC1.7

RCA6I0 206 — AD61 IC3 X B — A6 — TO PIN 13
RCA5I0 002 — AD51 IC4 X D — A5 — TO PIN 10
RCA4I0 201 — AD41 IC4 X C — A4 — TO PIN 11
RCA3I0 203 — AD31 IC4 X A — A3 — TO PIN 12
RCA2I0 006 — AD21 IC3 X D — A2 — TO PIN 6
RCA1I0 205 — AD11 IC4 X B — A1 — TO PIN 7
RCA0I0 007 — AD01 IC3 X A — A0 — TO PIN 5
RWI0 001 — WRITE1 IC10 41BP B — WRITE0 IC5 X C — W — TO PIN 3

TO ALL MEMORY DIPS (SEE NOTE 1)

NOTES:

1. LEADS W, CAS, A6, A5, A4, A3, A2, A1, A0 SHOWN ON THE 28A AT LOC 2A4 ARE TYPICAL FOR ALL 28A DIPS.
2. X DENOTES THAT IC CODE IS KS-21827,L14.
3. THIS NET IS ROUTED FROM IC10 TO IC2 TO IC5 AND IC6.
4. THIS NET IS ROUTED FROM IC2 (CASEN1) TO IC1 (RDD00,RDD10) TO IC2 (CAS00,CAS10).

JL16 CIRCUIT PACK	DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-JL16	SHEET 2

PART OF CPS JL16

POWER/GROUND DISTRIBUTION

-5 019
+5 211 011
GRD 219 217 215 213
GRD 2GD 008 207 005 204 004
+12 000
GRD 200

IC1 KS-21814,L1
IC2 KS-21827,L14
IC3 KS-21827,L14
IC4 KS-21827,L14
IC5 41U
IC6 41U
IC7 41CD
IC8 KS-21827,L14
IC9 KS-21827,L14
IC10 41BP

IC0.0 28A
IC0.1 28A
IC0.2 28A
IC0.3 28A
IC0.4 28A
IC0.5 28A
IC0.6 28A
IC0.7 28A
IC1.0 28A
IC1.1 28A
IC1.2 28A
IC1.3 28A
IC1.4 28A
IC1.5 28A
IC1.6 28A
IC1.7 28A

C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74

IC1 KS 21814, L1 B
IC1 KS 21814, L1 C
NC

IC10 41BP C
IC10 41BP F
NC

JL16 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-JL16		SHEET 3

PART OF CPS JL16

128K X 2 BIT MEMORY PLANE

COMPONENT LIST

INTEGRATED CIRCUITS

LOC CODE ELEM ID	IC1 KS-21814,L1 DESIG	SH LOC	IC2 KS-21827,L14 DESIG	SH LOC	IC3 KS-21827,L14 DESIG	SH LOC	IC4 KS-21827,L14 DESIG	SH LOC	IC5 41U DESIG	SH LOC	IC6 41U DESIG	SH LOC	IC7 41CD DESIG	SH LOC	IC8 KS-21827,L14 DESIG	SH LOC	IC9 KS-21827,L14 DESIG	SH LOC	IC10 41BP DESIG	SH LOC	LOC CODE ELEM ID
A	RDD10	2E9	CASEN1	2F1	AD01	2H1	AD31	2G1	RAS41	2C2	RAS21	2D2	RASDCOD	2C1	RAS40	2C3	RAS20	2D3	WRTD10	2B8	A
B			RASEN1	2E1	AD61	2F1	AD11	2H1	RAS71	2B2	RAS11	2D2			RAS70	2B3	RAS10	2D3	WRITE1	2H1	B
C	RDD00	2D9	CASD0	2F3	WRITE0	2H1	AD41	2G1	RAS61	2B2	RAS01	2D2			RAS60	2B3	RAS00	2D3			C
D			CAS10	2F3	AD21	2G1	AD51	2F1	RAS51	2B2	RAS31	2C2			RAS50	2B3	RAS30	2C3	REFEN0	2E1	D
E																			REFEN1	2E1	E
F																					F
G																			WRTD00	2A8	G
H																					H

INTEGRATED CIRCUITS (CONT)

	DESIG	CODE
[8]	IC0.0-IC0.7	28A OR KS-21980,L1
[8]	IC1.0-IC1.7	28A OR KS-21980,L1

CAPACITOR

	DESIG	CODE
[5]	C1-C3	601A, 5
[4]	C4-C7	KS-21901 L1, 0.1
[2]	C8,C9	601A, 5
[3]	C10-C12	KS-21901 L1, 0.1
[3]	C13-C15	601A, 5.
[3]	C16-C18	KS-21901 L1, 0.1
[4]	C19-C22	601A, 5
[48]	C23-C70	KS-21901 L1, 0.1
[4]	C71-C74	601A, 5

RESISTOR

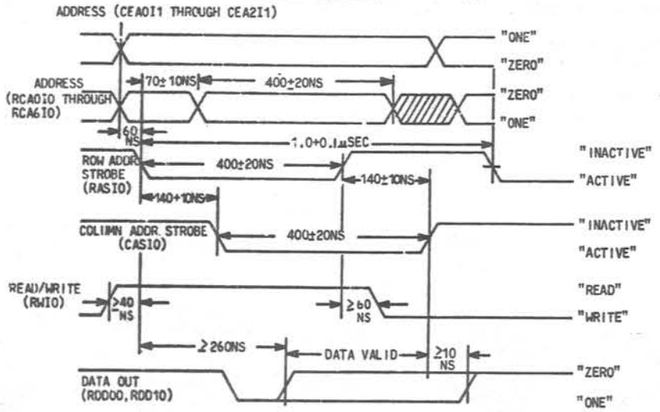
	DESIG	CODE
	R1	KS-20616 L1A, 2.15KΩ
[2]	R2,R3	KS-20616 L1A, 3KΩ
	R4	KS-20616 L1A, 2.15K
	R5	KS-20616 L1A, 10KΩ
	R6	KS-20616 L1A, 1KΩ
[2]	R7,R8	KS-20616 L1A, 20.5KΩ
[4]	R9-R12	KS-20616 L1A, 14.7KΩ
	R13	KS-20616 L1A, 10KΩ

JL16 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS - JL16		SHEET 4

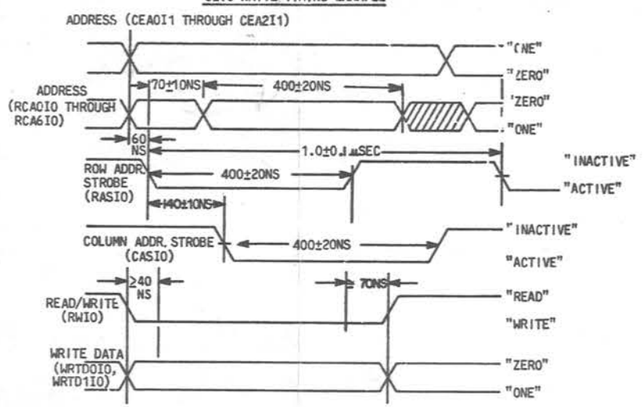
PART OF CPS JL16

CIRCUIT DESCRIPTION/TIMING

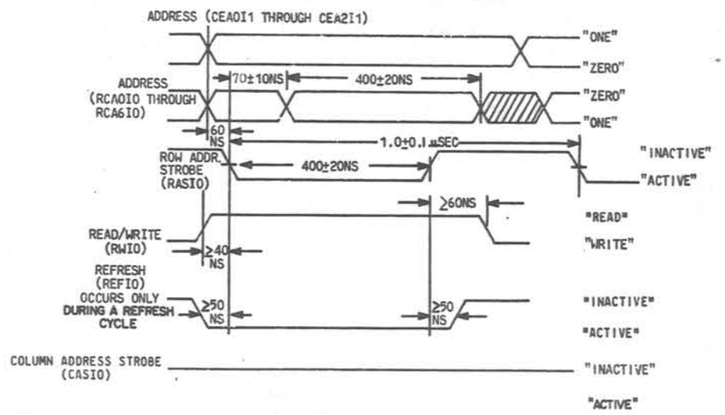
JL16 READ TIMING EXAMPLE



JL16 WRITE TIMING EXAMPLE



JL16 REFRESH TIMING EXAMPLE



CIRCUIT DESCRIPTION

THE JL16 MEMORY PLANE CONTA'NS RANDOM-ACCESS STORAGE ELEMENTS MADE UP OF 16K BY 1 BIT (K = 1024) INSULATED GATE FIELD EFFECT TRANSISTOR (IGFET) DUAL IN-LINE PACKAGES (DIPS) ARRANGED IN A 128K BY 2-BIT ARRAY. THE MEMORY IS VOLATILE, IN THAT THE STORED INFORMATION WILL BE LOST IF POWER IS INTERRUPTED, AND DYNAMIC, IN THAT THE STORED INFORMATION MUST BE REGENERATED (REFRESHED) AT SPECIFIED INTERVALS. IN ADDITION TO STORAGE ELEMENTS, THE MEMORY PLANE CONTAINS ADDRESS AND DATA BUFFERS, CONTROL LOGIC, DEVICE SELECT DECODERS. ALL INPUTS AND OUTPUTS ARE +5 V TTL COMPATIBLE.

ADDRESS BITS CEA0I1 THROUGH CEA2I1 ARE GATED BY ONE OF THE TIMING SIGNALS RASIO AND ARE USED TO SELECT 2-OF-16 MEMORY DIPS. THE 16K RAM REQUIRES 14 ADDRESS BITS WHICH ARE MULTIPLEXED TO THE MEMORY PLANE ON INPUTS GRCA00 THROUGH GRCA60. THESE SIGNALS ARE BUFFERED AND CONNECTED TO ALL MEMORY DIPS. A SECOND TIMING SIGNAL, CASIO, IS NECESSARY TO ACHIEVE PROPER OPERATION. THIS SIGNAL IS BUFFERED INTO TWO BRANCHES WHICH EACH DRIVE EIGHT DEVICES IN THE MEMORY ARRAY.

THE MEMORY PLANE IS PUT INTO THE "WRITE MODE" BY FORCING A LOW LEVEL ON RWIO. DATA IS WRITTEN FROM INPUTS WRTD0IO AND WRTD1IO DURING THE TIME WHEN BOTH RASIO AND CASIO ARE LOW.

DATA IS READ FROM THE MEMORY DEVICES WHEN RWIO IS HIGH AND BOTH RASIO AND CASIO ARE LOW. DATA IS THEN GATED TO OUTPUTS RDD00 AND RDD10. THE DATA OUT TRANSITIONS ARE SHOWN IN THE READ TIMING EXAMPLE, CASIO STAYS HIGH DURING REFRESH CYCLES.

EACH STORAGE CELL ON THE MEMORY PLANE MUST BE REFRESHED AT LEAST ONCE EVERY 4.4 ms, OR ELSE THE STORED CHARGE WILL LEAK OFF CAUSING THE DATA TO BE LOST. THIS REFRESH OPERATION CAN BE ACCOMPLISHED BY ENABLING THE RASIO INPUT IN THE SAME MANNER THAT IT IS PERFORMED DURING A READ CYCLE WHILE THE CASIO INPUT IS INHIBITED. THIS MUST BE PERFORMED FOR EACH OF THE 128 ROWS OF EACH OF THE MEMORY DIPS AT LEAST ONCE EVERY 4.4 ms. THE REFRESH OPERATION FOR THIS MEMORY PLANE CAN BE PERFORMED IN 128 CYCLES BY FORCING REFIO TO THE LOW STATE AND EXECUTING A CYCLE THAT ENABLES RASIO BUT INHIBITS CASIO AT EACH OF THE 128 STATES OF ADDRESS INPUTS RCA0IO THROUGH RCA6IO AT LEAST ONCE EVERY 4.4 ms.

JL16 CIRCUIT PACK	DWG SIZE 6S	ISSUE /
BELL LABORATORIES	CPS-JL16	SHEET 5