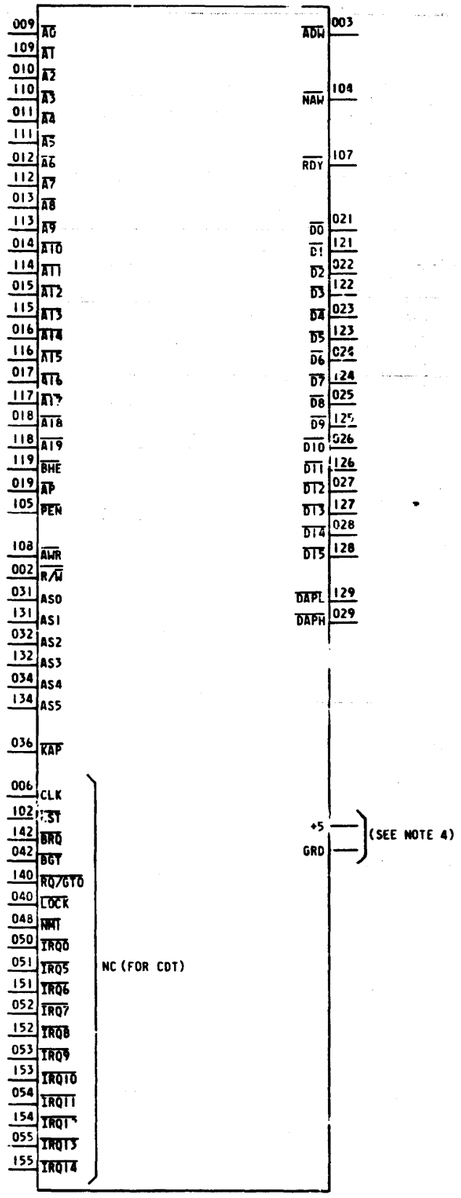
SHEET INDEX

CONTENTS	SHEET NO.	SHEET ISS NO.
SHEET INDEX RECORD OF CHANGES SUPPORTING INFORMATION SYSTEM USED ON SYMBOL NOTES	1	1
CPS SL65	2	1
	3	1
	4	1
	5	1
	6	1
	7	1
	8	1
	9	1
	10	1
	11	1
COMPONENT LIST INPUT/OUTPUT INFORMATION CIRCUIT DESCRIPTION	12	1

SYMBOL



RECORD OF CHANGES

DWG ISS	PREV FURN	STD.	MFR DISC	SEE NOTE

NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
2. ⏚ GROUND RETURN.
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS ARE:

IC CODE	BAT TERM +5V	GRD TERM
SN54LS368	16	8
SN54SL240	20	10
AM25SL2521		
SN54LS00	14	7
SN54LS38		
AM93S48DM	16	8
SN54LS280	14	7
SN54LS139	16	8
SN54LS85		
35A	19.20	10

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE:

FUNCTION	TERMINALS
+5	000,001,100,101
GRD	005,007,020,030, 033,035,037,039, 041,043,045,047, 049,056,103,106, 120,130,133,135, 137,139,141,143, 145,147,149,156

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	2-29-84	CDI DP	SS GWK RW

SYSTEM USED ON	DESIGN CONTROL
COMMON (CDT)	CB

SUPPORTING INFORMATION

CATEGORY	NO.
CONNECTOR ON FRAME	
CIRCUIT PACK SCHEMATIC DRAWING	SD-94868-01

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

1N99

SL65 CIRCUIT PACK

RANDOM ACCESS MEMORY

AT&TCO STANDARD

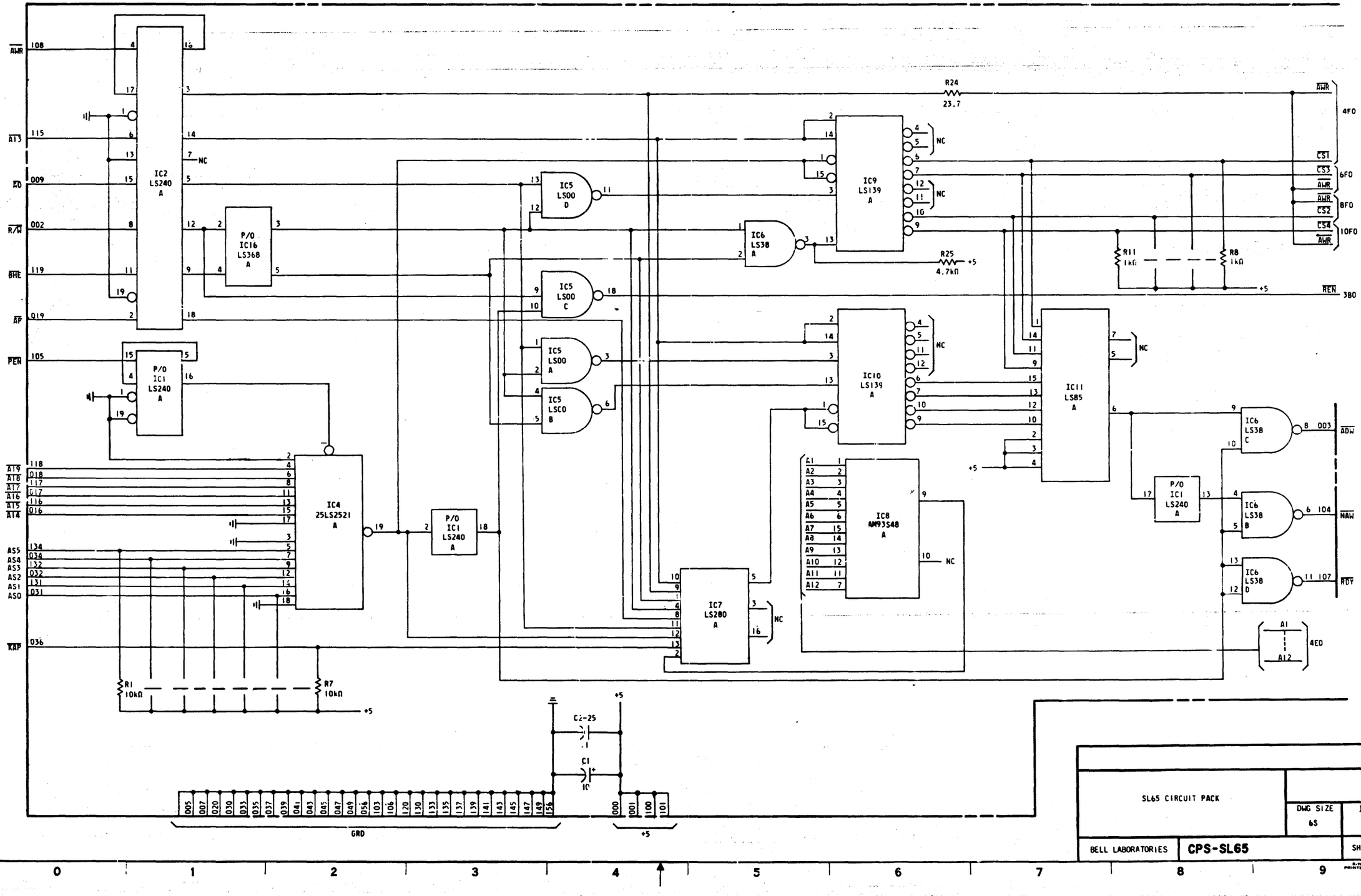
DWG SIZE 6S | ISSUE 1

BELL LABORATORIES | CPS-SL65 | 12 SHEETS

E-7000-A (6-79) PRINTED IN U.S.A.

PART OF CPS SL65

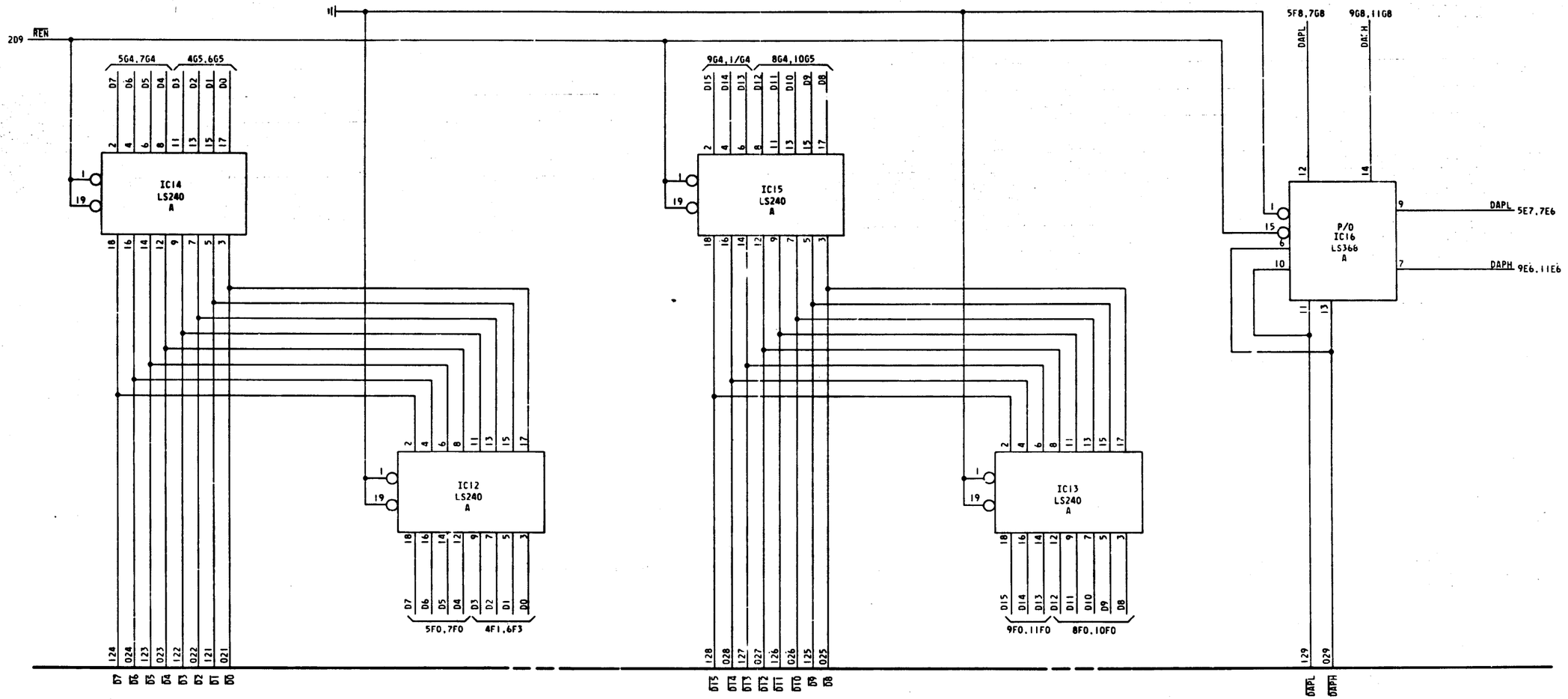
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 2

PART OF CPS SL65

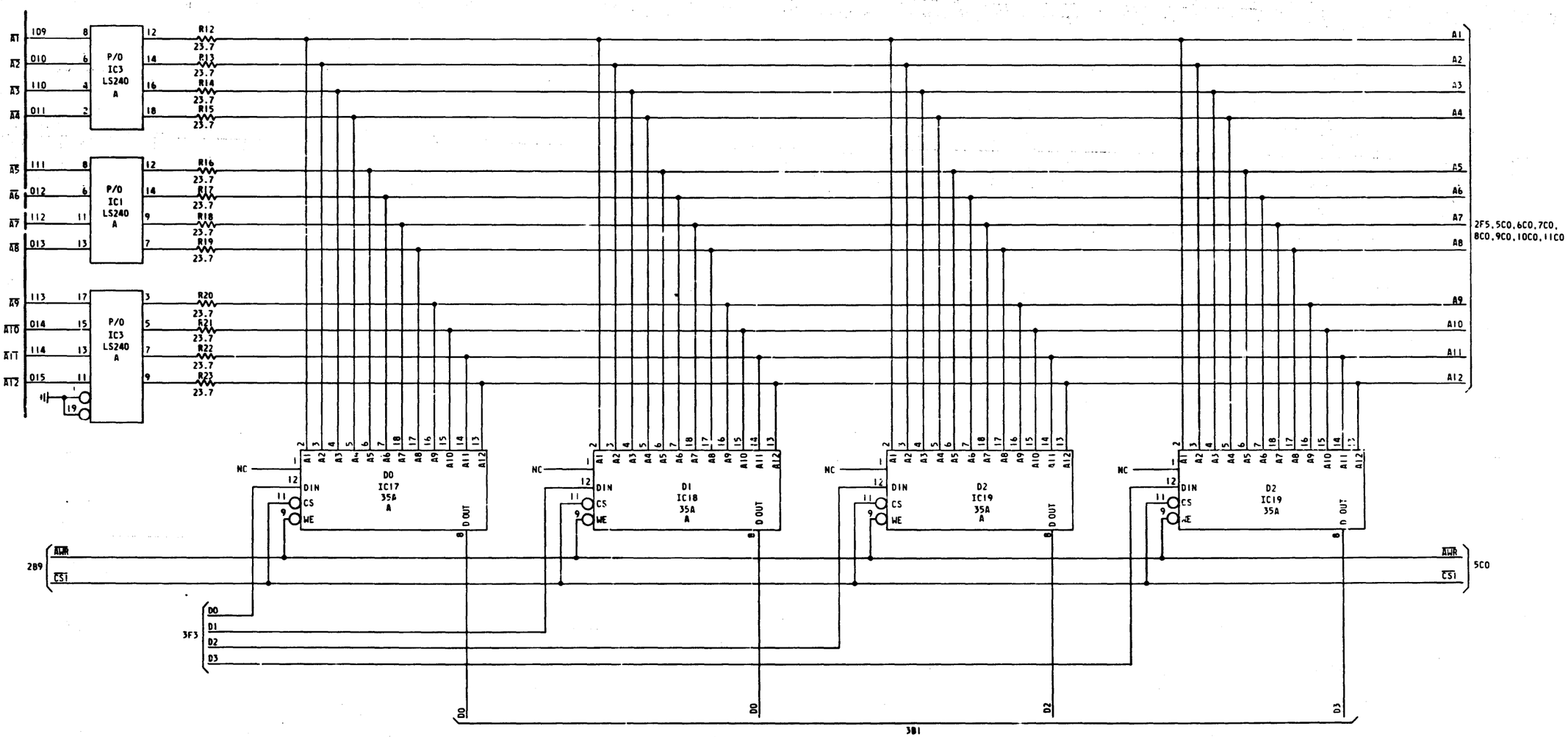
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 65	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 3

PART OF CPS SL65

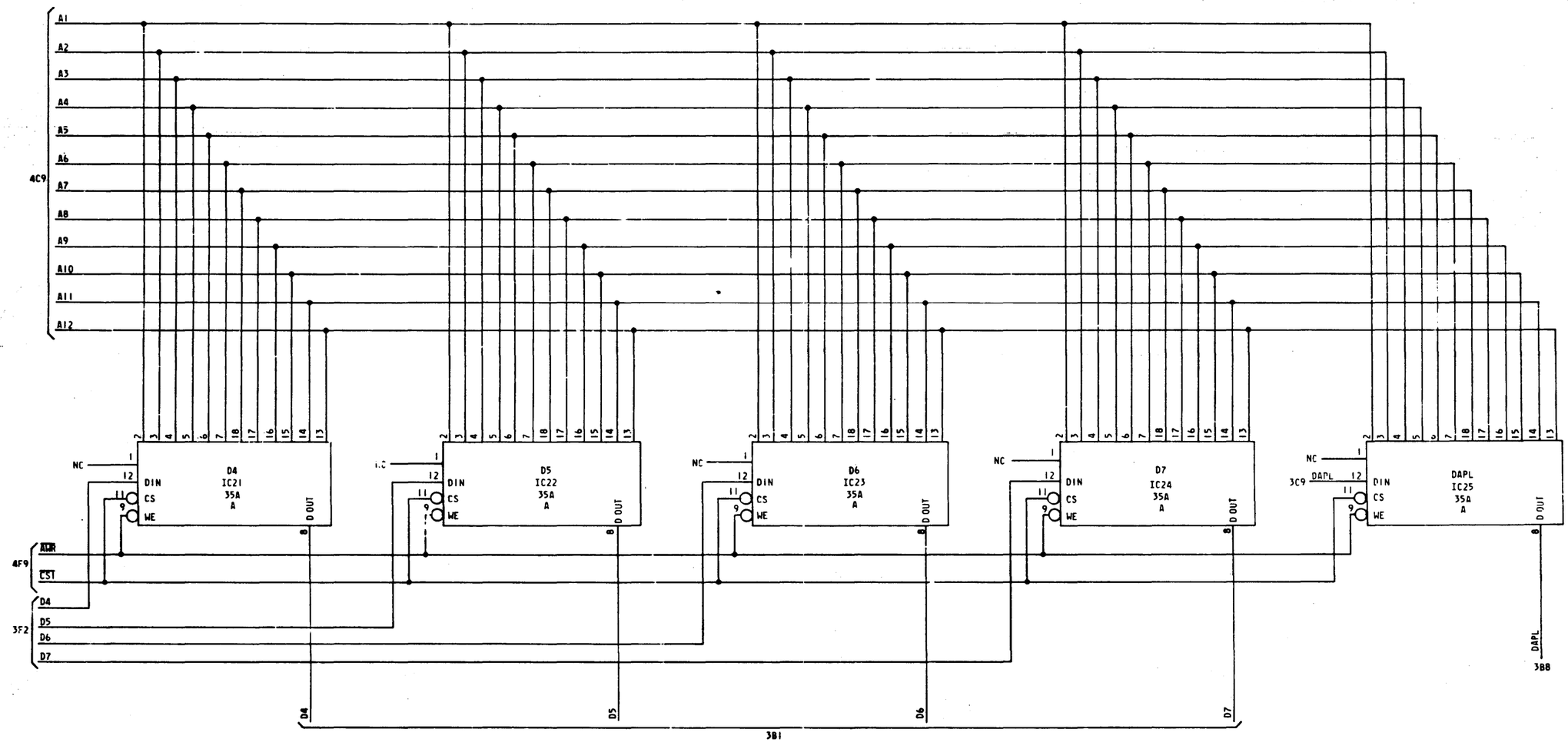
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 4

PART OF CPS SL65

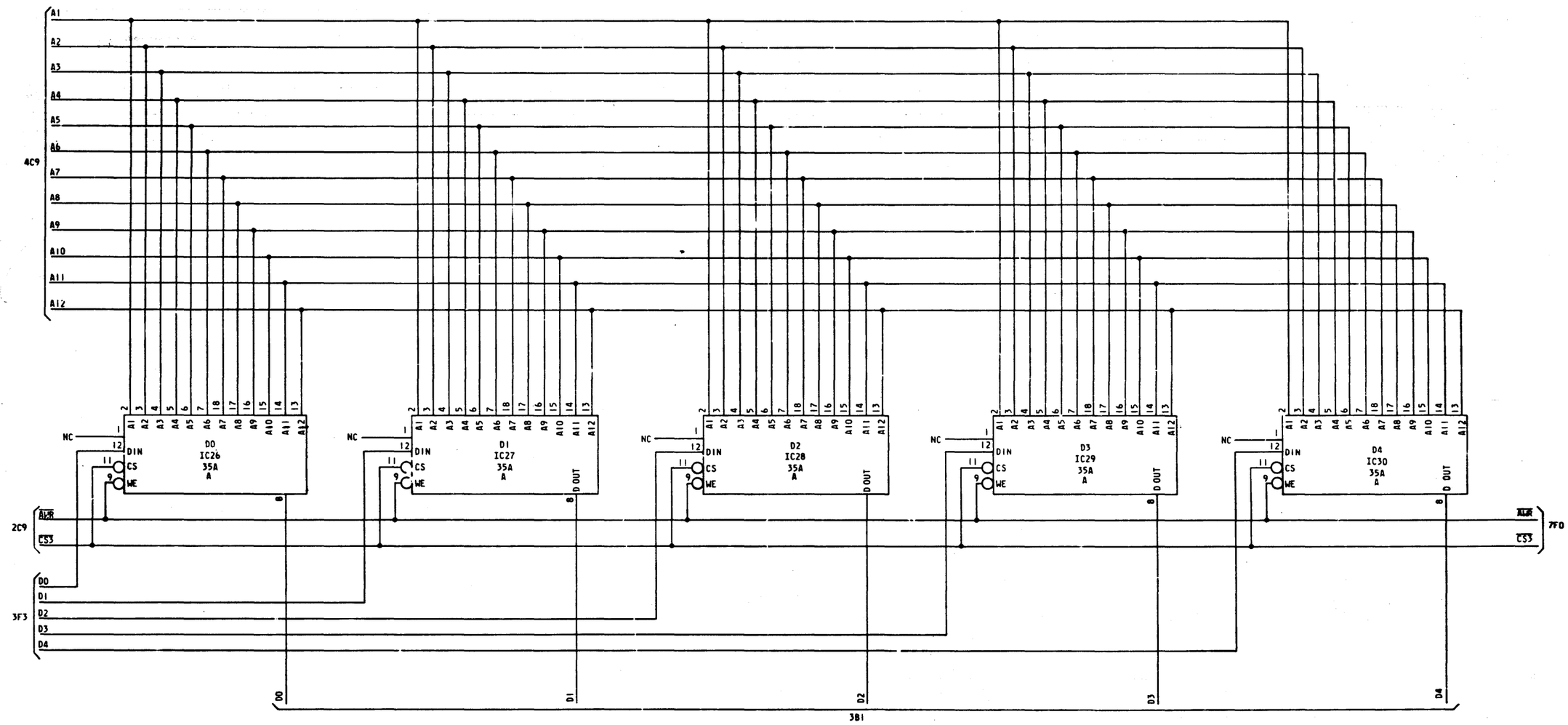
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 5

PART OF CPS SL65

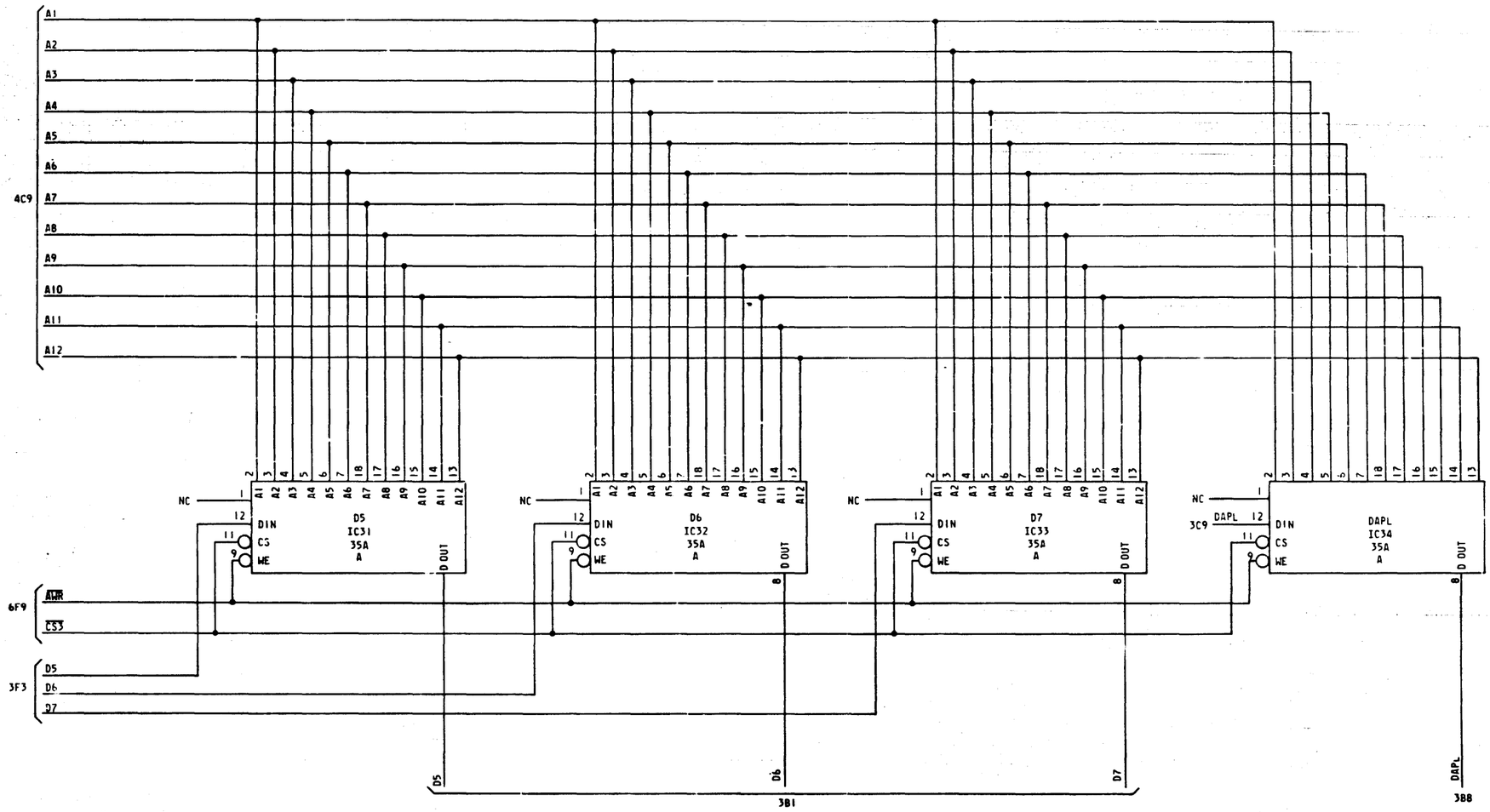
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 6

PART OF CPS SL65

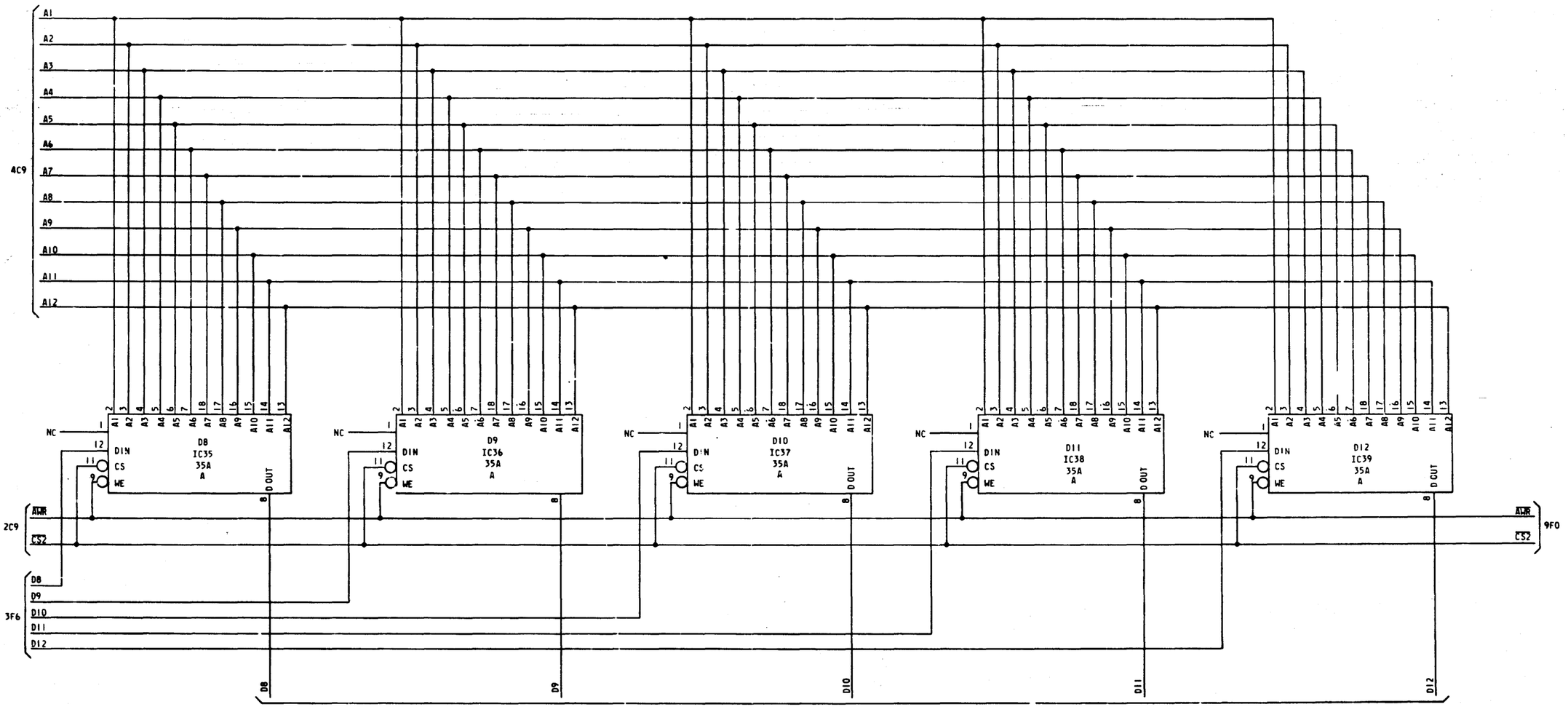
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK	DWG SIZE 65	ISSUE 1
BELL LABORATORIES CPS-SL65		SHEET 7

PART OF CPS SL65

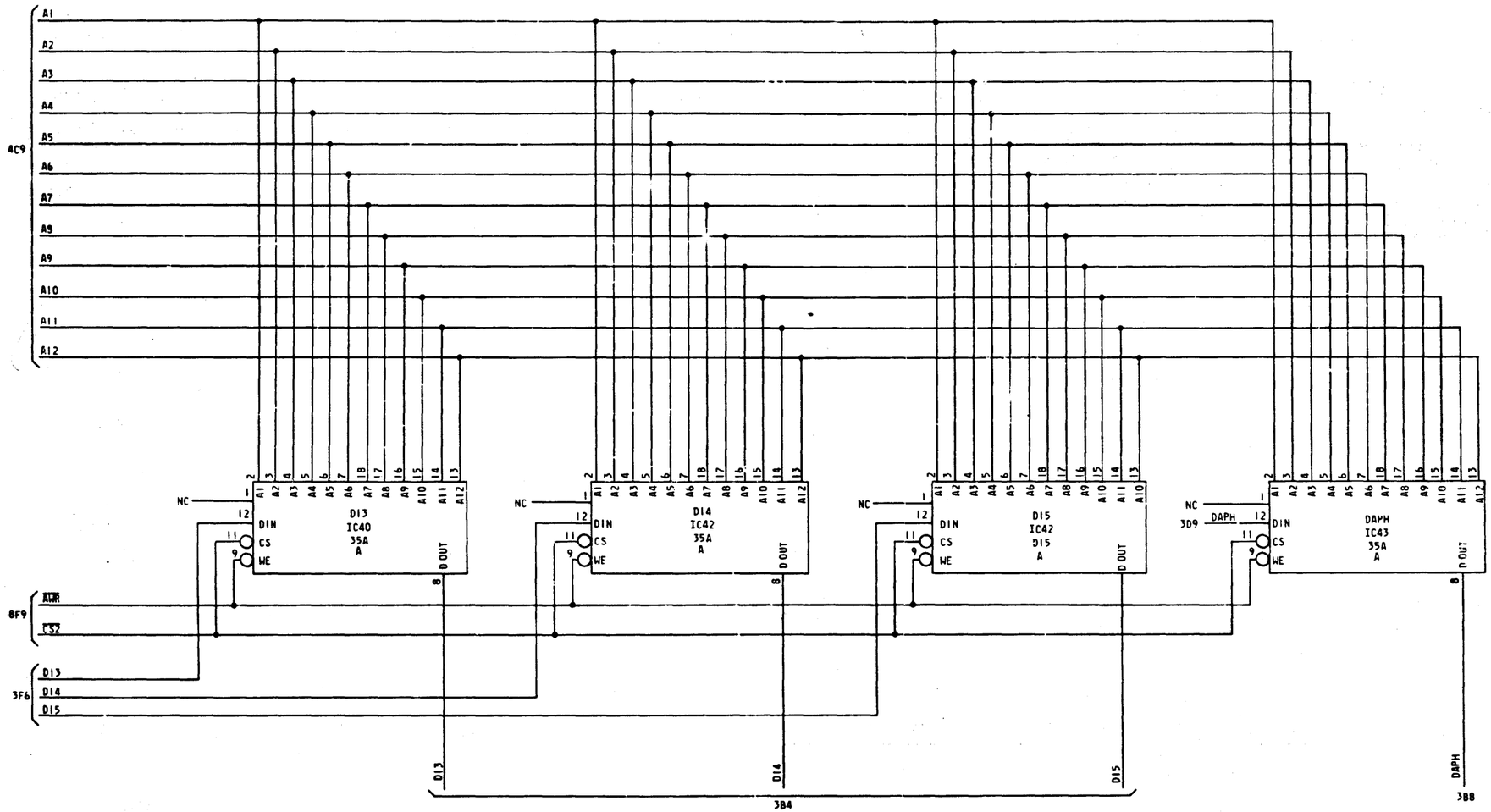
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK	DWG SIZE 6S	ISSUE 1
BELL LABORATORIES · CPS-SL65		SHEET 8

PART OF CPS SL65

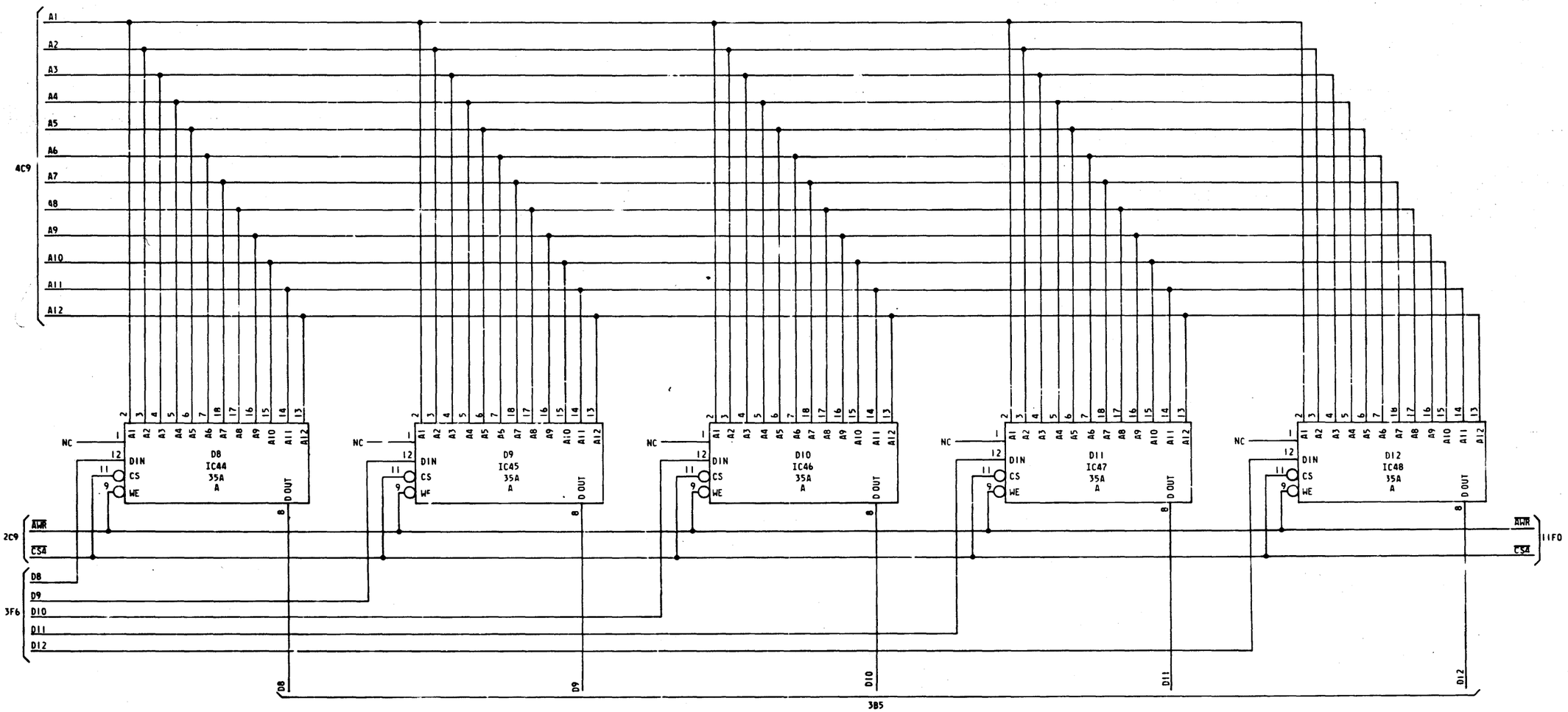
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK	DWG SIZE 65	ISSUE 1
BELL LABORATORIES CPS-SL65		SHEET 9

PART OF CPS SL65

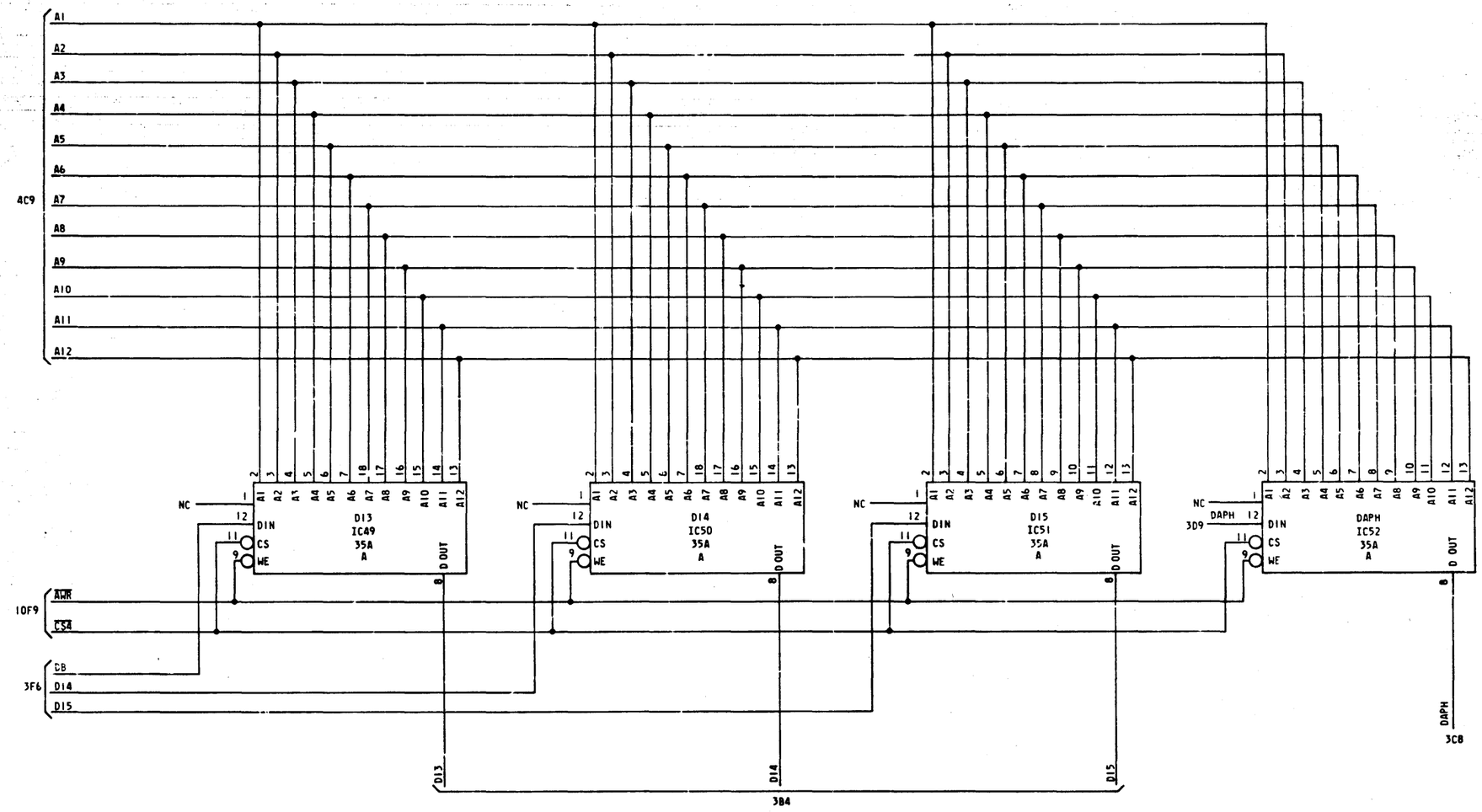
RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 10

PART OF CPS SL65

RANDOM ACCESS MEMORY



SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 11

PART OF CPS SL65

RANDOM ACCESS MEMORY

COMPONENT LIST

CIRCUIT, INTEGRATED

CP LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7		IC8		IC9	
CODE	WA-LS240 OR SN54LS240J*		WA-LS240 OR SN54LS240J*		WA-LS240 OR SN54LS240J*		AM25LS2521**		WA-LS00 OR SN54LS00J*		SN54LS38J* OR KS-21736,L25		SN54LS280J* OR KS-21285,L45		AM93548**		WA-LS139 OR SN54LS139J*	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	ELEM A	2D1		2C1	ELEM A	4B1 4D1		2E2		2D4		2C5 2E4 2E9 2F9		2F5		2F6		2C6
B		2E8								2E4								
C		2F3								2E4								
D		4C1								2C4								
E																		
F																		
G																		

CP LOC	IC10		IC11		IC12		IC13		IC14		IC15		IC16		IC17-20		IC21-25	
CODE	WA-LS139 OR SN54LS139J*		SN54LS85J* OR KS-21285,L21		WA-LS240 OR SN54LS240J*		WA-LS240 OR SN54LS240J*		WA-LS240 OR SN54LS240J*		WA-LS240 OR SN54LS240J*		SN54LS368AJ* OR KS-21285,L34		[4] 35A		[5] 35A	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		2D6		2D7		3E3		3E6		3C1		3C4	ELEM A	2C1 3C8		4E4		5E4
B																		
C																		
D																		
E																		
F																		
G																		

CP LOC	IC26-30		IC31-34		IC35-39		IC40-43		IC44-48		[4] IC49-52							
CODE	[5] 35A		[4] 35A		[5] 35A		[4] 35A		[5] 35A		[4] 35A							
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		6E4		7E5		8E4		9E5		10E4		11E5						
B																		
C																		
D																		
E																		
F																		
G																		

LEGEND:
* = TEXAS INSTRUMENT ** = ADVANCED MICRO DEVICES

CAPACITOR

DESIG	CODE
C1	6019.10
[19] C2-20	KS-21902,L1,0.1
[5] C21-25	KS-20736,L4,0.1

RESISTOR

DESIG	CODE
[7] R1-7	KS-20616,L1A,10kΩ
[4] R8-11	KS-20616,L1A,1kΩ
[13] R12-24	KS-20616,L1A,23.7
R25	KS-20616,L1A,4.7kΩ

INPUT/OUTPUT INFORMATION

INPUTS

FUNCTION	LEAD	DEFINITION
I	$\overline{A0-19}$	ADDRESS LEAD
I	$\overline{AP}$	ADDRESS PARITY
I	AS0-5	ADDRESS STRAPS
I	$\overline{AWR}$	ADVANCED WRITE
I	$\overline{BHE}$	BUS HIGH ENABLE
I	$\overline{D0-15}$	DATA LEADS
I	$\overline{DAPH}$	DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
I	$\overline{DAPL}$	DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
I	$\overline{KAP}$	ADDRESS PARITY STRAP
I	$\overline{PEN}$	PERIPHERAL ENABLE
I	$\overline{R/W}$	READ/WRITE LEAD

OUTPUTS

O	$\overline{ADW}$	ALL DECODE WELL
O	$\overline{D0-15}$	DATA LEADS
O	$\overline{DAPH}$	DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
O	$\overline{DAPL}$	DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
O	$\overline{NAW}$	NOT ALL WELL
O	$\overline{RDY}$	READY SIGNAL

ON BOARD LEADS

A1-12	ADDRESS LEADS
$\overline{CS1-4}$	CHIP SELECTS
D0-15	DATA LEADS
DAPH	DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
DAPL	DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
$\overline{REN}$	READ ENABLE
+5	BATTERY
GRD	GROUND RETURN
NC	NO CONNECTION

CIRCUIT DISCRIPTION

1. TOTAL RAM CAPACITY IS 16K BYTES USING 4K x 1 STATIC RAM DEVICES.
2. IC4, AN 8-BIT COMPARATOR, COMPARES STRAP PROGRAMMABLE BOARD ADDRESSES WITH THE ADDRESS GENERATED BY THE CPU. WHEN THESE TWO ADDRESSES MATCH, A BOARD ENABLE ($\overline{EOUT}$), IS GENERATED.
3. $\overline{ADW}$ IS THE ODD PARITY OVER A0-A13, $\overline{BHE}$, BOARD ENABLE ($\overline{EOUT}$), CONTROL LEADS $\overline{AWR}$ AND W/R, AND PARITY LEADS AP AND $\overline{KAP}$. $\overline{KAP}$ IS ALSO STRAP PROGRAMMABLE AND IS THE ODD PARITY OVER A14-A19.
4. $\overline{AWR}$ IS USED FOR $\overline{WE}$ ON MEMORY DEVICES.
5. THE LS240s FOR DATA IN-OUT TO MEMORY DEVICES ARE PERMANENTLY ENABLED WHEREAS THE LS240s FOR DATA OUTPUT FROM MEMORY DEVICES ARE ENABLED BY $\overline{REN}$, WHICH IS GENERATED BY USING THE NAND OF W/R AND EOUT.
6. MEMORY BANK SELECTION IS DONE BY MEANS OF A LS139. THE LS139 AND SUPPORTING CIRCUITS USED FOR CS ARE DUPLICATED IN ORDER TO PREVENT UNDETECTED ERRORS IF WRONG DATA IS WRITTEN WITH CORRECT PARITY WHEN THE CHIP SELECT CIRCUIT IS MALFUNCTIONING. ALSO, A PROVISION IS MADE TO WRITE LOWER BYTES, UPPER BYTES, OR COMPLETE WORDS, WHEREAS, A WORD IS READ DURING A MEMORY OPERATION. OUTPUTS OF THE LS139 ARE COMPARED BY THE LS85 COMPARATOR AND THIS OUTPUT IS USED FOR $\overline{ADW}$ AND $\overline{NAW}$.
7. ONE OF THE TWO LS139s IS ENABLED BY ADW1. A WRONG PARITY OVER THE ADDRESSES THIS LS139. THIS IN TURN WILL NOT GENERATE AN $\overline{ADW}$.
8. THE FOLLOWING PATTERN CAN BE USED TO DETECT FUNCTIONAL FAILURES OF MEMORY DEVICES. FUNCTIONAL FAILURES INCLUDE ONE OR MORE BITS STUCK AT FAILURES, ADDRESS LINES STUCK, DE ODER FAILURES, ETC.
   A. WRITE "1" IN ALL LOCATIONS OF THE MEMORY UNDER TEST.
   B. READ "1"/WRITE "0" IN ALL LOCATIONS, TAKING ONE LOCATION AT A TIME.
   C. READ "0"/WRITE "1" IN ALL LOCATIONS, TAKING ONE LOCATION AT A TIME.
   D. READ "1" IN COMPLETE MEMORY.

SL65 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL65		SHEET 12