

SHEET INDEX

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RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

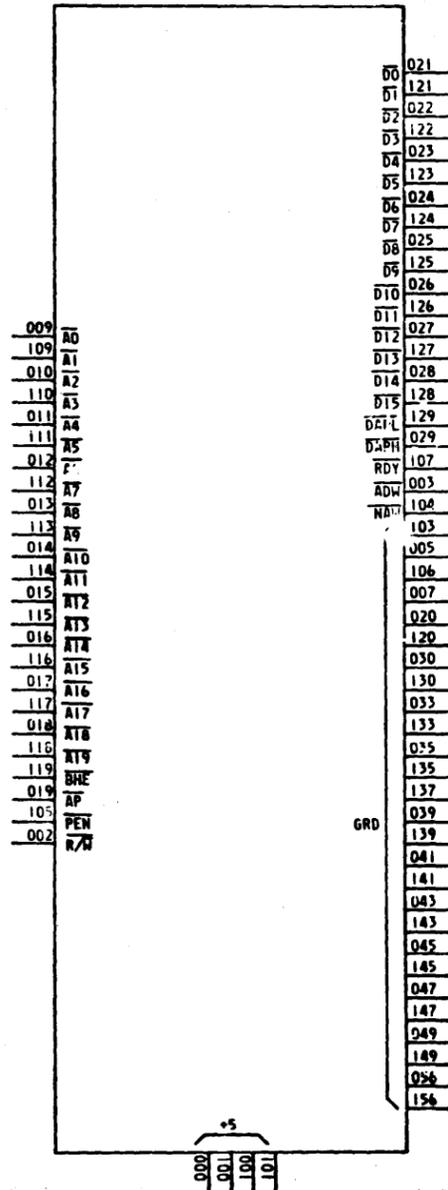
NOTES:

- GROUND RETURN.
- UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS. VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
- BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	BAT TERM	GRD TERM
32A()	+5	12
AM93S48DM	16	9
LSu4	14	7
LS32	14	7
LS240	20	10
SN54LS38	14	7
SN54S253J	16	8
SN54S471	20	10

DWG ISSUE	DATE	DRAWN	APPRO
1	4-28-80	CDI TNE STA	RW BR RW

SYMBOL



SYSTEM USED ON	DESIGN CONTROL
COMMON (CDT)	CB

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK SCHEMATIC DRAWING	SD-94868-01

SHEET INDEX NOTES

- ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
- FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
- THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELLSYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

1N99

SL66 CIRCUIT PACK
READ ONLY MEMORY

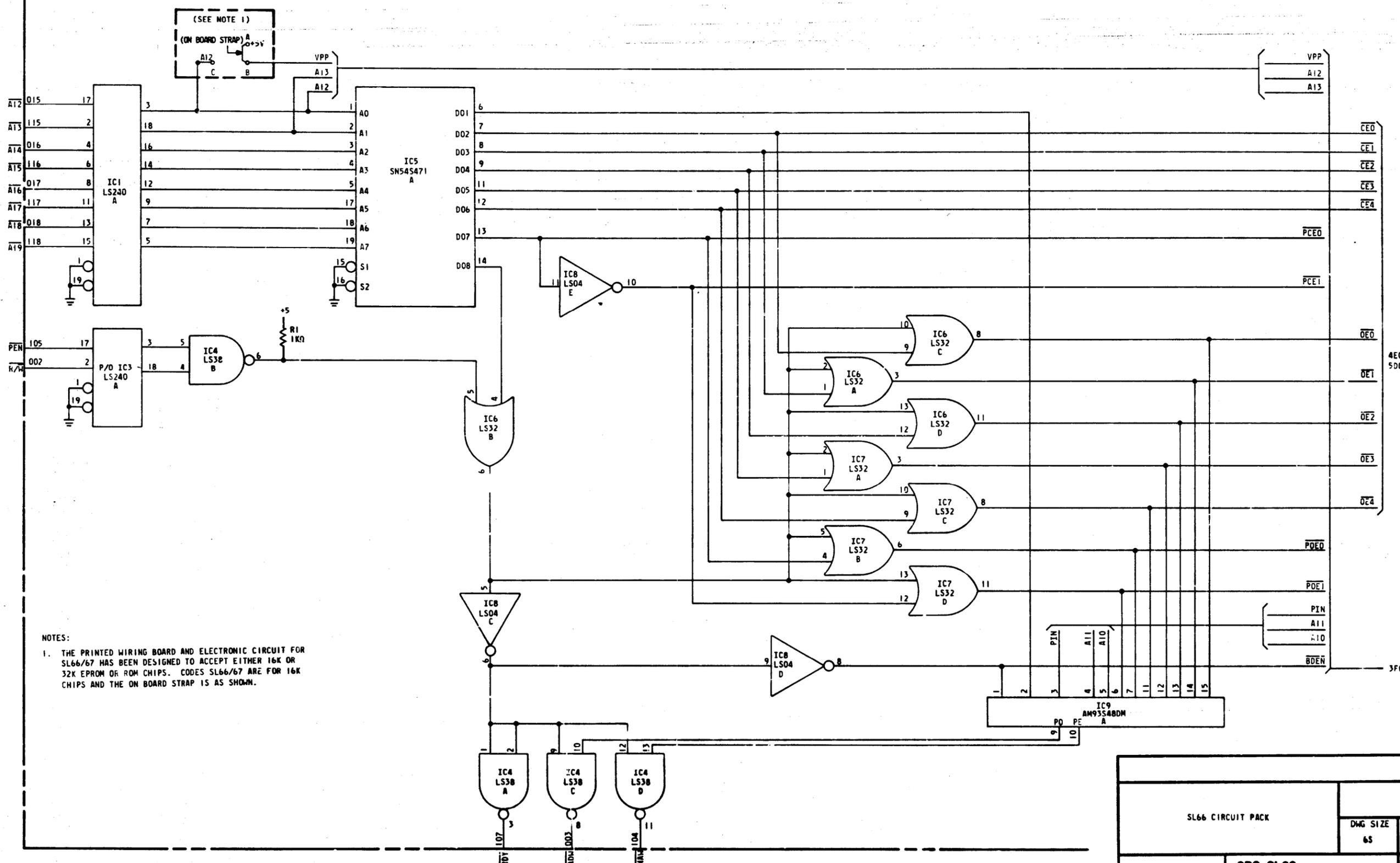
AT&T CO
STANDARD

DWG SIZE 65 ISSUE 1

BELL LABORATORIES **CPS-SL66** 6 SHEETS

PART OF CPS SL66
READ ONLY MEMORY

BOARD ENABLE AND DATA OUTPUT SELECT



NOTES:
1. THE PRINTED WIRING BOARD AND ELECTRONIC CIRCUIT FOR SL66/67 HAS BEEN DESIGNED TO ACCEPT EITHER 16K OR 32K EPROM OR ROM CHIPS. CODES SL66/67 ARE FOR 16K CHIPS AND THE ON BOARD STRAP IS AS SHOWN.

SL66 CIRCUIT PACK		DWG SIZE	ISSUE
		65	1
BELL LABORATORIES	CPS-SL66	SHEET 2	

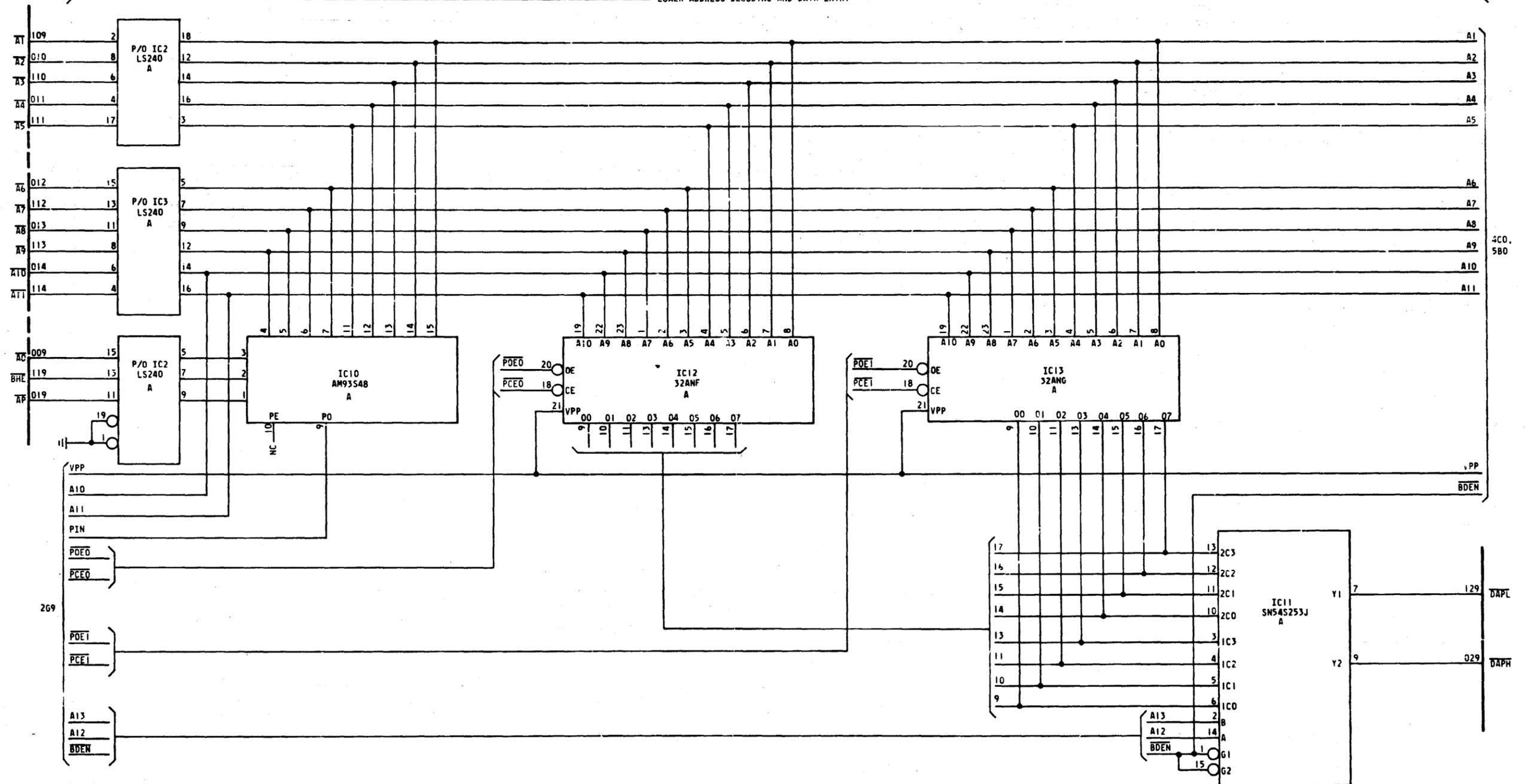
4E0.
500

3F0

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PART OF CPS SL66
READ ONLY MEMORY

LOWER ADDRESS DECODING AND DATA ENTRY



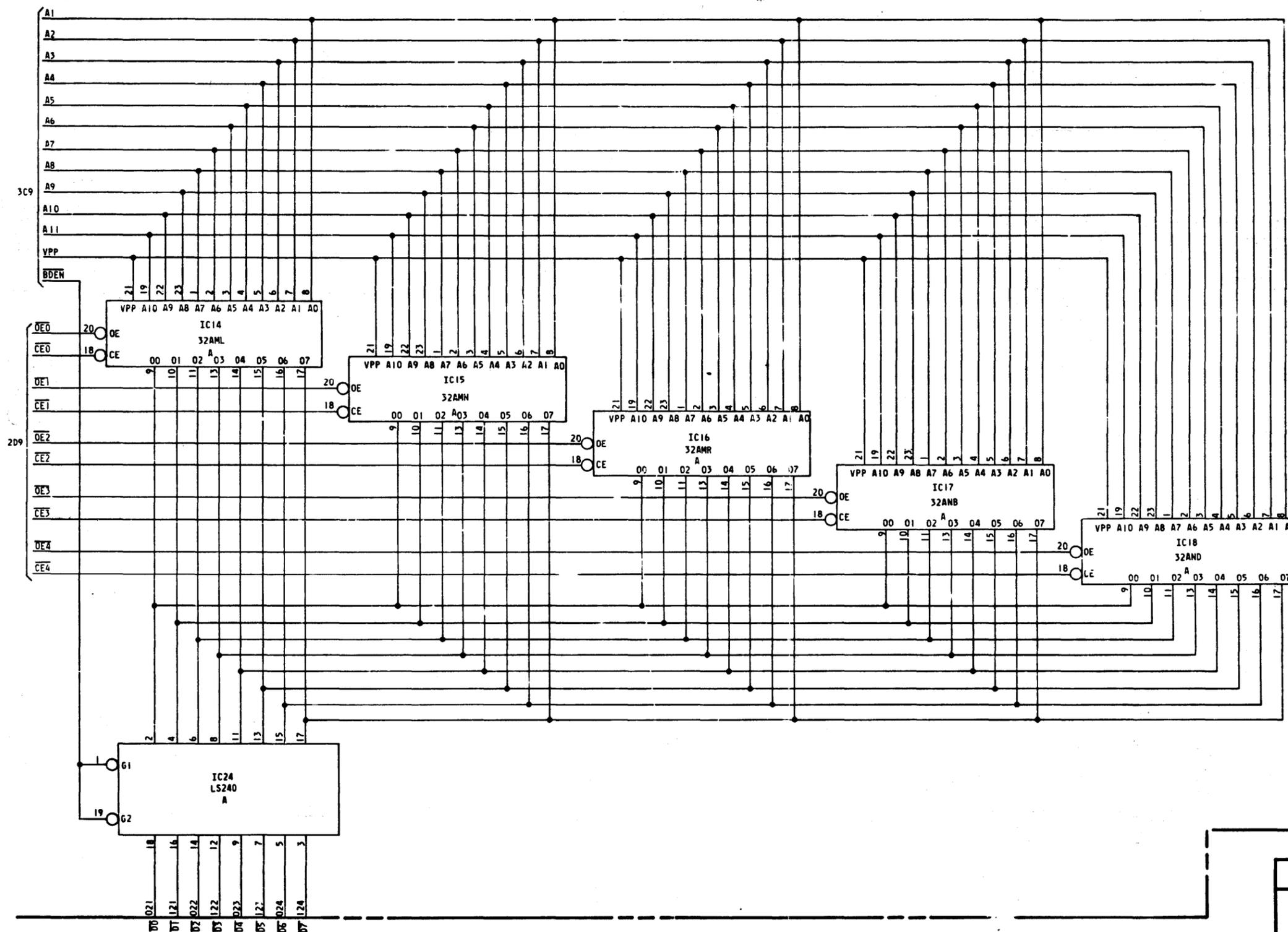
400, 580

SL66 CIRCUIT PACK		DWG SIZE	ISSUE
		65	I
BELL LABORATORIES	CPS-SL66	SHEET 3	

PART OF CPS SL66

READ ONLY MEMORY

LOW BYTE DATA

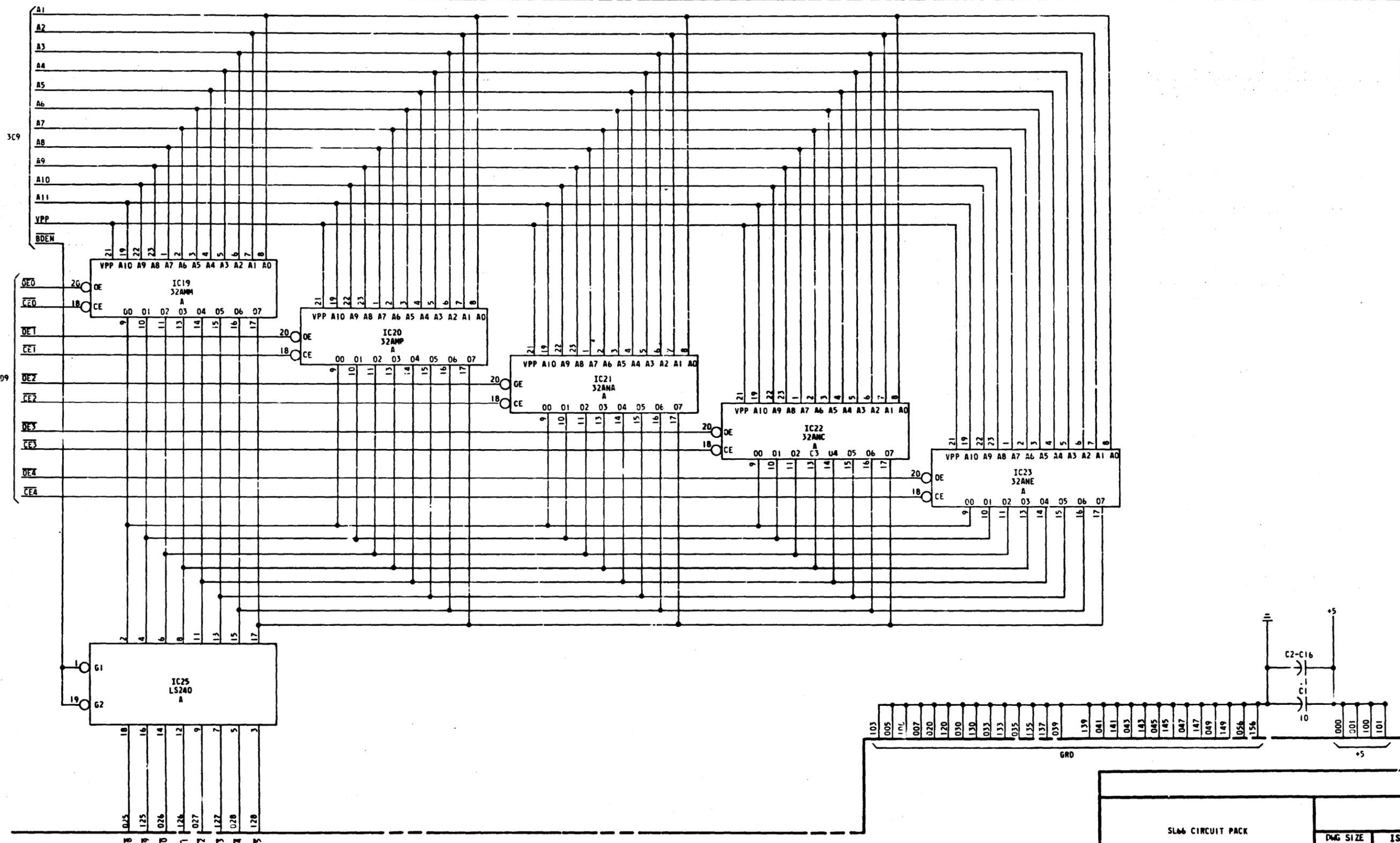
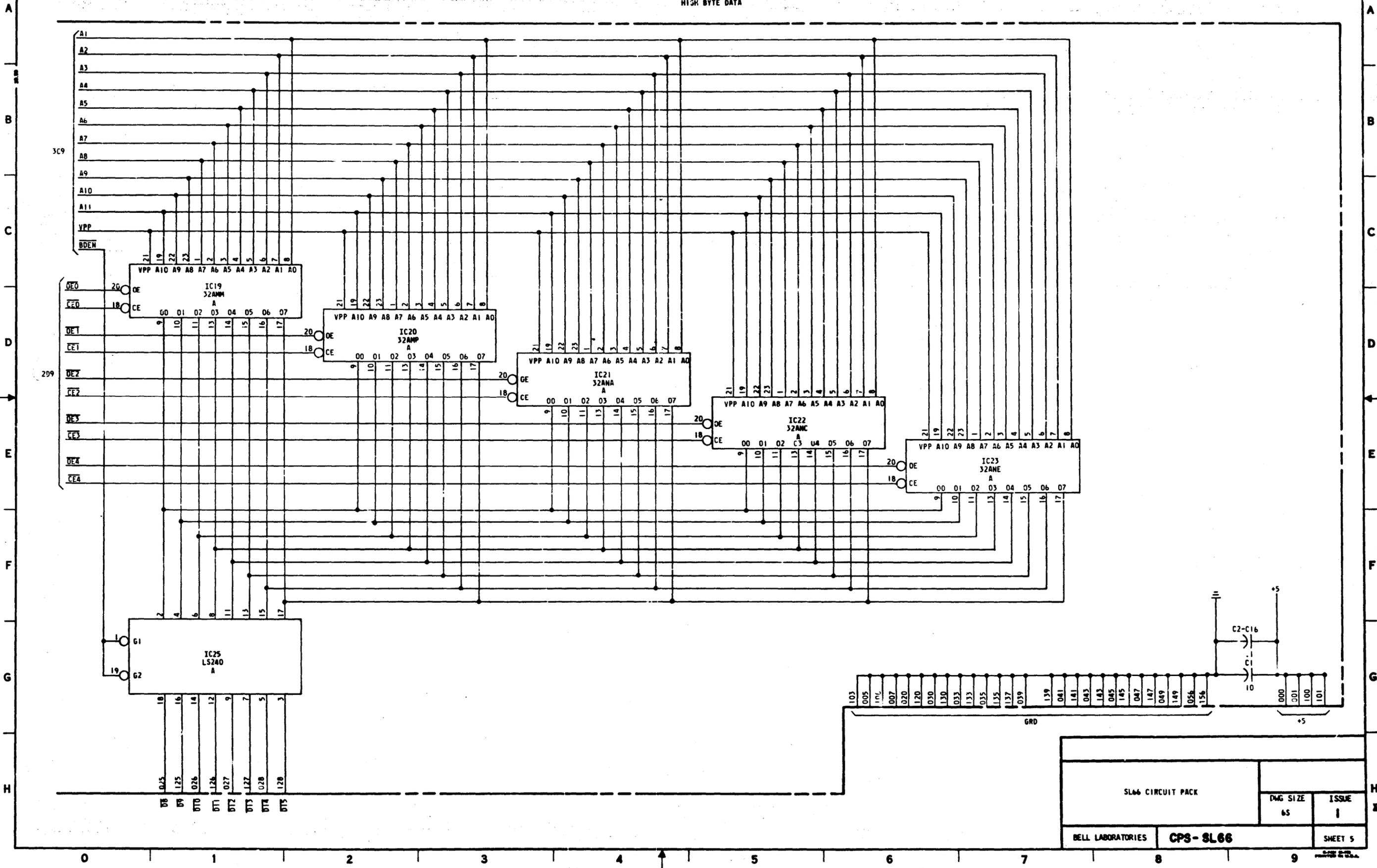


SL66 CIRCUIT PACK		DWG SIZE	ISSUE
		65	I
BELL LABORATORIES	CPS-SL66		SHEET 4

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PART OF CPS SL66

READ ONLY MEMORY
HIGH BYTE DATA



PART OF CPS SL66

COMPONENT LIST

CIRCUIT INTEGRATED

CP LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7	
CODE	SN54LS240J# OR WA-LS240		SN54LS240J# OR WA-LS240		SN54LS240J# OR WA-LS240		SN54LS30J#		SN54S471J#		SN54LS32J# OR WA-LS32		SN54LS32J# OR WA-LS32	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		2C1	ELEM	3B1	ELEM	2D1		2M3		2C3		2E6		2E5
B			A	3D1	A	3C1		2D1				2E3		2F6
C								2M4				2D6		2F6
D								2M4				2E6		2'6
E														
F														
G														

-- SEE NOTE 1

CP LOC	IC8		IC9		IC10		IC11		IC12		IC13		IC14	
CODE	SN54LS04J# OR 11A-LS04		AM93S48DM#		AM93S48DM#		SN54S33J#		32ANF		32ANG		32AML	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		SPARE		2G7		3D2		3F9		3D4		3D6		4D1
B		SPARE												
C		2F3												
D		2G5												
E		2D4												
F		SPARE												
G														

SEE NOTE 1

CP LOC	IC15		IC16		IC17		IC18		IC19		IC20		IC21	
CODE	32AMN		32AMR		32ANB		32AND		32AMM		32AMP		32ANA	
ELEMENT	DESIG	SH LOC												
A		4D2		4E4		4E5		4E7		5C1		5D2		5D4
B														
C														
D														
E														
F														
G														

SEE NOTE 1

CP LOC	IC22		IC23		IC24		IC25							
CODE	32ANC		32ANE		SN54LS240J# WA-LS240		SN54LS240J# WA-LS240							
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		5E5		5E7		4G1		5G1						
B														
C														
D														
E														
F														
G														

= TEXAS INSTRUMENT

= ADVANCED MICRO DEVICES

CAPACITOR

DESIG	CODE
C1	601B10
[15] C(2-16)	KS-20736, L4.1

RESISTOR

DESIG	CODE
R1	KS-20616, L1A, 1K0

NOTES:

- EPROMS KS-22060, L3 (INTEL B2716-1) WILL BE USED IN INITIAL INSTALLATIONS. THESE WILL BE REPLACED BY WECCO 32A() MASK PROGRAMMED ROMS. THE B2716-1'S WILL BE RETURNED TO BTL.
- PROGRAMMING INFORMATION FOR IC5 CALL DATA TRANSMITTER GENERIC PROGRAM CAN BE FOUND ON MASTERDEVICE SPECIFICATION PC 25460 LDI ISSUE 1, PK 25463-01, ISSUE 1, IC REFERENCE NO 1 FOR IC5.

READ ONLY MEMORY INPUT/OUTPUT INFORMATION

INPUTS

LEAD

AD-19
AP
BHE
PEN
R/W

DEFINITION

ADDRESS LEADS
ADDRESS PARITY
BUS HIGH ENABLE
PERIPHERAL ENABLE
READ/WRITE ENABLE

OUTPUTS

ADW
DO-15
DAPH
DAPL
NAW
RDY

ALL DECODE WELL
DATA LEADS
DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
NOT ALL WELL
READY LEAD

ON BOARD LEADS

A'-13
BEN
CEO-4
OEO-4
PCEO,1
PIN
POEO,1
VPP

ADDRESS LEADS
BOARD ENABLE
CHIP ENABLES
OUTPUT ENABLES
PARITY CHIP ENABLES
PARITY INPUT
PARITY OUTPUT ENABLES
MEMORY EXPANSION LEAD

IC5 PROM SAMPLE PROGRAM, SEE NOTE 2.

ADDRESS INPUTS										DATA OUTPUTS							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H		
L	L	L	L	L	L	L	H	L	L	H	H	H	L	H	L		
L	L	L	L	L	L	H	L	L	L	H	H	L	H	H	L		
L	L	L	L	L	L	H	H	L	L	H	L	H	H	H	H		
L	L	L	L	L	H	L	L	L	H	L	H	H	H	H	L		
ALL OTHER ADDRESSES									H	H	H	H	H	H	P		

ODD PARITY OVER THE ADDRESS INPUTS
P SHOULD BE A HIGH IF THE NUMBER OF HIGH'S IN THE ADDRESS IS EVEN.
P SHOULD BE A LOW IF THE NUMBER OF HIGH'S IN THE ADDRESS IS ODD.

CIRCUIT DESCRIPTION

THE SL66/67 IS A READ ONLY MEMORY FOR THE CDT (CALL DATA TRANSMITTER) SYSTEM. THE BOARD IS DESIGNED FOR THE WESTERN ELECTRIC 32A ROM WITH A CAPACITY OF 20 KILO-BYTES PLUS SINGLE BIT PARITY. (THIS BOARD WILL ALSO ACCEPT THE 2716 EPROM OR THE 2732 EPROM FOR A CAPACITY OF 40 KILO-BYTES).

BOARD ADDRESS DECODING AND GENERATION OF EPROM CHIP SELECTS (CEO-CE4) IS PERFORMED BY A BIPOLAR PROM (IC5) AS SHOWN IN INPUT/OUTPUT INFORMATION. THE OUTPUT ENABLE STROBES FOR THE ROMS (OEO-OE4) ARE DERIVED FROM THE CHIP SELECTS GATED WITH PEN THROUGH THE OR GATES (IC6, IC7). THE SELECTION OF THE APPROPRIATE PARITY BITS ARE HANDLED BY A MULTIPLEXER (IC11). ERROR DETECTION FOR THE ADDRESS BUS AND ADDRESS DECODING IS PERFORMED BY THE PARITY GENERATORS (IC9, IC10) AND THE DECODING PROM (IC5).

SL66 CIRCUIT PACK		DWG SIZE	ISSUE
		65	1
BELL LABORATORIES	CPS-SL66		SHEET 6