SHEET INDEX

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RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

NOTES:

1. ⏚ GROUND RETURN

2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS. VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.

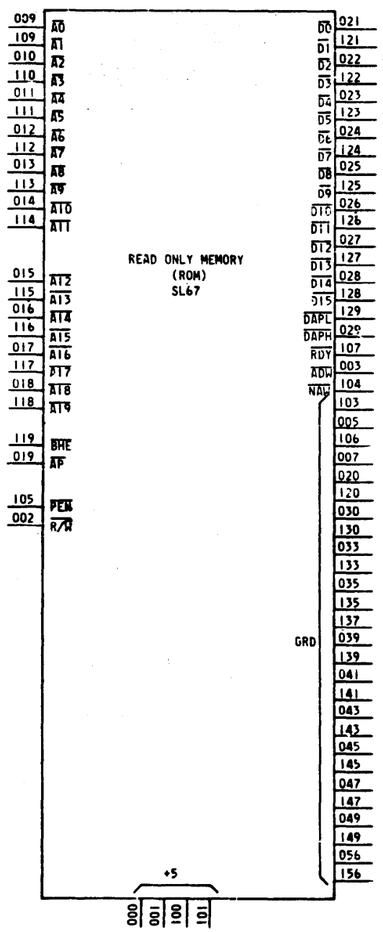
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	BAT TERM +5	GRD TERM
32A( )	24	12
AM54S253DM	16	8
AM93S48DM	16	8
LS04	14	7
LS32	14	7
LS240	20	10
SN54LS38	14	7
SN54S471	20	10

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	4-28-80	CDI THE STA	HW BK RW

CB

SYMBOL



SYSTEM USED ON	DESIGN CONTROL
COMMON (CDT)	CB

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK INFORMATION DRAWING	SD-94868-01

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

NOTICE— NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

IN99

SL67 CIRCUIT PACK
READ ONLY MEMORY

AT&TCO STANDARD

DWG SIZE 6S | ISSUE 1

BELL LABORATORIES | CPS-SL67 | 6 SHEETS

E-7509-4 (6-79) PRINTED IN U.S.A.

PART OF CPS SL67

READ ONLY MEMORY

BOARD ENABLE AND DATA OUTPUT SELECT

(SEE NOTE 1)
(ON BOARD STRAP) A +5V
A12 C B
VPP
A13
A12

IC1 LS240 A
IC5 SN54S471 A
IC8 LS04 E
IC6 LS32 C
IC6 LS32 A
IC6 LS32 D
IC7 LS32 A
IC7 LS32 C
IC7 LS32 B
IC7 LS32 D
IC6 LS32 B
P/O IC3 LS240 A
IC4 LS38 B
R1 1KΩ
IC8 LS32 C
IC8 LS04 D
IC9 AM93S48DM A
IC4 LS38 A
IC4 LS38 C
IC4 LS38 D

$\overline{A12}$ 015 $\overline{A13}$ 115 $\overline{A14}$ 016 $\overline{A15}$ 116 $\overline{A16}$ 017 $\overline{A17}$ 117 $\overline{A18}$ 018 $\overline{A19}$ 118
$\overline{PEN}$ 105 R/$\overline{W}$ 002
D01 D02 D03 D04 D05 D06 D07 D08
A0 A1 A2 A3 A4 A5 A6 A7 S1 S2

VPP A12 A13

$\overline{CE0}$ $\overline{CE1}$ $\overline{CE2}$ $\overline{CE3}$ $\overline{CE4}$ $\overline{PCE0}$ $\overline{PCE1}$
$\overline{OE0}$ $\overline{OE1}$ $\overline{OE2}$ $\overline{OE3}$ $\overline{OE4}$ $\overline{POE0}$ $\overline{POE1}$
4E0, 5D0
PIN A11 A10 $\overline{BDEN}$ 3F0

107 $\overline{RDY}$ 103 $\overline{ADV}$ 104 $\overline{MAV}$

NOTES:

1. THE PRINTED WIRING BOARD AND ELECTRONIC CIRCUIT FOR SL66/67 HAS BEEN DESIGNED TO ACCEPT EITHER 16K OR 32K EPROM OR ROM CHIPS. CODES SL66/67 ARE FOR 16K CHIPS AND THE ON BOARD STRAP IS AS SHOWN.

SL67 CIRCUIT PACK	DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL67	SHEET 2

PART OF CPS SL67

READ ONLY MEMORY

LOWER ADDRESS AND DATA PARITY

P/O IC2 LS240 A

P/O IC3 LS240 A

P/O IC2 LS240 A

IC10 AM93S48DM A

IC12 32APC A

IC13 32APD A

IC11 SN54S253J A

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11

A0 BHE AP

VPP A10 A11 PIN POE0 PCE0 POE1 PCE1 A13 A12 BDEN

DAPL DAPH

269

4C0, 5b0

SL67 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL67		SHEET 3

PART OF CPS SL67

READ ONLY MEMORY

LOW BYTE DATA

A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
VPP
BDEN

OE0
CE0
OE1
CE1
OE2
CE2
OE3
CE3
OE4
CE4

IC14
32ANH
A

IC15
32ANK
A

IC16
32ANM
A

IC17
32ANP
A

IC18
32APA
A

VPP A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
OE
CE
00 01 02 03 04 05 06 07

IC24
LS240
A

G1
G2

021 121 022 122 023 123 024 124

SL67 CIRCUIT PACK			
		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL67		SHEET 4

PART OF CPS SL67

READ ONLY MEMORY

HIGH BYTE DATA

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 VPP BDEN

3C9

2D9

OE0 CE0 OE1 CE1 OE2 CE2 OE3 CE3 OE4 CE4

IC19 32ANJ A

IC20 32ANL A

IC21 32ANN A

IC22 32ANR A

IC23 32APB 1

VPP A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

OE CE

00 01 02 03 04 05 06 07

IC25 LS240 A

G1 G2

D8 D9 D10 D11 D12 D13 D14 D15

GRD

+5

C2-16 .1

C1 10

SL67 CIRCUIT PACK

DWG SIZE 6S

ISSUE 1

BELL LABORATORIES

CPS-SL67

SHEET 5

PART OF CPS SL67

READ ONLY MEMORY

COMPONENT LIST

CIRCUITS, INTEGRATED

CP LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7	
CODE	SN54LS240J* OR WA-LS240		SN54LS240J* OR WA-LS240		SN54LS240J* OR WA-LS240		SN54LS38J*		SN54S471J*		SN54LS32J* OR WA-LS32		SN54LS32J* OR WA-LS32	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		2B1	ELEM A	3A1 3D1	ELEM A	2D1 3C1	ELEM A	2D1 2H6		2B3	ELEM A	2D3 2D5		2E5
B														
C														
D														
E														
F														
G														

SEE NOTE 1

CP LOC	IC8		IC9**		IC10**		IC11		IC12		IC13		IC14	
CODE	SN54LS04J* OR WA-LS04		AM93S48DM**		AM93S48DM**		SN54253J**		32APC		32APD		32ANH	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	ELEM A	2D4 2F6		2G7		3D2		3F8		3D4		3D6		4D1
B														
C														
D														
E														
F														
G														

SEE NOTE 1

CP LOC	IC15		IC16		IC17		IC18		IC19		IC20		IC21	
CODE	32ANK		32ANM		32ANP		32APA		32ANJ		32ANL		32ANN	
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		4D2		4D4		4E5		4E7		5C1		5D2		5D4
B														
C														
D														
E														
F														
G														

SEE NOTE 1

CP LOC	IC22		IC23		IC24		IC25							
CODE	32ANR		32APB		SN54LS240J* WA-LS240		SN54LS240J* WA-LS240							
ELEMENT	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A		5E5		5E7		4G1		5G1						
B														
C														
D														
E														
F														
G														

* = TEXAS INSTRUMENT

** = ADVANCED MICRO DEVICES

CAPACITOR

DESIG	CODE
C1	6018.10uf
[15] C(2-16)	KS-20736,L4.1uf

RESISTOR

DESIG	CODE
R1	KS-202616,L1A,1KΩ

NOTES:

1. EPROMS KS-22060, L3 (INTEL B2716-1) WILL BE USED IN INITIAL INSTALLATIONS. THESE WILL BE REPLACED BY WECO 32A() MASK PROGRAMMED ROMS. THE B27161-1'S WILL BE RETURNED TO BTL.

2. PROGRAMMING INFORMATION FOR 4A5 CALL DATA TRANSMITTER GENERIC PROGRAM CAN BE FOUND ON MASTERDEVICE SPECIFICATION PG 25460 LDI ISSUE 1, PK 25464-01, ISSUE 1, IC REFERENCE NO 1 FOR IC5.

INPUT/OUTPUT INFORMATION

LEAD DESIGNATION LIST

INPUTS

LEAD	DEFINITION
A0-19	ADDRESS LEADS
AP	ADDRESS PARITY
BHE	BUS HIGH ENABLE
PEN	PERIPHERAL ENABLE
R/W	READ/WRITE ENABLE

OUTPUTS

ADW	ALL DECODE WELL
DO-15	DATA LEADS
DAPH	DATA ADDRESS PARITY OVER THE HIGH BYTE OF DATA
DAPL	DATA ADDRESS PARITY OVER THE LOW BYTE OF DATA
NAW	NOT ALL WELL
RDY	READY LEAD

ON BOARD LEADS

A1-13	ADDRESS LEADS
BDEN	BOARD ENABLE
CE0-4	CHIP ENABLES
OE0-4	OUTPUT ENABLES
PCE0,1	PARITY CHIP ENABLES
PIN	PARITY INPUT
POE0,1	PARITY OUTPUT ENABLES
VPP	MEMORY EXPANSION LEAD

IC5 PROM SAMPLE PROGRAM, SEE NOTE 2.

ADDRESS INPUTS								DATA OUTPUTS							
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
L	L	L	L	L	H	L	H	L	L	H	H	H	H	L	H
L	L	L	L	L	H	H	L	L	L	H	H	H	L	H	H
L	L	L	L	L	H	H	H	L	L	H	H	L	H	H	L
L	L	L	L	H	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	H	H	L	H	L	H	L	H	H	H	H	H
ALL OTHER ADDRESS								H	H	H	H	H	H	H	P

ODD PARITY OVER THE ADDRESS INPUTS

P SHOULD BE A HIGH IF THE NUMBER OF HIGH'S IN THE ADDRESS IS EVEN.

P SHOULD BE A LOW IF THE NUMBER OF HIGH'S IN THE ADDRESS IS ODD.

CIRCUIT DESCRIPTION

THE SL66/67 IS A READ ONLY MEMORY FOR THE CDT (CALL DATA TRANSMITTER) SYSTEM. THE BOARD IS DESIGNED FOR THE WESTERN ELECTRIC 32A ROM WITH A CAPACITY OF 20 KILO-BYTES PLUS SINGLE BIT PARITY. (THIS BOARD WILL ALSO ACCEPT THE 2716 EPROM OR THE 2732 EPROM FOR A CAPACITY OF 40 KILO-BYTES).

BOARD ADDRESS DECODING AND GENERATION OF ROM CHIP SELECTS (CE0-CE4) IS PERFORMED BY A BIPOLAR PROM (IC5) AS SHOWN IN INPUT/OUTPUT INFORMATION. THE OUTPUT ENABLE STROBES FOR THE ROMS (OE0-OE4) ARE DERIVED FROM THE CHIP SELECTS GATED WITH PEN THROUGH THE OR GATES (IC6,IC7). THE SELECTION OF THE APPROPRIATE PARITY BITS ARE HANDLED BY A MULTIPLEXER (IC11). ERROR DETECTION FOR THE ADDRESS BUS AND ADDRESS DECODING IS PERFORMED BY THE PARITY GENERATORS (IC9,IC10) AND THE DECODING PROM (IC5).

SL67 CIRCUIT PACK		DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-SL67		SHEET 6