SHEET INDEX

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RECORD OF CHANGES

DWG ISS	PREV TURN	STD	MFR DISC	SEE NOTE

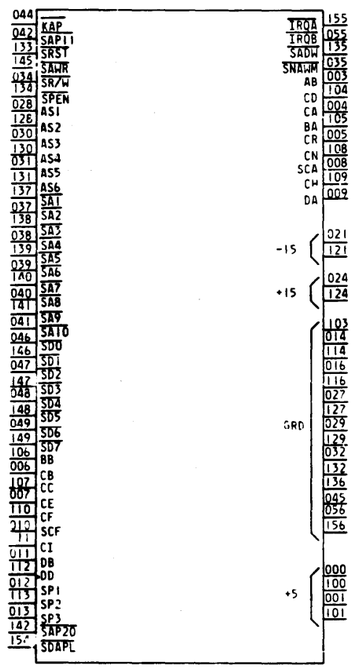
NOTES:

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE IN VOLTS.
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS.

IC CODE	BAT TERM	GRD TERM
LS368	16	8
LS244	20	10
25LS2521	20	10
93S48	16	8
LS00	14	7
LS139	16	8
LS85	16	8
LS32	14	7
2651	26	4
LS640	20	10
LS38	14	7
LS273	20	10
LS373	20	10
LS04	14	7
LS125	14	7
75188	1,14	7
75189	14	7

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	9-17-80	CDI THE LG	MFW NAR RW
2	9-24-81	CDI JRB	MFW NAR RW

SYMBOL



SYSTEM USED ON	DESIGN CONTROL
COMMON (CDT)	CB

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK SCHEMATIC DRAWING	SD-94868-01

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

IN99

SL85 CIRCUIT PACK
SERIAL I/O BOARD

AT&TCO STANDARD

DWG SIZE 6S | ISSUE 2

BELL LABORATORIES | CPS-SL85 | 5 SHEETS

E-7005-A10-791 PRINTED IN U.S.A.

PART OF CPS SL85

SERIAL I/O BOARD

R1 10kΩ
R2 10kΩ
R3 10kΩ
R4 10kΩ
R5 10kΩ
R6 10kΩ
R7 10kΩ
R8 10kΩ
R9 10kΩ
R10 1kΩ
R11 390
R17 1kΩ
C11 .05

IC1 LS368 A
IC2 LS244 A
IC3 AM25LS2521 A
IC4 LS368 A
IC5 AM93S48 A
IC6 LS00 A
IC6 LS00 B
IC6 LS00 D
IC7 LS139 A
IC8 LS85 A
IC9 LS32 A
IC9 LS32 B
IC16 LS04 A
IC16 LS04 D
IC16 LS04 E
IC16 LS04 F
IC17 LS125 D

SR/W
AS6
AS5
AS4
AS3
AS2
AS1
SPEN
SA10
SA9
SA8
SA7
SA6
SA5
SAWR
KAP
SA2
SA1
SRST
SAPIT
SA4
SA3
EOUT
EIN
A2
A1
RST
3DO
PE
PO
NC
R/W
R/M
BEN
REN
DOCLK
DIE
CE
IC
BEN
CO
4DO

SL85 CIRCUIT PACK		DWG SIZE 65	ISSUE 2
BELL LABORATORIES	CPS-SL85		SHEET 2

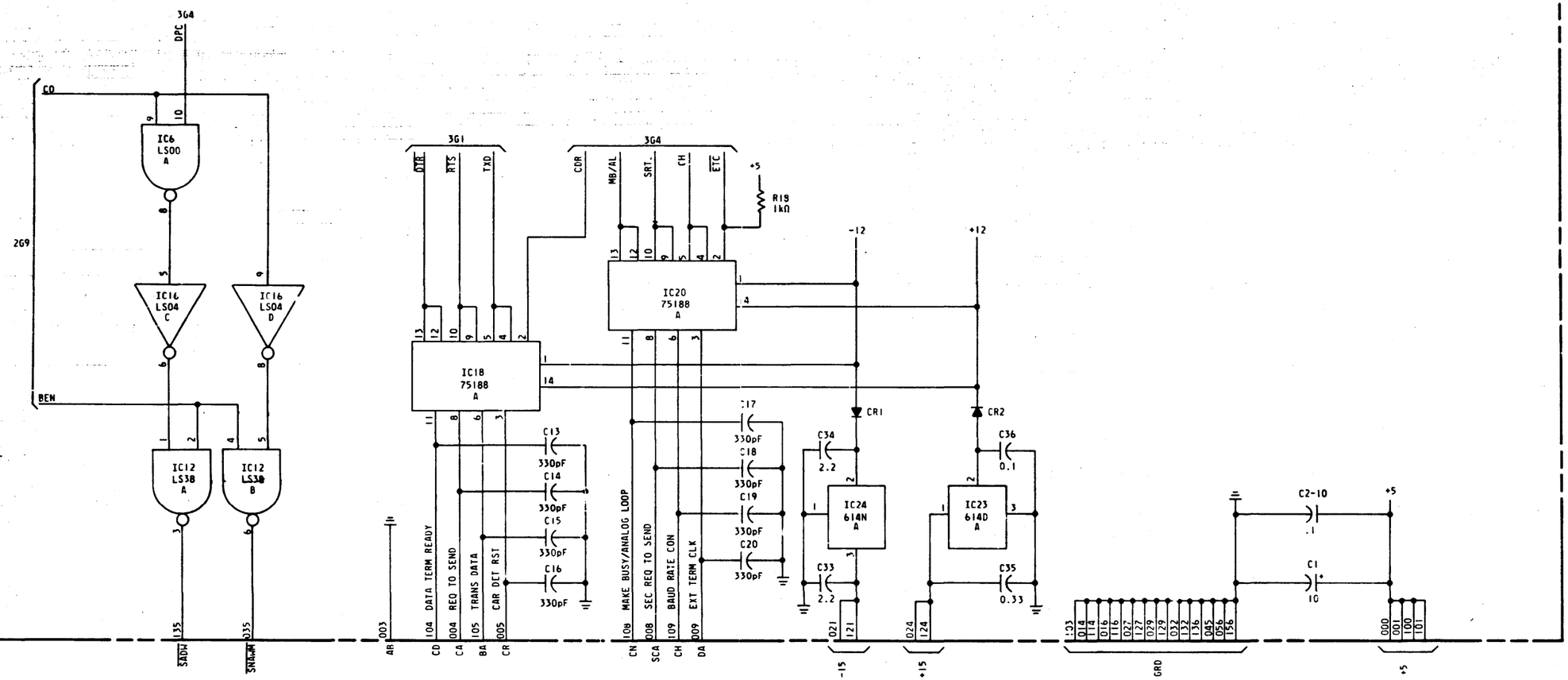
PART OF CPS SL85

IC11 LS640 A
IC19 75189 A
IC21 75189 A
IC22 75189 A
IC14 LS373 A
P/O IC4 LS366 A
IC9 LS32 C
IC10 N2651 A
IC13 LS273 A
IC15 AM93548 A
IC17 LS125 A
IC17 LS125 B
IC17 LS125 C
IC16 LS04 B
IC9 LS32 D
P/O IC4 LS368 A
IC12 LS38 C
IC12 LS38 D
CRYSTAL Y1 1276 5.0688 MHz
R15 5110
R16 5110
R14 5110
R12 5110
R13 5110
C24 220pF
C23 220pF
C22 220pF
C21 220pF
C28 220pF
C27 220pF
C26 220pF
C25 220pF
C32 220pF
C31 220pF
C30 220pF
C29 220pF
C37 470pF

SL85 CIRCUIT PACK		DWG SIZE 6S	ISSUE 2
BELL LABORATORIES	CPS-SL85		SHEET 3

PART OF CPS SL85

SERIAL I/O BOARD



SL85 CIRCUIT PACK		DWG SIZE 6S	ISSUE 2
BELL LABORATORIES	CPS-SL85		SHEET 4

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PART OF CPS SL85

SERIAL I/O BOARD

COMPONENT LIST

CIRCUIT, INTEGRATED

CP LOC	IC1		IC2		IC3		IC4		IC5		IC6		IC7		IC8	
CODE	SN54LS368AJ-00*		SN54LS244J-00* OR WA-LS244		AM25LS2521DM***		SN54LS368AJ-00*		AM93S48DM***		SN54LS00J-00* OR WALS00		SN54_S139J-00* OR WA-LS139		SN54LS85J-00*	
ELEMENT	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC
A		2D1		2C1		2B3		2B4		2D5		2C8		2F3		2G3
B								3C7				2F8				
C								3F2				4C1				
D								SPARE				2L6				
E																
F																
G																
H																

CP LOC	IC9		IC10		IC11		IC12		IC13		IC14		IC15		IC16	
CODE	SN54LS32J-00* OR WA-LS32		N2651I**		SN54LS640J-00*		SN54LS38J-00*		SN54LS273J-00*		SN54LS373J-00*		AM93S48DM***		SN54LS04J-00* OR WA-LS04J	
ELEMENT	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC
A		2D7		3E2		3B2		4E2		3E3		3C4		3E6		2C4
B		2E7						4E2								3E2
C		3D7						3G2								4D1
D		3F6														4D2
E																2G7
F																2B6
G																
H																

CP LOC	IC17		IC18		IC19		IC20		IC21		IC22		IC23		IC24	
CODE	SN54LS125AJ-00*		SN75188J-00*		SN75189J-00*		SN75188J-00*		SN75189J-00*		SN75189J-00*		6140		614N	
ELEMENT	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC	DESIG	LOC
A		3E4		4E3		3B2		4D4		3B4		3B5		4F6		4F5
B		3F4														
C		3F7														
D		2E3														
E																
F																
G																
H																

* TEXAS INSTRUMENTS
** SIGNETICS
*** ADVANCED MICRO DEVICES

CAPACITOR

DESIG	CODE
C1	6018,10
[9] C2-C10	KS-20736,L4,0.1,50VDC
C11	KS-13814,L14,.05,150VDC
[8] C13-C20	KS-19774,L7,330pF,100VDC
[12]C21-32	KS-19774,L7,220pF,100VDC
C33,34	603H,2.2UF,60VDC
C35	KS-19774,L5,0.33,50VDC
C36	KS-20736,L4,0.1,50VDC
C37	KS-19774,L7,470pF,10%,100VDC

DIODE

DESIG	CODE
CR1	458A
CR2	458A

CRYSTAL

DESIG	CODE
Y1	127G

RESISTOR

DESIG	CODE
[9] R1-R9	KS-20616,L1A,10kΩ
[3] R10,R17,R18	KS-20616,L1A,1kΩ
R11	KS-20616,L1A,38Ω
[5] R12-R16	KS-20616,L1A,511Ω

INPUT/OUTPUT INFORMATION

ALL INPUTS AND OUTPUTS EXCEPT THE EIA RS232C SIGNALS SHOULD BE TTL LEVELS OF 0 TO +0.8 VDC FOR A LOW AND +2.4 TO +5.5 VDC FOR A HIGH. THE TTL SIGNALS ARE ACTIVE LOW. THE EIA RS232C INPUTS AND OUTPUTS SHOULD BE -25 TO -3 VDC FOR A LOW AND +3 TO +25 VDC FOR A HIGH AND ARE ACTIVE HIGH.

CIRCUIT DESCRIPTION

1. SIGNETICS 2651, PROGRAMMABLE COMMUNICATIONS INTERFACE, IS USED AS USART. THIS DEVICE CONTAINS A BAUD RATE GENERATOR ON CHIP, WHICH CAN BE PROGRAMMED FROM 50 TO 19,200 BAUD. WESTERN ELECTRIC'S 127G IS USED AS CRYSTAL OSCILLATOR. THIS DEVICE INTERFACES CPU DATA CHARACTERS TO AN EXTERNAL DATA SET VIA LS640. DETAILED INFORMATION ABOUT THE USART DEVICE CAN BE OBTAINED FROM THE DATA SHEET. TWO CONTROL SIGNALS $\overline{RXRDY}$ AND $\overline{TXRDY}$ CREATES INTERRUPTS TO THE CPU FOR THE TRANSMITTING OR RECEIVING OF CHARACTERS.

2. USART AND EIA TRANSMITTER/RECEIVER: TWO EIA DRIVERS AND THREE EIA RECEIVERS ARE USED. SIX INTERFACE SIGNALS PROVIDED BY THE DATA SET ARE $\overline{DSR}$,$\overline{CTS}$,RXD,$\overline{DTR}$,$\overline{RTS}$ AND TXD. SEVERAL LEADS ON EIA RECEIVERS AND DRIVERS ARE KEPT OPTIONAL FOR FUTURE USE. THE WESTERN ELECTRICS VOLTAGE REGULATORS PROVIDE ±12 VOLTS NECESSARY FOR EIA DRIVERS. ONE BY PROGRAMMING USART, CAN USE INTERFACE CLOCK OF USART TO DRIVE MODEM CLOCK, ALSO ONE CAN DRIVE USART BY MODEM CLOCK. THIS REQUIRES PROGRAMMING Q5 AND Q6 ON LS273.

3. SELECT LOGIC: THE 25LS2521 COMPARATER CHIP GENERATES BOARD ENABLE WHEN THE ADDRESS INPUTS (B0-B7) ARE MATCHES WITH PROGRAMMED STRAPS (A0-A7). A3 AND A4 SELECT ONE OUT OF THREE DEVICES USART OR LS273 OR LS373. DATA ARE LATCHED IN LS273 AT THE TRAILING EDGE OF $\overline{AWR}$. DATA LATCHED IN LS374 WHEN Y1 AND R/$\overline{W}$ BOTH ARE LOW. A1 AND A2 SELECTS ONE OF FOUR REGISTERS, NAMELY, STATUS REGISTER, MODE REGISTERS 1 AND 2 AND COMMAND REGISTER.

4. ERROR CHECKING CAPABILITY: ADRESS PARITY, CONTROL LEADS (R/$\overline{W}$ AND $\overline{AWR}$) AND BOARD ENABLE ARE CHECKED USING A PARITY GENERATOR 93S48. DECODER LS139 IS CHECKED BY USING BOTH DECODERS. ONE OF THE DECODERS IS ENABLED BY BOARD ENABLE AND THE OTHER DECODER IS ENABLED BY AN OUTPUT OF 93S48. BOTH DECODERS OUTPUTS ARE COMPARED BY LS85. THIS ARRANGEMENT ALLOWS ONE TO CHECK LS85 OUTPUT LEAD BY PROVIDING FAULTY ADDRESS PARITY AND THUS NOT ENABLING LOWER DECODER OF LS139. ALSO, CHECKED ARE +12 AND -12 POWER REQUIREMENTS BY PARITY CHECKER. ANOTHER 93S48 IS USED TO CREATE DATA PARITY WHILE READING THE BOARD AND CHECKING THE DATA PARITY WHILE WRITING. ALL DECODE WELL AND NOT ALL WELL ARE GENERATED BY USING EQUATIONS:

$$\overline{SADW} = \overline{BDEN \cdot ERROR \cdot DATA\ PARITY}$$

$$\overline{SNAWN} = \overline{BDEN \cdot ERROR}$$

5. BRCLK OF 2561 IS BROUGHT OUT AS A PIN, WHICH CAN BE CONNECTED TO TSI. TSI IS CONNECTED TO CLOCK OSCILLATOR 127G THIS GIVES A VERSATILITY OF USING ANY OTHER CLOCK GENERATOR ON BRCLK TO DRIVE USART. THIS BOARD IS A UNIVERSAL SIO BOARD FOR RS232C INTERFACE. THE BOARD CAN BE USED IN SYNCHRONOUS OR ASYNCHRONOUS MODE.

6. NOTE: THE 2651 (IC10) AND LS273 (IC13) MUST BE INITIALIZED. INITIALIZATION OF THE LS273 DEPENDS ON WHETHER THE LS125 (IC17) IS ENABLED OR NOT AS WELL AS EXERCISING THE INTERRUPT LEADS.

SL85 CIRCUIT PACK	DWG SIZE 6S	ISSUE 2
BELL LABORATORIES	CPS-SL85	SHEET 5

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