SHEET INDEX

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RECORD OF CHANGES

| DWG ISS | PREV FURN | STD | MFR DISC | SEE NOTE |
|---|---|---|---|---|
| | | | | |

NOTES

1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS; VALUES PROCEEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.
3. BATTERY AND GROUND TERMINALS FOR INTERGRATED CIRCUITS ARE:

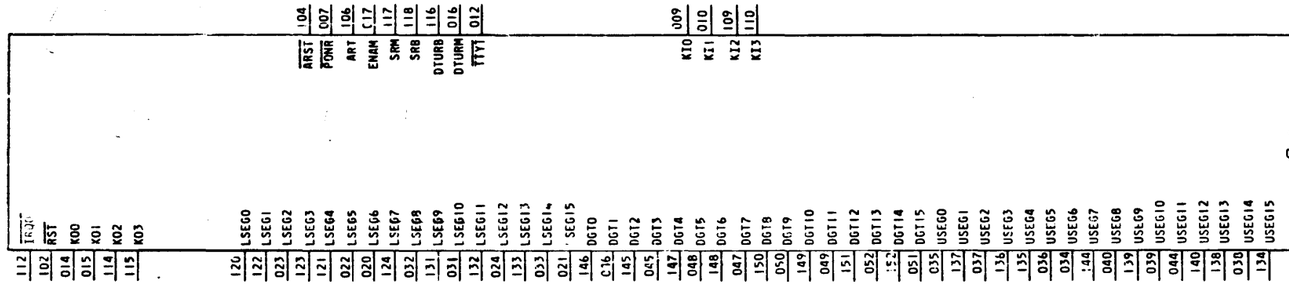
| IC CODE | BAT TERM +5 | GRD TERM |
|---|---|---|
| C8748 | 40 | 20 |
| MTX-81 | 40 | 20 |
| SN5403. | 14 | 7 |
| SN54LS273J | 20 | 10 |
| ULN2033A OR KS-22400.L1 | 15 | 5 |
| WA-LS08 | 14 | 7 |
| WA-LS20 | 14 | 7 |
| WA-LS74 | 14 | 7 |
| WA-LS138 | 16 | 8 |
| WA-LS240 | 20 | 10 |
| SN54LS241 | 20 | 10 |
| WA-LS279 | 16 | 8 |
| ULN2815A OR KS-22399,L1 | 10 | 9 |

4. IC'S 5 AND 6 MUST BE EQUIPPED WITH SOCKETS.
5. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE:

| FUNCTION | TERMINALS |
|---|---|
| +5 | 000.001.100.101 |
| GRD | 003.005.008.011.<br>013.019.025.027.<br>030.041.043.056.<br>103.105.108.111.<br>113.119.125.127.<br>130.141.143.156 |

| DWG ISSUE | DATE ISSUE | DRAWN | APPD |
|---|---|---|---|
| 1 | 2-22-84 | CDI ZP | BPE GNK RW |

SYMBOL




| SYSTEM USED ON | DESIGN CONTROL |
|---|---|
| COMMON (CDT) | CB |

SUPPORTING INFORMATION

| CATEGORY | NO. |
|---|---|
| CIRCUIT PACK SCHEMATIC DRAWING | SD-94868-01 |

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.



iN99

SL88 CIRCUIT PACK
DTP CONTROLLER

AT&T CO STANDARD

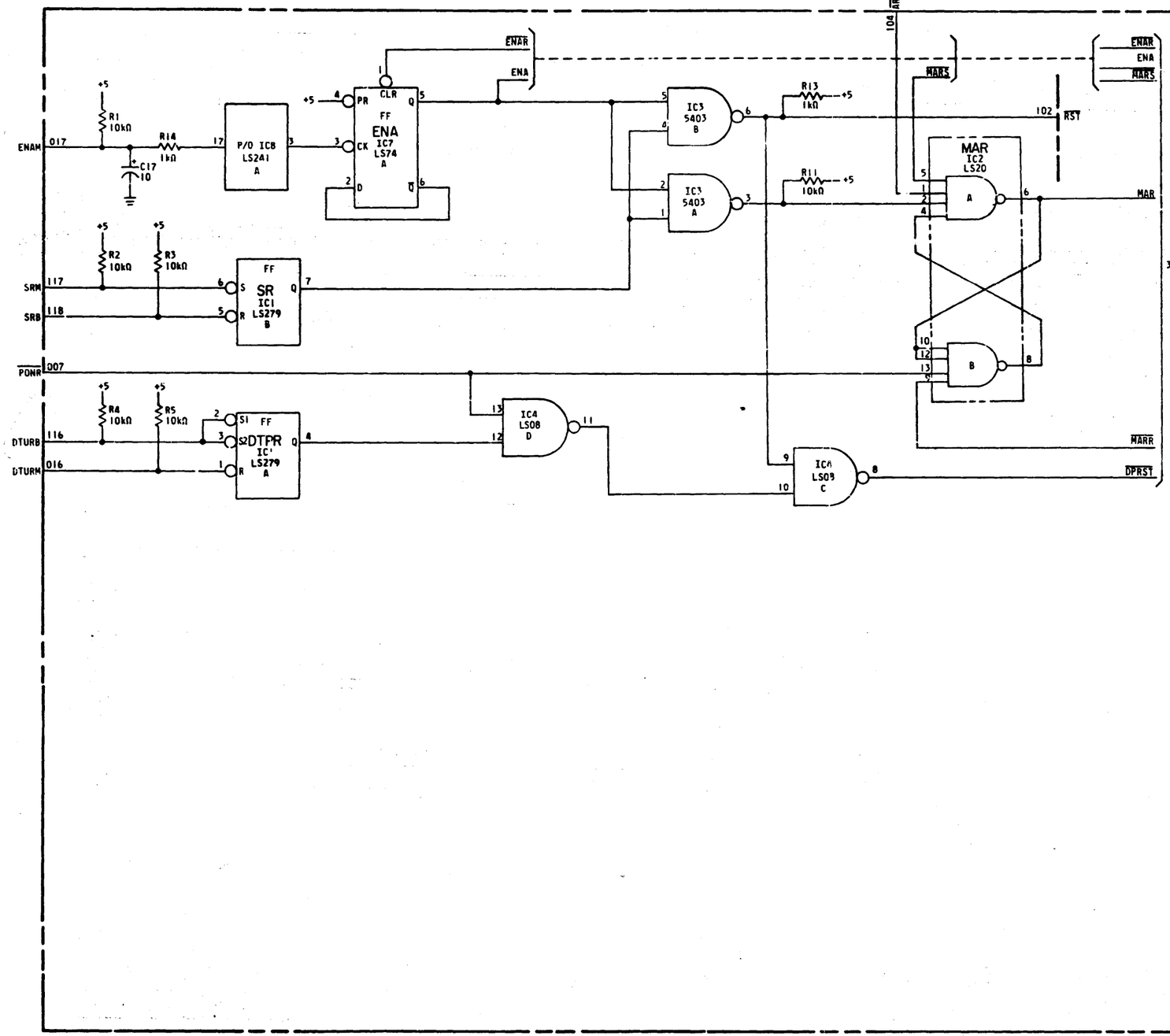
DWG SIZE 6S | ISSUE 1

BELL LABORATORIES | CPS-SL88 | 6 SHEETS

E-7000-A(8-79)
PRINTED IN U.S.A.

# PART OF CPS SL88

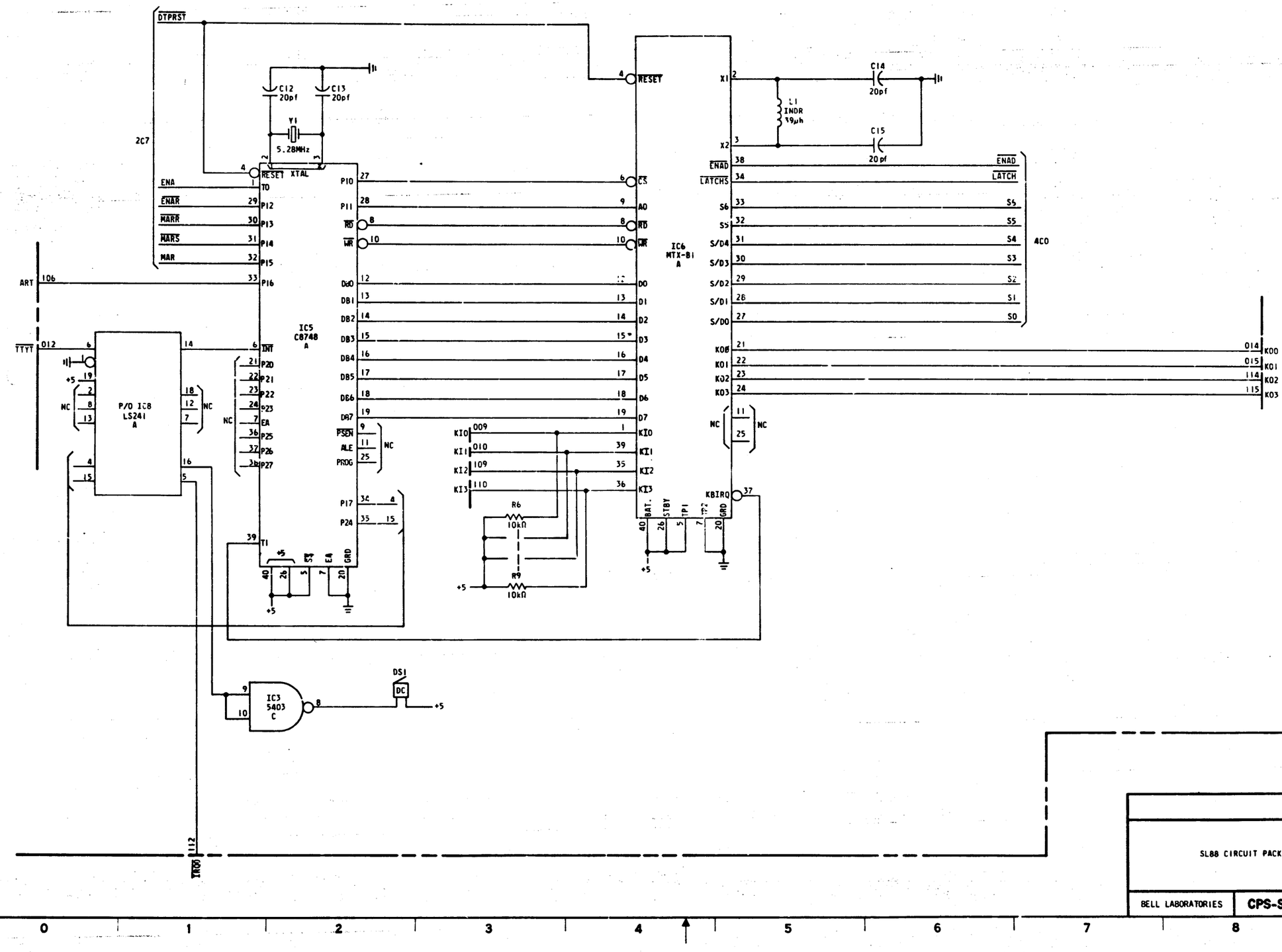
DTP CONTROLLER




| | | | |
|---|---|---|---|
| SL88 CIRCUIT PACK | | DWG SIZE 6S | ISSUE 1 |
| BELL LABORATORIES | CPS-SL88 | | SHEET 2 |

# PART OF CPS SL88

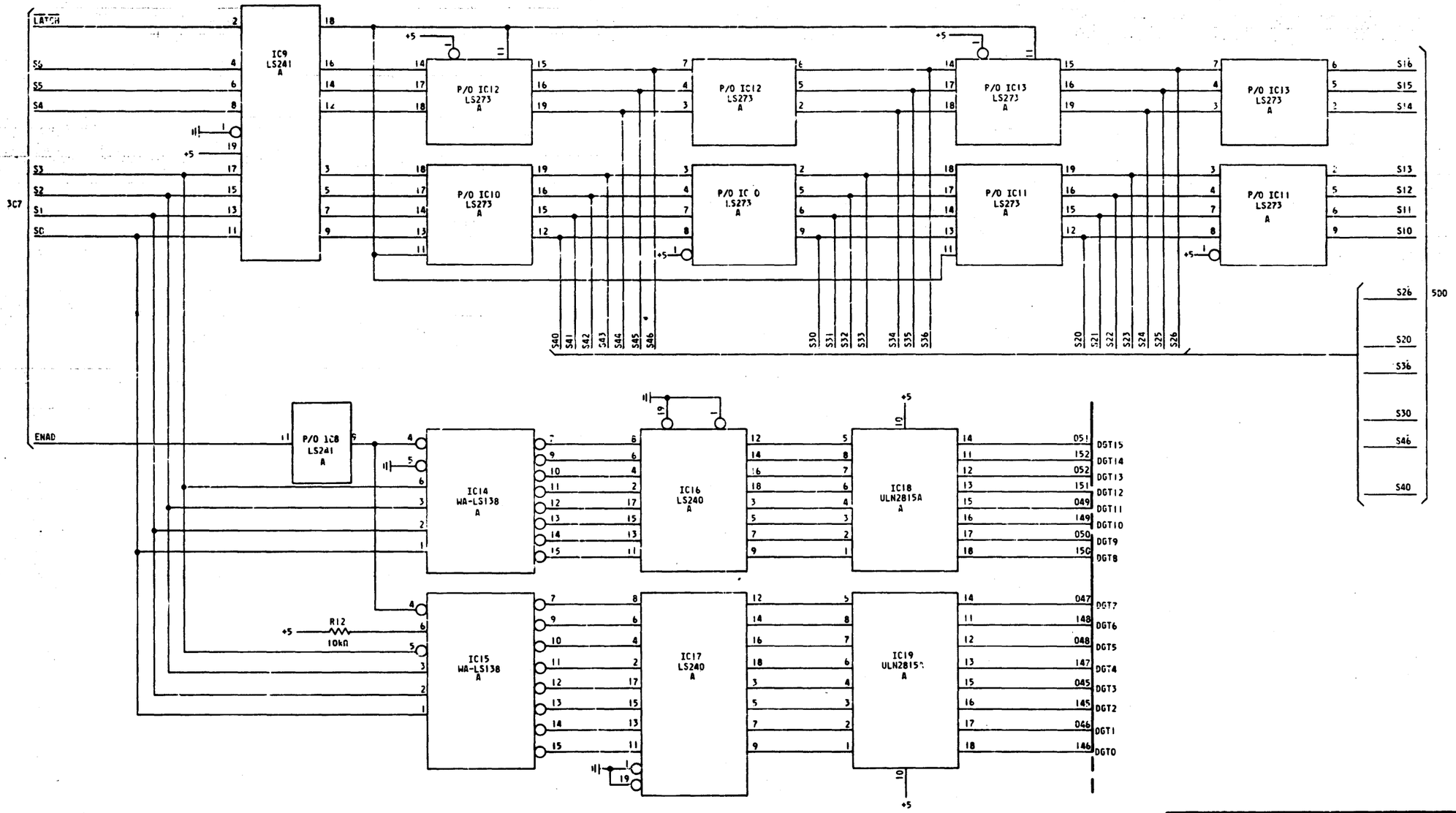
DTP CONTROLLER




| | | | |
|---|---|---|---|
| SL88 CIRCUIT PACK | | DWG SIZE 65 | ISSUE 1 |
| BELL LABORATORIES | CPS-SL88 | | SHEET 3 |

# PART OF CPS SL88

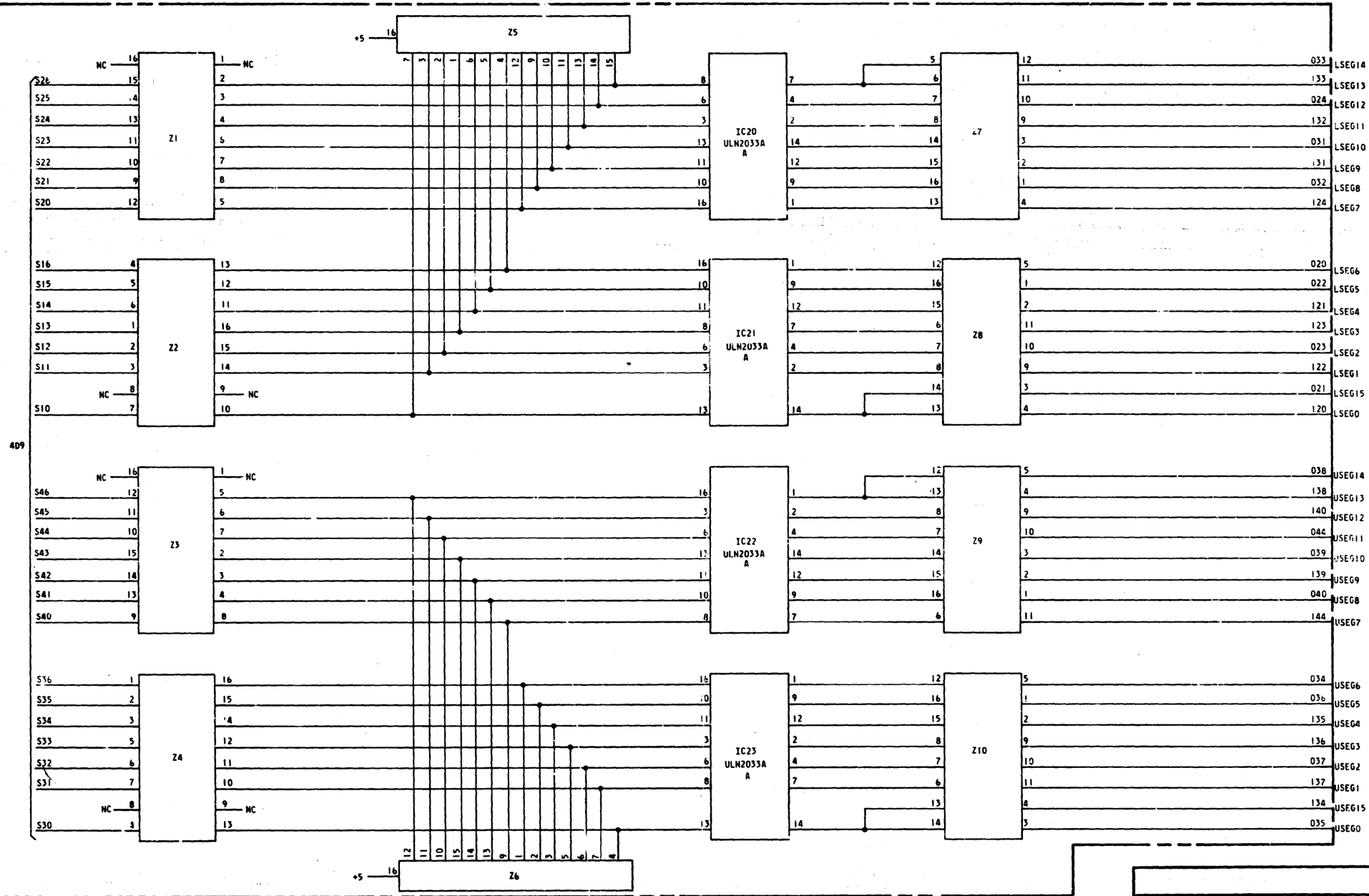
DTP CONTROLLER




| | | |
|---|---|---|
| SL88 CIRCUIT PACK | DWG SIZE 6S | ISSUE 1 |
| BELL LABORATORIES | CPS-SL88 | SHEET 4 |

# PART OF CPS SL88

DTP CONTROLLER




| | | |
|---|---|---|
| SL88 CIRCUIT PACK | DWG SIZE 6S | ISSUE 1 |
| BELL LABORATORIES | CPS-SL88 | SHEET 5 |

# PART OF CPS SL88

DTP CONTROLLER

COMPONENT LIST

CIRCUITS, INTEGRATED

| DESIG | IC1 | | IC2 | | IC3 | | IC4 | | IC5 | | IC6 | | IC7 | | IC8 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CODE | WA-LS279 | | WA-LS20 | | SN5403J* | | WA-LS08 | | C8748 OR C8748-4 | | MTX-81 | | WA-LS74 | | SN54LS241* | |
| ELEMENT | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC |
| A | DTPR | 2D1 | MAR | 2B5 | | 2B4 | | SPARE | | 3B2 | ENA | 3C4 | | 2B2 | 8 ELEM A | 2B1 |
| B | SR | 2C1 | | 2B3 | | 2C4 | | SPARE | | | | | | SPARE | | 3D0 |
| C | | SPARE | | | | 3G2 | | 2C4 | | | | | | | | 4E2 |
| D | | SPARE | | | | SPARE | | 2D3 | | | | | | | | |
| E | | | | | | | | | | | | | | | | |
| F | | | | | | | | | | | | | | | | |
| G | | | | | | | | | | | | | | | | |

| DESIG | IC9 | | IC10 | | IC11 | | IC12 | | IC13 | | IC14 | | IC15 | | IC16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CODE | SN54LS241* | | SN54LS273J* | | SN54LS273J* | | SN54LS273J* | | SN54LS273J* | | WA-LS138 | | WA-LS138 | | WA-LS240 | |
| ELEMENT | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC |
| A | | 4B2 | ELEM A | 4C3 | ELEM A | 4C6 | ELEM A | 3B3 | ELEM A | 4B6 | | 4E3 | | 4F3 | | 4E4 |
| B | | | | 4C5 | | 4C8 | | 4B5 | | 4B8 | | | | | | |
| C | | | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | | | |
| E | | | | | | | | | | | | | | | | |
| F | | | | | | | | | | | | | | | | |
| G | | | | | | | | | | | | | | | | |

| DESIG | IC17 | | IC18 | | IC19 | | IC20 | | IC21 | | IC22 | | IC23 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CODE | WA-LS240 | | KS-22399,L1,OR ULN2815** | | KS-22399,L1,OR ULN2815** | | KS-22400,L1,OR ULN2033** | | KS-22400,L1,OR ULN2033** | | KS-22400,L1,OR ULN2033** | | KS-22400,L1,OR ULN2033** | | | |
| ELEMENT | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC | DESIG | SH LOC |
| A | | 4F4 | | 4E6 | | 4F6 | | 5B5 | | 5D5 | | 5E5 | | 5G5 | | |
| B | | | | | | | | | | | | | | | | |
| C | | | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | | | |
| E | | | | | | | | | | | | | | | | |
| F | | | | | | | | | | | | | | | | |
| G | | | | | | | | | | | | | | | | |

* = TEXAS INSTRUMENTS
** = SPRAGUE

BUZZER

| DESIG | CODE |
|---|---|
| DS1 | AI-254, PROJECTS UNLIMITED |

CAPACITOR

| DESIG | CODE |
|---|---|
| C1 | 6018 |
| [10] C2-11 | KS-20736,L4,.1 |
| [4] C12-15 | KS-19774,L7,22pf |
| C16 | 6046 |
| C17 | 6018 |
| C18 | KS-20736,L4,.1 |

CRYSTAL

| DESIG | CODE |
|---|---|
| Y1 | EC-18,5.28 MHz |

INDUCTOR

| DESIG | CODE |
|---|---|
| L1 | 3399-32,39,uH (CAMBION) |

NETWORK

| DESIG | CODE |
|---|---|
| [4] Z1-4 | 761-3-R,2.2kΩ,C.T.S. BYRNE INC OR KS-21288,L1,2.2kΩ |
| [2] Z5,6 | 761-1-R,3.3kΩ,C.T.S. BYRNE INC OR KS-21288,L4,3.3kΩ |
| [4] Z7-10 | 761-3-R,50,C.T.S. BYRNE INC OR KS-21288,L1,50 |

RESISTORS

| DESIG | CODE |
|---|---|
| [12] R1-12 | KS-20616,L1A,10kΩ |
| [2] R13,14 | KS-20616,L1,1kΩ |

INPUT/OUTPUT INFORMATION

CIRCUIT DESCRIPTION

THE DTP CONTROLLER (SL88) IN CONJUNCTION WITH THE DTP PANEL (ED-94984-30) AND THE RESET AND SANITY BOARD (SL87) PROVIDE THE MANUAL INTERFACE TO THE CPU (SL86,SD-94868-01) AND TO THE ALARM CIRCUITS OF SD-28130-01.

SYSTEM & DTP RESET CIRCUITS ARE SHOWN ON SHEET 2. THE SYSTEM RESET (SR) F/F DEBOUNCES THE SYSTEM RESTART KEY AND ASSERTS THE $\overline{RST}$ LEAD (LOW) IF THE ENABLE (ENA) F/F IS SET. ENA IS SET BY OPERATING THE ENABLE KEY. THE ENABLE KEY MUST ALSO BE OPERATED BEFORE THE DTP WILL RESPOND TO THE COMMAND RELATED KEYS.

A MANUAL SYSTEM RESTART OR AN AUTOMATIC RESTART WILL SET THE THE MANUAL/AUTOMATIC F/F (MAR). MAR CAN BE TESTED BY THE SYSTEM TO DETERMINE THE SOURCE OF A RESTART. MAR CAN ALSO BE CONTROLLED BY THE SYSTEM SOFTWARE FOR TESTING. MAR IS INITIALIZED RESET BY THE POWER ON RESET (PONR) LEAD.

THE DTP IS ALSO RESET BY ANY SYSTEM RESTART OR BY OPERATION OF THE DTU RESTART KEY. THE DTPR F/F DEBOUNCES THIS KEY AND ASSERTS THE $\overline{DTP\ RST}$ LEAD. $\overline{DTP\ RST}$ RESTARTS THE MICRO-COMPUTER (IC5 SHEET 3) SOFTWARE AND INITIALIZES THE KEYBOARD, DISPLAY CONTROLLER IC6.

THE DTP IS CONTROLLED BY THE MICRO-COMPUTER IC5. IC5 SOFTWARE CONTROLS THE FOLLOWING:

- SERIAL COMMUNICATIONS TO AND FROM THE CPU SL86.
- COMMUNICATIONS WITH THE KEYBOARD AND DISPLAY CONTF IC6.
- TESTS THE ENA F/F TO DETERMINE IF IT SHOULD RESPOND TO INPUT FROM THE COMMAND KEYS.
- TEST AND CONTROL THE MAR F/F (MAR,$\overline{MARS}$,$\overline{MARR}$).
- TEST THE AUTOMATIC RESTART LEAD (ART).
- RESET THE ENA F/F (ENAR) AFTER IT DETERMINES THAT THERE HAVE BEEN NO INPUTS FROM THE PANEL IN THE LAST 5 MINUTES.
- BLANK DISPLAY IF NO ACTIVITY FROM THE SYSTEM OR PANEL.
- INITIALIZE KEYBOARD AND DISPLAY CONTROL REGISTERS.

SERIAL INPUT FROM THE SL86 GENERATES AN EXTERNAL INTERRUPT ON IC5 WHEN A "MARK" TO "SPACE" CHANGE ON THE $\overline{TTY}$ IS DETECTED. THE IC5 INTERNAL TIMER IS THEN USED TO GENERATE INTERRUPTS TO SAMPLE THE $\overline{TTYT}$ LEAD.

SERIAL OUTPUT IS ALSO TIMER INTERRUPT DRIVEN. THE $\overline{IRQO}$ LEAD IS CONTROLLED BY AN IC5 I/O PORT. DATA RATE TO THIS PORT IS DETERMINED BY THE IC5 INTERVAL TIMER. THE CHANNEL DATA RATE IS 110 BAUD. THE STATUS OF THE CHANNEL IS TESTED FOR IDLE BEFORE TRANSMITTING.

THE KEYBOARD AND DISPLAY CONTROLLER IC6, SCANS THE 16 KEY KEYMATRIX AND THE 32 CHARACTER ALPHA-NUMERIC DISPLAY IN A TIME MULTIPLEX FASHION. WHEN A KEY IS OPERATED AN INTERRUPT IS GENERATED TO IC5. IC5 THEN ADDRESSES

CIRCUIT DESCRIPTION (CONT'D)

IC6 (A0,$\overline{CE}$) AND READS (RD) THE ADDRESS OF THE KEY. IC5 INTERPRETS THE KEY AND TRANSMITS IT TO THE CPU SL86. THE CPU ECHOS THE DATA BACK TO THE DTP CONTROLLER IN A COMMAND WHICH WILL DISPLAY THE KEY OPERATED.

IC6 CONTAINS A 32 BYTE DISPLAY REFRESH RAM. THE CPU SL86 WRITES A PARTICULAR CHARACTER BY FIRST POSITIONING THE DISPLAY CURSOR AND THEN WRITING THE NEW DATA AT THAT CURSOR LOCATION. THE CURSOR IS THE RAM ADDRESS. COMMANDS FROM THE CPU SL86 TO THE DISPLAY CONTROLLER ARE VIA THE SERIAL LINK AND IC5. IC5 INTERPRETS THE CPU COMMANDS AND PERFORMS THE HANDSHAKING WITH IC6.

THE DISPLAY IS REFRESHED IN A DUAL SCAN MODE. THE MODE, PROVIDED BY IC6 REDUCES PEAK CURRENT REQUIREMENTS BY STROBING TWO CHARACTERS SIMULTANEOUSLY WHICH INCREASES THE DUTY CYCLE.

SEGMENT DATA (S0-S6) FOR TWO OF THE 16 SEGMENT DISPLAYS IS LATCHED ($\overline{LATCH}$) INTO IC10-IC13 (SHEET 4). ONE OF THE DIGIT DRIVERS ON IC18 OR IC19 IS THEN ENABLED ($\overline{ENAD}$) WHICH LIGHTS TWO CHARACTERS. NEW SEGMENT DATA IS THEN LATCHED AND THE NEXT DIGIT DRIVER IS ENABLED. THE REFRESH RATE IS ~ 100 Hz.

DIGIT INFORMATION IS SYNCHRONIZED WITH THE SEGMENT DATA BY IC6. DIGIT INFORMATION IS CONTROLLED BY DATA ON THE S0-S3 LEADS AND ONE-OUT-OF-16 PAIRS OF CHARACTERS IS DECODED BY IC14 AND IC15.

THE SEGMENT DRIVERS IC20-23 ARE SHOWN ON SHEET 5. THE PEAK SEGMENT CURRENT IS 20MA. ALTHOUGH THE DISPLAYS ARE 16 SEGMENT, THE DISPLAY CONTROLLER IC6 PROVIDES DATA FOR A 14 SEGMENT DISPLAY. THEREFORE TWO OF THE SEGMENTS ARE DRIVEN WITH THE SAME DATA AS ARE TWO OTHERS.

| | | | |
|---|---|---|---|
| SL88 CIRCUIT PACK | | DWG SIZE E5 | ISSUE 1 |
| BELL LABORATORIES | CPS-SL88 | | SHEET 6 |