

A01

MAY 1 1981

BELL TELEPHONE LABORATORIES, INCORPORATED

5-89

COMMON SYSTEMS  
FOR USE WITH NO. 3 ESS  
ARRANGED WITH 2-WIRE FEATURES  
INTERPROCESSOR STORE BUS TEST  
(CDGSON)

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ISSUE 5  
02/05/81

AT&TCO  
SPCS

PR-1C928-50  
89 PAGES

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## SECTION DICTIONARY

NUMBER	NAME	MAXIMUM	ORIGIN	TYP	ADDRESS-MODIFICATION
01	CSTON1	0000515		C	
02	CSOONUB	0000023		C	
03	CPATCH	0000000		C	
04	CPATCH1	0000000		C	
05	CPATCH2	0000000		C	
06	CPATCH3	0000000		C	
07	CPATCH7	0000000		C	
08	TFAPCH2	0000000		C	
09	TPATCH	0000000		C	

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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VERSION W77D OF SWAP; VERSION

OF EPL

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CDGSON

W77D

0027122  
0027122  
0027122

```

01      DBNAM  N033E3I3.OFF.DATABASE
02      RELNAM N03ESS
03      GETLIB LIBRARY, MEMBER=MOPTBL
04      GETLIB LIBRARY, MEMBER=SYSMAC
05      GETLIB LIBRARY, MEMBER=SYSSYM
06      GETLIB LIBRARY, MEMBER=PATCH2
07      FIRSTOPTSS
08      VERSION 3ACC, FIELD, ESS2E
09      PATCHINIT
10     N033E3I3.OFF.OPMS(0) DECK
11      DSQUAL  N033E3I3
12      LISTING N, CRUNCH=Y, SYSOUT=N
13     #####
14     ##
15     ## UNIX ID = N03PAG
16     ##
17     #####
18     #####
19     ###
20     #### pid date      time rel
21     ###
22     #### cdgson 1/24/81 17:38:05 7.1.1.1
23     ###
24     #####

```

```

31 # THE LATEST REGEN OF THIS DATA SET OCCURRED ON PD1/06/77
32     NAME      CDGSON

```

```

36 ## The following is a list of the valid csects for program CDGSON

```

```

38 CSTON1 CSECT
39 CSNSUB CSECT

```

```

42 ## The following csects are necessary for patching

```

```

44 CPATCH CSECT
45 CPATCH1 CSECT
46 CPATCH2 CSECT
47 CPATCH3 CSECT
48 CPATCH7 CSECT

```

0027122  
00276370111432  
0112562  
0114107  
0115073  
0121236

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CDGSON

W77D

0116774

01 TFAPCH2 CSECT

0600000

03 TPATCH CSECT

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CDGSON W77D

```
07 GETLIB MEMBER=DGNMAC
08 GETLIB MEMBER=MEMDGM
09 GETLIB MEMBER=BSAIMAC
10 GETLIB MEMBER=CTVTAB
```

```
17 TDATA EXTERN STRLIM
18 TDATA EXTERN WDSTR
19 CBLM EXTERN WAIT
20 CDGMM EXTERN LOOPIND
21 CSYSUB EXTERN INSYNC
22 CTSD EXTERN PAGSCR
```

INTERPROCESSOR STORE BUS TEST

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0600000

```
01 BEGIN DIAG DGSON
-001- 02 CDGNN EXTERN NMICRO
-001- 03 CDGNN EXTERN NRETRN
-001- 04 CDGNN EXTERN N2RETRN
-001- 05 CDGNN EXTERN NSTRT
-001- 06 CDGNN EXTERN NSTOP
-001- 07 CDGNN EXTERN NDISABA
-001- 08 CDGNN EXTERN NDISABB
-001- 09 CDGNN EXTERN NSTRTCLK
-001- 10 CDGNN EXTERN NSTPCLK
-001- 11 CDGNN EXTERN NTGCLK
-001- 12 CDGNN EXTERN NRESCLK
-001- 13 CDGNN EXTERN NZERO_ER
-001- 14 CDGNN EXTERN NPROS
-001- 15 CDGNN EXTERN NTESTSEG
-001- 16 CDGNN EXTERN NFAILTST
-001- 17 CDGNN EXTERN NTTY
-001- 18 CDGNN EXTERN NMASK
-001- 19 CDGNN EXTERN NPASSTST
-001- 20 CDGNN EXTERN NSEND
-001- 21 CDGNN EXTERN N2SEND
-001- 22 CDGNN EXTERN NADD OFF
-001- 23 CDGNN EXTERN NADMIC
-001- 24 CDGNN EXTERN NLD MIR
-001- 25 CDGNN EXTERN NEXECUTE
-001- 26 CDGNN EXTERN NCOMPARE
-001- 27 CDGNN EXTERN NFRZ
-001- 28 CDGNN EXTERN NBEGIN
-001- 29 CDGNN EXTERN NLP_END
-001- 30 CDGNN EXTERN NSKIP
-001- 31 CDGNN EXTERN NABT
-001- 32 CDGNN EXTERN NRD MICRO
-001- 33 CDGNN EXTERN NCLRMS
-001- 34 CDGNN EXTERN NNO3CD
-001- 35 CDGNN EXTERN NMTTEST
-001- 36 CDGNN EXTERN NZERPT
-001- 37 CDGNN EXTERN NFLBITS
-001- 38 CDGNN DIRECT INTRPN03
-001- 39 CDGNN EXTERN NBGN
-001- 40 CDGNOF EXTERN PASSOFF
-001- 41 CDGNOF EXTERN FAILOFF
-001- 42 CDGNN EXTERN SLDNCHBF
-001- 43 CDGNN EXTERN SLDMIRLF
-001- 44 CDGNN EXTERN SMCHF
-001- 45 CDGNN EXTERN NRTNBLM
-001- 46 CDGNN EXTERN NWDTST
```

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CDGSON W77D

-001- 01 # THIS DIAGNOSTIC PROGRAM IS ALL OR PARTIALLY WRITTEN IN A MACRO  
-001- 02 # LANGUAGE WHICH PRODUCES TABLES WHICH ARE INTERPRETED BY THE  
-001- 03 # DIAGNOSTIC MONITOR PROGRAM. FOR INFORMATION REGARDING THE  
-001- 04 # STRUCTURE OF THE TABLES, SEE THE SECTION OF PROGRAM CDGNM (PR-1C910-01)  
-001- 05 # ENTITLED "DIAGNOSTIC TABLE INTERPRETER". FOR A GENERAL DESCRIPTION  
-001- 06 # OF THE DIAGNOSTIC PHILOSOPHY AND THE DETAILED REPAIR PROCEEDURE,  
-001- 07 # SEE THE TROUBLE LOCATION MANUAL (TLM-1C900) SECTION B.

INTERPROCESSOR STORE BUS TEST

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0600000

01 SYMLIB

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CDGSON

W77D

## -002- 01 # EXTERNS REQUIRED BY STORE DIAGNOSTIC TESTS:

-002- 04 MASACS EXTERN MASCIOSC

-002- 06 CBLM EXTERN PRTMASER

-002- 07 CBLM EXTERN WAIT

-002- 09 CDGNM EXTERN LOOPIND

-002- 10 CDGNM EXTERN NOSTPMES

-002- 11 CDGNM EXTERN PASSTST

-002- 12 CTSD EXTERN DGNLIM

-002- 14 CDGSBS EXTERN MEMOP

-002- 15 CDGSBS EXTERN MEMOPI

-002- 17 CDGSFA EXTERN FOBNDX

-002- 19 CDGSIO DIRECT MASIOM

-002- 20 CDGSIO EXTERN MSELMSK

-002- 21 CDGSIO EXTERN MODSIZE

-002- 22 CDGSIO EXTERN STRSIZE

-002- 23 CDGSIO EXTERN STSELMSK

-002- 24 CDGSIO EXTERN FINAL

-002- 25 CDGSIO EXTERN CONTPREP

-002- 28 CSYSUB EXTERN EXCOFLPG

-002- 29 CSYSUB EXTERN INIT\_OCC

-002- 30 CSYSUB EXTERN INITOST

-002- 31 CSYSUB EXTERN INSYNC

-002- 32 CSYSUB EXTERN RGCHKADR

-002- 33 CSYSUB EXTERN UPD\_OTS

-002- 35 CTSD EXTERN MASERCNT

-002- 36 CTSD EXTERN PAGSCR

-002- 37 CTSD EXTERN DGREQ

-002- 39 MASACS EXTERN MASONOFF

-002- 41 TDATA EXTERN STRLIM

-002- 42 TDATA EXTERN WDSTR

-002- 43 TDATA EXTERN WPTBL

INTERPROCESSOR STORE BUS TEST

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## -002- 01 # STORE DIAGNOSTIC REGISTER DEFINITIONS

0000010	-002- 04	CHKNDX	EQR	8	# INDEX REGISTER FOR REFRESH SELECT CHECK
0000010	-002- 05	F0BCNT	EQR	8	# SCRATCH REG FOR CURRENT FANOUT BOARD COUNT
0000011	-002- 07	RANGE	EQR	9	# NUMBER OF OFF-LINE WORDS TO BE TESTED

## -002- 11 # REGISTER SYMBOLS USED IN THE MEMORY MODULE TEST:

0000000	-002- 12	PATBAK	EQR	R0	# DATA READ/WRITTEN VIA OTHER-STORE
0000001	-002- 13	HIPATBAK	EQR	R1	# HIGH DATA READ/WRITTEN VIA OTHER-STORE
	-002- 14	HIPATBAKXT	SYN	R1XT	# DEFINE FOR IGNORANT MIMODE MACRO
0000002	-002- 15	BLKMSK	EQR	R2	# MASK TO BLOCK INTERRUPTS & CHECKS
0000003	-002- 16	STRSTAT	EQR	R3	# SAVE (WIDE) STORE STATUS
0000004	-002- 17	LSTPAT	EQR	R4	# PATTERN PREVIOUSLY WRITTEN
0000005	-002- 18	NXTPAT	EQR	R5	# PATTERN CURRENTLY BEING WRITTEN
0000006	-002- 19	PATNDX	EQR	R6	# NUMBER OF TEST PATTERN BEING MATCHED
0000007	-002- 20	MNRNDX	EQR	R7	# MINOR LOOP INDEX
0000010	-002- 21	ERSAVE	EQR	R8	# ERROR REGISTER AFTER OTHER-STORE READ
0000010	-002- 22	PARSLT	EQR	R8	# PARITY TEST RESULTS - FIELD ONLY
0000014	-002- 23	MEMADDR0	EQR	R12	# UPPER ADDRESS BITS OF MEMORY TEST AREA
0000015	-002- 24	MEMADDR1	EQR	R13	# LOWER ADDRESS BITS OF MEMORY TEST AREA
0000014	-002- 25	MEMADDR	EQUA	RA0	# BASE ADDRESS OF MEMORY TEST AREA
0000016	-002- 26	PATADDR	EQUA	RA1	# ADDRESS OF TEST PATTERN TABLE

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CDGSON W77D

-002- 01 # FUNCTION OF BITS WITHIN I/O MESSAGE SENT TO STORE:  
 -002- 02 CIOBUF LAYOUT

-002- 05 CINIT	ITEM	1	# MAIN STORE CONTROLLER INITIALIZATION
-002- 06 CKSTP	ITEM	1	# CONTROLLER CLOCK STEP
-002- 07 CKHLT	ITEM	1	# CONTROLLER CLOCK HALT
-002- 08 REFST	ITEM	1	# STORE REFRESH STOP
-002- 09 STORDER	ITEM	8	# 4/8 MAINTENANCE STATE CODE
-002- 10 O10TM	ITEM	1	# 0-10 BIT TIMING SHIFTER FAKE
-002- 11 LDFG	ITEM	1	# ORDER CHECKER EXCLUSIVE-OR LOAD
-002- 12 FSEL	ITEM	1	# STORE SELECT FORCE ON TIMING BOARD A
-002- 13 FBT09	ITEM	1	# FORCE BIT 15 ACTIVE IN MAIN SHIFTER
-002- 14	LOEND		
-005- 15	#		

CIOBUF	FBT09	FSEL	LDFG	O10TM	STORDER	REFST	CKHLT	CKSTP	CINIT							
001	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

4/8 MAINTENANCE STATE CODE

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

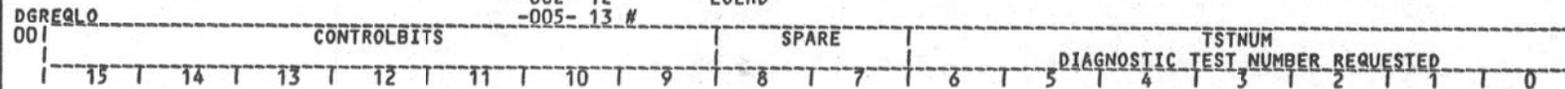
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CDGSON W77D

-002- 01 # LAYOUT OF DIAGNOSTIC REQUEST WORD (DGREQ) WITH TEST NUMBER REQUESTED  
 -002- 02 # NOTES: 1. REST OF BITS (CONTROLBITS) ARE DEFINED BY DGREQIP LAYOUT  
 -002- 03 # FOUND IN PROLOGUE OF DIAGNOSTIC MONITOR (CDGNM)  
 -002- 04 # 2. IF TEST NUMBER (TSTNUM) IS ZERO, THE ENTIRE DIAGNOSTIC  
 -002- 05 # TEST SEQUENCE HAS BEEN REQUESTED  
 -002- 06 # 3. STORAGE SPACE FOR DGREQ IS ALLOCATED IN CTSD

-002- 09 TSTNUM ITEM 7 # DIAGNOSTIC TEST NUMBER REQUESTED  
 -002- 10 SPARE ITEM 2  
 -002- 11 CONTROLBITS ITEM 7  
 -002- 12 LOEND  
 -005- 13 #



INTERPROCESSOR STORE BUS TEST

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-002- 01 # STORAGE FORMAT FOR MAIN STORE (MY & OTHER) SUBCHANNEL ADDRESS:

-002- 04	MSSCO	ITEM	16	#	ADDRESS OF MY STORE SUBCHANNEL 0
-002- 05	OSSCO	ITEM	16	#	ADDRESS OF OTHER STORE SUBCHANNEL 0
-002- 06	MSSC1	ITEM	16	#	ADDRESS OF MY STORE SUBCHANNEL 1
-002- 07	OSSC1	ITEM	16	#	ADDRESS OF OTHER STORE SUBCHANNEL 1
-002- 08	MSSC2	ITEM	16	#	ADDRESS OF MY STORE SUBCHANNEL 2
-002- 09	OSSC2	ITEM	16	#	ADDRESS OF OTHER STORE SUBCHANNEL 2
-002- 10	MSSC3	ITEM	16	#	ADDRESS OF MY STORE SUBCHANNEL 3
-002- 11	OSSC3	ITEM	16	#	ADDRESS OF OTHER STORE SUBCHANNEL 3
-002- 12		LOEND			
-002- 13	#				

MASCIOSC

00	MSSCO	ADDRESS OF MY STORE SUBCHANNEL 0
01	OSSCO	ADDRESS OF OTHER STORE SUBCHANNEL 0
02	MSSC1	ADDRESS OF MY STORE SUBCHANNEL 1
03	OSSC1	ADDRESS OF OTHER STORE SUBCHANNEL 1
04	MSSC2	ADDRESS OF MY STORE SUBCHANNEL 2
05	OSSC2	ADDRESS OF OTHER STORE SUBCHANNEL 2
06	MSSC3	ADDRESS OF MY STORE SUBCHANNEL 3
07	OSSC3	ADDRESS OF OTHER STORE SUBCHANNEL 3

INTERPROCESSOR STORE BUS TEST

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```

-002- 01 # WORDS IN PAGING BUFFER USED BY STORE DIAGNOSTIC TESTS:
-002- 02 LOOPSUB ITEM 16 # ADDRESS OF SUBSTITUTE FOR 'LOOP' IN TTY
                           TROUBLE MESSAGE
-002- 04 IOADDR ITEM 16 # I/O SUBCHANNEL ADDRESS FOR CURRENT
                           STORE CONTROLLER
-002- 06 FOBNUM ITEM 16 # NUMBER OF MEMORY MODULES (OR FANOUT
                           BOARDS) IN STORE CURRENTLY UNDER TEST
-002- 08 TIMSAV ITEM 16 # SAVE TIMING CONSTANT FOR TIMEOUT
                           SUBROUTINE
-002- 10 UPADDR ITEM ADDR # ADDRESS OF NEXT BLOCK OF MEMORY TO BE
                           UPDATED AFTER MEMORY PATTERN TEST
-002- 12 BASADDR ITEM ADDR # BASE ADDRESS OF STORE/MOD UNDER TEST

```

```

-002- 15 LOEND
-005- 16 #

```

PAGSCR

24	LOOPSUB
25	ADDRESS OF SUBSTITUTE FOR 'LOOP' IN TTY TROUBLE MESSAGE
26	IOADDR
27	I/O SUBCHANNEL ADDRESS FOR CURRENT STORE CONTROLLER
28	FOBNUM
29	NUMBER OF MEMORY MODULES (OR FANOUT BOARDS) IN STORE CURRENTLY UNDER TEST
30	TIMSAV
31	SAVE TIMING CONSTANT FOR TIMEOUT SUBROUTINE
	UPADDR
	BASADDR
	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

INTERPROCESSOR STORE BUS TEST

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CDGSON W77D

-002- 01 # STORE ERROR REGISTER (SER) BIT ASSIGNMENT:

-002- 02 # NOTE: THESE INPUTS ARE ENABLED BY BIT09 OF THE MAIN SHIFTER

-002- 05 SER LAYOUT  
 -002- 06 FOBTERB ITEM 1 # STORE TIMING ERROR FROM UNSELECTED FOB  
 -002- 07 MPXER ITEM 1 # MULTIPLEXOR ERROR DETECTED BY CHECK BOARD  
 -002- 09 CHDIF ITEM 1 # ERROR INDICATED BY STORE COMMAND CHECKER  
 -002- 11 SCMER ITEM 1 # PREMATURE STORE COMPLETE(SCM)  
 -002- 12 SHER ITEM 1 # ERROR IN MAIN SHIFTER OPERATION  
 -002- 13 MODER ITEM 1 # ALL-SEEMS-WELL SIGNAL NOT RECEIVED FROM MODULE(FOB) ACCESSED DURING NORMAL CYCL  
 -002- 15 RSELER ITEM 1 # ALL MEMORY MODULES(FOBS) NOT SELECTED DURING REFRESH  
 -002- 17 FOBTERA ITEM 1 # STORE TIMING ERROR FROM SELECTED FOB  
 -002- 18 FOBPARER ITEM 1 # PARITY ERROR DETECTED IN ADDRESS REACHING FANOUT BOARD(S)  
 -004- 20 ##### FOBPARER WILL APPEAR AS FOBPARE IN PICTURES  
 -002- 21 DHPER ITEM 1 # ERROR IN PARITY OVER HIGH DATA BITS  
 -002- 22 PWER ITEM 1 # ERROR IN PARITY FOR WIDE STORE  
 -002- 23 TBER ITEM 1 # ERROR DETECTED ON TIMING BOARD  
 -002- 24 ITEM 1 # SPARE  
 -002- 25 DLPER ITEM 1 # ERROR IN PARITY OVER LOW DATA BITS  
 -002- 26 ITEM 1 # SPARE  
 -002- 27 ITEM 1 # RESERVED  
 -002- 28 LOEND  
 -005- 29 #

SER	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
001	SPARE	SPARE	DLPER	SPARE	TBER	PWER	DHPER	FOBPARE	FOBTERA	RSELER	MODER	SHER	SCMER	CHDIF	MPXER	FOBTERB

INTERPROCESSOR STORE BUS TEST

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-002- 01 # STORE BUS CHECK BIT ASSIGNMENTS IN RESPONSE MESSAGE:  
 -002- 02 # NOTE: THESE INPUTS ARE ENABLED BY ISOLATE CHECK(ISOCHK) I/O ORDER  
 -002- 03 # W/ LOAD F & G(LDFG) OPTION SET

-002- 06 ISOBTS ITEM 7 # SDO-6,SD8-14 ISOLATE TEST RESULTS  
 -002- 07 RSVDO ITEM 1 # SD7,SD15 ISOLATE TEST RESULT - ONLY  
 # GATED INTO BY LOAD I/O DECODER CHECK  
 # (LOADCHK) OPTION  
 -002- 10 WDISOL ITEM 4 # RESULTS OF WIDE DATA(SD16-23) ISOLATE  
 -002- 11 SDPCK ITEM 1 # RESULT OF STORE DATA PARITY ISOLATION  
 -002- 12 ZEPCK ITEM 1 # RESULT OF EXTENDED(3 BIT) PARITY  
 # ISOLATE  
 -002- 14 CTRLCK ITEM 1 # RESULT OF STORE CONTROL LEADS ISOLATION  
 -002- 15 FXORG ITEM 1 # I/O ORDER CHECKER EXCLUSIVE-OR RESULT  
 -002- 16 LOEND  
 -005- 17 #

CHKWRD	FXORG	CTRLCK	ZEPCK	SDPCK	WDISOL	RSVDO	ISOBTS	SDO-6,SD8-14 ISOLATE TEST RESULTS								
001	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

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CDGSON W77D

-002- 01 # REFRESH SELECT CHECK BIT ASSIGNMENTS IN STORE ERROR REGISTER  
 -002- 02 # NOTE: THESE INPUTS ARE ENABLED BY EXTERNAL-ERROR-LOAD(EXERLD) ORDER

-002- 05 RSEL06 ITEM 7 # REFRESH SELECTS FROM FANOUT BOARDS 0-6  
 -002- 06 RSVD1 ITEM 1 # RESERVED - FOBTERA IS SET AFTER INIT  
 -002- 07 SAPHLP ITEM 1 # STORE ADDRESS PARITY HIGH LOOP RESULT  
 -002- 08 SA17LP ITEM 1 # STORE ADDRESS BIT 17 LOOP RESULT  
 -002- 09 STRSLP ITEM 1 # STORE SELECT ADDRESS BITS LOOP RESULT  
 -002- 10 ITEM 1 # SPARE  
 -002- 11 RSEL7 ITEM 1 # REFRESH SELECT FROM FANOUT BOARD 7  
 -002- 12 ITEM 3 # SPARE BITS  
 -002- 13 LOEND  
 -005- 14 #

RSLCHK

001	SPARE BITS			RSEL7	STRSLP	SA17LP	SAPHLP	RSVD1	RSEL06						REFRESH SELECTS FROM FANOUT BOARDS 0-6	
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0010177 -002- 22 RSELBTS EQU M(RSEL06)IM(RSEL7) # MASK FOR REFRESH SELECT BITS  
 0167600 -002- 23 RSELBTSN EQU (~RSELBTS)&B(1111111111111111)

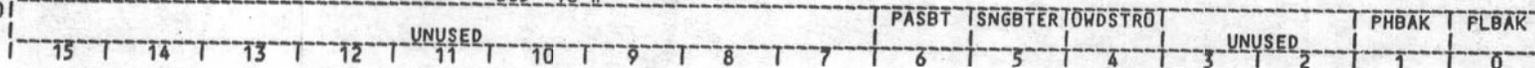
INTERPROCESSOR STORE BUS TEST

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-002- 01 # STORE STATUS REGISTER LAYOUT -- INCL BITS USED IN FIELD VERSION(S) OF TESTS  
 -002- 02 PLBAK ITEM 1 # PARITY LOW VALUE READ BACK  
 -002- 03 PHBAK ITEM 1 # PARITY HIGH VALUE READ BACK  
 -002- 04 ITEM 2 # UNUSED  
 -002- 05 OWDSTRO ITEM 1 # WIDE STORE INDICATOR BIT  
 -002- 06 SNGBTER ITEM 1 # SINGLE BIT ERROR FLAG  
 -002- 07 PASBT ITEM 1 # REPEAT PASS THRU TEST INDICATOR  
 -002- 08 ITEM 9 # UNUSED  
 -002- 09 LOEND  
 -005- 10 #

STRSTAT  
 001



INTERPROCESSOR STORE BUS TEST

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## -002- 01 # STORE DIAGNOSTIC SYMBOL LIBRARY:

```

0000000 -002- 05 BIT0 EQU 0
0000001 -002- 06 BIT1 EQU 1
0000002 -002- 07 BIT2 EQU 2
0000003 -002- 08 BIT3 EQU 3
0000004 -002- 09 BIT4 EQU 4
0000005 -002- 10 BIT5 EQU 5
0000006 -002- 11 BIT6 EQU 6
0000007 -002- 12 BIT7 EQU 7
0000010 -002- 13 BIT8 EQU 8
0000011 -002- 14 BIT9 EQU 9
0000012 -002- 15 BIT10 EQU 10
0000013 -002- 16 BIT11 EQU 11
0000014 -002- 17 BIT12 EQU 12
0000015 -002- 18 BIT13 EQU 13
0000016 -002- 19 BIT14 EQU 14
0000017 -002- 20 BIT15 EQU 15
0000020 -002- 21 BIT16 EQU 16
0000021 -002- 22 BIT17 EQU 17
0000022 -002- 23 BIT18 EQU 18
0000023 -002- 24 BIT19 EQU 19
0000004 -002- 25 FOUR EQU 4
-002- 26 IOBRK TEXT '&' # DELIMITERS FOR I/O ORDER STRINGS
0000000 -002- 27 MOD0 EQU 0
0000001 -002- 28 MOD1 EQU 1
0000002 -002- 29 MOD2 EQU 2
0000003 -002- 30 MOD3 EQU 3
0000004 -002- 31 MOD4 EQU 4
0000005 -002- 32 MOD5 EQU 5
0000006 -002- 33 MOD6 EQU 6
0000007 -002- 34 MOD7 EQU 7
0000001 -002- 35 ONE EQU 1
0177777 -002- 36 ONES EQU 0(177777) # ALL ONE'S REGISTER
0000200 -002- 37 OFLNCHNK EQU B(10000000) # ON-LINE TESTS 128 WORDS/MINOR LOOP
0007760 -002- 38 OFLNDONE EQU B(111111110000) # SIGNAL THAT OFF-LINE MEMORY TEST IS
# DONE

-002- 41 # NOTE: THE FOLLOWING CONSTANTS ALLOW GENERATION OF ARBITRARY PARITY. APPLICABLE
-002- 42 # BITS ARE 0 & 1 SUCH THAT BIT 0 = VALUE FOR PARITY LOW
-002- 43 # BIT 1 = VALUE FOR PARITY HIGH
-002- 44 # DATA BITS (23-16) (15-8) (7-0)
0000020 -002- 45 PRH0LO EQU B(10000) # SET PARITY (WIDE=)HIGH=0 LOW=0
0000005 -002- 46 PRH0L1 EQU B(00101) # SET PARITY (WIDE=)HIGH=0 LOW=1
0000012 -002- 47 PRH1LO EQU B(01010) # SET PARITY (WIDE=)HIGH=1 LOW=0
0000017 -002- 48 PRH1L1 EQU B(01111) # SET PARITY (WIDE=)HIGH=1 LOW=1
0000002 -002- 49 PRWH1LO EQU B(00010) # SET PARITY WIDE=0 HIGH=1 LOW=0

```

0600000

INTERPROCESSOR STORE BUS TEST

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CDGSON W77D

```

0000007 -002- 01 PRWOH1L1 EQU B(00111) # SET PARITY WIDE=0 HIGH=1 LOW=1
0000010 -002- 02 PRW1H0L0 EQU B(01000) # SET PARITY WIDE=1 HIGH=0 LOW=0
0000015 -002- 03 PRW1H0L1 EQU B(01101) # SET PARITY WIDE=1 HIGH=0 LOW=1

0000003 -002- 05 THREE EQU 3
0000002 -002- 06 TWO EQU 2
0010000 -002- 07 WPBLKSIZE EQU 0(10000) # WRITE PROTECT BLOCK SIZE = 4K (4096)
0000000 -002- 08 ZERO EQU 0
0000000 -002- 09 ZEROS EQU 0 # ZERO CONSTANT
0000000 -002- 10 OTEST EQU 0 # VALUES FOR
0000001 -002- 11 ITEST EQU 1 # TEST MACRO

```

```

-002- 18 # MAIN MEMORY STATUS CONSTANTS ASSUMING FOLLOWING CONDITIONS:
-002- 19 # 1. MY STORE BUS PORT IS ISOLATED FROM INPUT FROM OTHER PROCESSOR
-002- 20 # 2. MAIN MEMORY CONTROLLER IS NOT UPDATING OTHER STORE
-002- 21 # 3. MY STORE BUS PORT IS ACCESSING MY STORE, E. NOT REVERSED

```

```

0106263 -002- 24 MTCRD EQU 0(106263) # MAIN MEMORY STATUS FOR MAINTENANCE READ
OPERATION
0106203 -002- 26 MTCWR EQU 0(106203) # MAIN MEMORY STATUS FOR MAINTENANCE
WRITE OPERATION
0106260 -002- 28 NMLRD EQU 0(106260) # MAIN MEMORY STATUS FOR NORMAL READ
OPERATION
0106200 -002- 30 NMLWR EQU 0(106200) # MAIN MEMORY STATUS FOR NORMAL WRITE
OPERATION
0106274 -002- 32 SPRRD EQU 0(106274) # MAIN MEMORY STATUS FOR SPARE READ
OPERATION
0106214 -002- 34 SPRWR EQU 0(106214) # MAIN MEMORY STATUS FOR SPARE WRITE
OPERATION

```

INTERPROCESSOR STORE BUS TEST

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## -002- 01 # MAIN STORE I/O ORDERS:

0020016	-002- 04 ALLZERO EQU	0(20016)
	-002- 05 ALLZEROT TEXT	'APPLY ERRONEOUS ORDER(0/8) TO CHECKER'
0063476	-002- 06 BADCODE EQU	0(63476)
	-002- 07 BADCODEY TEXT	'APPLY ERRONEOUS ORDER(5/8) TO CHECKER'
0047214	-002- 08 BUSCHK EQU	0(47214)
	-002- 09 BUSCHKY TEXT	'CHECK BUS ISOLATION USING SER'
0040374	-002- 10 CKTINIT EQU	0(40374) # STORE CONTROLLER INITIALIZATION (W/O WRITE PROTECT CLEAR)
	-002- 12 CKTINITT TEXT	'INITIALIZE ALL STORE CONTROLLER CIRCUITS'
0043310	-002- 13 CLRSER EQU	0(43310)
	-002- 14 CLRSERT TEXT	'CLEAR STORE ERROR REGISTER'
0046074	-002- 15 CLKSTOP EQU	0(46074)
	-002- 16 CLKSTOPT TEXT	'DISABLE STORE CONTROLLER CLOCK OUTPUT'
0046070	-002- 17 CLKSTRT EQU	0(46070)
	-002- 18 CLKSTRTT TEXT	'ENABLE STORE CONTROLLER CLOCK OUTPUT'
0146074	-002- 19 ERCOLL EQU	0(146074)
	-002- 20 ERCOLLT TEXT	'COLLECT ERRORS IN STORE ERROR REG'
0145454	-002- 21 EXERLD EQU	0(145454) # FAST REFRESH WITH REFRESH & CLOCK STOPPED
	-002- 23 EXERLDT TEXT	'ENABLE EXTERNAL LOAD OF STORE ERROR REG'
0145454	-002- 24 EXLDB15 EQU	0(145454)
	-002- 25 EXLDB15T TEXT	'ENABLE EXTERNAL LOAD OF STORE ERROR REG W/ ERROR COLLECT OPTION'
0005440	-002- 26 FASTREF EQU	0(5440)
	-002- 27 FASTREFT TEXT	'PERFORM FAST REFRESH ON STORE'
0045454	-002- 28 FASRNC EQU	0(45454)
	-002- 29 FASRNCY TEXT	'FORCE FAST REFRESH W/O CLOCK'
0145454	-002- 30 FFRMB15 EQU	0(145454)
	-002- 31 FFRMB15T TEXT	'FORCE FAST REFRESH & BIT 15'
0146074	-002- 32 FBIT09 EQU	0(146074) # FORCE BIT 09 (COMMON ERROR STROBE) ACTIVE
	-002- 34 FBIT09T TEXT	'COLLECT ERRORS IN STORE ERROR REGISTER'
0146064	-002- 35 FBIT09R EQU	0(146064)
	-002- 36 FBIT09RT TEXT	'COLLECT ERRORS IN SER W/ REFRESH ON'
0146076	-002- 37 FBRMB15 EQU	0(146076)
	-002- 38 FBRMB15T TEXT	'FANOUT BOARD REFRESH W/ ERROR COLLECT'
0046314	-002- 39 FCHKBT EQU	0(46314) # FORCE MAIN SHIFTER CHECK BIT ACTIVE
	-002- 40 FCHKBTY TEXT	'ACTIVATE MAIN SHIFTER CHECK BIT'
0046304	-002- 41 FCHKBTR EQU	0(46304)
	-002- 42 FCHKBTRT TEXT	'ACTIVATE SHIFTER CHECK BIT W/ REFRESH ENABLED'
0040574	-002- 43 FCHKOS EQU	0(40574)
	-002- 44 FCHKOST TEXT	'FORCE ZEROS TO MODULE SELECT XOR CHECK & WRITE PROTECT SELECT XOR CHECK CIRCUITS'
0041274	-002- 46 FCHK1S EQU	0(41274)
	-002- 47 FCHK1ST TEXT	'FORCE ONES TO MODULE SELECT XOR CHECK & WRITE PROTECT SELECT XOR CHECK CIRCUITS'
0140574	-002- 49 FCKOS15 EQU	0(140574)

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0141274	-002- 01	FCKOS15T TEXT	'FORCE ZEROS TO CHECK CKTS W/ ERROR COLLECT'
	-002- 02	FCK1S15 EQU	0(141274)
0043074	-002- 03	FCK1S15T TEXT	'FORCE ONES TO CHECK CKTS W/ ERROR COLLECT'
	-002- 04	FDISIDLE EQU	0(43074)
0046156	-002- 05	FDISIDLET TEXT	'FORCE DISABLE OF IDLE FLOP'
	-002- 06	FLSHO EQU	0(46156) # FORCE LOAD THE SHIFTER WITH ZERO (W/CLOCK)
0046154	-002- 08	FLSHOT TEXT	'START ZERO INTO MAIN SHIFTER'
	-002- 09	FLSHONC EQU	0(46154) # PUT ZERO ON INPUT OF SHIFTER (W/O CLOCK)
0045434	-002- 11	FLSHONCT TEXT	'PRESENT ZERO TO INPUT OF MAIN SHIFTER'
	-002- 12	FNOWRT EQU	0(45434)
0045430	-002- 13	FNOWRTT TEXT	'FORCE WRITING OF ALL-ONES DATA'
	-002- 14	FNOWRTC EQU	0(45430)
0044474	-002- 15	FNOWRTCT TEXT	'FORCE WRITING OF ONES W/ CLOCK RUNNING'
	-002- 16	FNOTIM EQU	0(44474) # DISABLE TRANSMISSION OF TIMING SIGNALS TO FANOUT BOARDS
0044470	-002- 18	FNOTIMT TEXT	'INHIBIT TIMING SIGNALS TO FANOUT BOARDS'
	-002- 19	FNOTIMC EQU	0(44470)
0041550	-002- 20	FNOTIMCT TEXT	'BLOCK TIMING TO FANOUT BOARDS(W/CLOCK)'
	-002- 21	FOBMT EQU	0(41550)
0041474	-002- 22	FOBMTT TEXT	'FANOUT BOARD MAINTENANCE TEST'
	-002- 23	FRFSELO EQU	0(41474) # FORCE REFRESH SELECT SIGNAL FROM FOB0
0042334	-002- 24	FRFSELO1 TEXT	'CANCEL SELECT FROM FOB0 DURING REFRESH'
	-002- 25	FRFSEL1 EQU	0(42334) # FORCE REFRESH SELECT SIGNAL FROM FOB1
0042534	-002- 26	FRFSEL1T TEXT	'CANCEL SELECT FROM FOB1 DURING REFRESH'
	-002- 27	FRFSEL2 EQU	0(42534) # FORCE REFRESH SELECT SIGNAL FROM FOB2
0043234	-002- 28	FRFSEL2T TEXT	'CANCEL SELECT FROM FOB2 DURING REFRESH'
	-002- 29	FRFSEL3 EQU	0(43234) # FORCE REFRESH SELECT SIGNAL FROM FOB3
0043434	-002- 30	FRFSEL3T TEXT	'CANCEL SELECT FROM FOB3 DURING REFRESH'
	-002- 31	FRFSEL4 EQU	0(43434) # FORCE REFRESH SELECT SIGNAL FROM FOB4
0044354	-002- 32	FRFSEL4T TEXT	'CANCEL SELECT FROM FOB4 DURING REFRESH'
	-002- 33	FRFSEL5 EQU	0(44354) # FORCE REFRESH SELECT SIGNAL FROM FOB5
0044554	-002- 34	FRFSEL5T TEXT	'CANCEL SELECT FROM FOB5 DURING REFRESH'
	-002- 35	FRFSEL6 EQU	0(44554) # FORCE REFRESH SELECT SIGNAL FROM FOB6
0045254	-002- 36	FRFSEL6T TEXT	'CANCEL SELECT FROM FOB6 DURING REFRESH'
	-002- 37	FRFSEL7 EQU	0(45254) # FORCE REFRESH SELECT SIGNAL FROM FOB7
0044334	-002- 38	FRFSEL7T TEXT	'CANCEL SELECT FROM FOB7 DURING REFRESH'
	-002- 39	FRREQA EQU	0(44334) # SET REFRESH REQUEST FLOP (DFFREQ) ON TIMING BOARD (FA1071)
0040674	-002- 41	FRREQAT TEXT	'SET REFRESH REQUEST ON TIMING BOARD (FA1071)'
	-002- 42	FRREQB EQU	0(40674) # SET REFRESH REQUEST FLOP (RREQB) ON CHECK BOARD A (FA1062)
0040664	-002- 44	FRREQBT TEXT	'SET REFRESH REQ COPY ON CHECK BOARD A (FA1062)''
	-002- 45	FRREQBR EQU	0(40664)
0046074	-002- 46	FRREQBRT TEXT	'SET REFRESH REQUEST ON FA1062 W/ REFRESH ENABLED'
	-002- 47	FSELA EQU	0(46074)
0006074	-002- 48	FSELAT TEXT	'FORCE STORE SELECT(ISOLATE) SIGNAL ON FA1071'
	-002- 49	NSELA EQU	0(6074)

INTERPROCESSOR STORE BUS TEST

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0004714	-002- 01 NSELAT TEXT	'RESET STORE SELECT(ISOLATE) SIGNAL ON FA1071'
	-002- 02 FSELB EQU	0(4714) # FORCE STORE SELECT (TBSEL) FROM CHECK BOARD A (FA1062)
0004710	-002- 04 FSELBT TEXT	'FORCE DUPLICATED STORE SELECT(SELB) ACTIVE'
	-002- 05 FSELBC EQU	0(4710)
0046516	-002- 06 FSELBCT TEXT	'FORCE DUPLICATED STORE SELECT(SELB) W/ CLOCK'
	-002- 07 FSTFBRM EQU	0(46516)
0042354	-002- 08 FSTFBRMT TEXT	'FORCE CONTROLLER & FANOUT BOARDS TO REFRESH'
	-002- 09 FSTNM EQU	0(42354) # FORCE MODE FLOP TO NORMAL STATE
0052354	-002- 10 FSTNMT TEXT	'FORCE MODE FLOP TO NORMAL STATE'
	-002- 11 FSTNMFR EQU	0(52354)
0042344	-002- 12 FSTNMFRMT TEXT	'FORCE NORMAL MODE IN CONTROLLER & REFRESH TO FANOUT BOARDS'
	-002- 13 FSTNMR EQU	0(42344)
0046514	-002- 14 FSTNMRT TEXT	'FORCE MODE TO NORMAL W/ REFRESH ENABLED'
	-002- 15 FSTRM EQU	0(46514) # FORCE MODE FLOP TO REFRESH STATE
0046234	-002- 16 FSTRMT TEXT	'FORCE MODE FLOP TO REFRESH STATE'
	-002- 17 FTINWP EQU	0(46234)
0006220	-002- 18 FTINWPT TEXT	'FORCE IN-WRITE-PROTECT INHIBIT'
	-002- 19 IOGO EQU	0(6220)
0125252	-002- 20 IOGOT TEXT	'ENABLE ON-LINE I/O ACCESS TO OFF-LINE STORE'
	-002- 21 IOTSTA EQU	0(125252)
0052525	-002- 22 IOTSTAT TEXT	'I/O TEST PATTERN #1'
	-002- 23 IOTST5 EQU	0(52525)
0067214	-002- 24 IOTST5T TEXT	'I/O TEST PATTERN #2'
	-002- 25 ISOCHK EQU	0(67214) # CHECK ISOLATION FROM HIGHER STORES - PUT RESULTS OF TEST INTO STORE ERROR REGISTER (SER)
0027214	-002- 28 ISOCHKT TEXT	'ISOLATE FROM FAR STORES & VERIFY VIA SER'
	-002- 29 ISOCHKU EQU	0(27214)
0043454	-002- 30 ISOCHKUT TEXT	'APPLY ONES TO STORE DATA BUS(W/O ISOLATE)'
	-002- 31 KILL12 EQU	0(43454) # WIPE OUT SHIFTER BIT AT POSITION 12
0046071	-002- 32 KILL12T TEXT	'CLEAR SHIFTER BIT IN POSITION 12'
	-002- 33 MASCINT EQU	0(46071)
0006071	-002- 34 MASCINTT TEXT	'INITIALIZE STORE CONTROLLER'
	-002- 35 MSCITNS EQU	0(6071)
0046076	-002- 36 MSCITNST TEXT	'INITIALIZE STORE CONTROLLER W/O FORCE SELECT'
	-002- 37 MASCLK EQU	0(46076) # ACTIVATE STORE CONTROLLER CLOCK (CK) SIGNAL
0046074	-002- 39 MASCLKT TEXT	'FAKE FIRST HALF OF STORE CLOCK CYCLE'
	-002- 40 MASCLKN EQU	0(46074)
0047410	-002- 41 MASCLKNT TEXT	'FAKE SECOND HALF OF STORE CLOCK CYCLE'
	-002- 42 RDAD EQU	0(47410)
0047414	-002- 43 RDADT TEXT	'GATE STORE ADDRESS BUS(SAO-16,PL) TO STORE DATA BUS(SDO-15,PL,PH) W/ CLOCK'
	-002- 45 RDADNC EQU	0(47414)
0006070	-002- 46 RDADNCT TEXT	'GATE STORE ADDRESS BITS TO STORE DATA BUS'
	-002- 47 REFSTOP EQU	0(6070)
0006060	-002- 48 REFSTOPT TEXT	'INHIBIT REFRESHING OF STORE'
	-002- 49 REFSTRT EQU	0(6060)

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0046060 -002- 01 REFSTRTT TEXT 'RESUME REGULAR REFRESHING OF STORE'
-002- 02 RFWISOL EQU 0(46060)
0047214 -002- 03 RFWISOLT TEXT 'RESUME REGULAR REFRESH W/ STORE ISOLATED'
-002- 04 RTNADHI EQU 0(47214) # RETURN UPPER ADDRESS (SA16-19) BITS &
SELECTED CONTROL SIGNALS VIA I/O CHANNE

0044714 -002- 06 RTNADHIT TEXT 'LOAD SA17 & SAPH INTO SER'
-002- 07 SPAREA EQU 0(44714)
0047114 -002- 08 SPAREAT TEXT 'SPARE I/O ORDER'
-002- 09 SERREAD EQU 0(47114) # STORE ERROR REGISTER (SER) READ
-002- 10 SERREADT TEXT 'READ BACK STORE ERROR REGISTER(SER)'
0041634 -002- 11 STSBY EQU 0(41634)
-002- 12 STSBYT TEXT 'SET STORE BUSY(SBY) SIGNAL'
0041630 -002- 13 STSBYCL EQU 0(41630)
-002- 14 STSBYCLT TEXT 'SET STORE BUSY(SBY) W/ CLOCK'
0007114 -002- 15 USERRED EQU 0(7114)
-002- 16 USERREDT TEXT 'READ STORE ERROR REG (W/O ISOLATE)'
0046061 -002- 17 WPCLR EQU 0(46061)
-002- 18 WPCLRT TEXT 'STORE INITIALIZE, INCL. WRITE PROTECT'
0052354 -002- 19 O1ONOR EQU 0(52354) # FORCE 0-10 (O1OTIM) SIGNAL & RESET
REFRESH REQUEST FLOP
0054334 -002- 21 O1ONORT TEXT '0-10 TIMING(O1OTIM)THEN REFRESH REQUEST CLEAR'
-002- 22 O1OREF EQU 0(54334) # FORCE 0-10 (O1OTIM) SIGNAL & SET
REFRESH REQUEST FLOP
0056074 -002- 24 O1OLEFT TEXT '0-10 TIMING(O1OTIM)THEN REFRESH REQUEST SET'
-002- 25 O1OTIM EQU 0(56074)
-002- 26 O1OTIMT TEXT 'FORCE 0-10 TIMING SIGNAL ACTIVE'

```

## -002- 33 # STORE MAINTENANCE ORDER OPTIONS:

```

0010000 -002- 36 FAK010 EQU 0(10000) # FAKE 0-10 TIMING SIGNAL
-002- 37 # NOTE: NEXT OPTION BIT IS SHARED
0020000 -002- 38 FBUSRDN EQU 0(20000) # FORCE BUS READ INACTIVE TO BIT-SLICES
0020000 -002- 39 LOADCHK EQU 0(20000) # LOAD I/O ORDER CHECK RESULTS
0040000 -002- 40 ISOLATE EQU 0(40000) # ISOLATE THIS STORE FROM HIGHER STORES
0100000 -002- 41 FSBIT09 EQU 0(100000) # FORCE SHIFTER BIT 09 ACTIVE
0000001 -002- 42 INITBIT EQU 0(1) # INITIALIZE STORE CONTROLLER
-002- 43 # NOTE: NEXT OPTION BIT IS SHARED
0000002 -002- 44 FFOBRM EQU 0(2) # FORCE FANOUT BOARDS TO REFRESH MODE
0000002 -002- 45 STEPCLK EQU 0(2) # HALF-CYCLE OF STORE CLOCK
0000004 -002- 46 HALTCLK EQU 0(4) # DISABLE STORE CONTROLLER CLOCK
0000010 -002- 47 STOPREF EQU 0(10) #DISABLE AUTONOMOUS REFRESH

```

INTERPROCESSOR STORE BUS TEST

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0177771 -002- 01 CLOCKON EQU 0(177771)  
0020016 -002- 02 FGLDNCFR EQU 0(20016)

# MASK OUT CLOCK OFF OPTIONS  
# LOAD I/O ORDER CHECK RESULTS WITH CLOCK  
STOPPED AND FANOUT BOARDS IN REFRESH  
MODE

INTERPROCESSOR STORE BUS TEST

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TEST 52

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INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

-001- 01 # *****
-001- 02 # *****
-001- 03 # **
-001- 04 # ** CU DIAGNOSTIC TEST NO. 52, INTERPROCESSOR_STORE_BUS
-001- 05 # **
-001- 06 # *****
-001- 07 # *****
    
```

0027122

-001- 10 CSTON1 CSECT

0027122 01 000000 000145 ----- CDGSM

-001- 14 VFD 1,0 2,0 2,0 2,0 3,1 6,NBGN

```

18 # THIS TEST DIAGNOSES THE STORE BUS WHICH IS USED
19 # BY THE ON-LINE CC TO COMMUNICATE WITH OFF-LINE STORE 0.
20 # DOING THE TEST IN THIS DIRECTION RESULTS IN A NUMBER OF ON-LINE
21 # PACKS IN THE TLM. AN ALTERNATIVE TEST WHICH WOULD HAVE BEEN MORE
22 # CONSISTENT WITH OTHER DIAGNOSTIC TESTS WOULD HAVE BEEN A TEST OF
23 # THE BUS BY WHICH THE OFF-LINE CC COMMUNICATES WITH THE ON-LINE STORE.
24 # THE LATTER APPROACH HAS THE DISADVANTAGE OF POSSIBLE INTERFANCE
25 # WITH CALL PROCESSING IN THE PRESENCE OF SOME FAULTS AND WAS NOT ADOPTED.
    
```

```

27 # SEGMENT 1
28 # THIS SEGMENT TESTS THE STORE COMMAND PORTION OF THE STORE
29 # BUS. ONLY TWO 2/4 COMMANDS ARE REQUIRED WHICH ARE
30 # COMPLEMENTS OF EACH OTHER. LOS AND STOS WILL BE USED.
31 # IF THESE LEADS WORK AND ALL CONTROL LEADS WORK AS WELL,
32 # THE ERROR REGISTER IN THE STORE CONTROL WILL HAVE BIT CHDIF=0 AND
33 # THE ERROR REGISTER IN THE CC WILL HAVE BIT OFSTM = 0.
    
```

```

35 # SEGMENT 2
36 # THIS SEGMENT VERIFIES THE INTEGRITY OF STORE BUS ADDRESS LEADS
37 # 0-16 AND PL. THIS IS DONE BY SENDING ALL ZEROS AND ALL ONES
38 # ADDRESSES FROM THE ON-LINE PROCESSOR TO THE OFF-LINE STORE
39 # AND USING THE READ-ADDRESS (RDAD) STORE MAINTENANCE ORDER
40 # TO PERMIT RETRIEVING OF THESE PATTERNS OVER THE STORE DATA BUS.
    
```

```

42 # SEGMENT 3
43 # THIS SEGMENT VERIFIES TWO STORE BUS ADDRESS LEADS (17 AND PH).
44 # AN I/O MAINTENANCE ORDER IS USED (RTNADHI) WHICH DIVERTS
45 # THESE BITS INTO BITS SA17LP AND BIT SAPHLP OF THE
46 # STORE ERROR REGISTER RESPECTIVELY.
    
```

INTERPROCESSOR STORE BUS TEST

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TEST 52

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INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

01 # SEGMENT 4  
02 # THIS SEGMENT VERIFIES TWO STORE BUS ADDRESS LEADS (18 AND 19).  
03 # AN I/O MAINTENANCE ORDER IS USED (ISOCHKU) IS USED TO DIVERT  
04 # THE LOGICAL "OR" OF THESE BITS INTO THE STORE ERROR REGISTER BIT  
05 # STRSLP. THREE CONSTANTS ARE USED, THE FIRST WITH BOTH BITS  
06 # ZERO AND THE OTHERS HAVING ONE BIT A ONE AND THE OTHER A ZERO.

INTERPROCESSOR STORE BUS TEST

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TEST 52

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## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

-001- 01 # RTN_BLM
-001- 02 # TURN OFF AUTOMATIC RETURNS TO BLM EVERY 20 TABLE ENTRIES.
0027123 01 000001 000144 ----- CDGNM -001- 03 VFD 1,0 2,0 6,0 1,1 6,NRTNBLM

-001- 05 # NO3_CODE
-001- 06 # PROCESS 3ACC CODED ROUTINE AT ADDRESS DOSEGO.
0027124 01 000002 040043 000000 CDGNM -001- 07 VFD 1,0 2,2 7,0 6,NN03CD
0027125 01 000003 000000 027127 0027127 -001- 08 ADDR DOSEGO

0027127 15 DOSEGO
0027127 01 000005 131221 016447 MASACS 16 LAL R9,MASCIOSC+1,RAO # SET UP R9 TO I/O ADDRESS FOR OTHER STORE 0.

0027131 01 000007 034620 043133 CTSD 18 STL R9,IOADDR
0027133 19 SIOX MASCINT # INITIALIZE STORE CONTROLLER.
0027133 01 000011 037020 012667 CDGSIO -002- 20 BSA MASIOM
0027135 01 000013 046071 ----- -001- 21 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027136 22 RTN_TBL DOSEG1
0027136 01 000014 171400 ----- -001- 23 GA
0027137 01 000015 031000 027143 0027143 -001- 24 LAL R0,DOSEG1,RAO
0027141 01 000017 037000 011162 CDGNM -001- 25 BL INTRPN03

0027143 28 DOSEG1

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 1

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INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

-001- 01 # *****
-001- 02 # *
-001- 03 # * TEST 52 SEGMENT 1
-001- 04 # *
-001- 05 # *****

0027143 01 000021 000100 ----- CDGNM -001- 08 VFD 1,0 2,0 2,0 5,D(1) 6,NTESTSEG

11 # THIS SEGMENT TESTS THE STORE COMMAND PORTION OF THE STORE
12 # BUS. ONLY TWO 2/4 COMMANDS ARE REQUIRED WHICH ARE
13 # COMPLEMENTS OF EACH OTHER. LOS AND STOS WILL BE USED.
14 # IF THESE LEADS WORK AND ALL CONTROL LEADS WORK AS WELL,
15 # THE ERROR REGISTER IN THE STORE CONTROL WILL HAVE BIT CHDIF=0 AND
16 # THE ERROR REGISTER IN THE CC WILL HAVE BIT OFSTM = 0.

-001- 18 # CALLPROS
-001- 19 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027144 01 000022 000004 ----- CDGNM -001- 20 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 22 # N03 CODE
-001- 23 # PROCESS 3ACC CODED ROUTINE AT ADDRESS CMDTST.
0027145 01 000023 040043 000000 CDGNM -001- 24 VFD 1,0 2,2 7,0 6,NNO3CD
0027146 01 000024 000000 027150 0027150 -001- 25 ADDR CMDTST

0027150 27 CMDTST
0027150 28 # SAVE IM AND THEN MASK ERROR INTERRUPT
# AND BLOCK HARDWARE CHECKS

0027150 30 CALL BKCHKINT
0027150 01 000026 137020 027637 0027637 -001- 31 BSA BKCHKINT
0027152 01 000030 131400 000000 32 LAL R0,0,RA1 # DO STOS. USE ADDRESS 0.
0027154 33 STOS Q(RA1)
E0027154 01 000032 000420 ----- -001- 34 MSTF Q(RA1)
0027155 01 000033 136100 ----- -001- 35 DATA B(1011110001000000)
0027156 36 LOS Q(RA1) AC=NO,PC=NO
E0027156 01 000034 000420 ----- -001- 37 MSTF Q(RA1)
0027157 01 000035 106160 037020 -001- 38 DATA B(1000110001110000) # READ BACK STORE ERROR REGISTER
0027160 39
0027160 40 SRIO SERREAD
0027160 01 000036 037020 012667 CDGSI0 -002- 41 BSA MASIOM
0027162 01 000040 047114 ----- -001- 42 DATA SERREAD # READ BACK STORE ERROR REGISTER(SER)
0027163 43 TEST S(CHDIF),OTEST,FLCMND,SUBNAME=CLNONL
0027163 01 000041 124262 ----- -001- 44 TBN R11,S(CHDIF)
0027164 01 000042 055013 ----- 0027177 -001- 45 BNC P314
0027165 01 000043 037020 027646 0027646 -002- 46 BSA CLNONL
0027167 01 000045 107473 ----- -001- 47 LSR MCHB,R11
0027170 01 000046 071400 ----- -002- 48 GA
0027171 01 000047 031000 027175 0027175 -002- 49 LAL R0,++4,RA0

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 27

TEST 52 SEGMENT 1

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

0027173 01 000051 037000 011162 CDGNM -002- 01 BL INTRPN03
-002- 03 # FAILTST
-002- 04 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FLCMND.
-002- 05 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027175 01 000053 020017 ----- CDGNM -002- 06 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027176 01 000054 000002 ----- -002- 07 VFD 16,FLCMND

0027177 -001- 09 # TROUBLE PRINTOUT DATA = CONTENTS OF R11 IN ON-LINE PROCESSOR
-001- 10 P314

0027177 16 # IF THE OFF-LINE STORE RESPONDED TO THE
LOS AND STOS, THE ER IN THE CC SHOULD
HAVE BIT OFSTM=0.

0027177 01 000055 112412 ----- 19 UNPK ER
0027200 20 TEST S(OFSM)-16,OTEST,FLRSP,SUBNAME=CLNONL,REG=R2
0027200 01 000056 024040 ----- -001- 21 TBN R2,S(OFSM)-16
0027201 01 000057 055013 ----- 0027214 -001- 22 BNC P318
0027202 01 000060 037020 027646 0027646 -002- 23 BSA CLNONL
0027204 01 000062 107462 ----- -001- 24 LSR MCHB,R2
0027205 01 000063 071400 ----- -002- 25 GA
0027206 01 000064 031000 027212 0027212 -002- 26 LAL RO,*+4,RAD
0027210 01 000066 037000 011162 CDGNM -002- 27 BL INTRPN03

-002- 29 # FAILTST
-002- 30 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FLRSP.
-002- 31 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027212 01 000070 020017 ----- CDGNM -002- 32 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027213 01 000071 000003 137020 -002- 33 VFD 16,FLRSP

-001- 35 # TROUBLE PRINTOUT DATA = CONTENTS OF R2 IN ON-LINE PROCESSOR
-001- 36 P318
0027214 37 CALL CLNONL
0027214 01 000072 137020 027646 0027646 -001- 38 BSA CLNONL
0027216 39 RTN_TBL DOSEG2
0027216 01 000074 171400 ----- -001- 40 GA
0027217 01 000075 031000 027223 0027223 -001- 41 LAL RO,DOSEG2,RAD
0027221 01 000077 037000 011162 CDGNM -001- 42 BL INTRPN03

0027223 44 DOSEG2

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 2

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W770

```

-001- 01 # *****
-001- 02 # *
-001- 03 # * TEST 52 SEGMENT 2
-001- 04 # *
-001- 05 # *****

```

```

0027223 01 000101 000200 ----- CDGNM -001- 08 VFD 1,0 2,0 2,0 5,D(2) 6,NTESTSEG

```

```

11 # THIS SEGMENT VERIFIES THE INTEGRITY OF STORE BUS ADDRESS LEADS
12 # 0-16 AND PL. THIS IS DONE BY SENDING ALL ZEROS AND ALL ONES
13 # ADDRESSES FROM THE ON-LINE PROCESSOR TO THE OFF-LINE STORE
14 # AND USING THE READ-ADDRESS (RDAD) STORE MAINTENANCE ORDER
15 # TO PERMIT RETRIEVING OF THESE PATTERNS OVER THE STORE DATA BUS.

```

```

-001- 17 # CALLPROS
-001- 18 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027224 01 000102 000004 ----- CDGNM -001- 19 VFD 1,0 2,0 6,0 1,0 6,NPROS

```

```

-001- 21 # NO3 CODE
-001- 22 # PROCESS 3ACC CODED ROUTINE AT ADDRESS CHKADD.
0027225 01 000103 040043 000000 CDGNM -001- 23 VFD 1,0 2,2 7,0 6,NN03CD
0027226 01 000104 000000 027230 0027230 -001- 24 ADDR CHKADD

```

```

0027230 29 CHKADD
0027230 30
0027230 01 000106 137020 027637 0027637 -001- 31
0027232 01 000110 131400 000000 32
0027234 33
0027234 01 000112 037020 012667 CDGSI0 -002- 34
0027236 01 000114 047410 ----- -001- 35

```

```

CALL BKCHKINT
BSA BKCHKINT
LAL RO,0,RA1
SIOM RDAD
BSA MASIOM
DATA RDAD

```

# GATE STORE ADDRESS BUS(SAO-16,PL) TO STORE DATA BUS(SDO-15,PL,PH) W/ CLOCK

```

0027237 37 MLOS O(RA1) PC=NO
E0027237 01 000115 100420 ----- -001- 38 MSTF O(RA1)
0027240 01 000116 136163 ----- -001- 39 DATA B(1011110001110011)
0027241 01 000117 007460 ----- 40 LSR MCHB,RO
0027242 41 CALL CLNONL
0027242 01 000120 037020 027646 0027646 -001- 42 BSA CLNONL
0027244 43 RTN_TBL TSTADD
0027244 01 000122 171400 ----- -001- 44 GA
0027245 01 000123 031000 027251 0027251 -001- 45 LAL RO,TSTADD,RAO
0027247 01 000125 037000 011162 CDGNM -001- 46 BL INTRPN03

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

TEST 52 SEGMENT 2

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

0027251          01 TSTADO
-001- 02 # COMPARE
-001- 03 # COMPARE ON-LINE MCHB BIT PL TO 1.
-001- 04 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027251 01 000127 022414 ----- CDGNM -001- 05 VFD 1,LPINDX 2,1 1,0 1,SUCCE 5,PL 6,NCOMPARE
0027252 01 000130 000001 ----- -001- 06 VFD 15,0 1,1

-001- 08 # FAILTST
-001- 09 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS SAFALP.
-001- 10 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027253 01 000131 020017 ----- CDGNM -001- 11 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027254 01 000132 000025 ----- -001- 12 VFD 16,SAFALP

0027255          14 # ADDRESS BIT 16 LOOPS AROUND TO DATA
# BIT PH
-001- 16 # COMPARE
-001- 17 # COMPARE ON-LINE MCHB BIT PH TO 0.
-001- 18 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027255 01 000133 022514 ----- CDGNM -001- 19 VFD 1,LPINDX 2,1 1,0 1,SUCCE 5,PH 6,NCOMPARE
0027256 01 000134 000000 ----- -001- 20 VFD 15,0 1,0

-001- 22 # FAILTST
-001- 23 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS SAFAL16.
-001- 24 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027257 01 000135 020017 ----- CDGNM -001- 25 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027260 01 000136 000024 ----- -001- 26 VFD 16,SAFAL16

-001- 28 # MASK
-001- 29 # MASK CONTENTS OF ON-LINE MCHB WITH 0(0377777).
0027261 01 000137 040013 ----- CDGNM -001- 30 VFD 1,0 2,2 7,0 6,NMASK
0027262 01 000140 000001 177777 -001- 31 ADDR 0(0377777)

-001- 33 # COMPARE
-001- 34 # COMPARE ON-LINE MAINTENANCE CHANNEL BUFFER TO 0(0000000).
-001- 35 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027264 01 000142 050014 ----- CDGNM -001- 36 VFD 1,LPINDX 2,2 1,1 1,SUCCE 5,0 6,NCOMPARE
0027265 01 000143 000000 000000 -001- 37 ADDR 0(0000000)

-001- 39 # FAILBIT
-001- 40 # FAILURE EXIT. SYMBOLIC TROUBLE NUMBER IS SAFALXX
-001- 41 # WHERE XX IS THE LOWEST FAILING BIT NUMBER.
0027267 01 000145 020020 ----- CDGNM -001- 42 VFD 1,0 2,1 5,0 2, 6,NFLBITS
0027270 01 000146 000004 ----- -001- 43 VFD 16,SAFAL
    
```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

TEST 52 SEGMENT 2

23:41:18 2/05/81 \*\*\*\*

## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

-001- 01 # CALLPROS
-001- 02 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027271 01 000147 000004 ----- CDGNM -001- 03 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 05 # NO3_CODE
-001- 06 # PROCESS 3ACC CODED ROUTINE AT ADDRESS CHKAD1.
0027272 01 000150 040043 000000 CDGNM -001- 07 VFD 1,0 2,2 7,0 6,NN03CD
0027273 01 000151 000000 027275 0027275 -001- 08 ADDR CHKAD1

0027275 10 CHKAD1
0027275 11 # TRY ALL ONES ADDRESS
0027275 12 CALL BKCHKINT
0027275 01 000153 137020 027637 0027637 -001- 13 BSA BKCHKINT
0027277 01 000155 103341 ----- 14 LN R14,1
0027300 01 000156 003761 177777 15 LI R15,0(177777)
0027302 16 SIOM MASCINT
0027302 01 000160 037020 012667 CDGSIO -002- 17 BSA MASIOM
0027304 01 000162 046071 137020 -001- 18 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027305 19 SIOM RDAD
0027305 01 000163 137020 012667 CDGSIO -002- 20 BSA MASIOM
0027307 01 000165 047410 ----- -001- 21 DATA RDAD # GATE STORE ADDRESS BUS(SAO-16,PL) TO
STORE DATA BUS(SDO-15,PL,PH) W/ CLOCK

0027310 23 MLOS O(RA1) PC=NO
E0027310 01 000166 100420 ----- -001- 24 MSTF O(RA1)
0027311 01 000167 136163 ----- -001- 25 DATA B(1011110001110011)
0027312 01 000170 007460 ----- 26 LSR MCHB,RO
0027313 27 CALL CLNONL
0027313 01 000171 037020 027646 0027646 -001- 28 BSA CLNONL
0027315 29 RTN_TBL TSTAD1
0027315 01 000173 171400 ----- -001- 30 GA
0027316 01 000174 031000 027322 0027322 -001- 31 LAL RO,TSTAD1,RAD
0027320 01 000176 037000 011162 CDGNM -001- 32 BL INTRPN03

0027322 39 TSTAD1
0027322 40 # ADDRESS BIT 16 LOOPS AROUND TO DATA
BIT PH

-001- 42 # COMPARE
-001- 43 # COMPARE ON-LINE MCHB BIT PH TO 1.
-001- 44 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027322 01 000200 022514 ----- CDGNM -001- 45 VFD 1,LPINDX 2,1 1,0 1,SUCCE 5,PH 6,NCOMPARE
0027323 01 000201 000001 ----- -001- 46 VFD 15,0 1,1

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 2

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## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

-001- 01 # FAILTST
-001- 02 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS SAFAL16.
-001- 03 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027324 01 000202 020017 ----- CDGNM -001- 04 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027325 01 000203 000024 ----- -001- 05 VFD 16,SAFAL16

-001- 07 # MASK
-001- 08 # MASK CONTENTS OF ON-LINE MCHB WITH 0(0377777).
0027326 01 000204 040013 ----- CDGNM -001- 09 VFD 1,0 2,2 7,0 6,NMASK
0027327 01 000205 000001 177777 -001- 10 ADDR 0(0377777)

-001- 12 # COMPARE
-001- 13 # COMPARE ON-LINE MAINTENANCE CHANNEL BUFFER TO 0(0177777).
-001- 14 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027331 01 000207 050014 ----- CDGNM -001- 15 VFD 1,LPINDX 2,2 1,1 1,SUCCESS 5,0 6,NCOMPARE
0027332 01 000210 000000 177777 -001- 16 ADDR 0(0177777)

-001- 18 # FAILBIT
-001- 19 # FAILURE EXIT. SYMBOLIC TROUBLE NUMBER IS SAFALXX
-001- 20 # WHERE XX IS THE LOWEST FAILING BIT NUMBER.
0027334 01 000212 020020 ----- CDGNM -001- 21 VFD 1,0 2,1 5,0 2, 6,NFLBITS
0027335 01 000213 000004 ----- -001- 22 VFD 16,SAFAL

-001- 24 # CALLPROS
-001- 25 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027336 01 000214 000004 ----- CDGNM -001- 26 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 28 # NO3_CODE
-001- 29 # PROCESS 3ACC CODED ROUTINE AT ADDRESS CHKADPL.
0027337 01 000215 040043 000000 CDGNM -001- 30 VFD 1,0 2,2 7,0 6,NN03CD
0027340 01 000216 000000 027342 0027342 -001- 31 ADDR CHKADPL

0027342 38 CHKADPL
0027342 39
0027342 40 CALL BKCHKINT # TRY A CONSTANT WITH PL=0
0027342 01 000220 137020 027637 0027637 -001- 41 BSA BKCHKINT
0027344 01 000222 131400 000020 42 LAL RO,X(0010),RA1
0027346 43 SIOM MASCINT
0027346 01 000224 037020 012667 CDGSI0 -002- 44 BSA MASIOM
0027350 01 000226 046071 137020 -001- 45 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027351 46 SIOM RDAD
0027351 01 000227 137020 012667 CDGSI0 -002- 47 BSA MASIOM
0027353 01 000231 047410 ----- -001- 48 DATA RDAD # GATE STORE ADDRESS BUS(SAO-16,PL) TO
STORE DATA BUS(SDO-15,PL,PH) W/ CLOCK

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 2

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## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

0027354
E0027354 01 000232 100420 ----- -001- 01 MLOS O(RA1) PC=NO
0027355 01 000233 136163 ----- -001- 02 MSTF O(RA1)
0027356 01 000234 007460 ----- -001- 03 DATA B(1011110001110011)
0027357 01 000235 037020 027646 0027646 -001- 04 LSR MCHB,RO
0027361 01 000237 171400 ----- -001- 05 CALL CLNONL
0027362 01 000240 031000 027366 0027366 -001- 06 BSA CLNONL
0027364 01 000242 037000 011162 CDGNM -001- 07 RTN_TBL TSTADPL
0027366 01 000244 022414 ----- CDGNM -001- 08 GA
0027367 01 000245 000000 ----- CDGNM -001- 09 LAL RO,TSTADPL,RAO
0027370 01 000246 020017 ----- CDGNM -001- 10 BL INTRPN03
0027371 01 000247 000025 ----- CDGNM

```

0027366

17 TSTADPL

```

-001- 18 # COMFARE
-001- 19 # COMPARE ON-LINE MCHP BIT PL TO 0.
-001- 20 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027366 01 000244 022414 ----- CDGNM -001- 21 VFD 1,LPINDX 2,1 1,0 1,SUCCESS 5,PL 6,NCOMPARE
0027367 01 000245 000000 ----- CDGNM -001- 22 VFD 15,0 1,0

-001- 24 # FAILTST
-001- 25 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS SAFALP.
-001- 26 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027370 01 000246 020017 ----- CDGNM -001- 27 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027371 01 000247 000025 ----- CDGNM -001- 28 VFD 16,SAFALP

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 3

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

-001- 01 # *****
-001- 02 # *
-001- 03 # * TEST 52 SEGMENT 3
-001- 04 # *
-001- 05 # *****

0027372 01 000250 000300 ----- CDGNM -001- 08 VFD 1,0 2,0 2,0 5,D(3) 6,NTESTSEG

11 # THIS SEGMENT VERIFIES TWO STORE BUS ADDRESS LEADS (17 AND PH).
12 # AN I/O MAINTENANCE ORDER IS USED (RTNADHI) WHICH DIVERTS
13 # THESE BITS INTO BITS SA17LP AND BIT SAPHLP OF THE
14 # STORE ERROR REGISTER RESPECTIVELY.

-001- 16 # CALLPROS
-001- 17 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027373 01 000251 000004 ----- CDGNM -001- 18 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 20 # NO3 CODE
-001- 21 # PROCESS 3ACC CODED ROUTINE AT ADDRESS BT17PHO.
0027374 01 000252 040043 000000 CDGNM -001- 22 VFD 1,0 2,2 7,0 6,NNO3CD
0027375 01 000253 000000 027377 0027377 -001- 23 ADDR BT17PHO

0027377 30 BT17PHO # TRY BIT 17=0 AND PH=0
0027377 31 CALL BKCHKINT
0027377 01 000255 137020 027637 0027637 -001- 32 BSA BKCHKINT
0027401 33 SIOM MASCINT
0027401 01 000257 137020 012667 CDGSI0 -002- 34 BSA MASIOM
0027403 01 000261 046071 ----- -001- 35 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027404 01 000262 103341 ----- 36 LN R14,1
0027405 01 000263 003360 ----- 37 ZR R15
0027406 38 LOS O(RA1) AC=NO,PC=NO
E0027406 01 000264 000420 ----- -001- 39 MSTF O(RA1)
0027407 01 000265 106160 037020 -001- 40 DATA B(1000110001110000)
0027410 41 SIOM EXERLD # DIVERT BITS 17 AND PH INTO SER.
0027410 01 000266 037020 012667 CDGSI0 -002- 42 BSA MASIOM
0027412 01 000270 145454 137020 -001- 43 DATA EXERLD # ENABLE EXTERNAL LOAD OF STORE ERROR REG
0027413 44 SRI0 SERREAD
0027413 01 000271 137020 012667 CDGSI0 -002- 45 BSA MASIOM
0027415 01 000273 047114 ----- -001- 46 DATA SERREAD # READ BACK STORE ERROR REGISTER(SER)
0027416 01 000274 107473 ----- 47 LSR MCHB,R11
0027417 48 CALL CLNONL
0027417 01 000275 037020 027646 0027646 -001- 49 BSA CLNONL

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 3

23:41:18 2/05/81 \*\*\*\*

## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

0027421          01          000277 171400 -----          01          RTN_TBL TST17PHO
0027421 01 000277 171400 -----          -001- 02          GA
0027422 01 000300 031000 027426 0027426 -001- 03          LAL      RO,TST17PHO,RAO
0027424 01 000302 037000 011162 CDGNM    -001- 04          BL      INTRPNO3

0027426          06 TST17PHO
          -001- 07 #          COMPARE
          -001- 08 #          COMPARE ON-LINE MCHB BIT (S(SA17LP)) TO 0.
          -001- 09 #          IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027426 01 000304 021114 -----          -001- 10          VFD      1,LPINDX 2,1 1,0 1,SUCCESS 5,(S(SA17LP)) 6,NCOMPARE
0027427 01 000305 000000 -----          -001- 11          VFD      15,0 1,0

          -001- 13 #          FAILTST
          -001- 14 #          FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FL17.
          -001- 15 #          DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027430 01 000306 020017 -----          -001- 16          VFD      1,0 2,1 5,0 2,0 6,NFAILTST
0027431 01 000307 000026 -----          -001- 17          VFD      16,FL17

          -001- 19 #          COMPARE
          -001- 20 #          COMPARE ON-LINE MCHB BIT (S(SAPHL P)) TO 0.
          -001- 21 #          IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027432 01 000310 021014 -----          -001- 22          VFD      1,LPINDX 2,1 1,0 1,SUCCESS 5,(S(SAPHL P)) 6,NCOMPARE
0027433 01 000311 000000 -----          -001- 23          VFD      15,0 1,0

          -001- 25 #          FAILTST
          -001- 26 #          FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FLPH.
          -001- 27 #          DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027434 01 000312 020017 -----          -001- 28          VFD      1,0 2,1 5,0 2,0 6,NFAILTST
0027435 01 000313 000027 -----          -001- 29          VFD      16,FLPH

          -001- 31 #          CALLPROS
          -001- 32 #          RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027436 01 000314 000004 -----          -001- 33          VFD      1,0 2,0 6,0 1,0 6,NPROS

          -001- 35 #          NO3_CODE
          -001- 36 #          PROCESS 3ACC CODED ROUTINE AT ADDRESS BT17PH1.
0027437 01 000315 040043 000000 CDGNM    -001- 37          VFD      1,0 2,2 7,0 6,NNO3CD
0027440 01 000316 000000 027442 0027442 -001- 38          ADDR     BT17PH1

0027442          45 BT17PH1          #          TRY BIT 17=1 AND PH=1
0027442          46          CALL     BKCHKINT
0027442 01 000320 137020 027637 0027637 -001- 47          BSA     BKCHKINT
0027444          48          SIOM    MASCINT
0027444 01 000322 137020 012667 CDGSI0 -002- 49          BSA     MASIOM

```

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 3

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## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

0027446	01	000324	046071	-----	-001-	01	DATA	MASCINT	# INITIALIZE STORE CONTROLLER
0027447	01	000325	103343	-----		02	LN	R14,3	
0027450	01	000326	003360	-----		03	ZR	R15	
0027451						04	LOS	0(RA1) AC=NO,PC=NO	
0027451	01	000327	000420	-----	-001-	05	MSTF	0(RA1)	
0027452	01	000330	106160	037020	-001-	06	DATA	B(1000110001110000)	
0027453						07	SIOM	EXERLD	# DIVERT BITS 17 AND PH INTO SER.
0027453	01	000331	037020	012667 CDGSI0	-002-	08	BSA	MASIOH	
0027455	01	000333	145454	137020	-001-	09	DATA	EXERLD	# ENABLE EXTERNAL LOAD OF STORE ERROR REG
0027456						10	SRIO	SERREAD	
0027456	01	000334	137020	012667 CDGSI0	-002-	11	BSA	MASIOH	
0027460	01	000336	047114	-----	-001-	12	DATA	SERREAD	# READ BACK STORE ERROR REGISTER(SER)
0027461	01	000337	107473	-----		13	LSR	MCHB,R11	
0027462						14	CALL	CLNONL	
0027462	01	000340	037020	027646 0027646	-001-	15	BSA	CLNONL	
0027464						16	RTN_TBL	TST17PH1	
0027464	01	000342	171400	-----	-001-	17	GA		
0027465	01	000343	031000	027471 0027471	-001-	18	LAL	RO,TST17PH1,RAD	
0027467	01	000345	037000	011162 CDGNM	-001-	19	BL	INTRPNO3	

0027471

26 TST17PH1

					-001-	27 #	COMPARE		
					-001-	28 #	COMPARE ON-LINE MCHB BIT (S(SA17LP)) TO 1.		
					-001-	29 #	IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.		
0027471	01	000347	021114	----- CDGNM	-001-	30	VFD	1,LPINDX 2,1 1,0 1,SUCCESS 5,(S(SA17LP)) 6,NCOMPARE	
0027472	01	000350	000001	-----	-001-	31	VFD	15,0 1,1	
					-001-	33 #	FAILTST		
					-001-	34 #	FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FL17.		
					-001-	35 #	DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.		
0027473	01	000351	020017	----- CDGNM	-001-	36	VFD	1,0 2,1 5,0 2,0 6,NFAILTST	
0027474	01	000352	000026	-----	-001-	37	VFD	16,FL17	
					-001-	39 #	COMPARE		
					-001-	40 #	COMPARE ON-LINE MCHB BIT (S(SAPHL)) TO 1.		
					-001-	41 #	IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.		
0027475	01	000353	021014	----- CDGNM	-001-	42	VFD	1,LPINDX 2,1 1,0 1,SUCCESS 5,(S(SAPHL)) 6,NCOMPARE	
0027476	01	000354	000001	-----	-001-	43	VFD	15,0 1,1	
					-001-	45 #	FAILTST		
					-001-	46 #	FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FLPH.		
					-001-	47 #	DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.		
0027477	01	000355	020017	----- CDGNM	-001-	48	VFD	1,0 2,1 5,0 2,0 6,NFAILTST	
0027500	01	000356	000027	-----	-001-	49	VFD	16,FLPH	

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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TEST 52 SEGMENT 3

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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TEST 52 SEGMENT 4

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

-001- 01 # *****
-001- 02 # *
-001- 03 # * TEST 52 SEGMENT 4
-001- 04 # *
-001- 05 # *****

0027501 01 000357 000400 ----- CDGNN -001- 08 VFD 1,0 2,0 2,0 5,D(4) 6,NTESTSEG

11 # THIS SEGMENT VERIFIES TWO STORE BUS ADDRESS LEADS (18 AND 19).
12 # AN I/O MAINTENANCE ORDER IS USED (ISOCHKU) IS USED TO DIVERT
13 # THE LOGICAL "OR" OF THESE BITS INTO THE STORE ERROR REGISTER BIT
14 # STRSLP. THREE CONSTANTS ARE USED, THE FIRST WITH BOTH BITS
15 # ZERO AND THE OTHERS HAVING ONE BIT A ONE AND THE OTHER A ZERO.

-001- 17 # CALLPROS
-001- 18 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027502 01 000360 000004 ----- CDGNN -001- 19 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 21 # NO3 CODE
-001- 22 # PROCESS 3ACC CODED ROUTINE AT ADDRESS BT181900.
0027503 01 000361 040043 000000 CDGNN -001- 23 VFD 1,0 2,2 7,0 6,NNO3CD
0027504 01 000362 000000 027506 0027506 -001- 24 ADDR BT181900

0027506 31 BT181900
0027506 32 CALL BKCHKINT
0027506 01 000364 137020 027637 0027637 -001- 33 BSA BKCHKINT
0027510 34 SIOM MASCINT
0027510 01 000366 137020 012667 CDGSI0 -002- 35 BSA MASIOM
0027512 01 000370 046071 ----- -001- 36 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027513 01 000371 131400 000000 37 LAL RO,0,RA1 # ADDRESS WITH BIT 18=0 AND BIT 19=0.
0027515 38 LOS O(RA1) AC=NO,PC=NO
E0027515 01 000373 000420 ----- -001- 39 MSTF O(RA1)
0027516 01 000374 106160 037020 -001- 40 DATA B(1000110001110000)
0027517 41 SIOM EXERLD&-ISOLATE
0027517 01 000375 037020 012667 CDGSI0 -002- 42 BSA MASIOM
0027521 01 000377 105454 137020 -001- 43 DATA EXERLD&-ISOLATE # ENABLE EXTERNAL LOAD OF STORE ERROR REG
0027522 44 SRIO SERREAD
0027522 01 000400 137020 012667 CDGSI0 -002- 45 BSA MASIOM
0027524 01 000402 047114 ----- -001- 46 DATA SERREAD # READ BACK STORE ERROR REGISTER(SER)
0027525 01 000403 107473 ----- 47 LSR MCHB,R11
0027526 48 CALL CLNONL
0027526 01 000404 037020 027646 0027646 -001- 49 BSA CLNONL

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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TEST 52 SEGMENT 4

23:41:18 2/05/81 \*\*\*\*

## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

```

0027530 01 000406 171400 ----- -001- 01 RTN_TBL TS181900
0027531 01 000407 031000 027535 0027535 -001- 02 GA
0027533 01 000411 037000 011162 CD6NM -001- 03 LAL RD,TS181900,RAO
-001- 04 BL INTRPNO3

```

```

0027535 11 TS181900
-001- 12 # COMPARE
-001- 13 # COMPARE ON-LINE MCHB BIT (S(STRSLP)) TO 1.
-001- 14 # IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.
0027535 01 000413 021214 ----- CD6NM -001- 15 VFD 1,LPINDX 2,1 1,0 1,SUCCES 5,(S(STRSLP)) 6,NCOMPA?E
0027536 01 000414 000001 ----- -001- 16 VFD 15,0 1,1

-001- 18 # FAILTST
-001- 19 # FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FL1819.
-001- 20 # DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.
0027537 01 000415 020017 ----- CD6NM -001- 21 VFD 1,0 2,1 5,0 2,0 6,NFAILTST
0027540 01 000416 000030 ----- -001- 22 VFD 16,FL1819

-001- 24 # CALLPROS
-001- 25 # RETURN TO CALL PROCESSING FOR ONE BASE LEVEL LOOP.
0027541 01 000417 000004 ----- CD6NM -001- 26 VFD 1,0 2,0 6,0 1,0 6,NPROS

-001- 28 # NO3_CODE
-001- 29 # PROCESS 3ACC CODED ROUTINE AT ADDRESS BT181910.
0027542 01 000420 040043 000000 CD6NM -001- 30 VFD 1,0 2,2 7,0 6,NN03CD
0027543 01 000421 000000 027545 0027545 -001- 31 ADDR BT181910

```

```

0027545 38 BT181910
0027545 39 CALL BKCHKINT
0027545 01 000423 137020 027637 0027637 -001- 40 BSA BKCHKINT
0027547 41 SIOM MASCINT
0027547 01 000425 137020 012667 CD6SIO -002- 42 BSA MASIOH
0027551 01 000427 046071 ----- -001- 43 DATA MASCINT # INITIALIZE STORE CONTROLLER
0027552 01 000430 103344 ----- 44 LN R14,4
0027553 01 000431 003360 ----- 45 ZR R15
0027554 46 LOS O(RA1) PC=NO,AC=NO
E0027554 01 000432 000420 ----- -001- 47 MSTF O(RA1)
0027555 01 000433 106160 037020 -001- 48 DATA B(1000110001110000)
0027556 49 SIOM EXERLD&-ISOLATE

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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TEST 52 SEGMENT 4

23:41:18 2/05/81 \*\*\*\*

## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

0027556	01	000434	037020	012667	CDGSI0	-002-	01	BSA	MASIOM	
0027560	01	000436	105454	137020		-001-	02	DATA	EXERLD&-ISOLATE	# ENABLE EXTERNAL LOAD OF STORE ERROR REG
0027561							03	SRIO	SERREAD	
0027561	01	000437	137020	012667	CDGSI0	-002-	04	BSA	MASIOM	
0027563	01	000441	047114	-----		-001-	05	DATA	SERREAD	# READ BACK STORE ERROR REGISTER(SER)
0027564	01	000442	107473	-----			06	LSR	MCHB,R11	
0027565							07	CALL	CLNONL	
0027565	01	000443	037020	027646	0027646	-001-	08	BSA	CLNONL	
0027567							09	RTN_TBL	TS181910	
0027567	01	000445	171400	-----		-001-	10	GA		
0027570	01	000446	031000	027574	0027574	-001-	11	LAL	RO,TS181910,RAD	
0027572	01	000450	037000	011162	CDGNM	-001-	12	BL	INTRPN03	

0027574

19 TS181910

						-001-	20	#	COMPARE	
						-001-	21	#	COMPARE ON-LINE MCHB BIT (S(STRSLP)) TO 0.	
						-001-	22	#	IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.	
0027574	01	000452	021214	-----	CDGNM	-001-	23		VFD 1,LFINDX 2,1 1,0 1,SUCCESS 5,(S(STRSLP)) 6,NCOMPARE	
0027575	01	000453	000000	-----		-001-	24		VFD 15,0 1,0	
						-001-	26	#	FAILTST	
						-001-	27	#	FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FL1819.	
						-001-	28	#	DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.	
0027576	01	000454	020017	-----	CDGNM	-001-	29		VFD 1,0 2,1 5,0 2,0 6,NFAILTST	
0027577	01	000455	000030	-----		-001-	30		VFD 16,FL1819	
						-001-	32	#	N03_CODE	
						-001-	33	#	PROCESS JACC CODED ROUTINE AT ADDRESS BT181901.	
0027600	01	000456	040043	000000	CDGNM	-001-	34		VFD 1,0 2,2 7,0 6,NNO3CD	
0027601	01	000457	000000	027603	0027603	-001-	35		ADDR BT181901	

0027603

42 BT181901

0027603							43		CALL	BKCHKINT
0027603	01	000461	137020	027637	0027637	-001-	44		BSA	BKCHKINT
0027605							45		SIOM	MASCINT
0027605	01	000463	137020	012667	CDGSI0	-002-	46		BSA	MASIOM
0027607	01	000465	046071	-----		-001-	47		DATA	MASCINT
0027610	01	000466	103350	-----			48		LN	R14,8
0027611	01	000467	003360	-----			49		ZR	R15

# INITIALIZE STORE CONTROLLER

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 4

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## INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON

W77D

0027612					01	LOS	O(RA1) PC=NO,AC=NO	
E0027612	01	000470	000420	-----	-001- 02	MSTF	O(RA1)	
0027613	01	000471	106160	037020	-001- 03	DATA	B(1000110001110000)	
0027614					04	SIOM	EXERLD&-ISOLATE	
0027614	01	000472	037020	012667	CDGSI0 -002- 05	BSA	MASIOM	
0027616	01	000474	105454	137020	-001- 06	DATA	EXERLD&-ISOLATE	# ENABLE EXTERNAL LOAD OF STORE ERROR REG
0027617					07	SRIO	SERREAD	
0027617	01	000475	137020	012667	CDGSI0 -002- 08	BSA	MASIOM	
0027621	01	000477	047114	-----	-001- 09	DATA	SERREAD	# READ BACK STORE ERROR REGISTER(SER)
0027622	01	000500	107473	-----	10	LSR	MCHB,R11	
0027623					11	CALL	CLNONL	
0027623	01	000501	037020	027646	0027646 -001- 12	BSA	CLNONL	
0027625					13	RTN_TBL	TS181901	
0027625	01	000503	171400	-----	-001- 14	GA		
0027626	01	000504	031000	027632	0027632 -001- 15	LAL	RO,TS181901,RAO	
0027630	01	000506	037000	011162	CDGNN -001- 16	BL	INTRPNO3	

0027632					23 TS181901			
					-001- 24 #	COMPARE		
					-001- 25 #	COMPARE ON-LINE MCHB BIT (S(STRSLP)) TO 0.		
					-001- 26 #	IF COMPARISON EXISTS, SKIP NEXT TABLE ENTRY.		
0027632	01	000510	021214	-----	CDGNN -001- 27	VFD	1,LPINDX 2,1 1,0 1,SUCCES 5,(S(STRSLP)) 6,NCOMPARE	
0027633	01	000511	000000	-----	-001- 28	VFD	15,0 1,0	
					-001- 30 #	FAILTST		
					-001- 31 #	FAILURE EXIT - SYMBOLIC TROUBLE NUMBER IS FL1819.		
					-001- 32 #	DATA WORD IN FAILURE MESSAGE IS ON-LINE MCHB.		
0027634	01	000512	020017	-----	CDGNN -001- 33	VFD	1,0 2,1 5,0 2,0 6,NFAILTST	
0027635	01	000513	000030	-----	-001- 34	VFD	16,FL1819	
					-001- 36 #	PASSTST		
					-001- 37 #	GO TO DIAGNOSTIC MONITOR PASS BRANCH.		
0027636	01	000514	000021	-----	CDGNN -001- 38	VFD	1,0 2,0 7,0 6,NPASSTST	

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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TEST 52 SEGMENT 4

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

0027637  
0027637

01 CSONSUB CSECT  
 02 BKCHKINT  
 03 # SYNCHRONIZE WITH TIMED INTERRUPTS AND BLOCK HARDWARE CHECKS.

0027637  
 0027637 02 000000 103401 000020  
 0027641

07 BEGIN ()  
 08 LI RO,E(4)  
 09

# ALLOW AT LEAST 2.5 MS UNTIL THE NEXT  
 TIMED INTERRUPT ASSUMING THAT NO  
 INTERRUPT MORE FREQUENT THAN 5 MS. IS  
 EQUIPPED.

0027641  
 0027641 02 000002 037020 111163 CSYSUB -001- 13  
 0027643 -001- 14  
 0027643 02 000004 113001 ----- 15  
 0027644 02 000005 105722 ----- -001- 16  
 0027645 -002- 17  
 0027645 02 000006 056400 ----- 18  
 -001- 19

CALL INSYNC  
 BSA INSYNC  
 MIMODE L SS,S,YT DATA=S(BHC) # SET BLOCK HARDWARE CHECKS.  
 MIS S(BHC)  
 VFD 8,SS,SXT 8,YT XF  
 RETURN  
 BTSA

INTERPROCESSOR STORE BUS TEST

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TEST 52 SEGMENT 4

23:41:18 2/05/81 \*\*\*\*

INTERPROCESSOR\_STORE\_BUS DIAGNOSTIC TEST

CDGSON W77D

```

0027646          01 CLNONL
02 # SUBROUTINE TO CLEAN UP THE ON-LINE CU. RO AND R11
03 # ARE CLEARED TO INSURE GOOD PARITY, THE ER IS CLEARED,
04 # THE ERROR INTERRUPT IS CLEARED, BIN IS CLEARED, AND BHC IS CLEARED.

0027646          08 BEGIN      ( )
0027646 02 000007 103000 ----- 09 ZR          RO          # PUT GOOD PARITY IN RO
                                10 CSONSUB OW    0(10)      # 12581
                                -001- 11 NOTE      ***** THE FIRST ADDRESS OVERWRITTEN IS 000010 *****

0027647 02 000010 014673 ----- 14 OR          R11,R11
0027650          15                               # PUT GOOD PARITY IN R11
0027650          16 EOW          # 12581
                                -001- 17 NOTE      ***** THE LAST ADDRESS OVERWRITTEN IS 000010 *****

0027650          20 MIMODE ZER          # CLEAR ER
0027650 02 000011 013000 ----- -001- 21 MIS          0
0027651 02 000012 025750 ----- -002- 22 DATA      ZER%
                                23 CSONSUB OW    0(13)      # 12742
                                -001- 24 NOTE      ***** THE FIRST ADDRESS OVERWRITTEN IS 000013 *****

0027652 02 000013 026005 ----- 27 SBN          RO,S(ERRI)
0027653          28 EOW          # 12742
                                -001- 29 NOTE      ***** THE LAST ADDRESS OVERWRITTEN IS 000013 *****

0027653          32 MIMODE L IS_R,RO
0027653 02 000014 013000 ----- -001- 33 MIS          0
0027654 02 000015 033123 ----- -002- 34 VFD          8,IS_R%T 8,RO%F
0027655          35 ZBIN          # CLEAR BIN.
0027655 02 000016 013002 ----- -001- 36 MIS          2
0027656 02 000017 107322 ----- -001- 37 DATA      36562
0027657          38 MIMODE L SS_R,YT DATA=S(BHC) # CLEAR "BLOCK HARDHARE CHECK" BIT.
0027657 02 000020 013001 ----- -001- 39 MIS          S(BHC)
0027660 02 000021 107322 ----- -002- 40 VFD          8,SS_R%T 8,YT%F
0027661          41 RETURN
0027661 02 000022 056400 ----- -001- 42 BTSA

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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-001- 03 #& TBL 5201  
 -001- 04 #& TEST 52  
 -001- 05 #& SEGMENT 0, 1, OR 2  
 -001- 06 #& PR CDGSON  
 -001- 07 #  
 08 # TWO SUCCESSIVE I/O TRANSMISSIONS TO OFF-LINE STORE  
 09 # CONTROLLER 0 FROM THE ON-LINE CU HAVE FAILED TO COMPLETE.  
 10 # THE DATA FIELD IS THE I/O ORDER WHICH WAS SENT.  
 11 # THE ADDRESS FIELD IS THE FAILURE BRANCH OF THE "NASIOM"  
 12 # SUBROUTINE.  
 13 #  
 14 # MASCM 08-20 FA1064 MAIN STORE CONTROLLER - I/O ORDER DECODER  
 15 # MASCM 08-22 FA1063 MAIN STORE CONTROLLER - I/O ORDER RECEIVER  
 16 # MASCM 08-23 FC203 MAIN STORE CONTROLLER CLOCK & I/O INTERFACE  
 17 # PROC 02-35 FA1016 MICRO CONTROL 1

0027661

-001- 20 #& TBL 5202  
 -001- 21 #& TEST 52  
 -001- 22 #& SEGMENT 1  
 -001- 23 #& PR CDGSON  
 -001- 24 #  
 25 # FAILURE OF A CONTROL OR COMMAND LEAD IN INTERPROCESSOR STORE  
 26 # BUS WITH ON-LINE CU ACCESSING OFF-LINE STORE.  
 27 #  
 28 # PROC 02-21 FA1029 MAIN STORE CONTROL 0  
 29 # PROC 02-22 FA1029 MAIN STORE CONTROL 1  
 30 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL  
 31 # PROC 02-04 FB6 FUSES FOR OTHER STORE DATA 16-23 AND CONTROL  
 32 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19  
 33 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY  
 34 # NOTE--3 DMA 02-17 FC392 DMA MY STORE CONTROL  
 35 # NOTE--3 DMA 02-04 FB6 FUSE BOARD-STORE CONTROL  
 36 # PROC 02-23 FA1046 DOUBLE STORE READ  
 37 #  
 38 # ##### ON-LINE PACKS #####  
 39 # PROC 02-22 FA1029 MAIN STORE CONTROL 1  
 40 # PROC 02-21 FA1029 MAIN STORE CONTROL 0  
 41 #

0027661

0027661

0027661

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5203 FLRSP

CDGSON W77D

-001- 01 #& TBL 5203  
 -001- 02 #& TEST 52  
 -001- 03 #& SEGMENT 1  
 -001- 04 #& PR CDGSON  
 -001- 05 #

0027661

06 # FAILURE OF ON-LINE CU TO COMMUNICATE WITH OFF-LINE STORE

07 #

08 # PROC 02-21 FA1029 MAIN STORE CONTROL 0

09 # PROC 02-22 FA1029 MAIN STORE CONTROL 1

10 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18

11 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19

12 # BIT SLICED BOARDS HAVE POSSIBLE STUCK

13 # HIGH ADDRESS BITS.

14 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL

15 # PROC 02-04 FB6 FUSES FOR OTHER STORE DATA 16-23 AND CONTROL

16 # NOTE--3 DMA 02-17 FC392 DMA MY STORE CONTROL

17 # NOTE--3 DMA 02-04 FB6 FUSE BOARD-STORE CONTROL

18 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY

19 # NOTE--3 DMA 02-21 FC390 DMA STATUS BOARD 1

20 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19

21 # PROC 06-35 FA1021 MICRO CONTROL 6

22 # NOTE--1 MASCM 08-10 FA1060 MAIN STORE CONTROLLER - BITS 16&amp;20

23 #

24 # ##### ON-LINE PACKS #####

25 # PROC 02-22 FA1029 MAIN STORE CONTROL 1

26 # PROC 02-21 FA1029 MAIN STORE CONTROL 0

27 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18

28 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19

29 # PROC 10-22 FA1028 ERROR REG/DISPLAY BUFFER HIGH BITS

30 #

0027661

0027661

INTERPROCESSOR STORE BUS TEST

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TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5204 SAFAL00

CDGSON W77D

```

-001- 01 #& TBL 5204
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 0.
0027661 09 #
10 # PROC 02-08 FA1024 SPECIAL REGISTERS BITS 0 AND 8
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-14 FB382 DMA REGISTER BITS 0, 4, 8, 12
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 16 #
17 # ##### ON-LINE PACKS #####
18 # PROC 02-08 FA1024 SPECIAL REGISTERS BITS 0 AND 8
0027661 19 #

-001- 22 #& TBL 5205
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 1
0027661 30 #
31 # PROC 02-09 FA1024 SPECIAL REGISTERS BITS 1 AND 9
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-13 FB382 DMA REGISTER BITS 1, 5, 9, 13
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 #
38 # ##### ON-LINE PACKS #####
39 # PROC 02-09 FA1024 SPECIAL REGISTERS BITS 1 AND 9
0027661 40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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## TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5206 SA-ALD2

CDGSON

W770

```

-001- 01 #& TBL 5206
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 2
09 #
0027661 10 # PROC 02-10 FA1024 SPECIAL REGISTERS BITS 2 AND 10
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-12 FB382 DMA REGISTER BITS 2, 6, 10, 14
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-10 FA1024 SPECIAL REGISTERS BITS 2 AND 10
19 #

-001- 22 #& TBL 5207
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 3
30 #
0027661 31 # PROC 02-11 FA1024 SPECIAL REGISTERS BITS 3 AND 11
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-10 FC382 DMA REGISTER BITS 3, 7, 11, 15
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 #
38 # ##### ON-LINE PACKS #####
0027661 39 # PROC 02-11 FA1024 SPECIAL REGISTERS BITS 3 AND 11
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 47

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5208 SAFALD4

CDGSON

W77D

```

-001- 01 #& TBL 5208
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 4
09 #
0027661 10 # PROC 02-12 FA1024 SPECIAL REGISTERS BITS 4 AND 12
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-14 FB382 DMA REGISTER BITS 0, 4, 8, 12
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-12 FA1024 SPECIAL REGISTERS BITS 4 AND 12
19 #

-001- 22 #& TBL 5209
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 5
30 #
0027661 31 # PROC 06-14 FA1010 GENERAL REGISTERS BITS 5 AND 13
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-13 FB382 DMA REGISTER BITS 1, 5, 9, 13
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 #
38 # ##### ON-LINE PACKS #####
0027661 39 # PROC 06-14 FA1010 GENERAL REGISTERS BITS 5 AND 13
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 48

## TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5210 SAFAL06

CDGSON

W77D

```

-001- 01 #& TBL 5210
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 6
09 #
0027661 10 # PROC 02-16 FA1024 SPECIAL REGISTERS BITS 6 AND 14
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-12 FB382 DMA REGISTER BITS 2, 6, 10, 14
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-16 FA1024 SPECIAL REGISTERS BITS 6 AND 14
19 #

-001- 22 #& TBL 5211
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 7
30 #
0027661 31 # PROC 02-17 FA1024 SPECIAL REGISTERS BITS 7 AND 15
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-10 FC382 DMA REGISTER BITS 3, 7, 11, 15
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 #
38 # ##### ON-LINE PACKS #####
0027661 39 # PROC 02-17 FA1024 SPECIAL REGISTERS BITS 7 AND 15
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 49

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5212 SAFAL08

CDGSON

W77D

```

-001- 01 #& TBL 5212
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 8
0027661 09 #
10 # PROC 02-08 FA1024 SPECIAL REGISTERS BITS 0 AND 8
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-14 FB382 DMA REGISTER BITS 0, 4, 8, 12
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
0027661 15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-08 FA1024 SPECIAL REGISTERS BITS 0 AND 8
19 #

-001- 22 #& TBL 5213
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 9
0027661 30 #
31 # PROC 02-09 FA1024 SPECIAL REGISTERS BITS 1 AND 9
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-13 FB382 DMA REGISTER BITS 1, 5, 9, 13
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 # NOTE--3 DMA 02-14 FB382 DMA REGISTER BITS 0, 4, 8, 12
38 #
39 # ##### ON-LINE PACKS #####
0027661 40 # PROC 02-09 FA1024 SPECIAL REGISTERS BITS 1 AND 9
41 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 50

## TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5214 SAFAL10

CDGSON W77D

```

-001- 01 #& TBL 5214
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 10
09 #
0027661 10 # PROC 02-10 FA1024 SPECIAL REGISTERS BITS 2 AND 10
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-12 FB382 DMA REGISTER BITS 2, 6, 10, 14
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
0027661 15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-10 FA1024 SPECIAL REGISTERS BITS 2 AND 10
19 #

-001- 22 #& TBL 5215
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 11
30 #
0027661 31 # PROC 02-11 FA1024 SPECIAL REGISTERS BITS 3 AND 11
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-10 FC782 DMA REGISTER BITS 3, 7, 11, 15
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
0027661 36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
37 #
38 # ##### ON-LINE PACKS #####
0027661 39 # PROC 02-11 FA1024 SPECIAL REGISTERS BITS 3 AND 11
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 51

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5216 SAFAL12

CDGSON

W77D

```

-001- 01 #8 TBL 5216
-001- 02 #8 TEST 52
-001- 03 #8 SEGMENT 2
-001- 04 #8 PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 12
09 #
0027661 10 # PROC 02-12 FA1024 SPECIAL REGISTERS BITS 4 AND 12
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-14 FB382 DMA REGISTER BITS 0, 4, 8, 12
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
16 #
0027661 17 # ##### ON-LINE PACKS #####
18 # PROC 02-12 FA1024 SPECIAL REGISTERS BITS 4 AND 12
19 #

-001- 22 #8 TBL 5217
-001- 23 #8 TEST 52
-001- 24 #8 SEGMENT 2
-001- 25 #8 PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 13
30 #
0027661 31 # PROC 06-14 FA1010 GENERAL REGISTERS BITS 5 AND 13
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-13 FB382 DMA REGISTER BITS 1, 5, 9, 13
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
37 #
0027661 38 # ##### ON-LINE PACKS #####
39 # PROC 06-14 FA1010 GENERAL REGISTERS BITS 5 AND 13
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 52

## TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5218 SAFAL14

CDGSON

W77D

```

-001- 01 #& TBL 5218
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 2
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
08 # THE FAILURE WAS NOTED IN BIT 14
09 #
0027661 10 # PROC 02-16 FA1024 SPECIAL REGISTERS BITS 6 AND 14
11 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
12 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
13 # NOTE--3 DMA 02-12 FB382 DMA REGISTER BITS 2, 6, 10, 14
14 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
15 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 16 #
17 # ##### ON-LINE PACKS #####
0027661 18 # PROC 02-16 FA1024 SPECIAL REGISTERS BITS 6 AND 14
19 #

-001- 22 #& TBL 5219
-001- 23 #& TEST 52
-001- 24 #& SEGMENT 2
-001- 25 #& PR CDGSON
-001- 26 #
27 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
28 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.
29 # THE FAILURE WAS NOTED IN BIT 15.
30 #
0027661 31 # PROC 02-17 FA1024 SPECIAL REGISTERS BITS 7 AND 15
32 # PROC 06-08 FB6 FUSES FOR OTHER STORE ADDRESS 0-15
33 # PROC 06-07 FB6 FUSES FOR OTHER STORE DATA 0-15
34 # NOTE--3 DMA 02-10 FC382 DMA REGISTER BITS 3, 7, 11, 15
35 # NOTE--3 DMA 02-01 FB6 FUSE BOARD-STORE ADDRESS
36 # NOTE--3 DMA 02-02 FB6 FUSE BOARD-STORE DATA
0027661 37 #
38 # ##### ON-LINE PACKS #####
0027661 39 # PROC 02-17 FA1024 SPECIAL REGISTERS BITS 7 AND 15
40 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 53

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5220 SAFAL16

CDGSON W77D

-001- 01 #& TBL 5220  
 -001- 02 #& TEST 52  
 -001- 03 #& SEGMENT 2  
 -001- 04 #& PR CDGSON  
 -001- 05 #

0027661

06 # FAILURE OF ADDRESS LEAD OF BUS BETWEEN ON-LINE CC  
 07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.  
 08 # THE FAILURE WAS NOTED IN BIT 16.  
 09 #

10 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18  
 11 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH  
 12 # ADDRESS BIT 16 LOOPS AROUND TO DATA BIT PH.  
 13 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL  
 14 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY  
 15 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19  
 16 # NOTE--3 DMA 02-08 FC384 DMA REGISTER BITS PL, PH

0027661

17 #  
 18 # ##### ON-LINE PACKS #####  
 19 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18  
 20 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH  
 21 #

0027661

-001- 24 #& TBL 5221  
 -001- 25 #& TEST 52  
 -001- 26 #& SEGMENT 2  
 -001- 27 #& PR CDGSON  
 -001- 28 #

0027661

29 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC  
 30 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA DATA BUS.  
 31 # THE FAILURE WAS NOTED IN BIT PL  
 32 #

33 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH  
 34 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL  
 35 # NOTE--3 DMA 02-08 FC384 DMA REGISTER BITS PL, PH  
 36 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY  
 37 # NOTE--3 DMA 02-17 FC392 DMA MY STORE CONTROL  
 38 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19  
 39 #

0027661

40 # ##### ON-LINE PACKS #####  
 41 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH  
 42 #

0027661

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 54

## TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5222 FL17

CDGSON W77D

```

-001- 01 #& TBL 5222
-001- 02 #& TEST 52
-001- 03 #& SEGMENT 3
-001- 04 #& PR CDGSON
-001- 05 #
06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
07 # AND OFF-LINE STORE TO PASS LOOP_AROUND TEST VIA ERROR REGISTER.
08 # THE FAILURE WAS IN BIT 17.
09 #
0027661 10 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19
11 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL
12 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY
0027661 13 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19
14 #
15 # ##### ON-LINE PACKS #####
0027661 16 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19
17 #

-001- 20 #& TBL 5223
-001- 21 #& TEST 52
-001- 22 #& SEGMENT 3
-001- 23 #& PR CDGSON
-001- 24 #
25 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC
26 # AND OFF-LINE STORE TO PASS LOOP_AROUND TEST VIA ERROR REGISTER.
27 # THE FAILURE WAS IN BIT PH.
28 #
0027661 29 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH
30 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL
31 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY
32 # NOTE--3 DMA 02-08 FC384 DMA REGISTER BITS PL, PH
0027661 33 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18
34 #
35 # ##### ON-LINE PACKS #####
0027661 36 # PROC 02-18 FA1024 SPECIAL REGISTERS BITS PL AND PH
37 #

```

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 55

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5224 FL1819

CDGSON W77D

-001- 01 #& TBL 5224  
 -001- 02 #& TEST 52  
 -001- 03 #& SEGMENT 4  
 -001- 04 #& PR CDGSON  
 -001- 05 #  
 06 # FAILURE OF ADDRESS LEAD OF STORE BUS BETWEEN ON-LINE CC  
 07 # AND OFF-LINE STORE TO PASS LOOP-AROUND TEST VIA ERROR REGISTER.  
 08 # THE FAILURE WAS IN BIT 18 OR 19.  
 09 #  
 10 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18  
 11 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19  
 12 # PROC 06-05 FB6 FUSES FOR OTHER STORE ADDRESS 16-PH AND CONTROL  
 13 # NOTE--3 DMA 02-03 FB6 FUSE BOARD-STORE ERROR AND PARITY  
 14 # NOTE--3 DMA 02-09 FC383 DMA REGISTER BITS 16, 17, 18, 19  
 15 #  
 16 # ##### ON-LINE PACKS #####  
 17 # PROC 02-19 FA1030 MISC. DEC. - REGISTERS BITS 16 AND 18  
 18 # PROC 02-20 FA1030 MISC. DEC. - REGISTERS BITS 17 AND 19  
 19 #

0027661

0027661

0027661

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 56

C09

TROUBLE LOCATION MANUAL

23:41:18 2/05/81 \*\*\*\*

5224 FL1819

CDGSON W77D

01 CTON1 MAXSIZE 0,515  
02 CSONSUB MAXSIZE 0,23

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 57





## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	M77D
0000021	A	BIT17	17-22			
0000022	A	BIT18	17-23			
0000023	A	BIT19	17-24			
0000002	A	BIT2	17-07			
0000003	A	BIT3	17-08			
0000004	A	BIT4	17-09			
0000005	A	BIT5	17-10			
0000006	A	BIT6	17-11			
0000007	A	BIT7	17-12			
0000010	A	BIT8	17-13			
0000011	A	BIT9	17-14			
06 0027637	L	0KCHKINT	42-02	27-31, 29-31, 31-13, 32-41, 34-32, 35-47, 38-33, 39-40, 40-44		
	2	R BLKMSK	8-15			
'#		P				
ROC 06-14						
FA1010		GENE				
RAL REGISTER						
S BITS 5 AND						
13'						
'#		P				
ROC 02-18						
FA1024		SPEC				
IAL REGISTER						
S BITS PL AN						
D PH'						
'#		P				
ROC 02-08						
FA1024		SPEC				
IAL REGISTER						
S BITS 0 AND						
8'						
'#		P				
ROC 02-09						
FA1024		SPEC				
IAL REGISTER						
S BITS 1 AND						
9'						
'#		P				
ROC 02-10						
FA1024		SPEC				
IAL REGISTER						
S BITS 2 AND						
10'						
'#		P				
ROC 02-11						
FA1024		SPEC				
IAL REGISTER						
S BITS 3 AND						
11'						

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 60

## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
'#	P	ROC 02-12				
FA1024		SPEC				
IAL REGISTER						
S BITS 4 AND						
12'	T	BS10412		LIBNUM=11		
'#	P	ROC 02-16				
FA1024		SPEC				
IAL REGISTER						
S BITS 6 AND						
14'	T	BS10614		LIBNUM=11		
'#	P	ROC 02-17				
FA1024		SPEC				
IAL REGISTER						
S BITS 7 AND						
15'	T	BS10715		LIBNUM=11		
'#	P	ROC 02-19				
FA1030		MISC				
. DEC. - REG						
ISTERS BITS						
16 AND 18'	T	BS1618		LIBNUM=11		
'#	P	ROC 02-20				
FA1030		MISC				
. DEC. - REG						
ISTERS BITS						
17 AND 19'	T	BS1719		LIBNUM=11		
06 0027377	L	BT17PH0	34-30	34-23		
06 0027442	L	BT17PH1	35-45	35-38		
06 0027506	L	BT181900	38-31	38-24		
06 0027603	L	BT181901	40-42	40-35		
06 0027545	L	BT181910	39-38	39-31		
0047214	A	BUSCHK	19-08			
'CHECK BUS I						
SOLUTION USI						
NG SER'	T	BUSCHKT				
'SER+0'	T	CHDIF	W=1 S=2 N=0 CL=2	27-44		
06 0027342	L	CHKADPL	32-38	32-31		
06 0027230	L	CHKADO	29-29	29-24		
06 0027275	L	CHKAD1	31-10	31-08		
10 R		CHKNDX	8-04			
'CIOBUF+0'	T	CINIT	W=1 S=0 N=0 CL=2			
'CIOBUF+0'	T	CKHLT	W=1 S=2 N=0 CL=2			
'CIOBUF+0'	T	CKSTP	W=1 S=1 N=0 CL=2			
0040374	A	CKTINIT	19-10			
'INITIALIZE						

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 61

PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
ALL STORE CONTROLLER CIRCUITS'						
0046074	A	CLKSTOP	19-15			
'DISABLE STORE CONTROLLER CLOCK OUTPUT'						
0046070	A	CLKSTOPT	19-17			
'ENABLE STORE CONTROLLER CLOCK OUTPUT'						
06 0027646	L	CLNONL	43-01	27-46, 28-23, 28-38, 29-42, 31-28, 33-06, 34-49, 36-15, 38-49, 40-08, 41-12		
0177771	A	CLOCKON	23-01			
0043310	A	CLRSER	19-13			
'CLEAR STORE ERROR REGISTER'						
06 0027150	L	CMDTST	27-27	27-25		
'SERREAD'						

```

<_<(+18
!$*)?
-/_
%_>?
: #@'=" ab
cdefghi n<(+
+ jklmnopqr
x)z=-stuvv
xyz+Lr[≥e012
3456789↑↓,]x
-Cabdefghi
)jklmno
pqr \ s
tuvxyz
0123456789

```

'n T CONLC LIBNUM=10

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
←e<hplx v\$fgs						
-al !%>k jo#b'd" ab cdefghi n<←+ + jklmnopqr x)z=--stuvw xyz+Lr[≥012 3456789+Jj]# -CABCDEFGHI JJKLMNO PQR \ S TUVWXYZ 0123456789						
	T	CONSC	7-25	LIBNUM=10		
CDGSIO	V	CONTPREP		W=7 S=11 N=0 CL=2		
'DGREQLO+0'	T	CONTROLBITS	24-11	LIBNUM=14 44-01, 44-03, 44-20, 45-01, 46-01, 46-22, 47-01, 47-22, 48-01, 48-22, 49-01, 49-22, 50-01, 50-22, 51-01, 51-22, 52-01, 52-22, 53-01, 53-22, 54-01, 54-24, 55-01, 55-20, 56-01, 56-20		
0000000	A	COUNT				
0111432	L	CPATCH	1-44			
0112562	L	CPATCH1	1-45			
0114107	L	CPATCH2	1-46			
0115073	L	CPATCH3	1-47			
0121236	L	CPATCH7	1-48			
06 0027637	L	CSONSUB	1-39			
06 0027122	L	CSTON1	1-38 24-11			
'CHKWRD+0'	T	CTRLCK		W=1 S=16 N=0 CL=2		
0000000	A	DATAWD	24-11			

←.<(+18  
!\$\*)  
-/  
%>?  
:#@'=" n<←+  
+ jklmnopqr  
x)z=--  
+Lr[≥012  
3456789+Jj]#  
-CABCDEFGHI  
JJKLMNO  
PQR \ S

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 63

## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
TUVWXYZ 0123456789						
	T	DELLC		LIBNUM=10		
CTSD	V	DGNLIM	7-12			
CTSD	V	DGREQ	7-37			
'SER+0'	T	DHPER		W=1 S=11 N=0 CL=2		
'SER+0'	T	DLPER		W=1 S=15 N=0 CL=2		
'# NOTE--3 D MA 02-17 FC392 DMA MY STORE CON TROL'	T	DMAC		LIBNUM=11		
'# NOTE--3 D MA 02-01 FB6 FUSE BOARD-STORE ADDRESS'	T	DMAFUS1		LIBNUM=11		
'# NOTE--3 D MA 02-02 FB6 FUSE BOARD-STORE DATA'	T	DMAFUS2		LIBNUM=11		
'# NOTE--3 D MA 02-03 FB6 FUSE BOARD-STORE ERROR AND P ARITY'	T	DMAFUS3		LIBNUM=11		
'# NOTE--3 D MA 02-04 FB6 FUSE BOARD-STORE CONTROL'	T	DMAFUS4		LIBNUM=11		
'# NOTE--3 D MA 02-21 FC390 DMA STATUS BOARD 1'	T	DMASTS1		LIBNUM=11		
'# NOTE--3 D MA 02-14 FB382 DMA REGISTER BIT S 0, 4, 8, 1 2'	T	DMA1A		LIBNUM=11		
'# NOTE--3 D MA 02-13 FB382 DMA REGISTER BIT S 1, 5, 9, 1						

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

23:41:18 2/05/81 TRADE SECRET - SEE TRADE SECRET RESTRICTIVE NOTICE ON COVER SHEET CDGSON ISSUE 05 PAGE 64

## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
3'	T	DMA1B		LIBNUM=11		
'# NOTE--3 D						
MA		02-12				
FB382		DMA				
REGISTER BIT						
S		2, 6, 10,				
14'	T	DMA1C		LIBNUM=11		
'# NOTE--3 D						
MA		02-10				
FC382		DMA				
REGISTER BIT						
S		3, 7, 11,				
15'	T	DMA1D		LIBNUM=11		
'# NOTE--3 D						
MA		02-09				
FC383		DMA				
REGISTER BIT						
S		16, 17, 18				
19'	T	DMA2		LIBNUM=11		
'# NOTE--3 D						
MA		02-08				
FC384		DMA				
REGISTER BIT						
S		PL, PH'				
06	0027127	L	DOSEG0	26-15 26-08		
06	0027143	L	DOSEG1	26-28 26-24		
06	0027223	L	DOSEG2	28-44 28-41		
'# P						
ROC		02-23				
FA1046		DOUB				
LE		STORE REA				
D'						
		12	DSR	LIBNUM=11		
		R	ER	LIBNUM=13		28-19
0146074		A	ERCOLL	19-19		
'COLLECT ERR						
ORS IN STORE						
'ERROR REG'						
			T	ERCOLLT		
'# P						
ROC		10-22				
FA1028		ERRO				
R		REG/DISPLA				
Y		BUFFER HIG				
H		BITS'				
		15	ERHL1910	LIBNUM=11		
		R	ERRI	W=1 S=5 N=0 CL=1 LIBNUM=13		43-27
		10	ERSAVE	8-21		
		0	J ESS2	1-10		
		1	J ESS2E	1-09		
CSYSUB		V	EXCOFLPG	7-28		
0145454		A	EXERLD	19-21 34-43, 36-09, 38-43, 40-02, 41-06		

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
'ENABLE EXTE RNAL LOAD OF STORE ERROR REG'	T	EXERLDT				
0145454	A	EXLDB15	19-24			
'ENABLE EXTE RNAL LOAD OF STORE ERROR REG W/ ERRO R COLLECT OP TION'	T	EXLDB15T				
CDGNOF	V	FAILOFF	4-41			
0010000	A	FAK010	22-36			
0005440	A	FASTRF	19-26			
'PERFORM FAS T REFRESH ON STORE'	T	FASTREFT				
0045454	A	FASTRNC	19-28			
'FORCE FAST REFRESH W/O CLOCK'	T	FASTRNCT				
0146074	A	FBIT09	19-32			
0146064	A	FBIT09R	19-35			
'COLLECT ERR ORS IN SER W / REFRESH ON' 'COLLECT ERR ORS IN STORE ERROR REGIS TER'	T	FBIT09T				
0146076	A	FBRMB15	19-37			
'FANOUT BOAR D REFRESH W/ ERROR COLLE CT'	T	FBRMB15T				
'CIOBUF+0'	T	FBT09		W=1 S=17 N=0 CL=2		
0020000	A	FBUSRDN	22-38			
0046314	A	FCHKBT	19-39			
0046304	A	FCHKBTR	19-41			
'ACTIVATE SH IFTER CHECK BIT W/ REFRE SH ENABLED'	T	FCHKBTRT				
'ACTIVATE MA IN SHIFTER C HECK BIT'	T	FCHKBTT				
0040574	A	FCHKOS	19-43			
'FORCE ZEROS TO MODULE S						

INTERPROCESSOR STORE BUS TEST

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PATCH HISTORY				23:41:18	2/05/81	****
VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
ELECT XOR CH ECK & WRITE PROTECT SELE CT XOR CHECK CIRCUITS'	T	FCHKQST				
0041274	A	FCHK1S	19-46			
'FORCE ONES TO MODULE S ELECT XOR CH ECK & WRITE PROTECT SELE CT XOR CHECK CIRCUITS'	T	FCHK1ST				
0140574	A	FCKOS15	19-49			
'FORCE ZEROS TO CHECK CK TS W/ ERROR COLLECT'	T	FCKOS15T				
0141274	A	FCK1S15	20-02			
'FORCE ONES TO CHECK CK TS W/ ERROR COLLECT'	T	FCK1S15T				
0043074	A	FDISIDLE	20-04			
'FORCE DISAB LE OF IDLE F LOP'	T	FDISIDLET				
0	U	FFFF				
0000002	A	FBOBRM	22-44			
0145454	A	FFRMB15	19-30			
'FORCE FAST REFRESH & BI T 15'	T	FFRMB15T				
0020016	A	FGLDNCFR	23-02			
1	J	FIELD	1-09			
CDGSIO	V	FINAL	7-24			
0000002	A	FLCMND	44-20	28-07, 44-20		
0000027	A	FLPH	55-20	35-29, 36-49, 55-20		
0000003	A	FLRSP	45-01	28-33, 45-01		
0046156	A	FLSHD	20-06			
0046154	A	FLSHDNC	20-09			
'PRESENT ZER O TO INPUT O F MAIN SHIF T'	T	FLSHDNC				
'START ZERO INTO MAIN SH IFTER'	T	FLSHOT				
0000026	A	FL17	55-01	35-17, 36-37, 55-01		
INTERPROCESSOR STORE BUS TEST					PR-1C928-50	
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PATCH HISTORY				23:41:18	2/05/81	****
VALUE	T NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D	
0000030	A FL1819	56-01	39-22, 40-30, 41-34, 56-01			
0044474	A FN0TIM	20-16				
0044470	A FN0TIMC	20-19				
'BLOCK TIMIN G TO FANOUT BOARDS(W/CLO CK)'						
	T FN0TIMCT					
'INHIBIT TIM ING SIGNALS TO FANOUT BO ARDS'						
	T FN0TIMT					
0045434	A FN0WRT	20-12				
0045430	A FN0WRTC	20-14				
'FORCE WRITI NG OF ONES W / CLOCK RUNN ING'						
	T FN0WRTCT					
'FORCE WRITI NG OF ALL-ON ES DATA'						
	T FN0WRTT					
10	R F0BCNT	8-05				
0041550	A F0BMT	20-21				
'FANOUT BOAR D MAINTENANC E TEST'						
	T F0BMTT					
CDGSFA	V F0BNDX	7-17				
'PAGSCR+26'	T F0BNUM		W=20 S=0 N=32 CL=2			
'SER+0'	T F0BPARER		W=1 S=10 N=0 CL=2			
'SER+0'	T F0BTERA		W=1 S=7 N=0 CL=2			
'SER+0'	T F0BTERB		W=1 S=0 N=0 CL=2			
0000004	A F0UR	17-25				
0041474	A FRFSELO	20-23				
'CANCEL SELE CT FROM F0B0 DURING REFR ESH'						
	T FRFSELOT					
0042334	A FRFSEL1	20-25				
'CANCEL SELE CT FROM F0B1 DURING REFR ESH'						
	T FRFSEL1T					
0042534	A FRFSEL2	20-27				
'CANCEL SELE CT FROM F0B2 DURING REFR ESH'						
	T FRFSEL2T					
0043234	A FRFSEL3	20-29				
'CANCEL SELE CT FROM F0B3						
INTERPROCESSOR STORE BUS TEST				PR-1C928-50		
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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
DURING REFR						
ESH'	T	FRFSEL3T				
0043434	A	FRFSEL4	20-31			
'CANCEL SELE						
CT FROM FOB4						
DURING REFR						
ESH'	T	FRFSEL4T				
0044354	A	FRFSEL5	20-33			
'CANCEL SELE						
CT FROM FOB5						
DURING REFR						
ESH'	T	FRFSEL5T				
0044554	A	FRFSEL6	20-35			
'CANCEL SELE						
CT FROM FOB6						
DURING REFR						
ESH'	T	FRFSEL6T				
0045254	A	FRFSEL7	20-37			
'CANCEL SELE						
CT FROM FOB7						
DURING REFR						
ESH'	T	FRFSEL7T				
0044334	A	FRREQA	20-39			
'SET REFRESH						
REQUEST ON						
TIMING BOARD						
(FA1071)'	T	FRREQAT.				
0040674	A	FRREQB	20-42			
0040664	A	FRREQBR	20-45			
'SET REFRESH						
REQUEST ON						
FA1062 W/ RE						
FRESH ENABLE						
D'	T	FRREQBRT				
'SET REFRESH						
REQ COPY ON						
CHECK BOARD						
A (FA1062)'	T	FRREQBT				
0100000	A	FSBIT09	22-41			
'CIOBUF+0'	T	FSEL		W=1 S=16 N=0 CL=2		
0046074	A	FSELA	20-47			
'FORCE STORE						
SELECT (ISOL						
ATE) SIGNAL						
ON FA1071'	T	FSELAT				
0004714	A	FSELB	21-02			
0004710	A	FSELBC	21-05			
'FORCE DUPLI						
CATED STORE						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
SELECT(SELB) W/ CLOCK'	T	FSELBCT				
'FORCE DUPLI CATED STORE SELECT(SELB) ACTIVE'	T	FSELBT				
0046516	A	FSTFBRM	21-07			
'FORCE CONTR OLLER & FANO UT BOARDS TO REFRESH'	T	FSTFBRMT				
0042354	A	FSTNM	21-09			
0052354	A	FSTNMFR	21-11			
'FORCE NORMA L MODE IN CO NTROLLER & R EFRESH TO FA NOUT BOARDS'	T	FSTNMFR				
0042344	A	FSTNHR	21-13			
'FORCE MCDE TO NORMAL W/ REFRESH ENA BLED'	T	FSTNMRT				
'FORCE MODE FLOP TO NORM AL STATE'	T	FSTNMT				
0046514	A	FSTRM	21-15			
'FORCE MODE FLOP TO REFR ESH STATE'	T	FSTRMT				
0046234	A	FTINWP	21-17			
'FORCE IN-WR ITE-PROTECT INHIBIT'	T	FTINWPT				
'#	P					
ROC 06-05 FB6 FUSE S FOR OTHER STORE ADDRES S 16-PH AND CONTROL'	T	FUSADH		LIBNUM=11		
'#	P					
ROC 06-08 FB6 FUSE S FOR OTHER STORE ADDRES S 0-15'	T	FUSADL		LIBNUM=11		
'#	P					
ROC 02-04						

INTERPROCESSOR STORE BUS TEST

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VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W770
FB6		FUSE				
S FOR OTHER						
STORE DATA 1						
6-23 AND CON						
TROL'	T	FUSDTH		LIBNUM=11		
'#	P					
ROC 06-07						
FB6		FUSE				
S FOR OTHER						
STORE DATA 0						
-15'	T	FUSDTL		LIBNUM=11		
'CHKWRD+0'	T	FXORG		W=1 S=17 N=0 CL=2		
0000004	A	HALTCLK	22-46			
1	R	HIPATBAK	8-13			
HIPATBAKXT			8-14	IS A SYNONYM OF R1XT		
'ILLEGAL CON						
DITIONAL IN						
THE IF MACRO	T	IFERROR1				
'DATA > 0 OR						
DATA < 0 IS						
MEANINGLESS						
'USE DATA =						
'0'	T	IFERROR2				
'TWO CONSTAN						
TS ARE BEING						
COMPARED IN						
IF MACRO	T	IFERROR3				
'AN ITEM WAS						
COMPARED TO						
SOMETHING O						
THET THAN A						
CONSTANT	T	IFERROR4				
'DESTINATION						
OF AN = STA						
TEMENT IS A						
CONSTANT	T	IFERROR5				
'ATTEMPTING						
TO SET ITEM						
= TO SOMETHI						
NG OTHER THA						
N A CONSTANT	T	IFERROR6				
'ITEM MAY ON						
LY USE THE =						
AND = COND						
ITIONAL	T	IFERROR7				
CSYSUB	V	INIT_OCC	7-29			
0000001	A	INITBIT	22-42			
CSYSUB	V	INITOST	7-30			
CSYSUB	V	INSYNC	3-21	7-31, 42-14		

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
CDGNM	X	INTRPN03	4-38	26-25, 28-01, 28-27, 28-42, 29-46, 31-32, 33-10, 35-04, 36-19, 39-04, 40-12, 41-16		
'PAGSCR+25'	T	I0ADDR		W=20 S=0 N=31 CL=2		
'I&'	T	I0BRK		26-18		
0006220	A	I0GO	21-19			
'ENABLE ON-LINE I/O ACCESS TO OFF-LINE STORE'	T	I0GOT				
0000001	A	I0PRTYER	44-03			
0125252	A	I0TSTA	21-21			
'I/O TEST PATTERN #1'	T	I0TSTAT				
0052525	A	I0TST5	21-23			
'I/O TEST PATTERN #2'	T	I0TST5T				
0000066	A	IS_RXT		LIBNUM=13 43-34		
'CHKWRD+0'	T	ISOBTS		W=7 S=0 N=0 CL=2		
0067214	A	ISOCHK	21-25			
'ISOLATE FROM FAR STORES & VERIFY VIA SER'	T	ISOCHKT				
0027214	A	ISOCHKU	21-29			
'APPLY ONES TO STORE DATA BUS(W/O ISOLATE)'	T	ISOCHKUT				
0040000	A	ISOLATE	22-40	38-43, 40-02, 41-06		
0043454	A	KILL12	21-31			
'CLEAR SHIFTER BIT IN POSITION 12'	T	KILL12T				
'CIOBUF+0'	T	LDFG		W=1 S=15 N=0 CL=2		
0020000	A	LOADCHK	22-39			
'PAGSCR'	T	LONAM_BASADDR				
'SER'	T	LONAM_CHDIF				
'CIOBUF'	T	LONAM_CINIT				
'CIOBUF'	T	LONAM_CKHLT				
'CIOBUF'	T	LONAM_CKSTP				
'DGREQLO'	T	LONAM_CONTROLBITS				
'CHKWRD'	T	LONAM_CTRLCK				
'SER'	T	LONAM_DHPER				
'SER'	T	LONAM_DLPER				
'CIOBUF'	T	LONAM_FBT09				
'PAGSCR'	T	LONAM_FOBNUM				
'SER'	T	LONAM_FOBPAR				
		ER				

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
'SER'	T	LONAM_FOBTER				
	A					
'SER'	T	LONAM_FOBTER				
	B					
'CIOBUF'	T	LONAM_FSEL				
'CHKWRD'	T	LONAM_FXORG				
'PAGSCR'	T	LONAM_IOADDR				
'CHKWRD'	T	LONAM_ISOBTB				
'CIOBUF'	T	LONAM_LOFG				
'PAGSCR'	T	LONAM_LOOPSU				
	B					
'SER'	T	LONAM_MODER				
'SER'	T	LONAM_MPXER				
'MASCIOSC'	T	LONAM_MSSC0				
'MASCIOSC'	T	LONAM_MSSC1				
'MASCIOSC'	T	LONAM_MSSC2				
'MASCIOSC'	T	LONAM_MSSC3				
'STRSTAT'	T	LONAM_PASBT				
'STRSTAT'	T	LONAM_PHBAK				
'STRSTAT'	T	LONAM_PLBAK				
'SER'	T	LONAM_PWER				
'CIOBUF'	T	LONAM_REFST				
'SER'	T	LONAM_RSELER				
'RSLCHK'	T	LONAM_RSEL06				
'RSLCHK'	T	LONAM_RSEL7				
'CHKWRD'	T	LONAM_RSVDO				
'RSLCHK'	T	LONAM_RSVD1				
'RSLCHK'	T	LONAM_SAPHLP				
'RSLCHK'	T	LONAM_SA17LP				
'SER'	T	LONAM_SCMER				
'CHKWRD'	T	LONAM_SDPCK				
'SER'	T	LONAM_SHER				
'STRSTAT'	T	LONAM_SNGBTE				
	R					
'DGREQLO'	T	LONAM_SPARE				
'CIOBUF'	T	LONAM_STORDE				
	R					
'RSLCHK'	T	LONAM_STRSLP				
'SER'	T	LONAM_TBER				
'PAGSCR'	T	LONAM_TIMSAV				
'DGREQLO'	T	LONAM_TSTNUM				
'PAGSCR'	T	LONAM_UPADDR				
'CHKWRD'	T	LONAM_WDISOL				
'MASCIOSC'	T	LONAM_OSSC0				
'MASCIOSC'	T	LONAM_OSSC1				
'MASCIOSC'	T	LONAM_OSSC2				
'MASCIOSC'	T	LONAM_OSSC3				
'STRSTAT'	T	LONAM_OWDSTR				
	0					

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
'CIOBUF'	T	LONAM_010TM				
'CHKWRD'	T	LONAM_2EPCK				
CDGNM	V	LOOPIND	3-20	7-09		
'PAGSCR+24'	T	LOOPSUB		W=20 S=0 N=30 CL=2		
0000000	A	LPINDX	30-02	30-05, 30-16, 30-19, 30-33, 30-36, 31-42, 31-45, 32-12, 32-15, 33-18, 33-21, 35-07, 35-10, 35-19, 35-22, 36-27, 36-30, 36-39, 36-42, 39-12, 39-15, 40-20, 40-23, 41-24, 41-27		
	4	R LSTPAT	8-17			
'# NOTE--1	M					
ASCM 08-10						
FA1060	MAIN					
STORE CONTR						
OLLER - BITS						
16820'	T	MASCBS9		LIBNUM=11		
'#	M					
ASCM 08-23						
FC203	MAIN					
STORE CONTR						
OLLER CLOCK						
& I/O INTERF						
ACE'	T	MASCCLK		LIBNUM=11		
0046071	A	MASCINT	21-33	26-21, 31-18, 32-45, 34-35, 36-01, 38-36, 39-43, 40-47		
'INITIALIZE						
STORE CONTR						
LLER'	T	MASCINTT				
MASACS	V	MASCIOSC	7-04	26-16		
0046076	A	MASCLK	21-37			
0046074	A	MASCLKN	21-40			
'FAKE SECOND						
HALF OF STO						
RE CLOCK CYC						
LE'	T	MASCLKNT				
'FAKE FIRST						
HALF OF STOR						
E CLOCK CYCL						
E'	T	MASCLKT				
'#	M					
ASCM 08-22						
FA1063	MAIN					
STORE CONTR						
OLLER - I/O						
ORDER RECEIV						
ER'	T	MASCHTCA		LIBNUM=11		
'#	M					
ASCM 08-20						
FA1064	MAIN					
STORE CONTR						
OLLER - I/O						
ORDER DECODE						
R'	T	MASCHTCB		LIBNUM=11		

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
CTSD	V	MASERCNT	7-35			
CDGSIO	X	MASIAM	7-19	26-20, 27-41, 29-34, 31-17, 31-20, 32-44, 32-47, 34-34, 34-42, 34-45, 35-49, 36-08, 36-11, 38-35, 38-42, 38-45, 39-42, 40-01, 40-04, 40-46, 41-05, 41-08		
MASACS	V	MASONOFF	7-39			
	3	R MCHB		LIBNUM=13 27-47, 28-24, 29-40, 31-26, 33-04, 34-47, 36-13, 38-47, 40-06, 41-10		
'#	P					
ROC	02-35					
FA1016	MICR					
O CONTROL	1'	T MC1		LIBNUM=11		
'#	P					
ROC	06-35					
FA1021	MICR					
O CONTROL	6'	T MC6		LIBNUM=11		
CDGSIO	V	MDSELMSK	7-20			
	14	P MEMADDR	8-25			
	14	R MEMADDR0	8-23			
	15	R MEMADDR1	8-24			
CDGSBS	V	MEMOP	7-14			
CDGSBS	V	MEMOPI	7-15			

```

+._(18
  |s*);
  /
  ?
  :#0'=" ab
  cdefghi n<(+
  + jklmnopqr
  ):=--stuvw
  xyz+L[>=012
  3456789+J,]#
  -(ABCDEFGHI
    )JKLMNO
  PQR \ S
  TUVWXYZ
  0123456789

```

	T	MICODETR		LIBNUM=13		
'SER+0'	7	R MNRNDX	8-20			
CDGSIO	V	MODSIZE	7-21			
0000000	A	MOD0	17-27			
0000001	A	MOD1	17-28			
0000002	A	MOD2	17-29			
0000003	A	MOD3	17-30			
0000004	A	MOD4	17-31			

INTERPROCESSOR STORE BUS TEST

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PATCH HISTORY				23:41:18	2/05/81	****
VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
0000005	A	MOD5	17-32			
0000006	A	MOD6	17-33			
0000007	A	MOD7	17-34			
'SER+0'	T	MPXER	W=1 S=1 N=0 CL=2			
0006071	A	MSCITNS	21-35			
'INITIALIZE						
STORE CONTROL W/O FOR						
CE SELECT'	T	MSCITNST				
'MASCIOSC+0'	T	MSSCO	W=20 S=0 N=0 CL=2			
'MASCIOSC+2'	T	MSSC1	W=20 S=0 N=2 CL=2			
'MASCIOSC+4'	T	MSSC2	W=20 S=0 N=4 CL=2			
'MASCIOSC+6'	T	MSSC3	W=20 S=0 N=6 CL=2			
'#	P					
ROC 02-21						
FA1029 MAIN						
STORE CONTROL						
OL 0'	T	MSTCONTO	LIBNUM=11			
'#	P					
ROC 02-22						
FA1029 MAIN						
STORE CONTROL						
OL 1'	T	MSTCONT1	LIPNUM=11			
0106263	A	MTCRD	18-24			
0106203	A	MTCWR	18-26			
CDGNM	V	NABT	4-31			
CDGNM	V	NADD OFF	4-22			
CDGNM	V	NADMIC	4-23			
CDGNM	V	NBEGIN	4-28			
CDGNM	V	NBGN	4-39 24-14			
CDGNM	V	NCLRMS	4-33			
CDGNM	V	NCOMPARE	4-26 30-05, 30-19, 30-36, 31-45, 32-15, 33-21, 35-10, 35-22, 36-30, 36-42, 39-15, 40-23, 41-27,			
CDGNM	V	NDISABA	4-07			
CDGNM	V	NDISABB	4-08			
CDGNM	V	NEXECUTE	4-25			
CDGNM	V	NFAILTST	4-16 28-06, 28-32, 30-11, 30-25, 32-04, 33-27, 35-16, 35-28, 36-36, 36-48, 39-21, 40-29, 41-33,			
CDGNM	V	NFLBITS	4-37 30-42, 32-21			
CDGNM	V	NFRZ	4-27			
CDGNM	V	NLDMIR	4-24			
CDGNM	V	NLP END	4-29			
CDGNM	V	NMASK	4-18 30-30, 32-09			
CDGNM	V	NMICRO	4-02			
0106260	A	NMLRD	18-28			
0106200	A	NMLWR	18-30			
CDGNM	V	NNO3CD	4-34 26-07, 27-24, 29-23, 31-07, 32-30, 34-22, 35-37, 38-23, 39-30, 40-34			
CDGNM	V	NOSTPMES	7-10			
CDGNM	V	NPASSTST	4-19 41-38			
INTERPROCESSOR STORE BUS TEST						
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PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W770
CDGNM	V	NPROS	4-14	27-20, 29-19, 31-03, 32-25, 34-18, 35-33, 38-19, 39-26		
CDGNM	V	NRDMICRO	4-32			
CDGNM	V	NRESCLK	4-12			
CDGNM	V	NRETRN	4-03			
CDGNM	V	NRTNBLM	4-45	26-03		
0006074	A	NSELA	20-49			
'RESET STORE						
SELECT (ISOL						
ATE) SIGNAL						
ON FA1071'	T	NSELAT				
CDGNM	V	NSEND	4-20			
CDGNM	V	NSKIP	4-30			
CDGNM	V	NSTOP	4-06			
CDGNM	V	NSTPCLK	4-10			
CDGNM	V	NSTRT	4-05			
CDGNM	V	NSTRTCLK	4-09			
CDGNM	V	NTESTSEG	4-15	27-08, 29-08, 34-08, 38-08		
CDGNM	V	NTGCLK	4-11			
CDGNM	V	NTMTEST	4-35			
CDGNM	V	NTTY	4-17			
0000000	A	NUM	23-05			
CDGNM	V	NWDST	4-46			
5	R	NXTPAT	8-18			
CDGNM	V	NZERO ER	4-13			
CDGNM	V	NZERPT	4-36			
CDGNM	V	N2RETRN	4-04			
CDGNM	V	N2SEND	4-21			
0000200	A	OFLNCHNK	17-37			
0007760	A	OFLNDONE	17-38			
12	R	OFSTM		W=1 S=20 N=0 CL=1 LIBNUM=13 28-21		
0000001	A	ONE	17-35			
0177777	A	ONES	17-36			
'# #####						
## ON-LINE P						
ACKS #####' T ONLINE LIBNUM=11						
A						

```

<.(AON
  X$*);
-s/
X_>?
:##'L" ab
cdefghi n<<+
+ jklmnopqr
n):z=-stuvh
    
```

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W770
xyz+Lr[3#012						
3456789+J,]#						
-(IBCLEFGHI						
JKLMNO						
PQR		\ S				
LLLWLYZ						
0123456789						
	T	OPTR				
0000705	A	ORG_000010	43-11			
0000713	A	ORG_000013	43-24			
CTSD	V	PAGSCR	3-22	7-36, 26-18		
10	R	PARSLT	8-22			
3	R	PASBT	16-08	W=1 S=6 N=0 CL=1		
CDGN0F	V	PASSOFF	4-40			
CDGNM	V	PASSTST	7-11			
16	P	PATADDR	8-26			
0	R	PATBAK	8-12			
6	R	PATNDX	8-19			
0000025	A	PH		LIBNUM=13 30-19, 31-45		
3	R	PHBAK	16-04	W=1 S=1 N=0 CL=1		
0000024	A	PL		LIBNUM=13 30-05, 33-21		
3	R	PLBAK	16-03	W=1 S=0 N=0 CL=1		
'CDGSON'	T	PNAME				
0000020	A	PRH0L0	17-45			
0000005	A	PRH0L1	17-46			
0000012	A	PRH1L0	17-47			
0000017	A	PRH1L1	17-48			
CBLM	V	PRTHASER	7-06			
0000002	A	PRW0H1L0	17-49			
0000007	A	PRW0H1L1	18-01			
0000010	A	PRW1H0L0	18-02			
0000015	A	PRW1H0L1	18-03			
'SER+0'	T	PWER		W=1 S=12 N=0 CL=2		
06 0027177	L	P314	28-10	27-45		
06 0027214	L	P318	28-36	28-22		
11	R	RANGE	8-07			
14	P	RA0		LIBNUM=3 8-25, 26-16, 26-24, 27-49, 28-26, 28-41, 29-45, 31-31, 33-09, 35-03, 36-18, 39-03, 40-11, 41-15		
16	P	RA1		LIBNUM=3 8-26, 27-32, 27-34, 27-37, 29-32, 29-38, 31-24, 32-42, 33-02, 34-39, 36-05, 38-37, 38-39, 39-47, 41-02		
0047410	A	RDAD	21-42	29-35, 31-21, 32-48		
0047414	A	RDADNC	21-45			
'GATE STORE						
ADDRESS BITS						
TO STORE DA						
TA BUS'	T	RDADNCT				
'GATE STORE						
ADDRESS BUS(						
SA0-16,PL) T						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W770
0		STORE DATA				
BUS(SDD-15,						
PL,PH) W/ CL						
OCK'	T	RDADT				
'CIOBUF+0'	T	REFST		W=1 S=3 N=0 CL=2		
0006070	A	REFSTOP	21-47			
'INHIBIT REF						
RESHING OF S						
TORE'	T	REFSTOPT				
0006060	A	REFSTRY	21-49			
'RESUME REGU						
LAR REFRESHI						
NG OF STORE'	T	REFSTRTT				
0046060	A	RFWISOL	22-02			
'RESUME REGU						
LAR REFRESH						
W/ STORE ISO						
LATED'	T	RFWISOLT				
CSYSUB	V	RGCHKADR	7-32			
' BASE ADDE						
SS OF STORE/						
MOD UNDER TE						
ST'	T	RMK_BASADDR				
' ERROR INDI						
CATED BY STO						
RE COMMAND C						
HECKER'	T	RMK_CHDIF				
' MAIN STORE						
CONTROLLER						
INITIALIZATI						
ON'	T	RMK_CINIT				
' CONTROLLER						
CLOCK HALT'	T	RMK_CKHLT				
' CONTROLLER						
CLOCK STEP'	T	RMK_CKSTP				
'	T	RMK_CONTROLB				
'		ITS				
' RESULT OF						
STORE CONTRO						
L LEADS ISOL						
ATION'	T	RMK_CTRLCK				
' ERROR IN P						
ARITY OVER H						
IGH DATA BIT						
S'	T	RMK_DHPER				
' ERROR IN P						
ARITY OVER L						
OW DATA BITS'	T	RMK_DLPER				
' FORCE BIT						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
15 ACTIVE IN MAIN SHIFTE R'	T	RMK_FBT09				
' NUMBER OF MEMORY MODUL ES (OR FANOU T BOARDS) IN STORE CURRE NTLY UNDER T EST'	T	RMK_FOBNUM				
' PARITY ERR OR DETECTED IN ADDRESS R EACHING FANO UT BOARD(S)'	T	RMK_FOBPARER				
' STORE TIMI NG ERROR FRO M SELECTED F OB'	T	RMK_FOBTERA				
' STORE TIMI NG ERROR FRO M UNSELECTED FOB'	T	RMK_FOBTERB				
' STORE SELE CT FORCE ON TIMING BOARD A'	T	RMK_FSEL				
' I/O ORDER CHECKER EXCL USIVE-OR RES ULT'	T	RMK_FXORG				
' I/O SUBCHA NNEL ADDRESS FOR CURRENT STORE CONTR OLLER'	T	RMK_IOADDR				
' SDD-6,SDB- 14 ISOLATE T EST RESULTS'	T	RMK_ISOBTS				
' ORDER CHEC KER EXCLUSIV E-OR LOAD'	T	RMK_LDFG				
' ADDRESS OF SUBSTITUTE FOR 'LOOP' I N TTY TROUBL E MESSAGE'	T	RMK_LOOBSUB				
' ALL-SEEMS- WELL SIGNAL						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
NOT RECEIVED FROM MODULE (FOB) ACCESS ED DURING NORMAL CYCLE'	T	RMK_MODER				
' MULTIPLEXOR ERROR DETECTED BY CHECK BOARD'	T	RMK_MPXER				
' ADDRESS OF MY STORE SUBCHANNEL 0'	T	RMK_MSSCO				
' ADDRESS OF MY STORE SUBCHANNEL 1'	T	RMK_MSSC1				
' ADDRESS OF MY STORE SUBCHANNEL 2'	T	RMK_MSSC2				
' ADDRESS OF MY STORE SUBCHANNEL 3'	T	RMK_MSSC3				
' REPEAT PASS THRU TEST INDICATOR'	T	RMK_PASBT				
' PARITY HIGH VALUE READ BACK'	T	RMK_PHBAK				
' PARITY LOW VALUE READ BACK'	T	RMK_PLBAK				
' ERROR IN PARITY FOR WRITE STORE'	T	RMK_PWER				
' STORE REFRESH STOP'	T	RMK_REFST				
' ALL MEMORY MODULES (FOBS) NOT SELECTED DURING REFRESH'	T	RMK_RSELER				
' REFRESH SELECTS FROM FRONT BOARDS 0-6'	T	RMK_RSEL06				
' REFRESH SELECT FROM FRONT BOARD 7'	T	RMK_RSEL7				
' SD7, SD15 ISOLATE TEST						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
RESULT - ONL Y GATED INTO BY LOAD I/O DECODER CHE CK (LOADCHK) OPTION'	T	RMK_RSVD0				
' RESERVED - FOBTERA IS SET AFTER IN IT'	T	RMK_RSVD1				
' STORE ADDR ESS PARITY H IGH LOOP RES ULT'	T	RMK_SAPHLP				
' STORE ADDR ESS BIT 17 L OOP RESULT'	T	RMK_SA17LP				
' PREMATURE STORE COMPLE TE(SCM)'	T	RMK_SCMER				
' RESULT OF STORE DATA P ARITY ISOLAT ION'	T	RMK_SDPCK				
' ERROR IN M AIN SHIFTER OPERATION'	T	RMK_SHER				
' SINGLE BIT ERROR FLAG'	T	RMK_SNGBTER				
'	T	RMK_SPARE				
' 4/8 MAINT NANCE STATE CODE'	T	RMK_STORDER				
' STORE SELE CT ADDRESS B ITS LOOP RES ULT'	T	RMK_STRSLP				
' ERROR DETE CTED ON TIMI NG BOARD'	T	RMK_TBTER				
' SAVE TIMIN G CONSTANT F OR TIMOUT SU BROUTINE'	T	RMK_TIMSAV				
' DIAGNOSTIC TEST NUMBER REQUESTED'	T	RMK_TSTNUM				
' ADDRESS OF NEXT BLOCK						

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
OF MEMORY TO BE UPDATED AFTER MEMORY PATTERN TEST						
T		RMK_UPADDR				
' RESULTS OF WIDE DATA(S D16-23) ISOLATE'						
T		RMK_WDISOL				
' ADDRESS OF OTHER STORE SUBCHANNEL						
0		RMK_OSSCO				
' ADDRESS OF OTHER STORE SUBCHANNEL						
1		RMK_OSSC1				
' ADDRESS OF OTHER STORE SUBCHANNEL						
2		RMK_OSSC2				
' ADDRESS OF OTHER STORE SUBCHANNEL						
3		RMK_OSSC3				
' WIDE STORE INDICATOR BIT						
T		RMK_OWDSTRO				
' 0-10 BIT TIMING SHIFTER FAKE'						
T		RMK_O10TM				
' RESULT OF EXTENDED(3 BIT) PARITY ISOLATE'						
T		RMK_2EPCK				
0010177	A	RSELBTS	15-22	15-23		
0167600	A	RSELBTSN	15-23			
'SER+0'	T	RSELER	W=1	S=6	N=0	CL=2
'RSLCHK+0'	T	RSELO6	W=7	S=0	N=0	CL=2 15-22
'RSLCHK+0'	T	RSEL7	W=1	S=14	N=0	CL=2 15-22
'CHKWRD+0'	T	RSVDO	W=1	S=7	N=0	CL=2
'RSLCHK+0'	T	RSVD1	W=1	S=7	N=0	CL=2
0047214	A	RTNADHI	22-04			
'LOAD SA17 & SAPH INTO SER'						
T		RTNADHIT				
T		RTNAME				
0	R	RD	LIBNUM=3	8-12, 26-24, 27-32, 27-49, 28-26, 28-41, 29-32, 29-40, 29-45, 31-26, 31-31, 32-42, 33-04, 33-09, 35-03, 36-18, 38-37, 39-03, 40-11, 41-15, 42-08, 43-09, 43-27		

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

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VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
0000123	A	ROXF		LIBNUM=13 43-34		
	1, R	R1		LIBNUM=3 8-13		
0000125	A	R1XT		LIBNUM=13 8-14		
	13 R	R11		LIBNUM=3 27-44, 27-47, 34-47, 36-13, 38-47, 40-06, 41-10, 43-14		
	14 R	R12		LIBNUM=3 8-23		
	15 R	R13		LIBNUM=3 8-24		
	16 R	R14		LIBNUM=3 31-14, 34-36, 36-02, 39-44, 40-48		
	17 R	R15		LIBNUM=3 31-15, 34-37, 36-03, 39-45, 40-49		
	2 R	R2		LIBNUM=3 8-15, 28-21, 28-24		
	3 R	R3		LIBNUM=3 8-16		
	4 R	R4		LIBNUM=3 8-17		
	5 R	R5		LIBNUM=3 8-18		
	6 R	R6		LIBNUM=3 8-19		
	7 R	R7		LIBNUM=3 8-20		
	10 R	R8		LIBNUM=3 8-21, 8-22		
	11 R	R9		LIBNUM=3 26-16, 26-18		
0000004	A	SAFAL	46-01	30-43, 32-22		
0000025	A	SAFALP	54-24	30-12, 33-28, 54-24		
0000004	A	SAFAL00	46-01			
0000005	A	SAFAL01	46-22			
0000006	A	SAFAL02	47-01			
0000007	A	SAFAL03	47-22			
0000010	A	SAFAL04	48-01			
0000011	A	SAFAL05	48-22			
0000012	A	SAFAL06	49-01			
0000013	A	SAFAL07	49-22			
0000014	A	SAFAL08	50-01			
0000015	A	SAFAL09	50-22			
0000016	A	SAFAL10	51-01			
0000017	A	SAFAL11	51-22			
0000020	A	SAFAL12	52-01			
0000021	A	SAFAL13	52-22			
0000022	A	SAFAL14	53-01			
0000023	A	SAFAL15	53-22			
0000024	A	SAFAL16	54-01	30-26, 32-05, 54-01		
'RSLCHK+0'	T	SAPHLP		W=1 S=10 N=0 CL=2 35-22, 36-42		
'RSLCHK+0'	T	SA17LP		W=1 S=11 N=0 CL=2 35-10, 36-30		
'SER+0'	T	SCMER		W=1 S=3 N=0 CL=2		
'CHKWRD+0'	T	SDPCK		W=1 S=14 N=0 CL=2		
0000761	A	SERNO_047778	58-02			
0000765	A	SERNO_050420	58-14			
0047114	A	SERREAD	22-09	27-42, 34-46, 36-12, 38-46, 40-05, 41-09		
'READ BACK S TORE ERROR R EGISTER(SER)'	T	SERREADY				
'SER+0'	T	SHER		W=1 S=4 N=0 CL=2		
CDGMM	V	SLDMCHBF	4-42			
CDGMM	V	SLDMIRLF	4-43			
CDGMM	V	SMCHF	4-44			

INTERPROCESSOR STORE BUS TEST

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
	3	R SNGBTER	16-07	W=1 S=5 N=0 CL=1		
'DGREQL0+0'	T	SPARE		W=2 S=7 N=0 CL=2		
0044714	A	SPAREA	22-07			
'SPARE I/O 0						
RDER'	T	SPAREAT				
0106274	A	SPRRD	18-32			
0106214	A	SPRWR	18-34			
0000216	A	SS_RXT		LIBNUM=13 43-40		
0000213	A	SS_SXT		LIBNUM=13 42-17		
0000002	A	STEPCLK	22-45			
0000064	A	STON1		LIBNUM=14 23-05		
0000010	A	STOPREF	22-47			
'CIOBUF+0'	T	STORDER		W=10 S=4 N=0 CL=2		
TDATA	V	STRLIM	3-17	7-41		
CDGSIO	V	STRSIZE	7-22			
'RSLCHK+0'	T	STRSLP		W=1 S=12 N=0 CL=2 39-15, 40-23, 41-27		
	3	R STRSTAT	8-16	16-03, 16-04, 16-06, 16-07, 16-08		
0041634	A	STSBY	22-11			
0041630	A	STSBYCL	22-13			
'SET STORE B						
USY(SBY) W/						
CLOCK'	T	STSBYCLT				
'SET STORE B						
USY(SBY) SIG						
NAL'	T	STSBYT				
CDGSIO	V	STSELSK	7-23			
0000000	A	SUCCESS	30-02	30-05, 30-16, 30-19, 30-33, 30-36, 31-42, 31-45, 32-12, 32-15, 33-18, 33-21, 35-07, 35-10, 35-19, 35-22, 36-27, 36-30, 36-39, 36-42, 39-12, 39-15, 40-20, 40-23, 41-24, 41-27		
0000000	A	SV_REG				
'SER+0'	T	TBER		W=1 S=13 N=0 CL=2		
0000065	A	TESTNO	23-05	44-01, 56-20		
0116774	L	TFAPCH2	2-01			
0000003	A	THREE	18-05			
'PAGSCR+27'	T	TIMSAV		W=20 S=0 N=33 CL=2		
0000064	A	TLMFRST	6-01	23-05, 44-01		
0600000	L	TPATCH	2-03			
0000765	A	TR_012581	58-14			
0000761	A	TR_012742	58-02			
0000705	A	TR_12581	43-11			
0000713	A	TR_12742	43-24			
06 0027652	L	TRORG	43-11	43-24		
06 0027366	L	TSTADPL	33-17	33-09		
06 0027251	L	TSTADO	30-01	29-45		
06 0027322	L	TSTAD1	31-39	31-31		
'DGREQL0+0'	T	TSTNUM		W=7 S=0 N=0 CL=2		
06 0027426	L	TST17PHD	35-06	35-03		
06 0027471	L	TST17PH1	36-26	36-18		
06 0027535	L	TS181900	39-11	39-03		
06 0027632	L	TS181901	41-23	41-15		

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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## PATCH HISTORY

23:41:18 2/05/81 \*\*\*\*

VALUE	T	NAME	DEF/REF	ATTRIBUTES AND REFERENCES	CDGSON	W77D
06 0027574	L	TS181910	40-19	40-11		
0000002	A	TWO	18-06			
'A'	T	TXTSEG				
'PAGSCR+28'	T	UPADDR		W=4 S=0 N=34 CL=2		
CSYSUB	V	UPD_OTS	7-33			
0007114	A	USERRED	22-15			
'READ STORE						
ERROR REG (W						
/O ISOLATE)'	T	USERREDT				
CBLM	V	WAIT	3-19	7-07		
'CHKWRD+0'	T	WDISOL		W=4 S=10 N=0 CL=2		
TDATA	V	WDSTR	3-18	7-42		
0010000	A	WPBLKSZE	18-07			
0046061	A	WPCLR	22-17			
'STORE INITI						
ALIZE, INCL.						
WRITE PROTE						
CT'	T	WPCLRT				
TDATA	V	WPTBL	7-43			
0000322	A	YTXF		LIBNUM=13 42-17, 43-40		
0025750	A	ZERX		LIBNUM=13 43-22		
0000000	A	ZERO	18-08			
0000000	A	ZEROS	18-09			
'MASCIOSC+1'	T	OSSC0		W=20 S=0 N=1 CL=2		
'MASCIOSC+3'	T	OSSC1		W=20 S=0 N=3 CL=2		
'MASCIOSC+5'	T	OSSC2		W=20 S=0 N=5 CL=2		
'MASCIOSC+7'	T	OSSC3		W=20 S=0 N=7 CL=2		
0000000	A	OTEST	18-10			
3	R	OWDSTRO	16-06	W=1 S=4 N=0 CL=1		
0052354	A	O1ONOR	22-19			
'O-10 TIMING						
(O10TIM) THEN						
REFRESH REQ						
UEST CLEAR'	T	O1ONORT				
0054334	A	O1OREF	22-22			
'O-10 TIMING						
(O10TIM) THEN						
REFRESH REQ						
UEST SET'	T	O1OREFT				
0056074	A	O10TIM	22-25			
'FORCE O-10						
TIMING SIGNA						
L ACTIVE'	T	O10TIMT				
'CIOBUF+0'	T	O10TM		W=1 S=14 N=0 CL=2		
0	U	1FFFF				
0000001	A	1TEST	18-11			
'CHKWRD+0'	T	2EPCK		W=1 S=15 N=0 CL=2		
1	J	3ACC	1-09			

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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## PATCH HISTORY

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COUNT FLAG

PAGE-LINE OF FLAG

CDGSON

W77D

10 E

27-34, 27-37, 29-38, 31-24, 33-02, 34-39, 36-05, 38-39, 39-47, 41-02

10 FLAG(S) FOUND IN THIS ASSEMBLY

INTERPROCESSOR STORE BUS TEST

PR-1C928-50

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