

RD 30

CONTENTS	SHEET NO.	SHEET ISSUE NO.
SHEET INDEX		
LEAD INDEX	A1	15
OPTION INDEX		
APPARATUS INDEX	A2	14
MINEMONIC INDEX	A3	14
FS 1 POWER CIRCUIT	B1	11
FS 2 DCU CONTROLLER CIRCUIT	B2A B2B	6 6
FS 3 PICB INTERFACE CIRCUIT	B3A* B3B* B3C B3D	 13 12
FS 4 EQUIPMENT ACCESS NETWORK CIRCUITS	B4	13
FS 5 PMU CONTROLLER, INTERFACE, AND MEMORY CIRCUIT	B5A B5B B5C B5D	13 13 13 13
FS 6 PROGRAMMABLE SIGNAL GENERATOR CIRCUIT	B6	13
FS 7 LINE REFERENCE MODULE CIRCUIT	B7	13
FS 8 MEASUREMENT CONTROLLER 1 AND 2 CIRCUIT	B8A B8B	13 13
FS 9 DATA CONVERTER CIRCUIT	B9	13
FS 10 SIGNAL CONDITIONER CIRCUIT	B10	13
FS 11 FILTER CIRCUIT	B11	13
FS 12 CURRENT SENSOR CIRCUIT	B12	13
FS 13 TIP AND RING TERMINATION CIRCUIT	B13A B13B B13C	13 13 13
FS 14 SOURCE AMPLIFIER CIRCUIT	B14	13
FS 15 CORE ACCESS NETWORK CIRCUIT	B15	13
FS 16 PORT UNIT CIRCUIT	B16A B16B	14 14
FS 17 CPS982LM DCU BACKPLANE RESISTOR CIRCUIT MODULE	B17	14
APP FIG. 1,2,3,4,5,6,7,8,9	C1	15

* SHEET B3A, B3B CANCELLED ON ISSUE 6A

CONTENTS	SHEET NO.	SHEET ISSUE NO.
CIRCUIT NOTES	D1	15
EQUIPMENT NOTES		
EQUIPMENT NOTES (CONT)	D2	5
INFORMATION NOTES	D3	15
CAD 1	G1	11
CAD 2,3	G2	2
CAD 4,5	G3	1
CAD 6,7	G4	1
CAD 8,9,10,11	G5	14
CAD 12,13,14	G6	13
CAD 15,16,17	G7	13
CAD 18	G8	2
CAD 19	G9	13
CAD 20	G10	13
CAD 21	G11	13
CAD 22,23,24,25	G12	14
CAD 26,27	G13	14

DESIG	LOCATION	
	FS	CAD
5 ESS		
CN0	C/C1	5B1
CN1		5D1
CP0		5B1
CP1		5D1
DN4	C/C7	5B1
DN1		5D1
DP0		5B1
DP1		5D1
RNR00	}	5B4
RNP01		
RNR02		
RNR03		
RNR10	}	5D4
RNR11		
RNR12		
RNR13		
RNR20	}	5F4
RNR21		
RNR22		
RNR23		
RMT00	16A/C1, 16B/CO	5B4
RMT01		
RMT02		
RMT03		
RMT10	}	5D4
RMT11		
RMT12		
RMT13		
RMT20	}	5F4
RMT21		
RMT22		
RMT23		
NINTN0	}	5B1
NINTN1		5D1
NINTP0		5B1
NINTP1		5D1
DDN0	3C/C7	5B1
DDN1		5D1
DDP0		5B1
DDP1		5D1
SN0	}	5B1
SN1		5D1
SP0		5D1
SP1		5D1

APP OR ARG	RATED ON ISSUE	REF NOTES	LOCATION
Z			103, CAD 1,9,10,11, 13,14,16,18,20,21, 23,24,26,27
Y			NOT TO BE REASSIGNED
X			NOT TO BE REASSIGNED
H	5B MD	305	13B/F7, 13B/85, 13B/H7, APP FIG. 5,6
Q	5B STD	305	13C/A2, 13C/25, 13C/F7, APP FIG. 5,6
N	8B MD	306	SHEET 1, APP FIG. 1,8
M	8B STD	306	SHEET 1, APP FIG. 1,8
K	13AC (A & M)	312	APP FIG. 1,5,6
J	13AC STD	312	APP FIG. 4,5,6

DWG ISSUE	CD ISSUE	DATE ISSUED	BY	APPD
1	1	10-19-81	JST	RWF
2A	2A	8-18-82	FJB	SWH
3A	3A	7-22-83	JST	RWF
4B	3A	7-22-83	JST	RWF
5B	3A	7-22-83	JST	RWF
6A	3A	2-5-87	JST	RWF
7B	3A	2-5-87	JST	RWF
8B	3A	2-5-87	JST	RWF
9A	3A	2-5-87	JST	RWF
10AC	3A	2-5-87	JST	RWF
11B	3A	2-5-87	JST	RWF
12A	3A	2-5-87	JST	RWF
13AC	3A	2-5-87	JST	RWF
14A	3A	3-1-88	JST	RWF
15A	3A	3-1-88	JST	RWF

SUPPORTING INFORMATION		SHEET INDEX NOTES	
CATEGORY	NO		
EQUIPMENT DESIGN REVISIONS	17-123 (824-102-112)	1	WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
		2	THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
		3	THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE SHEET INDEX.
		4	SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
		5	THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING.

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ALHO

OPERATIONS SUPPORT SYSTEMS COMMON DIRECTLY CONNECTED TEST UNIT CIRCUIT

DWG SIZE: 8.5
ISSUE: 15A

AT&T BELL LABORATORIES SD -2P077-01 SHEET A1 OF 46

APPARATUS INDEX																	
EQUIP LOC	LOCATION		EQUIP LOC	LOCATION		DESIGN	LOCATION			DESIGN	LOCATION						
	FS	APP FIG.		FS	APP FIG.		FS	APP FIG.	EQUIP		FS	APP FIG.	EQUIP				
PACKS. CIRCUIT LIST 1			PACKS. CIRCUIT LIST 3			PACKS. CIRCUIT LIST 1			PACKS. CIRCUIT LIST 3			982LM CIRCUIT MODULE LIST 1,2,3					
004-010	5A/A7	6	004-010	5A/A7	6	CAN1	15A2	5	004-146	CAN()	15A7	6	004-146	982LM	17A4	3	004-178
004-018	5C/A5	6	004-018	5C/A5	6	DCONV1	9A7	5	004-078	DCONV()	9A7	6	004-078				
004-026	5D/A7	6	004-026	5D/A7	6	DCTUCTL	2A/A4	4	004-010	FLTR()	11B5	6	004-050				
004-034	8B/A5	6	004-034	8A/A5	6	FLTR1	2B/A1	5	004-050	ISENS()	12B6	6	004-042				
004-042	12B6	6	004-042	12B6	6	ISENS1	12B2	5	004-042	LRM()	7A7	6	004-094				
004-050	11B5	6	004-050	11B5	6	LRM1	7A7	5	004-084	LRM()	7A7	6	004-102				
004-058	10C7	6	004-058	10C7	6	LRM1	7A7	5	004-102	MCTL1-1	8A/A5	6	004-030				
004-070	9A7	6	004-070	9A7	6	MCTL1-1	8A/A2	5	004-038	MCTL2-1	8B/A5	6	004-034				
004-078	6A7	6	004-078	6A7	6	PICB INTER	3C/B5	4	004-018	PMUCTL1()	5A/A7	6	004-010				
004-086	7A7	6	004-086	7A7	6	PMUCTL1	3D/A5	5	004-018	PMUINT()	5C/A5	6	004-018				
004-094	7A7	6	004-094	7A7	6	PMUINT1	5C/A2	5	004-018	PMUMEM()	5C/A7	6	004-026				
004-102	7A7	6	004-102	7A7	6	PORT1	16A/A4	5	004-154	PORT()	16B/A2	6	004-162				
004-110	13A/A5	6	004-110	13A/A5	6	PORT1	16A/A4	5	004-162	PORT()	16B/A2	6	004-170				
004-118	13B/A5	6	004-118	13B/A5	6	PORT1	16A/A4	5	004-170	PSG()	6A7	6	004-086				
004-126	14A6	6	004-126	14A6	6	RTERM1	13B/A2	5	004-118	RTERM()	13B/A5	6	004-118				
004-134	14A6	6	004-134	14A6	6	SIG CON1	10A2	5	004-058	SIG CON()	10C7	6	004-058				
004-142	14A2	5	004-142	14A2	5	SIG CON1	10A2	5	004-070	SIG CON()	10C7	6	004-070				
004-146	15A2	5	004-146	15A2	5	SOAMP1	14A2	5	004-130	SOAMP()	14A6	6	004-130				
004-154	4A4	4	004-154	4A4	4	SWU1	4A4	4	004-138	SOAMP()	14A6	6	004-138				
004-154	16A/A4	5	004-154	16A/A4	5	TTERM1	3A/B2	5	004-110	SWU2	4A4	9	004-170				
004-162	16A/A4	5	004-162	16A/A4	5					TTERM()	13A/A5	6	004-110				
004-170	16A/A4	5	004-170	16A/A4	5												
004-178	16A/A4	5	004-178	16A/A4	5												

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

DWG SIZE: 8.5
ISSUE: 14A

AT&T BELL LABORATORIES SD -2P077-01
SHEET A2

DESIGNATION MNEMONIC INDEX

MNEMONIC	FS NO.	DESCRIPTION
1MHZ	8	DSP OUTPUT CLOCK SIGNAL
3MHZ_CLK	2	BUFFERED 3 MHZ CLOCK SIGNAL
4MHZ_CLK	3	PMU 4MHZ CLOCK
5_I_SENSE A	1	5 VOLT CURRENT SENSING FROM +5.1A POWER UNIT
5_I_SENSE B	1	5 VOLT CURRENT SENSING FROM +5.1B POWER UNIT
5_SAT	11	75MA SATURATION DETECTION CONTROL SIGNAL FOR SM258B
+/-9VREF	6	+/- DC REFERENCE VOLTAGE LEVEL FOR SM254
+/-15V	15	REFERENCE VOLTAGE FOR SM257
+/-SENSE	1	+5.1B REMOTE VOLTAGE SENSING FOR PMU2 AND PMU3
(A-B)_COS	7	SM254 COSINE CHANNEL SINUSOIDAL OUTPUTS
(A-B)_SIN	7	SM254 SINE CHANNEL SINUSOIDAL OUTPUTS
(A-B)_R	14	CROSS CONNECT BETWEEN TIP/RING SM263'S
(A-B)_T	14	CROSS CONNECT BETWEEN TIP/RING SM263'S
AC_CLR(1-2)	8	TIP/RING AC SATURATION DETECTOR RESET FOR SM258B
AC_PA(1-2)	8	TIP/RING AC PRE-AMP CONTROL FOR SM258B
AC_SAT_(1-2)	10	TIP/RING INTERRUPT FOR VOLTAGE OVERLOAD IN AC SECTION
ALMO(0-7)	3	POWER SUPPLY ALARM SIGNALS
AM_(1-3)	5	PMU MEMORY RAM TIEPOINTS
ARST	5	PMU INTERFACE ACQUISITION RESET
ATNB	2	BUFFERED GPIB ATTENTION SIGNAL
A/D_CLK	9	A/D CONVERTER CLOCK OUTPUT
A/D_DATA	9	A/D CONVERTER SERIAL DATA SYNCHRONOUS WITH A/D CLOCK
A/D_START	8	A/D CONVERTER START PULSE FOR SM257
CLK_PA	6	TIP AND RING DATA LATCH PULSE FOR SM254
CLK_PC	6	TIP AND RING CONTROL LATCH PULSE FOR SM254
CLR_RD	8	CLEAR TO READ FOR DSP
CN(0-1)	3	PICB CLOCK, NEGATIVE CHANNELS
CORE_PULSE	12	50 KHZ TRANSFORMER CORE SATURATION TEST POINT PULSE
COSO	6	COSINE CHANNEL SINUSOIDAL OUTPUT
CP(0-1)	3	PICB CLOCK, POSITIVE CHANNELS
CS_(0-1)	6	TIP/RING DC CHANNEL SELECT FOR SM254
CSTD	8	RING D/A CHIP SELECT FOR SM260
CS11	8	OCTAL LATCH CLOCK STROBE FOR SM259B
CS12	8	OCTAL LATCH CLOCK STROBE FOR SM264
CS1(3-4)	8	OCTAL LATCH CLOCK STROBE FOR SM257
CS15	8	D/A CONVERTER CHIP SELECT FOR SM257
CS1A	8	OCTAL LATCH CLOCK STROBE FOR SM264
CSOE	8	OCTAL LATCH CLOCK STROBE FOR SM260
CSOF	8	TIP D/A CHIP SELECT FOR SM260
DAC_REF	10	7.68V D/A REFERENCE VOLTAGE FOR SM260
DAVB	2	BUFFERED GPIB DATA VALID
DC_CLR(1-2)	8	TIP/RING DC SATURATION DETECTOR RESET FOR SM258B
DC_PA(1-2)	8	TIP/RING DC PRE-AMP CONTROL FOR SM258B
DC_SAT_(1-2)	10	TIP/RING INTERRUPT FOR VOLTAGE OVERLOAD IN DC SECTION
DC_(0-1)	7	POSITIVE/NEGATIVE DC LEVELS
DIO(1-8)	2	GPIB DATA BUS
DSP_RDY	8	INTERRUPT INDICATES DSP NOT READY FOR DATA
D_AB(00-15)	2	BUFFERED DCTU CONTROLLER ADDRESS BUS
D_CLK_OUT_B	2	BUFFERED BELLMAC-B CLOCKOUT LEAD
D_DB(00-07)	2	BUFFERED BIDIRECTIONAL TRI-STATE DATA BUS SIGNALS
D_TACKB	2	BUFFERED BELLMAC-B INTERRUPT ACKNOWLEDGE
D_IMRST	2	INPUT MASTER RESET SIGNAL
D_TOEB	2	BUFFERED I/O DECODE ENABLE
D_IREQ(00-07)	2	INTERRUPT REQUESTS
D_MMIR	2	NON-MASKABLE INTERRUPT REQUEST
D_OMRST	2	OUTPUT MASTER RESET SIGNAL
D_RDB	2	BUFFERED DCTU CONTROLLER BELLMAC-B READ SIGNAL
D_RDPB	2	BUFFERED PERIPHERAL READ
D_RDY	2	BELLMAC-B DATA READY
D_SAN	2	CPU SANITY SIGNAL FOR TM629B
D_SWAIT	2	SINGLE WAIT STATE SELECT LEAD
D_TP1	2	DCTU CONTROLLER TEREADYNE CIRCUIT PACK TEST POINT
D_WAIT	3	MULTIPLE WAIT STATE SELECT LEAD
D_WRB	2	BUFFERED DCTU CONTROLLER BELLMAC-B WRITE SIGNAL
D_WRPB	2	BUFFERED PERIPHERAL WRITE
D_U_CLKB	2	BUFFERED 8253 TIMER-1 OUTPUT
EAN(0-3)D	3	BUFFERED SWITCHING-UNIT WRITE ENABLE PULSE
EOIB	2	BUFFERED GPIB END OR IDENTITY

DESIGNATION MNEMONIC INDEX (CONT):

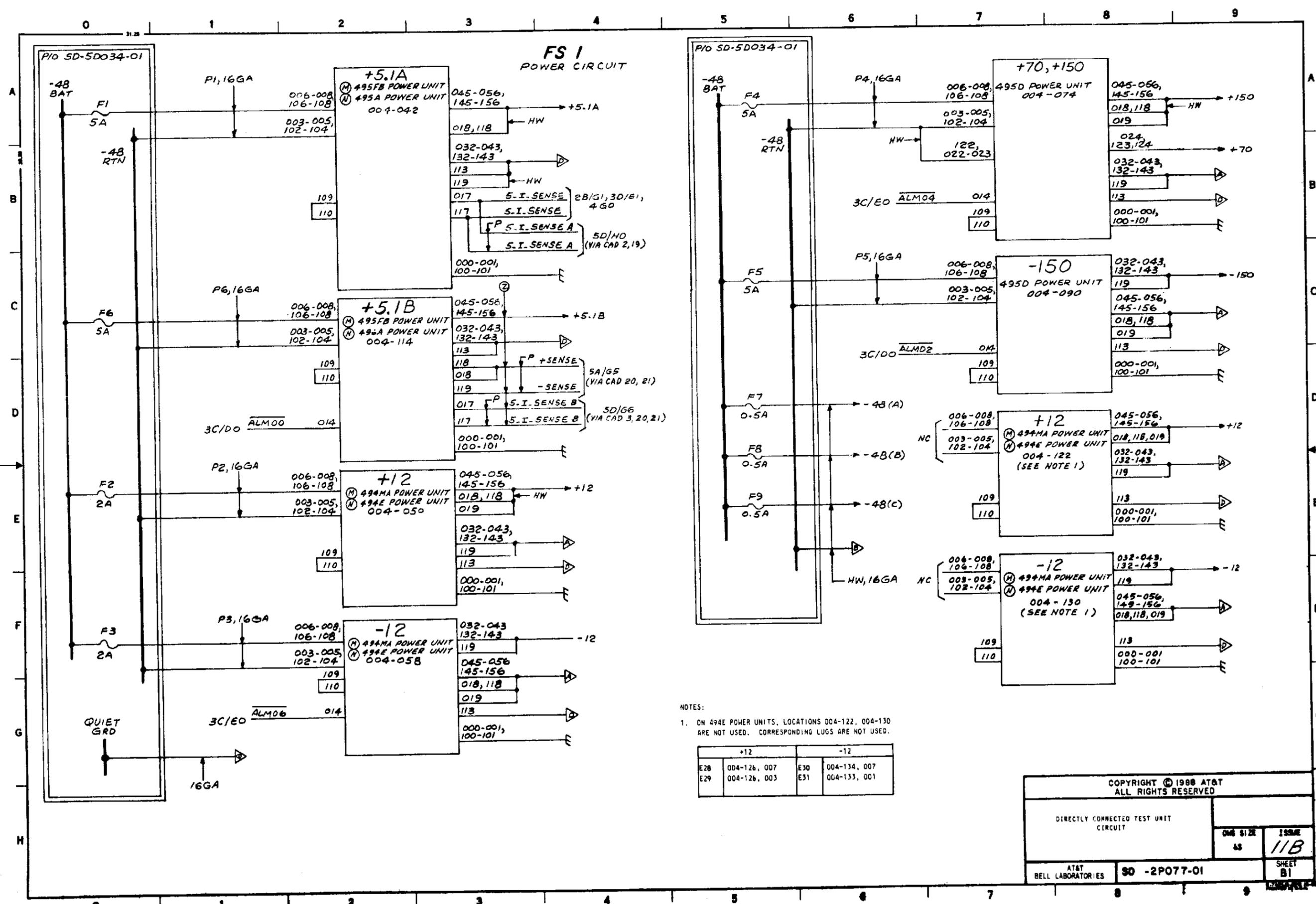
MNEMONIC	FS NO.	DESCRIPTION
FS(1-2)_(A-B)	5	PMU MEMORY BANK FEEDBACK
GPIB_DREQ	2	GPIB DMA REQUEST
GPIB_DACKB	2	GPIB DMA ACKNOWLEDGE
GPIB(0-2)	5	GPIB ADDRESS STRAPS FOR PMU# IDENTIFICATION
HAZ_SLV()	16	PORT HAZARDOUS SLEEVE
HP(0-3)(0-3)	16	PORT HAZARDOUS POTENTIAL SIGNAL
IBF	5	PMU INTERFACE DSP INPUT BUFFER FULL SIGNAL
IDN(0-1)	3	PICB INPUT DATA, NEGATIVE CHANNELS
IOP(0-1)	3	PICB INPUT DATA, POSITIVE CHANNELS
IFCB	2	BUFFERED GPIB INTERFACE CLEAR
NRFOB	2	BUFFERED GPIB NOT READY FOR DATA SIGNAL
NDACB	2	BUFFERED GPIB NOT DATA ACCEPT
K100-11)	6	TIP AND RING RELAY SELECTS FOR SM254
K9_TR	13	CROSS CONNECT BETWEEN SM261 AND SM262B
K10_TR	13	CROSS CONNECT BETWEEN SM261 AND SM262B
K10_R	13	CROSS CONNECT BETWEEN SM261 AND SM262B
K11_R	13	CROSS CONNECT BETWEEN SM261 AND SM262B
K12_T	13	CROSS CONNECT BETWEEN SM261 AND SM262B
LDAC	6	TIP AND RING SM254'S LOAD D/A CONVERTER PULSE
LTTO	2	LONG TERM TONE SIGNAL MODULATED AT 1 HZ
LTT1	2	LONG TERM TONE SIGNAL MODULATED AT 5 HZ
MS(0-7)	8	TIMING SYNCHRONIZATION SIGNALS
M(1-2)_(S1-2)	9	TIP/RING MULTIPLEXER SELECTS FOR SM258B
MINTP(0-1)	3	PICB INTERRUPT, POSITIVE CHANNELS
MINTN(0-1)	3	PICB INTERRUPT, NEGATIVE CHANNELS
MM(1-2)	6	TIP/RING SM254'S NON-MASKABLE INTERRUPT PULSE CONTROL FOR 2-1 ANALOG MUX ON SM257
M1/M2	8	CONTROL FOR 2-1 ANALOG MUX ON SM257
ODP(0-1)	3	PICB OUTPUT DATA, POSITIVE CHANNELS
ODN(0-1)	3	PICB OUTPUT DATA, NEGATIVE CHANNELS
OE/VPP	5	EPROM/ROM OUTPUT ENABLE AND PROGRAMMING LEAD
OM_(1-3)	5	PMU MEMORY ROM TIEPOINTS
OVRD	8	PROGRAMMABLE GAIN AMPLIFIER GAIN OVERRIDE FOR SM257
ORST	5	PMU INTERFACE CP OUTPUT RESET
PC2_(0-1)	7	TIP/RING LINE REFERENCE MODULE STATUS FLAG
PC3_(0-1)	7	TIP/RING LINE REFERENCE MODULE DATA ACCEPT FLAG
PGA(1,2,4,8)	8	PROGRAMMABLE GAIN AMPLIFIER GAIN LEVEL SELECTS
PGR	3	2712B EPROM PROGRAMMING ENABLE
PROMUS/NORM	5	PMU PROMUS MODE SELECT INPUT
PR_GRD	5	PMU MEMORY EPROM PROGRAMMING GROUND
PSUEDO_SAT	8	INTERRUPT CONDITION INDICATES PSUEDO-GAIN OVERLOAD
PSUEDO	8	INDICATES PSUEDO GAIN APPLIED TO MEASUREMENT
PTE(0-3)(0-3)	16	PORT ENABLES
RENB	2	BUFFERED GPIB REMOTE ENABLE
RMT(0-2)(0-3)	16	TIP SIDE OF TRUNK CONNECTION
RMR(0-2)(0-3)	16	RING SIDE OF TRUNK CONNECTION
RN_SAN	9	PMU CPU SANITY FOR SM256
RING1	14	RING SIDE AMPLIFIER FOR SM262B
RL	15	CURRENT TO LOOP THROUGH RING TRANSFORMER ON SM260
RN_SAN	9	PMU CPU SANITY FOR SM256
RO/AM_(A-C)	5	PMU MEMORY DEVICE TYPE JUMPER
RO/AM_D(1-2)	5	PMU MEMORY DEVICE TYPE JUMPER
R_AB(00-15)	5	PMU BUFFERED TRI-STATE ADDRESS BUS
R_AUX_CLK	5	PMU 8253 TIMERO SIGNAL
R_CLK_OUT_B	5	PMU CONTROLLER OUTPUT CLOCK
R_DBO(0-7)	5	PMU BUFFERED BELLMAC-B DATA BUS
R_DMA_ACKB	5	PMU DMA ACKNOWLEDGE
R_DMA_REQ	5	PMU CONTROLLER BELLMAC-B DMA REQUEST
R_TACKB	5	PMU BELLMAC-B INTERRUPT ACKNOWLEDGE
R_IGEB	5	PMU INTERFACE BUFFERED I/O ENABLE FOR ANALOG CPS
R_IREQ(1-6)	5	PMU INTERRUPT REQUESTS
R_MB3_A	5	PMU MEMORY BANK SELECT
R_MB4_A	5	PMU MEMORY BANK SWITCHING
R_MB11-21_(A-B)	5	PMU MEMORY BANK FEEDBACK
R_MMIR	5	PMU CONTROLLER BELLMAC-B NON-MASKABLE INTERRUPT
R_OMRST	5	PMU CONTROLLER OUTPUT MASTER RESET
R_RDB	5	PMU BELLMAC-B BUFFERED READ SIGNAL
R_RDPB	5	PMU BUFFERED PERIPHERAL READ
R_RDY	5	PMU CONTROLLER BELLMAC-B DATA READY SIGNAL
R_SA	13	CURRENT APPLIED TO RING TRANSFORMER ON SM260

DESIGNATION MNEMONIC INDEX (CONT):

MNEMONIC	FS NO.	DESCRIPTION
R_SWAIT	5	PMU CONTROLLER SINGLE WAIT STATE LEAD
R_U_CLKB	5	PMU BUFFERED 8253 TIMER1 SIGNAL
R_WAIT	5	PMU CONTROLLER MULTIPLE WAIT STATE LEAD
R_WRB	5	PMU BELLMAC-B BUFFERED WRITE
R_WRPB	5	PMU BUFFERED PERIPHERAL WRITE
SAN	13	PMU SANITY BUS ONLY
SAN1_R	14	SANITY CROSS CONNECT TO SM261
SAN1_T	14	SANITY CROSS CONNECT BETWEEN TIP/RING SM263'S
SAN2_R	14	SANITY CROSS CONNECT BETWEEN TIP/RING SM263'S
SAN(T)	9	PMU SANITY BUS OR D/A CONVERTER OUTPUT VOLTAGE
SAN_SC(1-2)	9	TIP/RING SANITY BUS SELECTS
SER_DATA	8	SERIAL INPUT DATA TO DSP
SHFT_CLK	8	INPUT DATA SHIFT CLOCK FOR DSP
(SIN,COS)_M	10	MEDIUM BAND SIGNALS BETWEEN TIP/RING SM258BS
(SIN,COS)_N	10	NARROW BAND SIGNALS BETWEEN TIP/RING SM258BS
SLV_DIAG()	16	SLEEVE DIAGNOSTIC CONNECTION
SN(0-1)	3	PICB SELECT, NEGATIVE CHANNELS
SRC_SCAN	6	SANITY BUS
SREQ	2	BUFFERED GPIB SERVICE REQUEST
SP(0-1)	3	PICB SELECT, POSITIVE CHANNELS
SYNC	8	INPUT SYNC LEAD TO DSP ON SM251
S/H	8	SAMPLE/HOLD CONTROL FOR AMPLIFIERS ON SM257
S(0-5)_(T(0-5)	15	TIP SIDE OF EAN CONNECTION TO PMU
S(0-5)_(R(0-5)	15	RING SIDE OF EAN CONNECTION TO PMU
TMR	6	TIP AND RING SM254 TIMER INTERRUPT PULSE
TIP1	14	TIP SIDE AMPLIFIER FOR SM261
TL	15	CURRENT TO LOOP THROUGH TIP TRANSFORMER ON SM260
TRST	5	PMU INTERFACE CP TEST RESET
TR_AUX	15	CURRENT TO LOOP FOR RESISTIVE FAULT SECTIONALIZATION
T_SA	13	CURRENT APPLIED TO TIP TRANSFORMER ON SM260
VPP	5	EPROM PROGRAMMING VOLTAGE LEAD
V_COS_R	10	RING CHANNEL SIGNAL FOR SM257
V_F_TIP	11	FILTERED TIP VOLTAGE FOR SM258B
V_F_RING	11	FILTERED RING VOLTAGE FOR SM259B
V_RING	12	VOLTAGE PROPORTIONAL TO RING CURRENT FOR SM259B
V_SIN_T	10	TIP CHANNEL SIGNAL FOR SM257
V_TIP	12	VOLTAGE PROPORTIONAL TO TIP CURRENT FOR SM259B
XTL1	6	TIP AND RING SM254'S 4.194 MHZ MICROPROCESSOR CLOCK
Y(0-3)_(T(0-11)	16	TIP SIDE OF EAN CONNECTION TO PORT
Y(0-3)_(R(0-11)	16	RING SIDE OF EAN CONNECTION TO PORT

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DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWB SIZE	ISSUE
	88	14A
AT&T BELL LABORATORIES SD -2P077-01		SHEET A3



**FS I
POWER CIRCUIT**

NOTES:
1. ON 494E POWER UNITS, LOCATIONS 004-122, 004-130 ARE NOT USED. CORRESPONDING LUGS ARE NOT USED.

+12		-12	
E28	004-126, 007	E30	004-134, 007
E29	004-126, 003	E31	004-133, 001

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

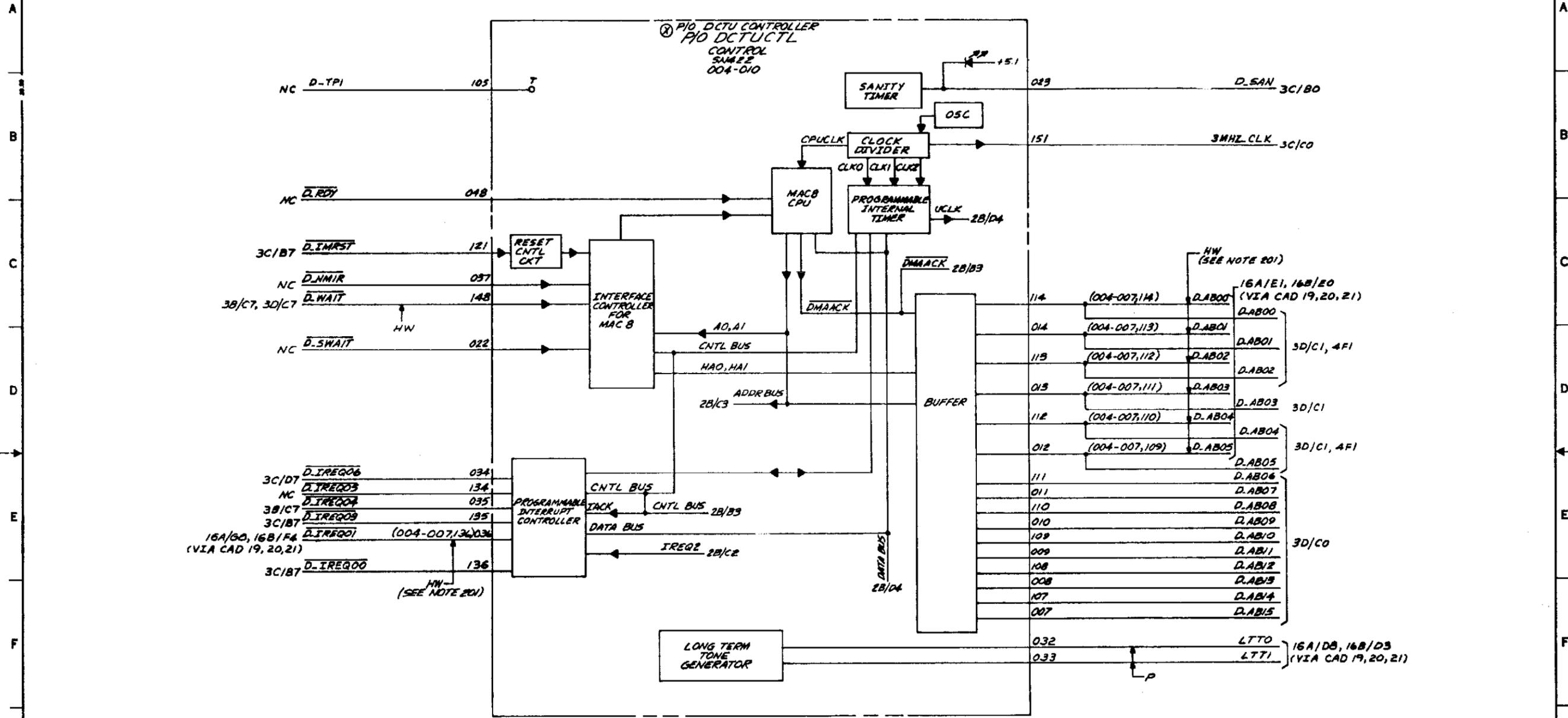
AT&T
BELL LABORATORIES

SD -2P077-01

DATE SIZE ISSUE
AS 11B

SHEET
B1

PART OF FS 2
DCTU CONTROLLER CIRCUIT



POWER DATA

CP	EUPY LOC	A. GRD	D. GRD	+5.1A TERM.	+12 TERM.	-12 TERM.
SN422	004-010	003, 004, 005, 051, 052, 053	000, 001, 002, 054, 055, 056	100, 101, 102, 154, 155, 156	123, 124	132, 133

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

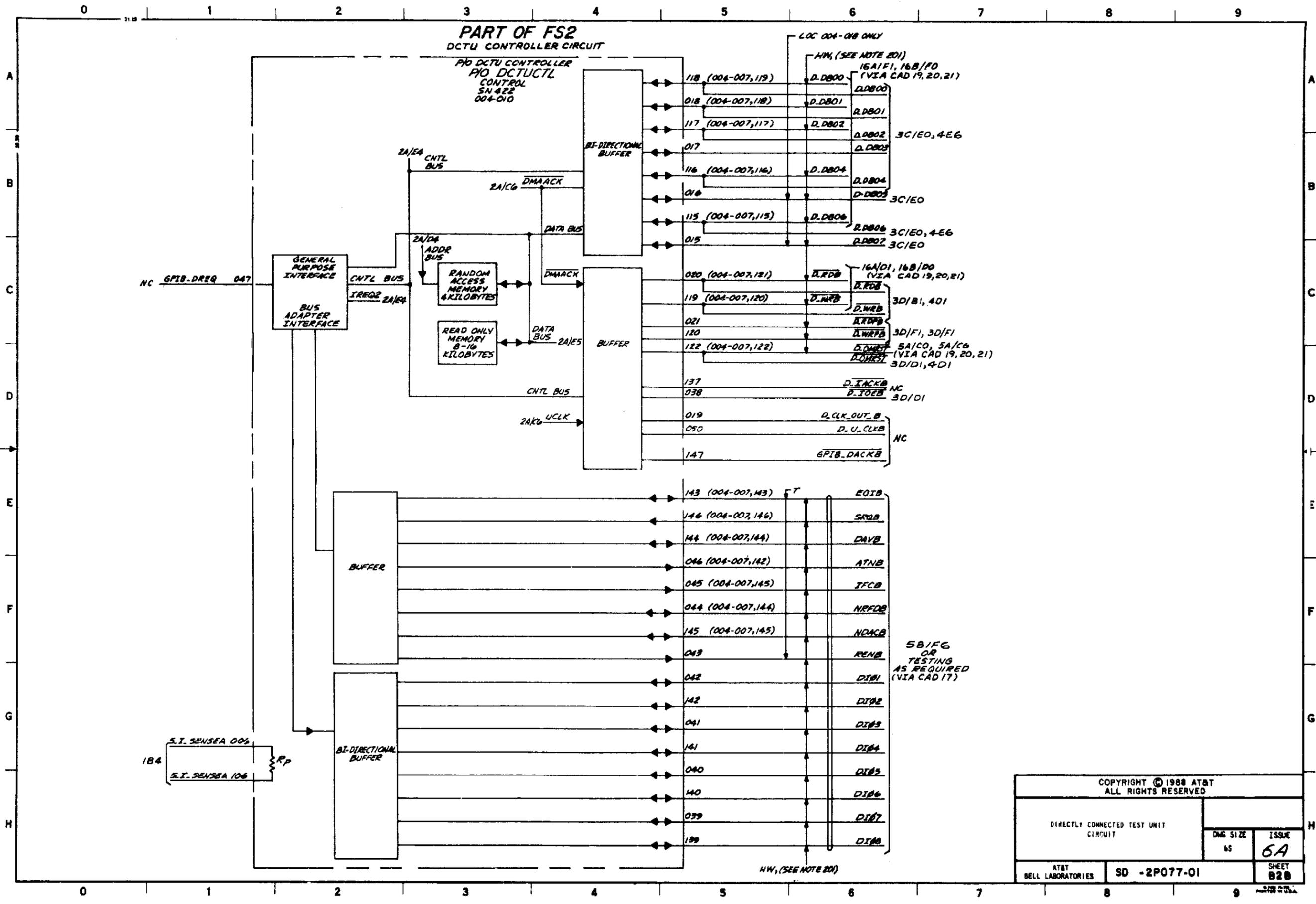
AT&T BELL LABORATORIES

SD -2P077-01

DWG SIZE: 65

ISSUE: 6A

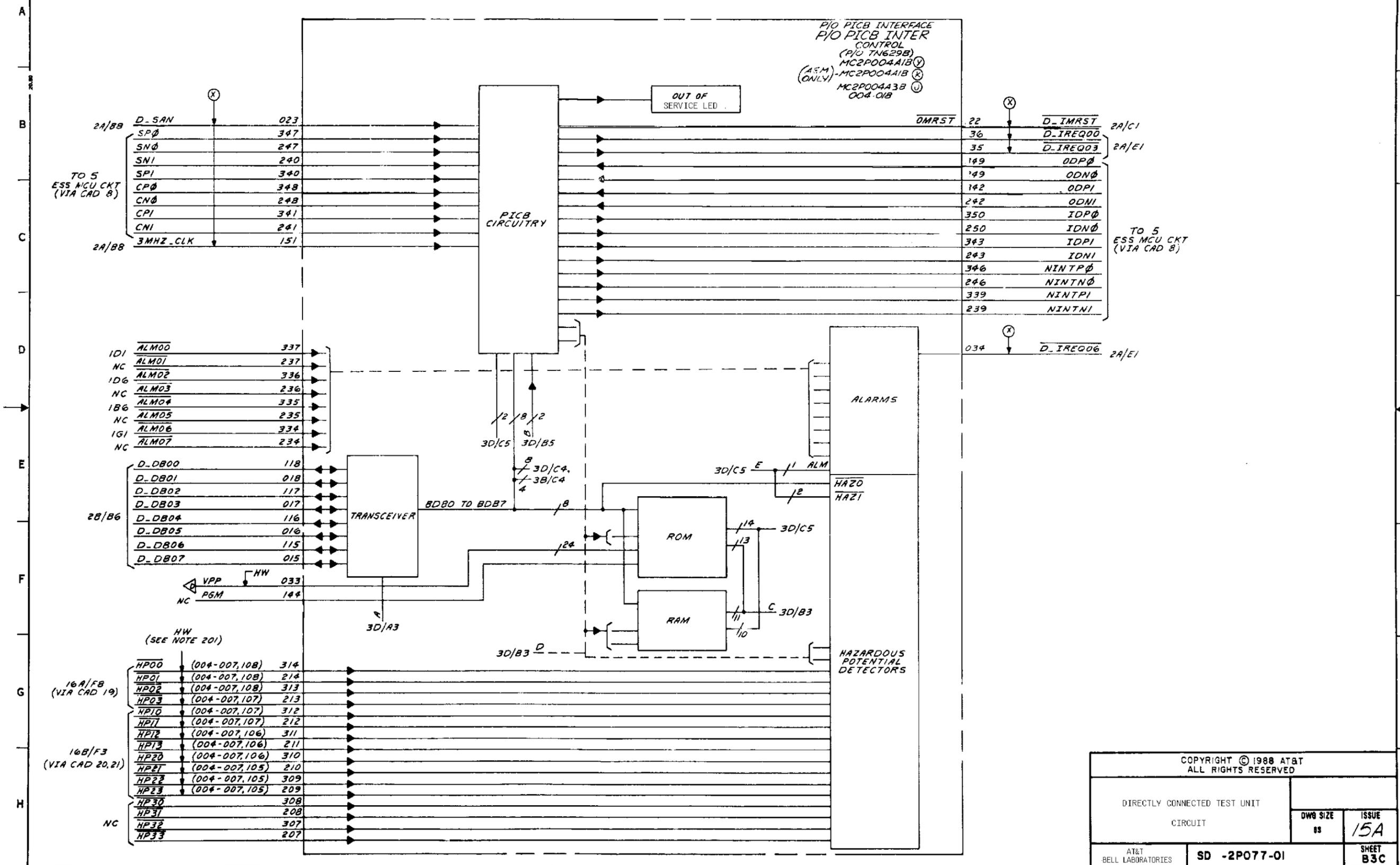
SHEET: B2A



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DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 65	ISSUE 6A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 828	

PART OF FS3
PICB INTERFACE CIRCUIT



TO 5
ESS MCU CKT
(VIA CAD 8)

2A/B8	D-SAN	023
	SP0	347
	SN0	247
	SN1	240
	SPI	340
	CP0	348
	CN0	248
	CPI	341
	CNI	241
2A/B8	3MHZ-CLK	151

22	D-IMRST	2A/C1
36	D-IREQ00	2A/E1
35	D-IREQ03	2A/E1
149	ODP0	
149	ODN0	
142	ODPI	
242	ODNI	
350	IDP0	
250	IDN0	
343	IDPI	
243	IDNI	
346	NINTP0	
246	NINTN0	
339	NINTPI	
239	NINTNI	

TO 5
ESS MCU CKT
(VIA CAD 8)

ID1	ALM00	337
NC	ALM01	237
ID6	ALM02	336
NC	ALM03	236
IB6	ALM04	335
NC	ALM05	235
IG1	ALM06	334
NC	ALM07	234

2B/B6

D-DB00	118
D-DB01	018
D-DB02	117
D-DB03	017
D-DB04	116
D-DB05	016
D-DB06	115
D-DB07	015

VPP	HW	033
NC	PGM	144

HW
(SEE NOTE 201)

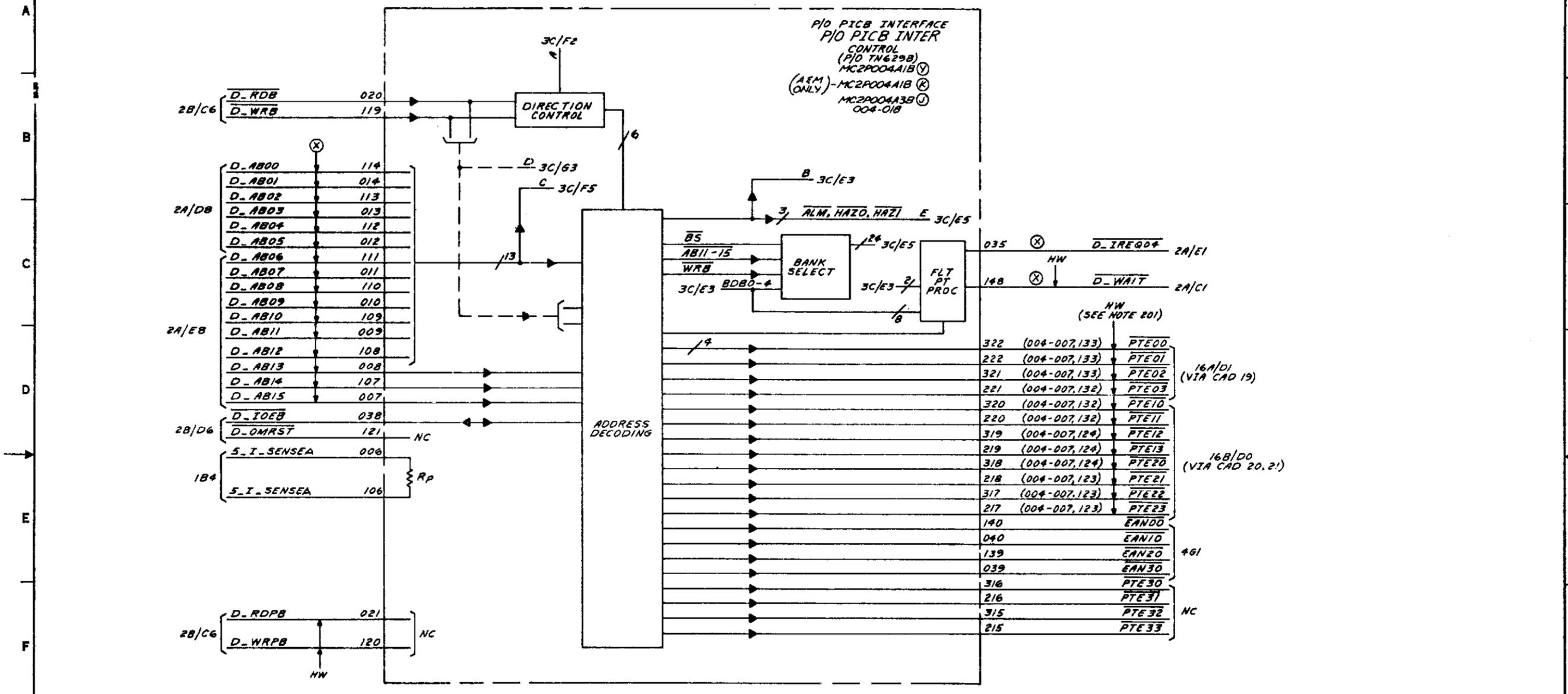
16A/FB
(VIA CAD 19)

16B/F3
(VIA CAD 20,21)

HP00	(004-007,108)	314
HP01	(004-007,108)	214
HP02	(004-007,108)	313
HP03	(004-007,107)	213
HP10	(004-007,107)	312
HP11	(004-007,107)	212
HP12	(004-007,106)	311
HP13	(004-007,106)	211
HP20	(004-007,106)	310
HP21	(004-007,105)	210
HP22	(004-007,105)	309
HP23	(004-007,105)	209
HP30		308
HP31		208
HP32		307
HP33		207
NC		

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DIRECTLY CONNECTED TEST UNIT		DWG SIZE
CIRCUIT		15
AT&T BELL LABORATORIES		ISSUE 15A
SD -2P077-01		SHEET B3C

PART OF FS3
PICB INTERFACE CIRCUIT



P10 PICB INTERFACE
P10 PICB INTER
CONTROL
(P10 TN629B)
MC2P004A1B (V)
(AEM ONLY) - MC2P004A1B (R)
MC2P004A3B (U)
004-01B

POWER DATA

CP	EQPT LOC	A. GRD	B. GRD	VOLTAGE		
				+5.1A TERM.	+12 TERM.	-12 TERM.
MC2P004A3B (TN629B)		003	000	100	123	132
		004	001	101	124	133
		005	002	102		
		051	054	154		
		052	055	155		
(V) MC2P004A1B (TN629)		053	056	156		

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

AT&T BELL LABORATORIES

SD -2P077-01

ISSUE
15A

SHEET
830

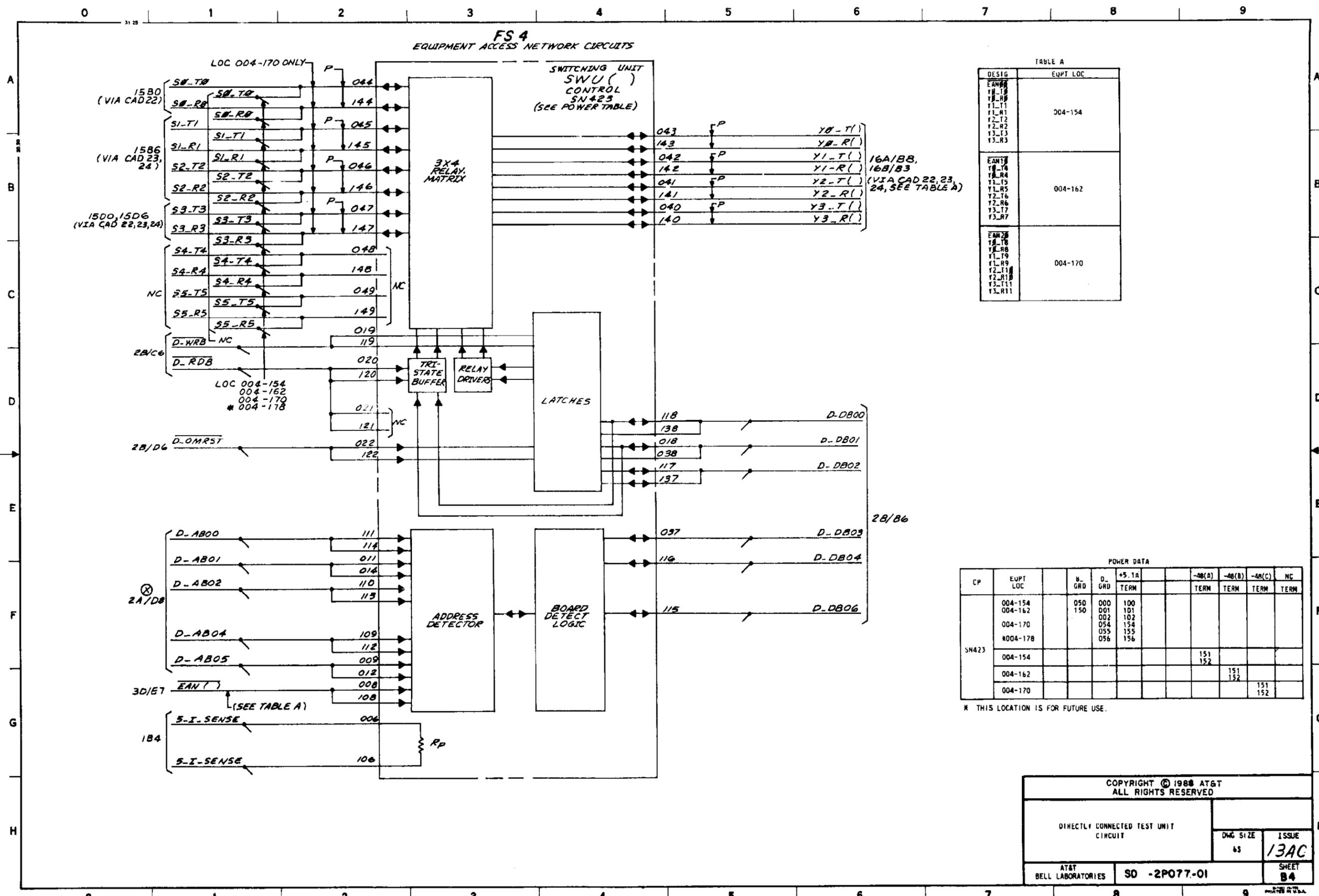


TABLE A

DESIG	EQPT LOC
EAN18 Y0-T0 Y0-R0 Y1-T1 Y1-R1 Y2-T2 Y2-R2 Y3-T3 Y3-R3	004-154
EAN19 Y0-T4 Y0-R4 Y1-T5 Y1-R5 Y2-T6 Y2-R6 Y3-T7 Y3-R7	004-162
EAN20 Y0-T8 Y0-R8 Y1-T9 Y1-R9 Y2-T10 Y2-R10 Y3-T11 Y3-R11	004-170

POWER DATA

CP	EQPT LOC	V. GRD	D. GRD	+5.1A TERM	-4B(A) TERM	-4B(B) TERM	-4B(C) TERM	NC TERM
SN423	004-154	050	000	100				
	004-162	150	001	101				
	004-170		002	102				
	*004-178		054	154				
			055	155				
	004-154				151			
	004-162				152	151		
	004-170						151	152

* THIS LOCATION IS FOR FUTURE USE.

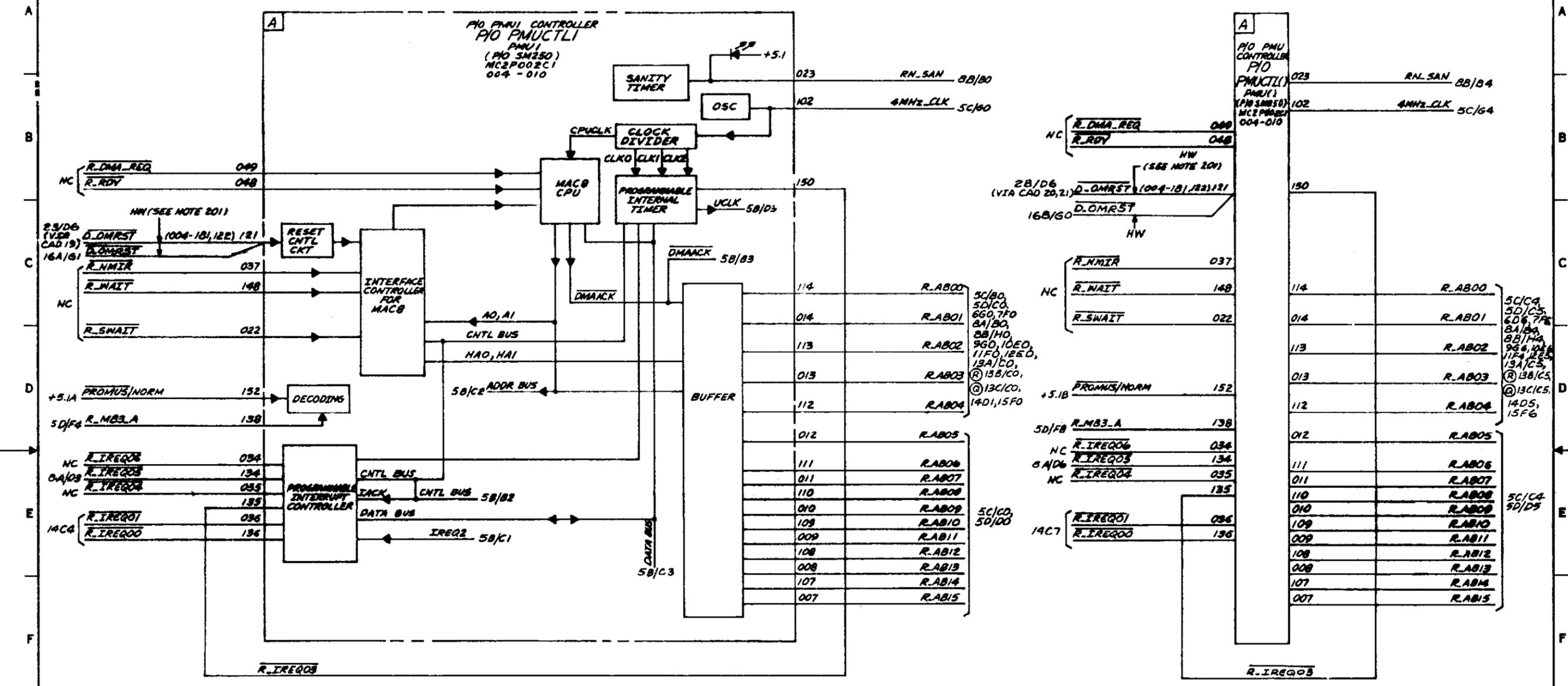
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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

AT&T BELL LABORATORIES SD -2P077-01

DWG SIZE 63 ISSUE 13AC SHEET 84

PART OF FS 5
PMU CONTROLLER, INTERFACE AND MEMORY CIRCUIT



POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0			
				+5.1A	+12	-12	
SM250	004-010	003 004 005 051 052 053	000 001 054 055 056	PMU1	+5.1A	+12	-12
				PMU2	+5.1B	+12	-12
				TERM.	TERM.	TERM.	
					100	123	132
					101	124	133
					153		
					154		
					155		
					156		

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD -2P077-01	SHEET B5A	

PART OF FS 5
PMU CONTROLLER, INTERFACE AND MEMORY CIRCUIT

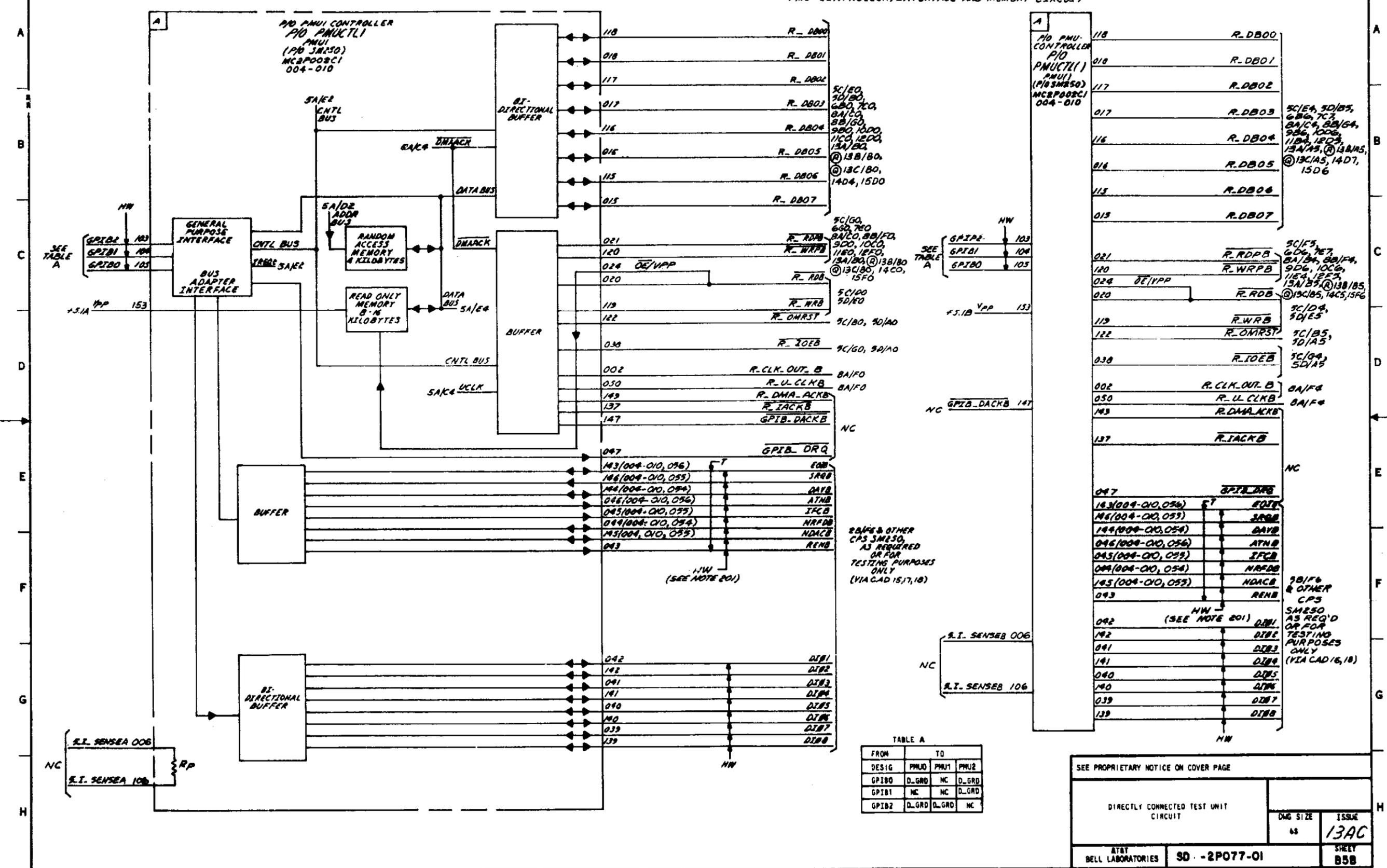


TABLE A

FROM	TO		
DESIG	PMU0	PMU1	PMU2
GPIB0	D.GRD	NC	D.GRD
GPIB1	NC	NC	D.GRD
GPIB2	D.GRD	D.GRD	NC

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		43	13AC
AT&T BELL LABORATORIES	SD - 2P077-01	SHEET	B5B

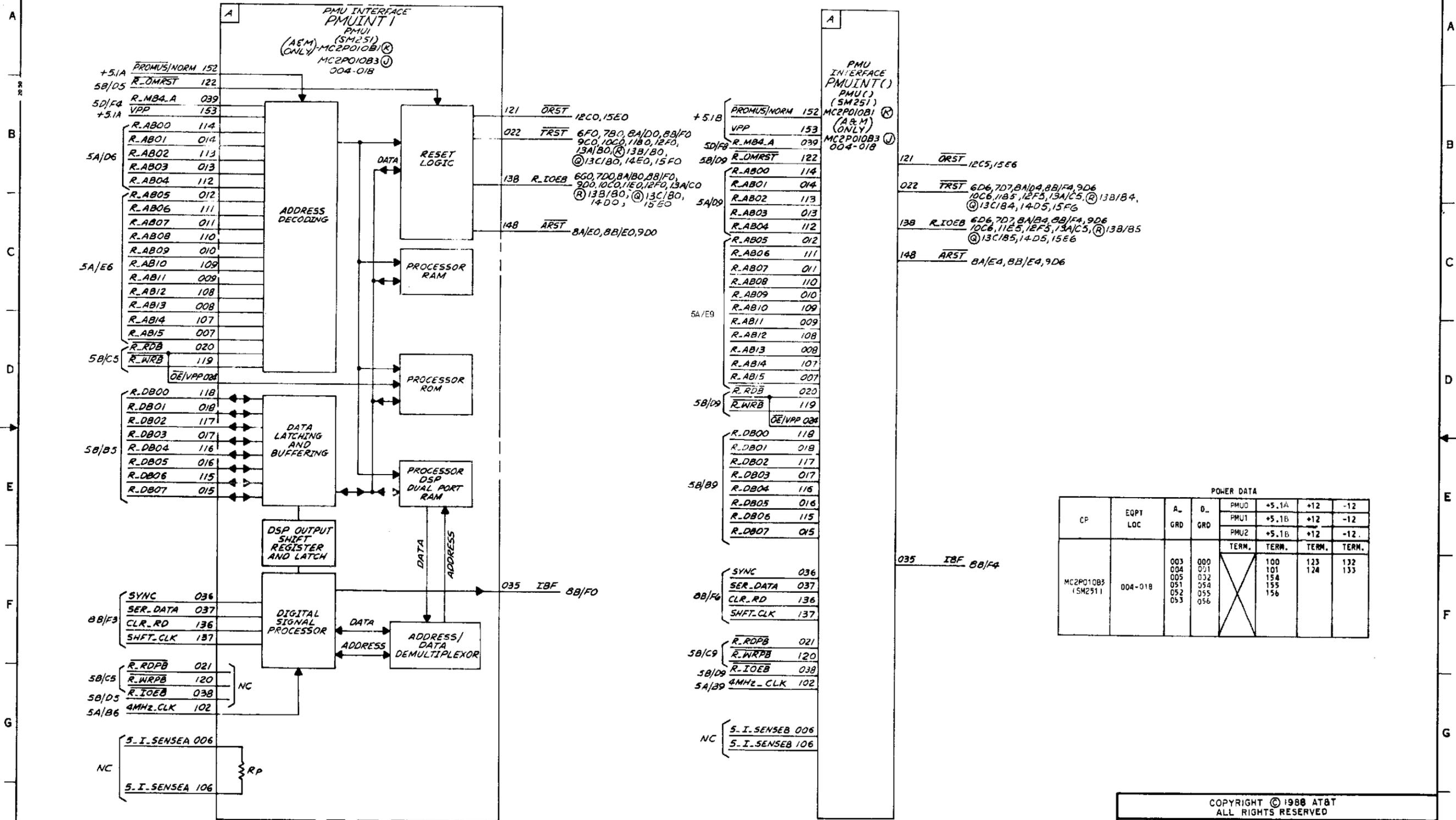
8A/16 & OTHER CPS S4250, AS REQUIRED OR FOR TESTING PURPOSES ONLY (VIA CAD 15,17,18)

7B/16 & OTHER CPS S4250, AS REQ'D OR FOR TESTING PURPOSES ONLY (VIA CAD 16,18)

SEE TABLE A

SEE TABLE A

PART OF FS 5
PMU CONTROLLER, INTERFACE AND MEMORY CIRCUIT



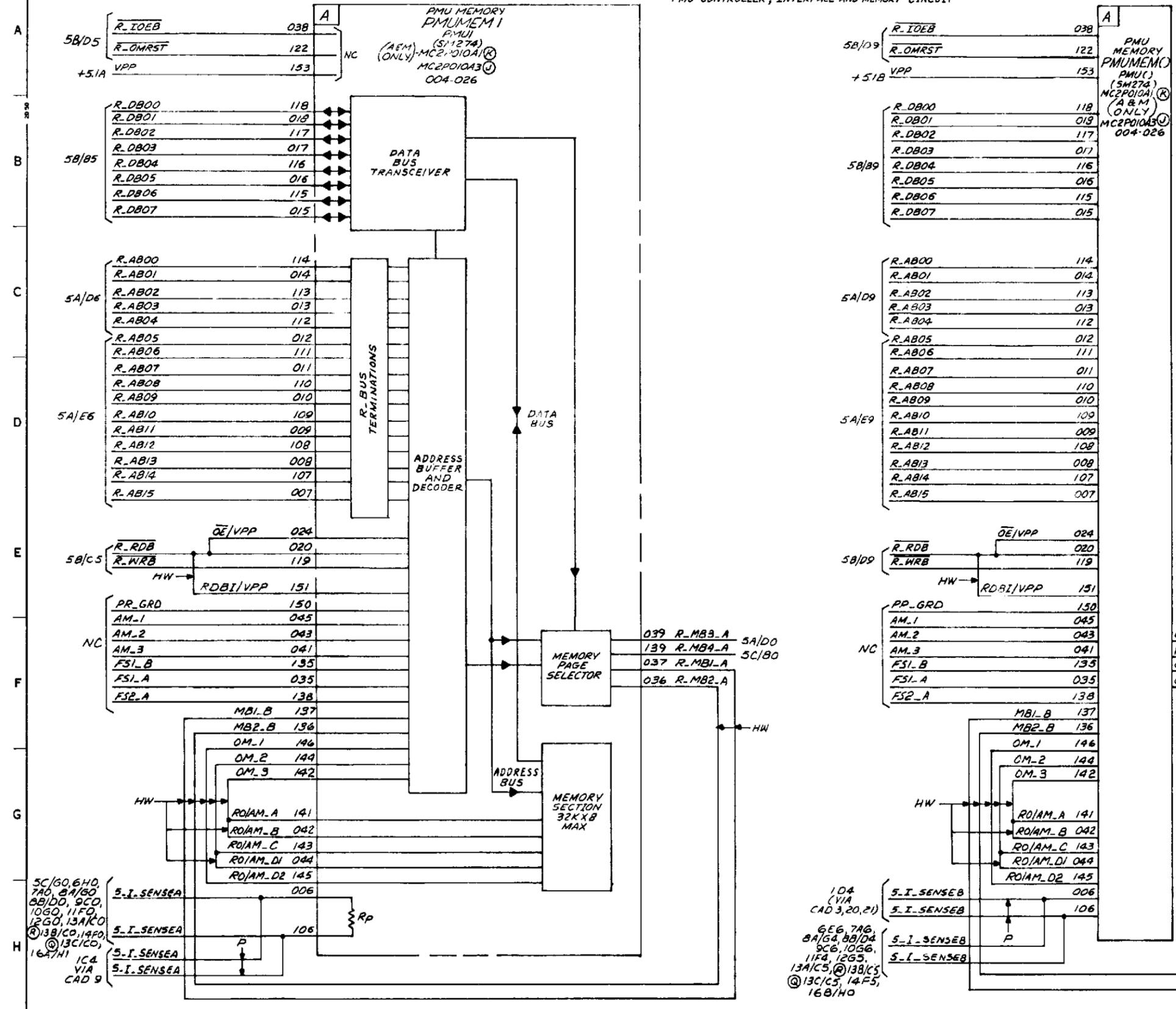
POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
				TERM.	TERM.	TERM.	TERM.
MC2P010B3 (SM251)	004-01B	003 004 005 051 052 053	000 021 032 054 055 056	X	100	123	132
				X	101	124	133
				X	154		
				X	155		
				X	156		
				X			

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DIRECTLY CONNECTED TEST UNIT		DWG SIZE	ISSUE
CIRCUIT		65	15A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET B5C	

PART OF FS 5
PMU CONTROLLER, INTERFACE AND MEMORY CIRCUIT



POWER DATA

CP	EQUIP LOC	R-GRD	D-GRD	PMU0		
				+5.1A	+12	-12
MC2P010A3 (SM274)	004 026	003 004 005 051 052 053	000 001 054 055 056 002	PMU1	+5.1B	+12
				PMU2	+5.1B	+12
				TERM.	TERM.	TERM.
				100	123	132
				101	124	133
				102		
				154		
				155		
				156		

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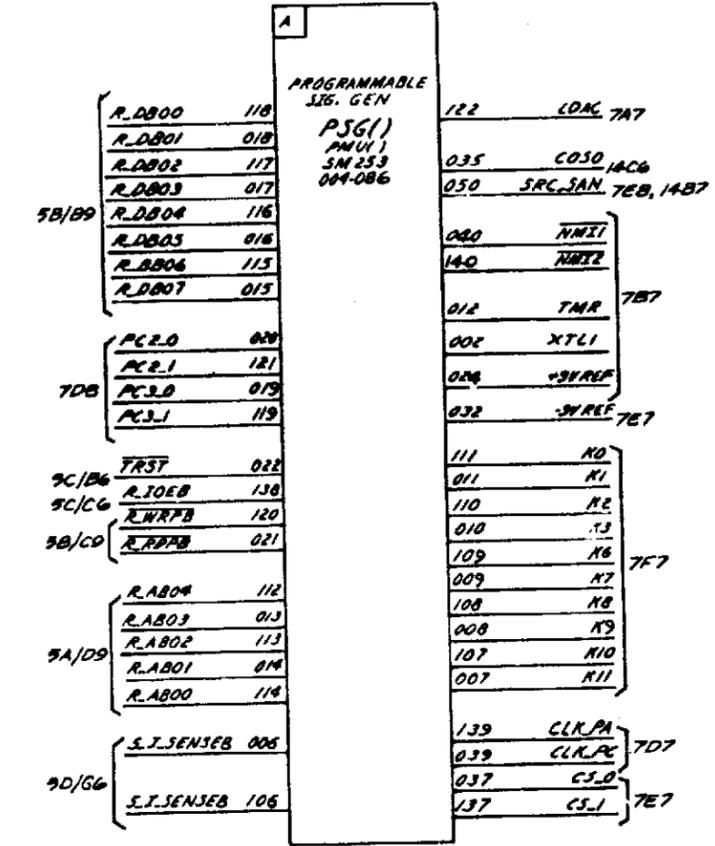
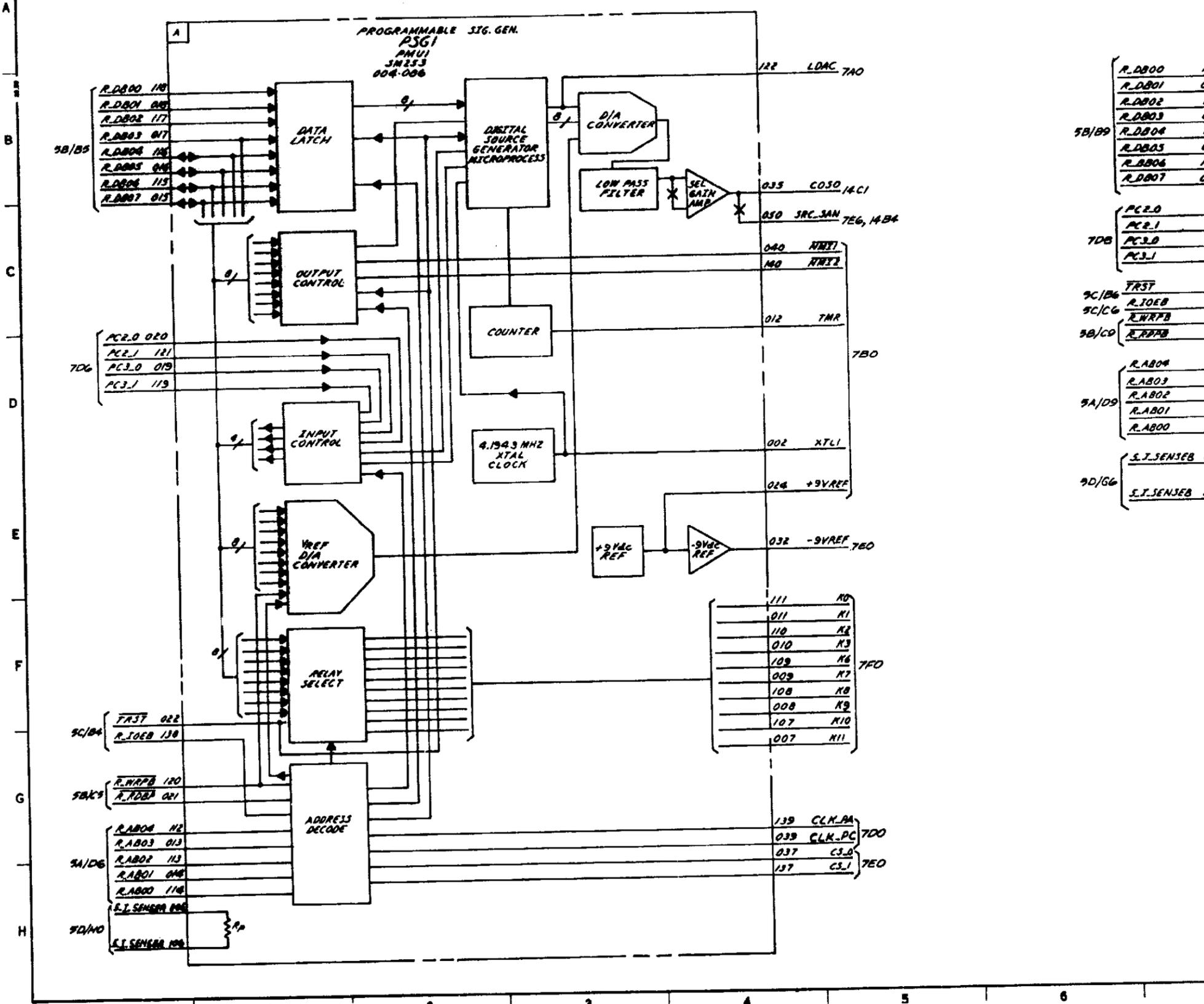
DIRECTLY CONNECTED TEST UNIT

CIRCUIT

AT&T BELL LABORATORIES	SD -2P077-01	DWG SIZE 65	ISSUE 15A
		SHEET 850	

PRINTED IN U.S.A.

FS 6
PROGRAMMABLE SIGNAL GENERATOR CIRCUIT



POWER DATA

CP	EQPT LDC	A GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
				PMU2	+5.1B	+12	-12
					TERM.	TERM.	TERM.
SM253	004-086	003	000	100	123	132	
		104	001	101	124	133	
		105	054	102			
		151	055	154			
		152	056	155			
		153		156			

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT
CIRCUIT

DWG SIZE: 65
ISSUE: 13AC

AT&T BELL LABORATORIES
SD -2P077-01

SHEET 86

FS 7
LINE REFERENCE MODULE CIRCUIT

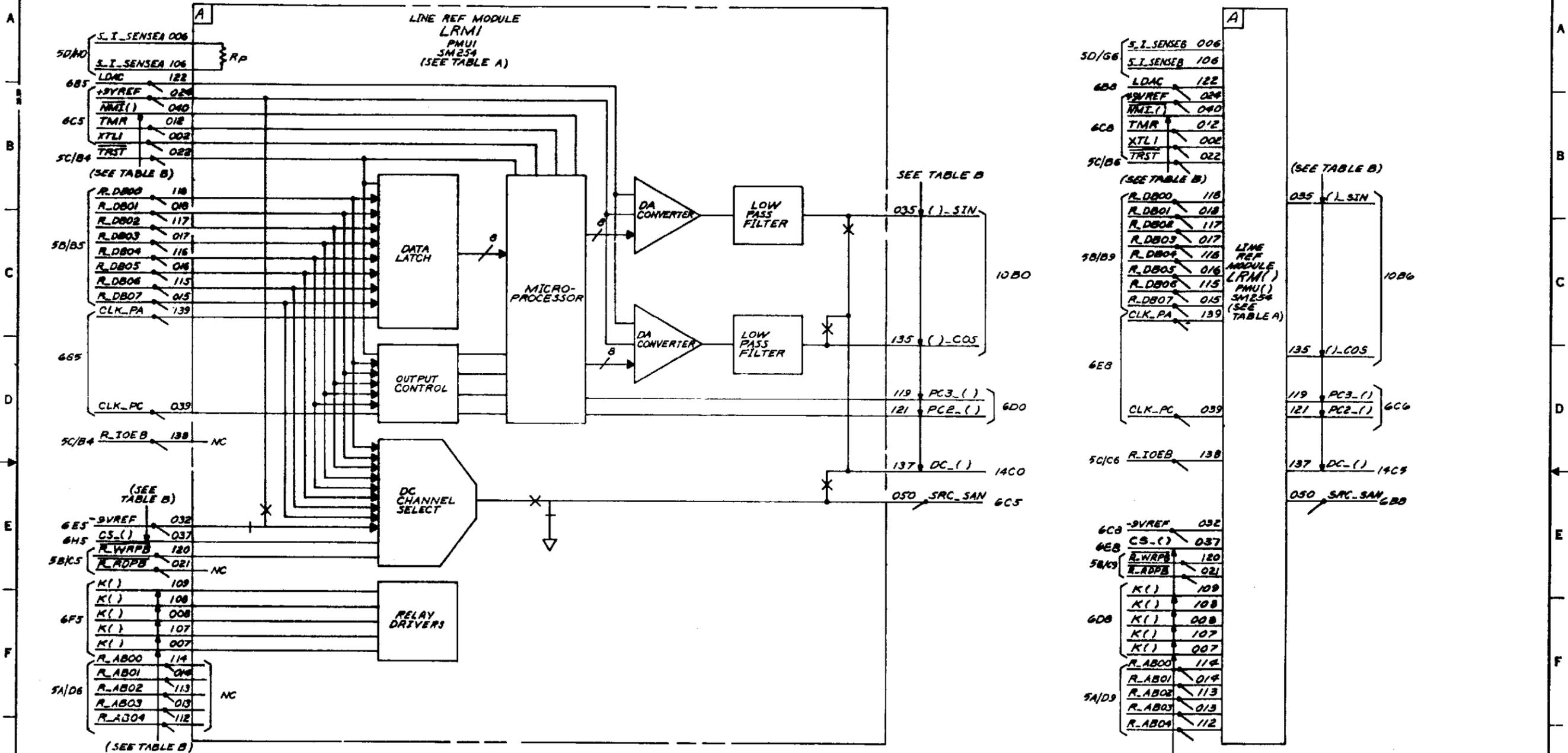


TABLE A

EQUIPMENT LOCATION	
SM254	
SHELF	LOC
PMU0	004-094
	004-102
PMU1	004-094
	004-102
PMU2	004-094
	004-102

TABLE B

SM254			
DESIG	EQUIPMENT LOCATION	DESIG	EQUIPMENT LOCATION
MM11		MM12	
CS_0		CS_1	
X0		K1	
X2		R5	
X6		R8	
X7		R9	
K10	004-094	R11	004-102
PC2_0		PC2_1	
PC3_0		PC3_1	
(A)_SIN		(B)_SIN	
(B)_COS		(A)_COS	
DC_0		DC_1	

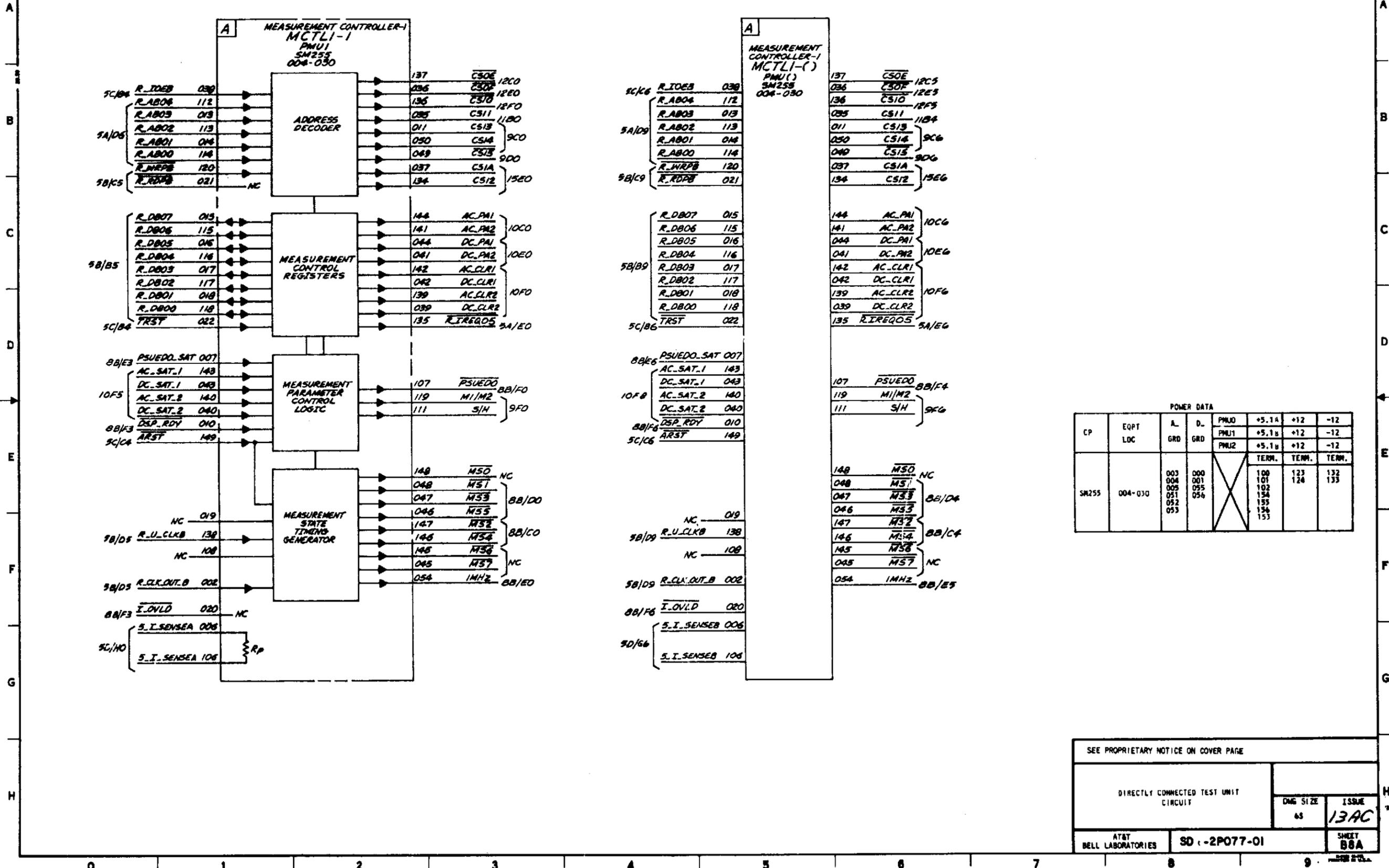
POWER DATA

CP	EQUIPMENT LOCATION	A-GRD	D-GRD	PMU0			PMU1			PMU2		
				+5.1A	+12	-12	+5.1A	+12	-12	+5.1A	+12	-12
SM254	004-094 004-102	003 004 005 051 052 053	000 001 054 055 056									
				TERM.								
				100	123	132	101	124	133	102	124	133
				154			154			154		
				155			155			155		
				156			156			156		

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD 1-2P077-01	SHEET 87	

PART OF FS 8
MEASUREMENT CONTROLLER 1 AND 2 CIRCUIT



POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
				PMU2	+5.1B	+12	-12
				TERM. TERM. TERM.			
SM255	004-030	003	000	001	100	123	132
				004	101	124	133
				005	102		
				051	103		
				052	104		
				053	105		
				054	106		
				055	107		

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DIRECTLY CONNECTED TEST UNIT CIRCUIT

AT&T BELL LABORATORIES

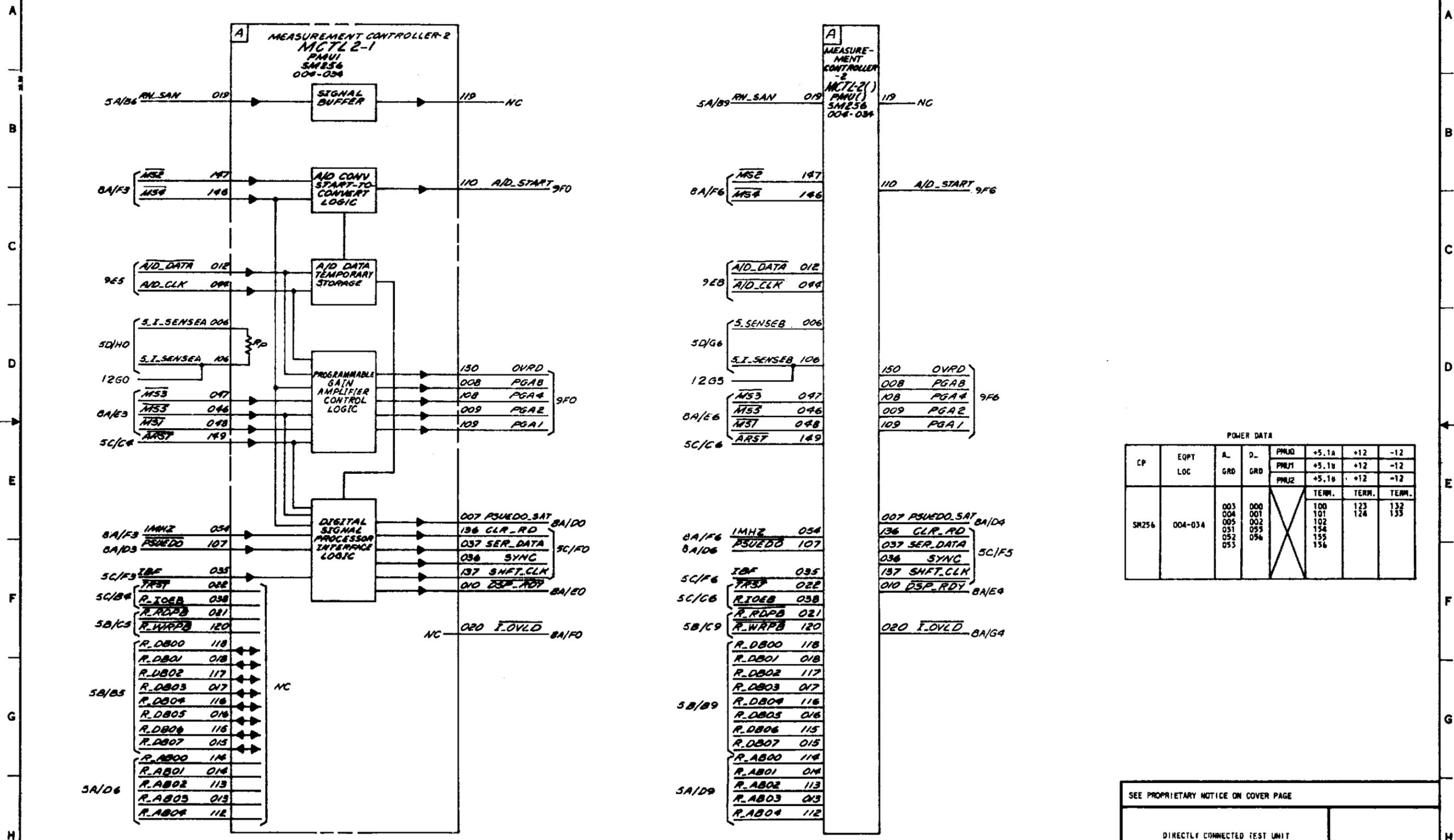
SD (-2P077-01)

DWG SIZE 65

ISSUE 13AC

SHEET 88A

P/O FS 8
MEASUREMENT CONTROLLER 1 AND 2 CIRCUIT



POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PHUJ	+5.1A	+12	-12	
				PHU1	+5.1B	+12	-12	
				PHU2	TERM.	TERM.	TERM.	
SM256	004-034	003	000	X	100	123	132	
					004	101	124	133
					005	102		
					051	154		
					052	155		
					053	156		

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DIRECTLY CONNECTED TEST UNIT CIRCUIT

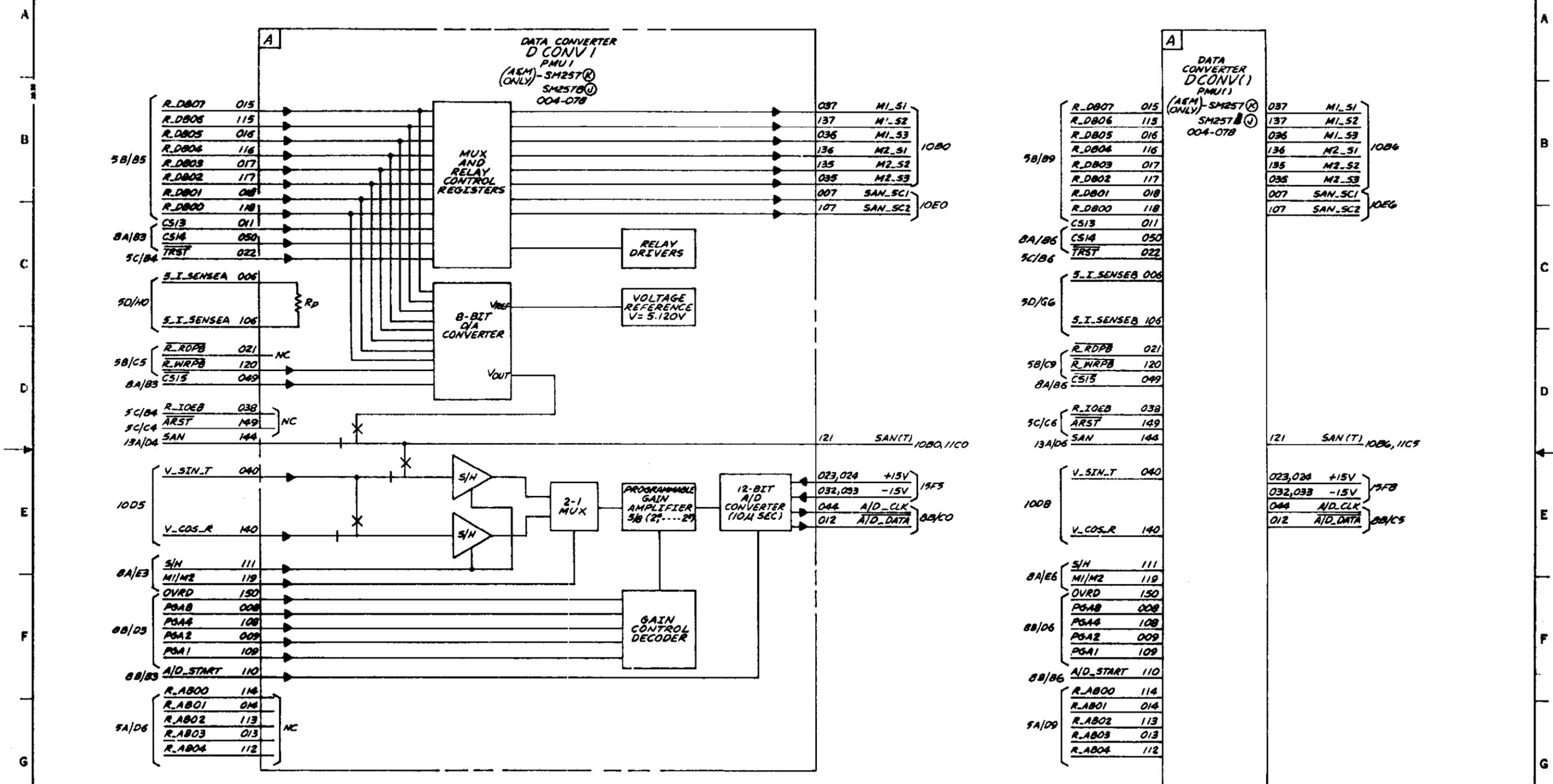
AT&T BELL LABORATORIES SD -2P077-01

DWG SIZE 6S

ISSUE 13AC

SHEET 888

FS 9
DATA CONVERTER CIRCUIT



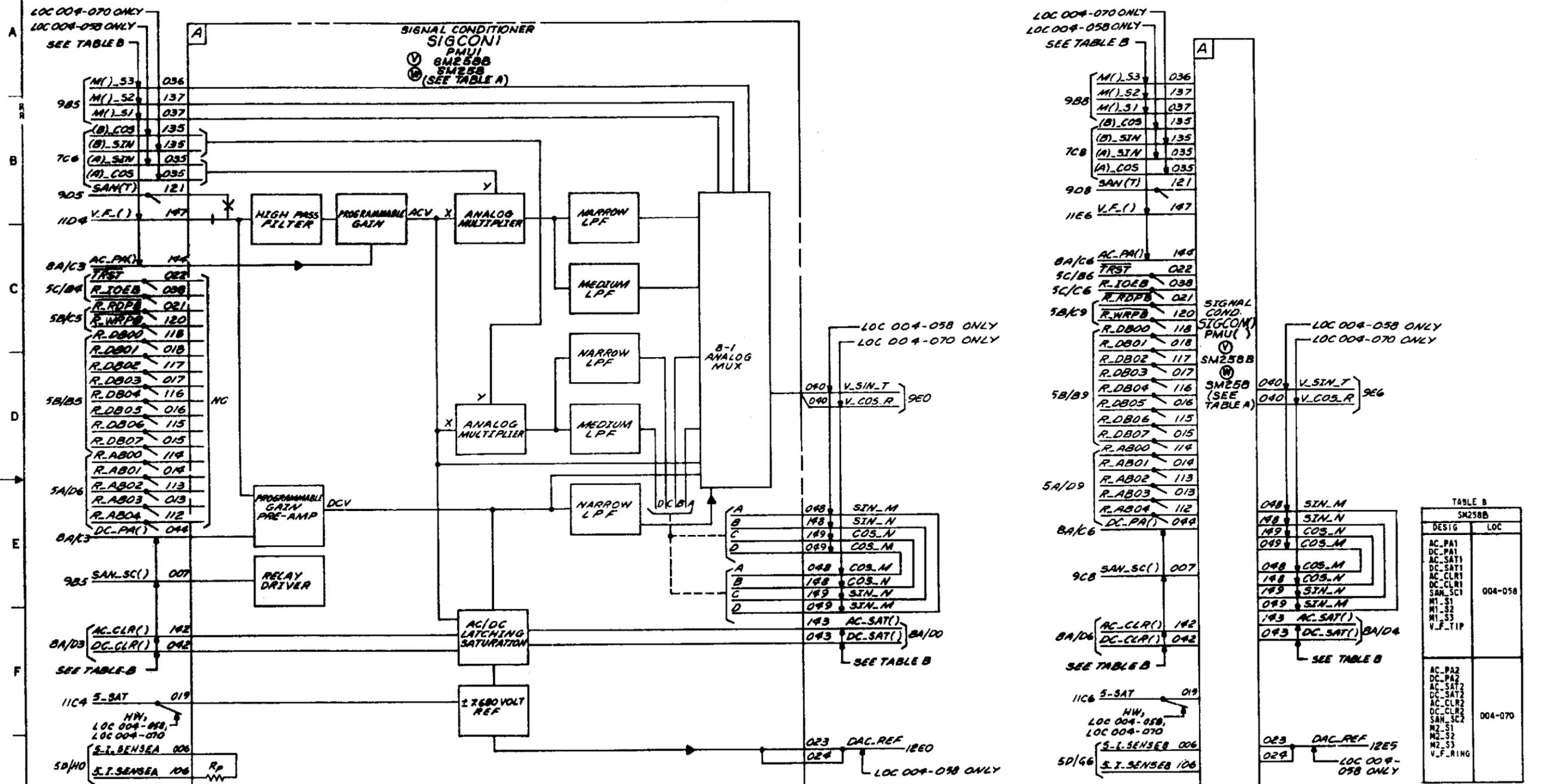
POWER DATA

CP	EQUIP LOC	A. GRD	D. GRD	PMU0			PMU1			PMU2		
				+5.1A	+12	-12	+5.1A	+12	-12	+5.1A	+12	-12
SM257	004-078	003 004 005 001 002 001	000 001 002 004 005 006	TERM.	TERM.	TERM.	100	123	132	100	123	132
				101	124	133	101	124	133			
				102			102					
				103			103					
				104			104					
				105			105					

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DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 89	

FS 10 SIGNAL CONDITIONER CIRCUIT



LOC 004-070 ONLY
LOC 004-058 ONLY
SEE TABLE B

985 M1.S3 036
M1.S2 137
M1.S1 037
7C6 (B).COS 135
(B).SIN 135
(A).SIN 035
(A).COS 035
905 SAN(T) 121
1104 V.F.(1) 147

8A/C3 AC.PA1 144
TRST 022
5C/B4 R.TOE8 028
R.RDP8 021
5A/C5 R.WRFB 120
R.DBO0 118
R.DBO1 018
R.DBO2 117
R.DBO3 017
5B/B5 R.DBO4 116
R.DBO5 016
R.DBO6 115
R.DBO7 015
R.AB00 114
R.AB01 014
5A/D6 R.AB02 113
R.AB03 013
R.AB04 112
DC.PA1 044

985 SAN.SC() 007

8A/D3 AC.CLR() 142
DC.CLR() 042
SEE TABLE B

11C4 5-SAT 019

HW:
LOC 004-058,
LOC 004-070

5D/H0 S.T.SENSEA 006
S.T.SENSEA 106

LOC 004-070 ONLY
LOC 004-058 ONLY
SEE TABLE B

988 M1.S3 036
M1.S2 137
M1.S1 037
7C8 (B).COS 135
(B).SIN 135
(A).SIN 035
(A).COS 035
908 SAN(T) 121
11E6 V.F.(1) 147

8A/C6 AC.PA1 144
TRST 022
5C/B6 R.TOE8 028
R.RDP8 021
5B/C9 R.WRFB 120
R.DBO0 118
R.DBO1 018
R.DBO2 117
R.DBO3 017
5B/B9 R.DBO4 116
R.DBO5 016
R.DBO6 115
R.DBO7 015
R.AB00 114
R.AB01 014
5A/D9 R.AB02 113
R.AB03 013
R.AB04 112
DC.PA1 044

9C8 SAN.SC() 007

8A/D6 AC.CLR() 142
DC.CLR() 042
SEE TABLE B

11C6 5-SAT 019

HW:
LOC 004-058,
LOC 004-070

5D/G6 S.T.SENSEB 006
S.T.SENSEB 106

TABLE A

EQPT LOC	
SM2588	
SHELF	LOC
PMU0	004-058 004-070
PMU1	004-058 004-070
PMU2	004-058 004-070

POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1A	+12	-12
				PMU2	+5.1A	+12	-12
					TERM.	TERM.	TERM.
					100	123	132
					101	124	133
					102		
					154		
					135		
					156		

TABLE B

SM2588	
DESIG	LOC
AC.PA1	004-058
DC.PA1	
AC.SAT1	
DC.SAT1	
AC.CLR1	
DC.CLR1	
SAN.SC1	
M1.S1	
M1.S2	
M1.S3	
V.F.TIP	
AC.PA2	004-070
DC.PA2	
AC.SAT2	
DC.SAT2	
AC.CLR2	
DC.CLR2	
SAN.SC2	
M2.S1	
M2.S2	
M2.S3	
V.F.RING	

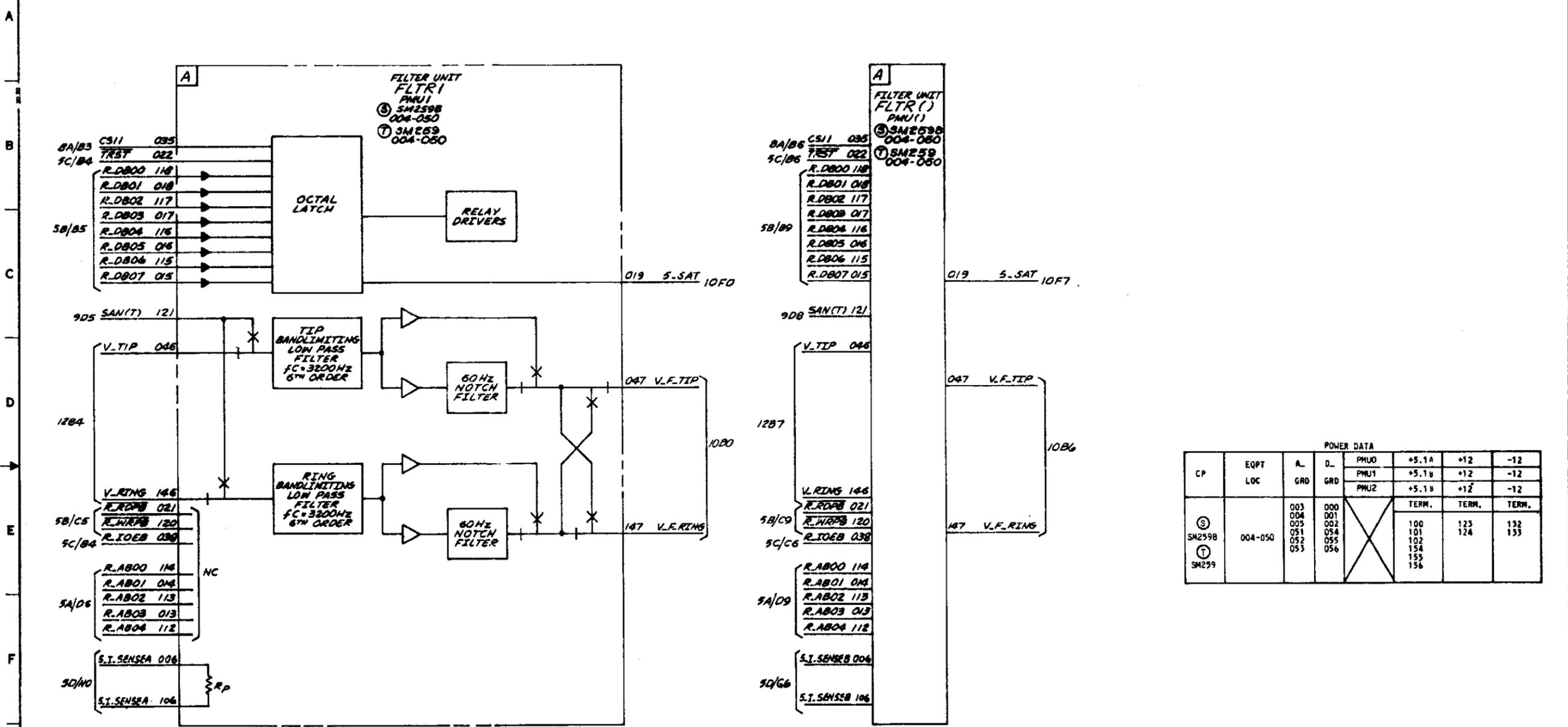
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DIRECTLY CONNECTED TEST UNIT CIRCUIT

DATE SIZE ISSUE
65 13AC

AT&T BELL LABORATORIES SD -2P077-01 SHEET BIO

FS 11
FILTER CIRCUIT



POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
(S) SM259B (T) SM259	004-050	003	000	X	TERM.	TERM.	TERM.
		004	001		100	123	132
		005	002		101	124	133
		051	054		102		
		052	055		154		
		053	056		155		

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DIRECTLY CONNECTED TEST UNIT CIRCUIT

AT&T BELL LABORATORIES

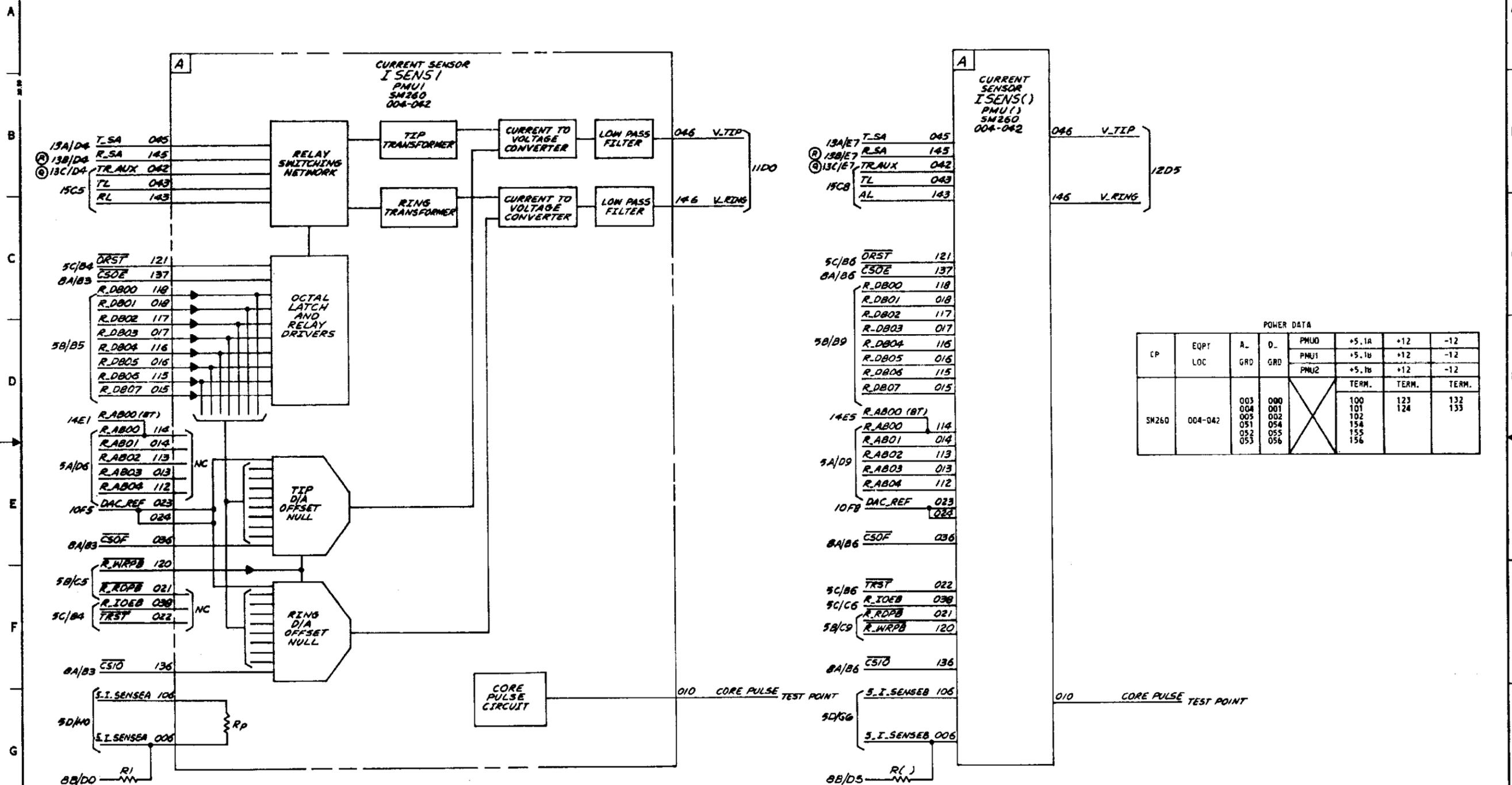
SD -2P077-01

DWG SIZE: 45

ISSUE: 13AC

SHEET: B11

FS 12
CURRENT SENSOR CIRCUIT



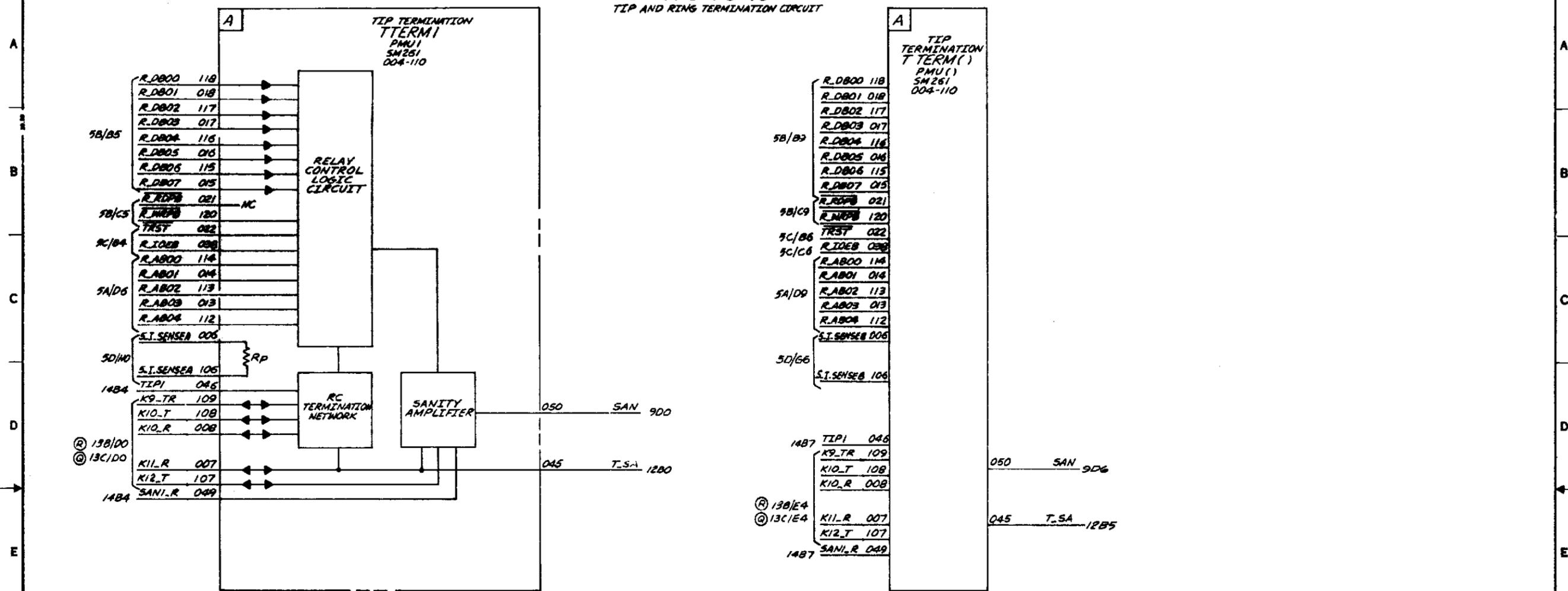
POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
				PMU2	+5.1B	+12	-12
					TERM.	TERM.	TERM.
SM260	004-042	003	000	X	100	123	132
		004	001		101	124	133
		005	002		102		
		001	003		103		
		002	004		104		
		006	006		106		

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DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		AS	13AC
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 812	

P/O FS 13
TIP AND RING TERMINATION CIRCUIT



POWER DATA

CP	EQPT LOC	A-GRD	D-GRD	PMU0	+5.1A	+12	-12
				PMU1	+5.1B	+12	-12
				PMU2	+5.1B	+12	-12
SM261	004-110	003 004 005 051 052 053	000 001 002 054 055 056	X	TERM. 100 101 102 154 155 156	TERM. 123 124	TERM. 132 133

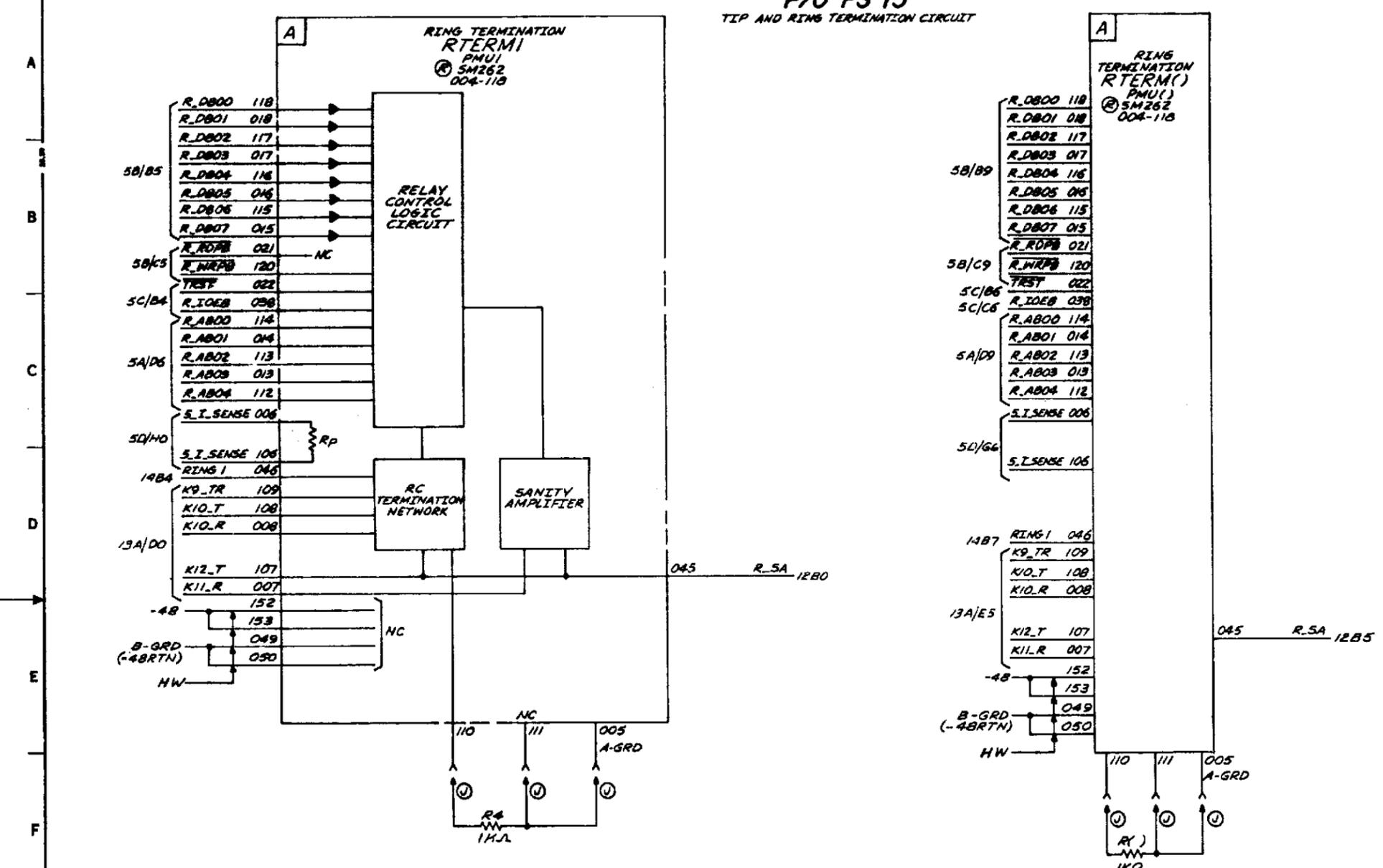
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DIRECTLY CONNECTED TEST UNIT CIRCUIT

DWG SIZE: 65 ISSUE: 13AC

AT&T BELL LABORATORIES SD -2P077-01 SHEET: B13A

P/O FS 13
TIP AND RING TERMINATION CIRCUIT



POWER DATA

CP	EQPT LOC	A-GRD	D-GRD	PMU			B-GRD	-48
				PMU0	+5.1A	+12		
SM262	004-118	003	000	X	TERM.	TERM.	TERM.	049
		004	001		100	123	132	090
		005	002		101	124	133	153
		051	054		102			
		052	055		154			
		053	056		155			
					156			

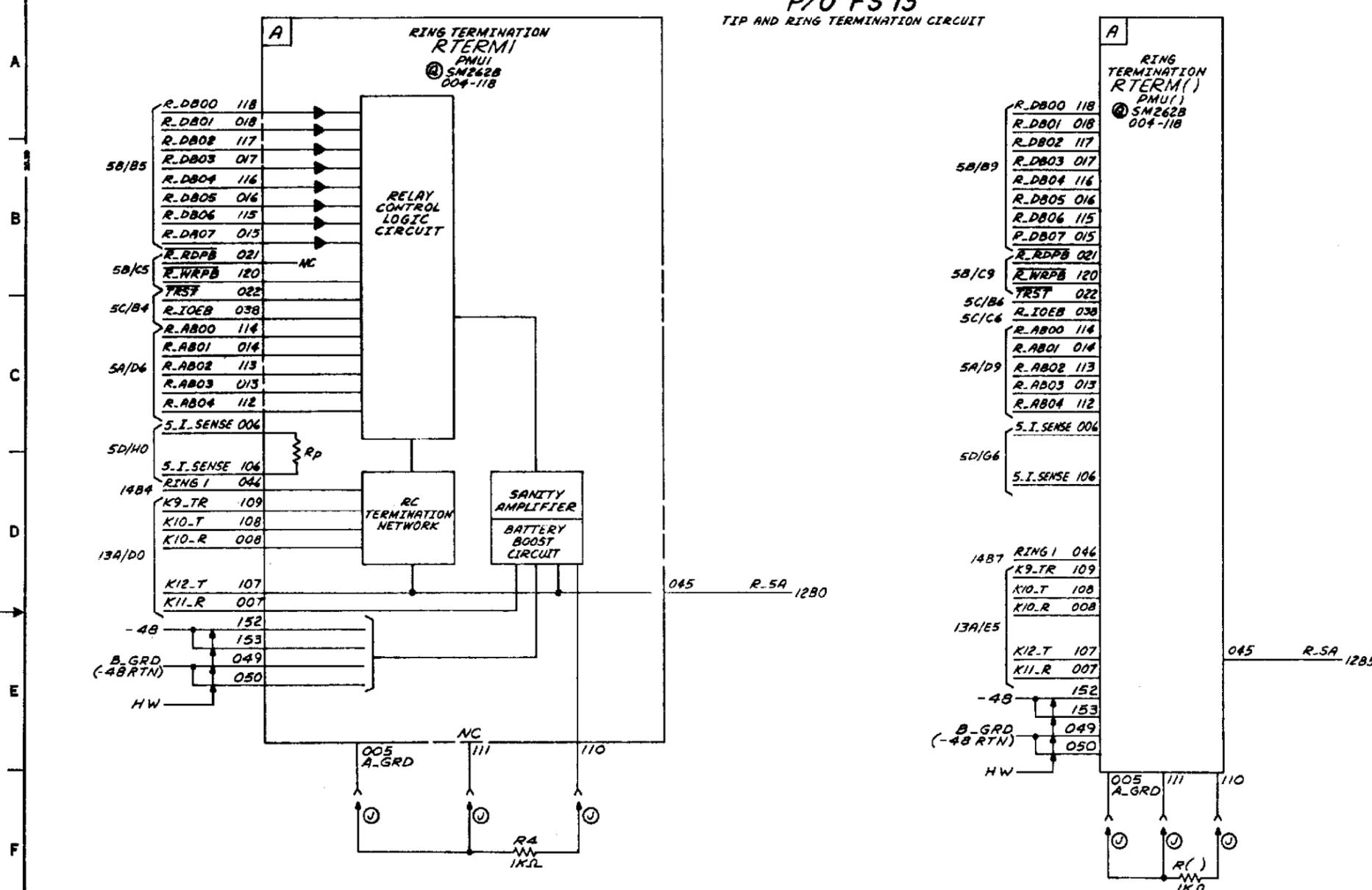
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DIRECTLY CONNECTED TEST UNIT CIRCUIT

AT&T BELL LABORATORIES SD -2P077-01

DWG SIZE 45 ISSUE 13AC SHEET 8130

P/O FS 13
TIP AND RING TERMINATION CIRCUIT



POWER DATA

CP	EQPT LOC	A-GRD	D-GRD	PMU0	+5.1A	+12	-12	B-GRD	-48			
				PMU1	+5.1B	+12	-12					
SM2628	004-118	003	000	X	TERM.	TERM.	TERM.	049	152			
		004	001									
		005	002									
		051	054									
		052	055									
		053	056									
		100	123							132	050	153
		101	124							133		154
102				155								
				156								

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DIRECTLY CONNECTED TEST UNIT CIRCUIT

DATE SIZE ISSUE
13AC

AT&T BELL LABORATORIES SD -2P077-01 SHEET B13C

FS 14 SOURCE AMPLIFIER CIRCUIT

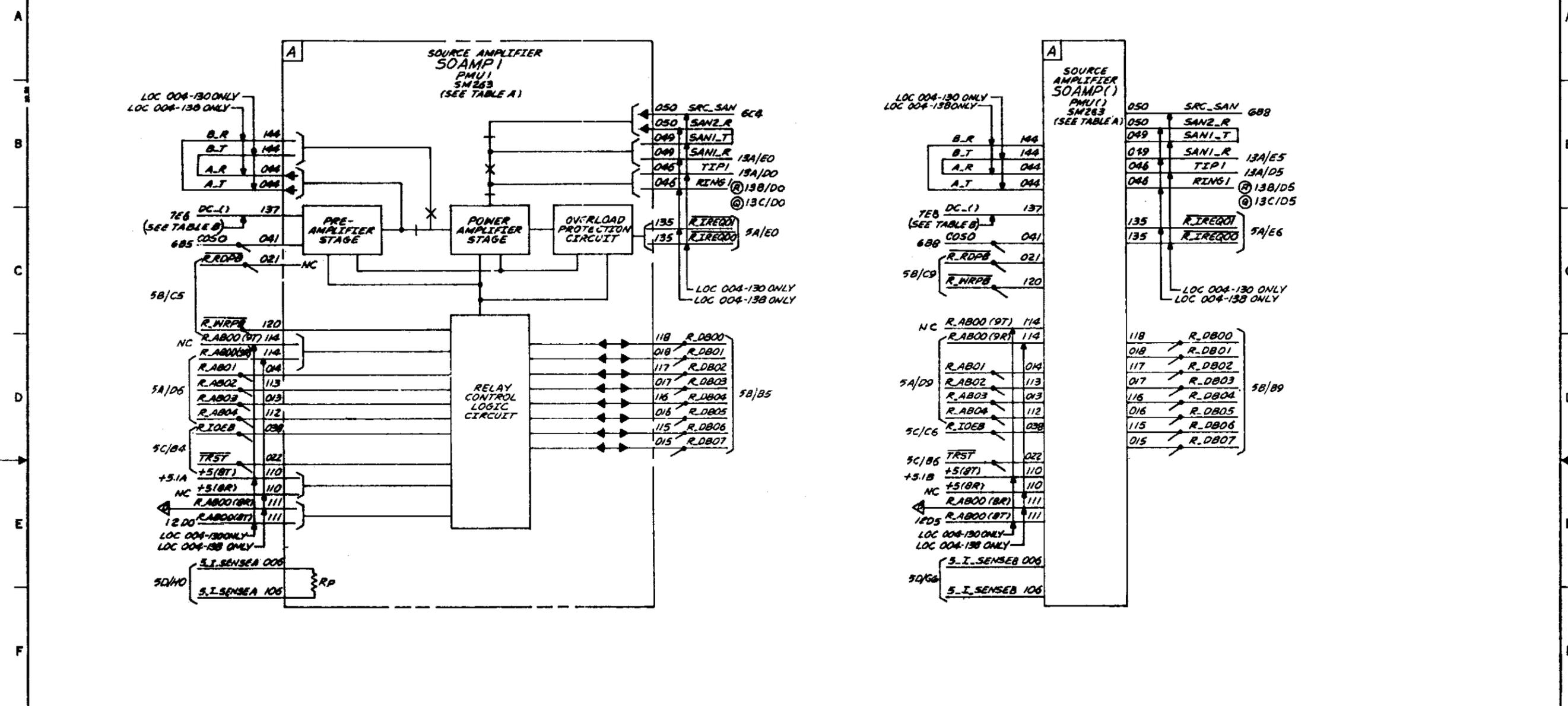


TABLE A

EQUIP. LOC	
SM263	
SHELF	LOC
PMU0	004-130 004-138
PMU1	004-130 004-138
PMU2	004-130 004-138

TABLE B

SM263	
DESIG	LOC
DC.0	004-130
DC.1	004-138

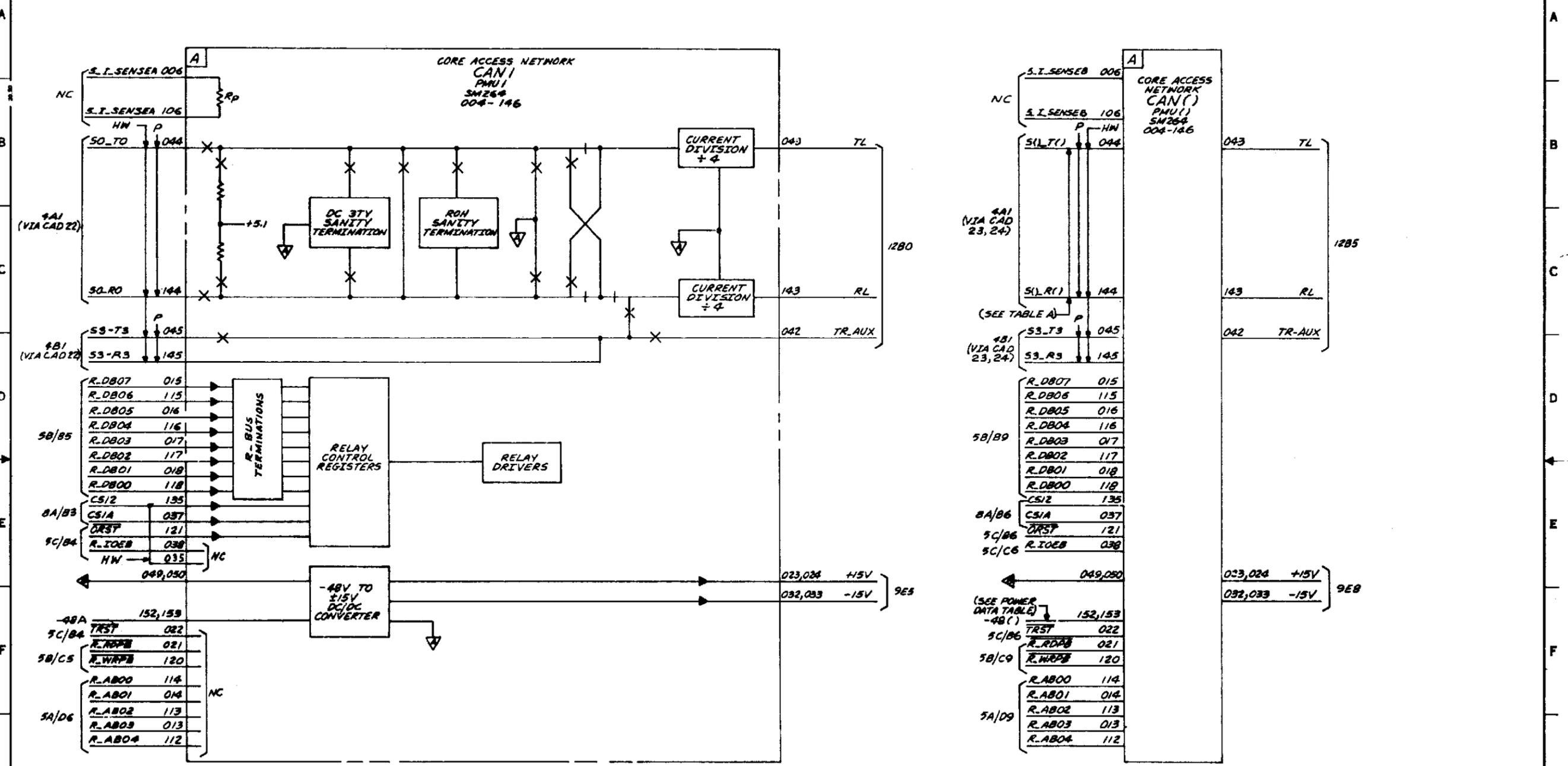
POWER DATA

CP	EQUIP. LOC	A. GRD	D. GRD	PMU0	+5.1A	+12	-12	+150	-150
				PMU1	+5.1B	+12	-12	+150	-150
SM263	004-130 004-138	003 004 005 051 052 053	000 001 002 054 055 056		TERM.	TERM.	TERM.	TERM.	TERM.
					100 101 102 154 155 156	123 124	132 133	104 105	151 152

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 65	ISSUE 13AC
AT&T BELL LABORATORIES		SD -2P077-01	
		SHEET 814	

FS 15
CORE ACCESS NETWORK CIRCUIT



- 4A1 (VIA CAD 22)
- 50-TO 044
- 50-RO 144
- 53-T3 045
- 53-R3 145
- R-DB07 015
- R-DB06 115
- R-DB05 016
- R-DB04 116
- R-DB03 017
- R-DB02 117
- R-DB01 018
- R-DB00 118
- CS12 135
- CS1A 037
- DRST 121
- R-IOEB 038
- HW 035
- 049,050
- 48A TRST 022
- 5C/84 R-RDPB 021
- 5B/C5 R-WRFB 120
- R-AB00 114
- R-AB01 014
- R-AB02 113
- R-AB03 013
- R-AB04 112

- 4A1 (VIA CAD 23, 24)
- 51-T1 044
- 51-R1 144
- 53-T3 045
- 53-R3 145
- R-DB07 015
- R-DB06 115
- R-DB05 016
- R-DB04 116
- R-DB03 017
- R-DB02 117
- R-DB01 018
- R-DB00 118
- CS12 135
- CS1A 037
- DRST 121
- R-IOEB 038
- 049,050
- (SEE POWER DATA TABLE)
- 48(C) -48(C)
- 5C/86 TRST 022
- 5C/86 R-RDPB 021
- 5B/C9 R-WRFB 120
- R-AB00 114
- R-AB01 014
- R-AB02 113
- R-AB03 013
- R-AB04 112

TABLE A

SM264	
DESIG	SHELF
S1.T1	PMU1
S1.R1	
S2.T2	PMU2
S2.R2	

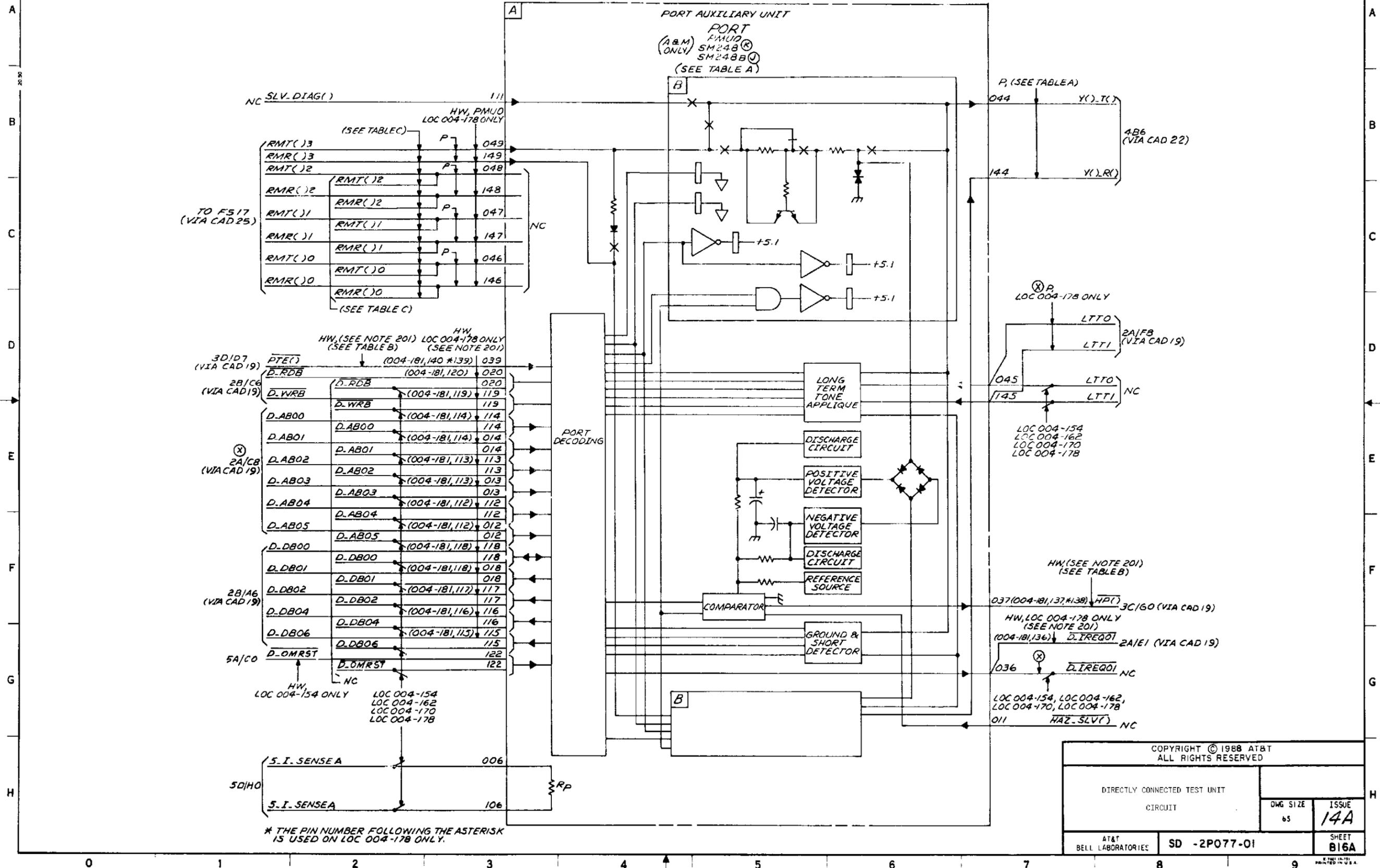
POWER DATA

CP	EQPT LOC	A. GRD	D. GRD	PMU1	+5.1A	+12	-12	-48(A)
				PMU2	+5.1W	+12	-12	-48(W)
SM264	004-146	003 004 005 051 052 053	000 001 002 054 055 056	TERM.	TERM.	TERM.	TERM.	
				100	123	132	152	
				101	124	133	153	
				102				
				154				
				155				
				156				

SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD - 2P077-01	SHEET 815	

PART OF FS16
PORT UNIT CIRCUIT



TO FS17
(VIA CAD 25)

3D/D7
(VIA CAD 19)

2B/C6
(VIA CAD 19)

2A/CB
(VIA CAD 19)

2B/A6
(VIA CAD 19)

5A/C0

50/H0

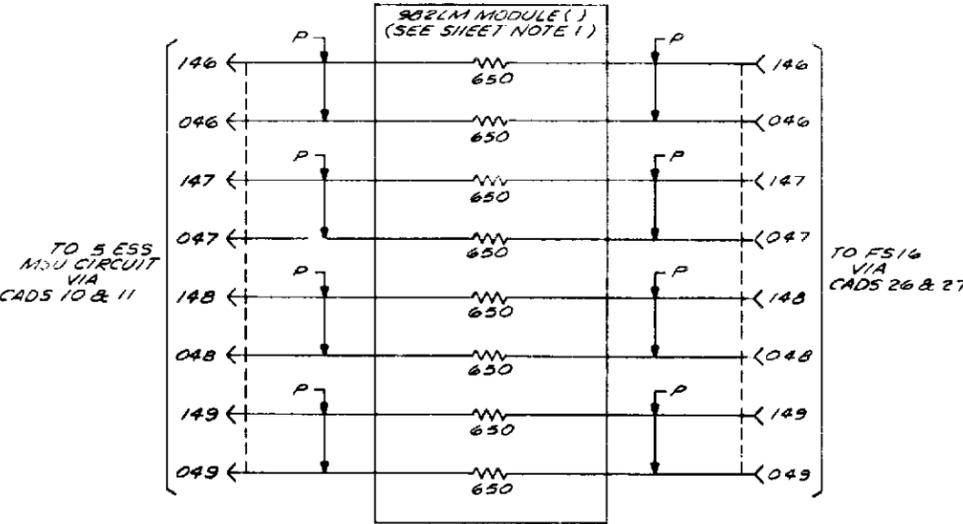
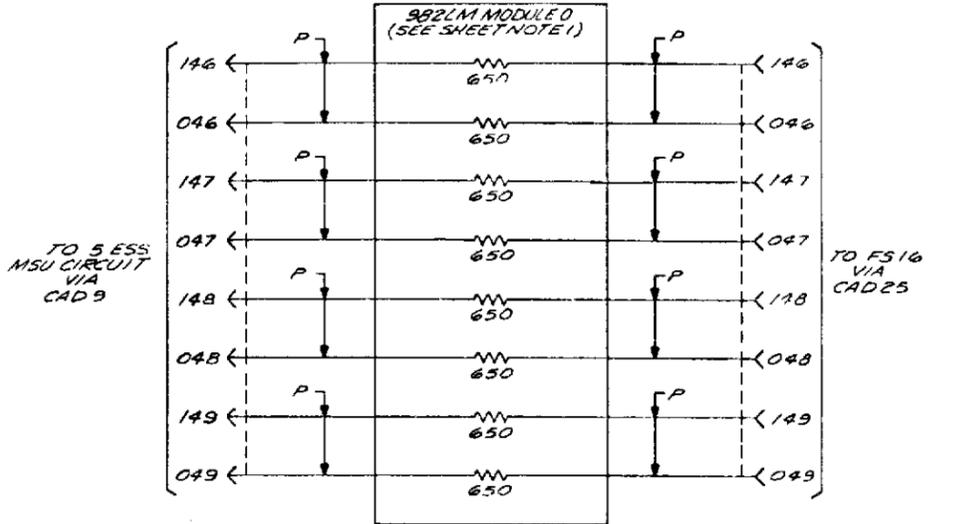
* THE PIN NUMBER FOLLOWING THE ASTERISK IS USED ON LOC 004-178 ONLY.

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DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 65
		ISSUE 14A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET B16A

PRINTED IN U.S.A.

0 1 2 3 4 5 6 7 8 9

FS 17
 CPS 982LM DCTU BACKPLANE RESISTOR
 CIRCUIT MODULE (10430-059)
 (SEE SHEET NOTE 2)



- SHEET NOTES :
1. THE 982LM RESISTOR MODULE PLUGS INTO THE BACKPLANE PINS.
 2. THE AT&T LEXINGTON ROAD FACTORY SHIPS DCTU'S WITHOUT THE 982LM BACKPLANE CIRCUIT MODULE. THESE MODULES ARE INSTALLED ON EACH DCTU'S BACKPLANE AT THE OKLAHOMA CITY WORKS. THE OKLAHOMA CITY WORKS PROCURES THESE MODULES FROM THE KANSAS CITY WORKS.

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DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 85
AT&T BELL LABORATORIES SD-2P077-01		ISSUE 14A
		SHEET B17

0 1 2 3 4 5 6 7 8 9

APP FIG. 1
(J1P023AM: LIST 1)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
M	+5.1A	004-042	1A2		PWP054CA	495FB	LB
	+5.1A	004-042	1A2		PWP021A	495A	LB
	+12	004-090	1D2		PWP053YA	494MA	LA
	-12	004-090	1D2		PWP02QE	494E	LA
M	+70,+150	004-074	1C8		PWP021D	495D	LE
	-12	004-058	1A8		PWP053YA	494MA	LA
	-12	004-058	1A8		PWP02QE	494E	LA
	-150	004-090	1E8		PWP021D	495D	LE

APP FIG. 2
(J1P023AM: LIST 1)

CONTROL SHELF	OPTION	DESIG	LOC	CODE
BACKPLANE WIRING PER FS1-FS4				ED-2P383-30

APP FIG. 3
(J1P023AM: LIST 1, 2, 3)

PRECISION MEASUREMENT UNIT SHELF	OPTION	DESIG	LOC	CODE
BACKPLANE WIRING PER FS5-FS16				ED-2P384-30
982LM RESISTOR MODULE		17A4		104385059

APP FIG. 4
(J1P023AM: LIST 1)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
J	DCTUCTL		004-010	2A/A4, 2B/A3	LMPQ15A	SN422	AF
	PICB INTER		004-018	3C/B5, 3D/A5	LMMQ04FAXX	MC2P004A3B (TN629B)	AH
K	PICB INTER		004-018	3C/B5, 3D/A5	LMMQ04B (I&M ONLY)	MC2P004A1B (TN629B)	AH
X	PICB INTER		004-018	3A/B6, 3B/B5	LMMQ04A	MC2P004A1 (TN629)	AH
Y	SWU1		004-154	4A4	LMPQ05CAXX	SN423	AG
			004-162		LMPQ05CAXX	SN423	
			004-170		LMPQ05CAXX	SN423	

APP FIG. 5
(J1P023AM: LIST 1)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
J	CANI		004-146	15A2	LMPQ23Y	SM264	
	DCONV1		004-078	9A3	LMPQ18A	SM257B	
K	DCONV1		004-078	9A3	LMPQ03R	SM257 (I&M ONLY)	
S	FLTR1		004-090	11B2	LMPQ13T	SM259B	
			004-090	11B2	LMPQ13T	SM259	
			004-042	12B2	LMPQ13U	SM260	
		(2) LRM1		004-094, 004-102	7A3	LMPQ03H	SM254
MC	MC1L1-1		004-030	8A/A2	LMPQ03J	SM255	
	MC1L2-1		004-034	8B/A2	LMPQ03K	SM256	
	PMUCTL1		004-010	5A/A3, 5B/A2	LMMQ08BA	MC2P002C1 (SM250)	
J	PMUIN1		004-018	5C/A2	LMMQ20FAXX	MC2P010B3 (SM251)	
K	PMUIN1		004-018	5C/A2	LMMQ20CAXX	MC2P010B1 (SM251)	
J	PMUMEM1		004-026	5D/A2	LMMQ21CAXX	MC2P010A3 (SM274)	
K	PMUMEM1		004-026	5D/A2	LMMQ21A (I&M ONLY)	MC2P010A1 (SM274)	
J	[4] PORT1		004-154	16A/A5	LMPQ17B	SM248B	
			004-162				
K	[4] PORT1		004-170		LMPQ03B	SM248 (I&M ONLY)	
			004-178				
Q	RTERM1		004-086	6A2	LMPQ03G	SM253	
			004-118	13C/A5	LMPQ04R	SM252B	
V	[2] SIG CON1		004-098	15B/A2	LMPQ03W	SM262	
			004-070	1CA2	LMPQ13S	SM258B	
W	[2] SIG CON1		004-130	14A2	LMPQ24X	SM263	
			004-138				
T	TTERM1		004-110	13A/B2	LMPQ03V	SM261	

RESISTOR	OPTION	DESIG	LOC	CODE
	J	R4	13B/F2, 13C/F2	KS-20616, L1A, 3480R KS-20616, L1A, 1KQ

APP FIG. 6
(J1P023AM: LIST 2, 3)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
J	CANI		004-146	15A7	LMPQ13Y	SM264	
	DCONV1		004-078	9A7	LMPQ18A	SM257B	
K	DCONV1		004-078	9A7	LMPQ03R	SM257 (I&M ONLY)	
S	FLTR1		004-090	11B5	LMPQ13T	SM259B	
			004-090	11B5	LMPQ13T	SM259	
			004-042	12B6	LMPQ03U	SM260	
		(2) LRM1		004-094, 004-102	7C7	LMPQ03H	SM254
MC	MC1L1		004-030	8A/A5	LMPQ03J	SM255	
	MC1L2		004-034	8B/A5	LMPQ03K	SM256	
	PMUCTL		004-010	5A/A7, 5B/A7	LMMQ08BA	MC2P002C1 (SM250)	
J	PMUIN1		004-018	5C/A5	LMMQ20FAXX	MC2P010B3 (SM251)	
K	PMUIN1		004-018	5C/A5	LMMQ20CAXX	MC2P010B1 (SM251)	
J	PMUMEM1		004-026	5D/A7	LMMQ21CAXX	MC2P010A3 (SM274)	
K	PMUMEM1		004-026	5D/A7	LMMQ21A	MC2P010A1 (SM274)	
J	[4] PORT1		004-154	16B/A2	LMPQ17B	SM248B	
			004-162				
K	[4] PORT1		004-170		LMPQ03B	SM248 (I & M ONLY)	
			004-178				

APP FIG. 6 (CONT)
(J1P023AM: LIST 2, 3)

PACK. CIRCUIT (CONT)	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
Q	RTERM1		004-086	5B7	LMPQ03G	SM253	
			004-118	13C/A5	LMPQ04R	SM252B	
R	RTERM1		004-118	133/A5	LMPQ03W	SM262	
V	[2] SIG CON1		004-096	10C7	LMPQ13S	SM258B	
			007-070				
W	[2] SIG CON1		004-098	10C7	LMPQ13S	SM258	
			007-070				
T	[2] SOAMP1		004-130	14A6	LMPQ24X	SM263	
			004-138	13A/A5	LMPQ03V	SM261	
	TTERM1		004-110				

RESISTOR	OPTION	DESIG	LOC	CODE
	J	R1	13B/F2, 13C/F2	KS-20616, L1A, 3480R KS-20616, L1A, 1KQ KS-20616, L1A, 3480R

APP FIG. 7
(J1P023AM: LIST 2)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
			SWU2	004-162	4A4	LMPQ05CAXX	SN423 AG
				004-154		LMPQ05CAXX	SN423
				004-170		LMPQ05CAXX	SN423

APP FIG. 8
(J1P023AM: LIST 2)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
M	SWU3		-5.1B	004-114	1E2	PWP054CA	495FB LB
			+5.1B	004-114	1E2	PWP022A	496A LB

APP FIG. 9
(J1P023AM: LIST 3)

PACK. CIRCUIT	OPTION	DESIG	EQPT LOC	FS LOC	CLEI CODE	CODE	STOP CODE
			SWU3	004-170	4A4	LMPQ05CAXX	SN423 AG
				004-162		LMPQ05CAXX	SN423
				004-154		LMPQ05CAXX	SN423

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

DWG SIZE: 65
ISSUE: 15A

AT&T BELL LABORATORIES SD -2P077-01
SHELL CI

A
B
C
D
E
F
G
H

A
B
C
D
E
F
G
H

CIRCUIT NOTES:

101.

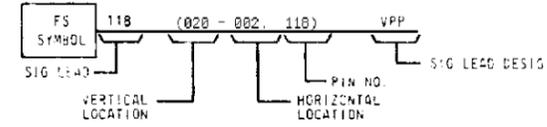
DESIG	FUSE AMP	POTENTIAL	ONE PER
F1	5	-48V	CIRCUIT
F2	2	-48V	CIRCUIT
F3	2	-48V	CIRCUIT
F4	5	-48V	CIRCUIT
F5	5	-48V	CIRCUIT
F6	5	-48V	CIRCUIT
F7	0.5	-48V	CIRCUIT
F8	0.5	-48V	CIRCUIT
F9	0.5	-48V	CIRCUIT

F1	GRD	CIRCUIT
F2	GRD	CIRCUIT
F3	GRD	CIRCUIT
F4	GRD	CIRCUIT
F5	GRD	CIRCUIT
F6	GRD	CIRCUIT
F7	GRD	CIRCUIT
F8	GRD	CIRCUIT
F9	GRD	CIRCUIT

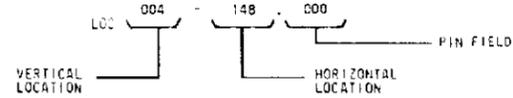
BATTERY SYMBOL	VOLTAGE RANGE
-48	-43.2 To -52.8

EQUIPMENT NOTES:

201. SIGNAL LEADS REFERENCING THIS NOTE ARE PAIRED WITH INDIVIDUAL GROUND LEADS. THE TERMINAL NUMBER CLOSEST TO THE CIRCUIT PACK IS THE SIGNAL LEAD. THE GROUND LEAD IS CONNECTED TO THE TERMINAL NUMBER SHOWN IN PARENTHESES.



202. ON ALL SHEETS THE LOCATION OF THE APPARATUS IS AS SHOWN.



203. UNLESS OTHERWISE SPECIFIED, ALL WIRE SHALL BE 26 GAUGE. ALL 14, 16, 18, AND 22 GAUGE WIRE SHALL BE STRANDED.

204. ALL TIP AND RING LEADS SHALL BE PAIRED.

205. THE QUIET GROUND SYSTEM CONSISTS OF A NO. 16 GAUGE INSULATED WIRE CONNECTED BETWEEN THE OCTU (LOC 004-037) AND 5 ESS GROUND BAR.

206. DS WIRING TO BE RUN USING TYPE BY, 26 GAUGE WITH ONE RIGHT ANGLE TURN, EACH RUN STARTING IN THE HORIZONTAL DIRECTION.

207. KEYING ARRANGEMENTS FOR THE CONTROL UNIT BACKPLANE (ED-2P070-30). THIS IS TO PREVENT POWER SUPPLIES AND CIRCUIT PACKS FROM BEING PLUGGED INTO THE WRONG POSITION.

CIRCUIT	EUL	BACKPLANE KEYCODE	FIVE KEY POSITIONS
495A	004-C42	2B1LB	0-1-5-7-9
494E	004-050	2b1LQ	0-1-5-8-9
494E	004-058	2B1LA	0-1-5-8-9
495D	004-074	2B1LE	0-1-5-6-8
495D	004-090	2B1LS	0-1-5-6-8
495A	004-114	2B1LQ	0-1-5-7-9
SN422	004-C10	2B1AP	4-5-6-7-8
MC2P004A3B	004-018	2B1AH	3-5-7-8-9
SN423	004-154	2B1AG	3-6-7-8-9
SN423	004-162	2B1AQ	3-6-7-8-9
SN423	004-170	2B1AS	3-6-7-8-9

208. WIRING TO BE RUN BY AN INSTALLER IS SPECIFIED IN AT&T TECHNOLOGIES DRAWING T-2P077-31.

209. UNLESS OTHERWISE SPECIFIED, ALL STANDARD WIRE SHOULD BE CRIMPED TO TERMINALS (41098 FASTON TYPE) AND THEN THE CONNECTION SOLDERED BEFORE MOUNTING TO "E" NUMBERED (221C TYPE) LUGS, (SEE CADS 1-7, 12-14).

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DIRECTLY CONNECTED TEST UNIT
CIRCUIT

DWG SIZE
65

ISSUE
15A

AT&T
BELL LABORATORIES

SD -2P077-01

SHEET
D1

INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS.
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.

FEATURE OR OPTION	PROVIDE		
	APP FIG.	APP OR WRG	QUANTITY
SYSTEM TO TEST 10,000 SUBSCRIBER LINES (4 PORTS, 1 PMU)	1.2, 3.4, 5		1 PER CKT
PMU1 & 4 PORTS TO TEST 40,000 ADDITIONAL	3.6, 7.8	Z	1 PER CKT
PMU2 & 4 PORTS TO TEST 50,000 ADDITIONAL LINES	3.6, 9	Z	1 PER CKT
5 ESS WITH GENERIC 5E2 OR HIGHER		J	1 PER CKT
5 ESS WITH GENERICS PR OR TO 5E2		K	1 PER CKT

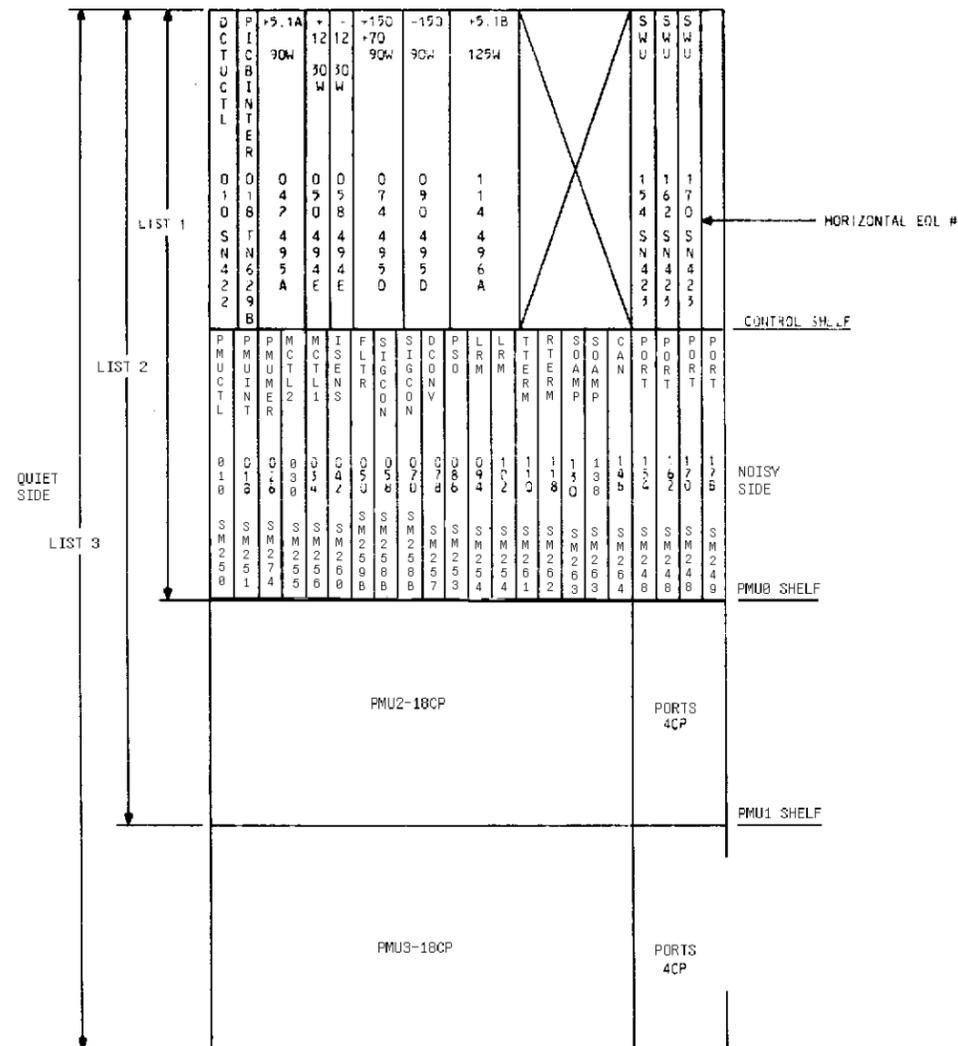
RECORD OF FIGURES, WIRING AND APPARATUS CHANGES						
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT		
				STD	A&M	MD
4B	Y	X	304	Y	X	
5B	Q OR R	R	305	Q		R
6A	V OR W	W	308	V		W
6A	S OR T	T	308	S		T
8B	M OR N	N	306	M		N
13AC	J OR K	K	312	J	K	
				AVAIL		DA
15A			313			

304. TO PROVIDE THE DCTU FLOATING POINT CAPABILITY, PER 5 ESS REQUEST. IT WAS NECESSARY TO MAKE CHANGES ON MC2P004A1 (TN629). THESE CHANGES CREATED A NEW RELEASE OF THIS CIRCUIT PACK, MC2P004A1B (TN629B) WHICH IS THE STANDARD.
MC2P004A1 (TN629) WILL BE MANUFACTURE DISCONTINUED.
305. TO PROVIDE THE DCTU WITH A CIRCUIT PACK WHICH HAS AN INCREASED RESISTANCE RANGE WHICH DIAL TONE CAN BE DRAWN. IT WAS NECESSARY TO MAKE CHANGES ON SM262.
SM262B WILL BECOME-STD
SM262 WILL BECOME-MD
306. POWER UNITS 495A, 496A, 494E ARE BEING MANUFACTURED DISCONTINUED. THEY WILL BE REPLACED BY 495FB, 495FB, AND 494MA RESPECTIVELY WHICH WILL BECOME THE STANDARD.

INFORMATION NOTES (CONT):

307. TO PROVIDE THE DCTU WITH THE CAPACITY OF BEING MOUNTED IN A 5ESS 6 FOOT HIGH SINGLE BAY FRAME (ED-50184-70) IT WAS NECESSARY FOR AT&T BL-WH TO DESIGN A BRACKET (L531169) FOR THE PMU SHELVES AT&T BL-IH DESIGNED THE MOUNTING BRACKET AND SUPPORT BAR FOR THE CONTROL SHELF.
308. TO PROVIDE THE DCTU WITH SOFTWARE CONTROLLED SATURATION DETECTION ON THE SIGCON CIRCUIT PACK, PER 5ESS REQUEST. IT WAS NECESSARY TO MAKE CHANGES ON SM258 AND SM259. SM258A AND SM259B WILL BECOME THE STANDARD AND SM258 AND SM259 WILL BECOME MANUFACTURE DISCONTINUED.

309. DCTU PHYSICAL ARRANGEMENTS (FRONT VIEW)



- NOTES:
1. 5.1A IS FOR CONTROL AND PMU2 SHELVES.
2. 5.1B IS FOR PMU1 AND PMU3 SHELVES.

INFORMATION NOTES: (CONT)

310. TO PERMIT USE OF A SM262B IN A DCTU, ADD 4W STRAPS FOR -48V AND B-3RD ON THE PMU SHELF BACKPLANE.
311. TO COMPLY WITH 5ESS STANDARDS ALL PMU NUMBERS WILL CHANGE FROM PMU1, PMU2, PMU3 TO PMU0, PMU1, PMU2. THIS CHANGE ONLY AFFECTS THE SD-2P077-01.
312. OPTION ① PROVIDES THE PRODUCT CODES NECESSARY FOR IMLT2 TESTING. THIS FEATURE ALLOWS THE ARSB TO PERFORM MLT TESTING DIRECTLY OVER A DATA LINK USING AN INTEGRATED DCTU IN A 5ESS OFFICE. OPTION ② IS TO BE APPLIED ONLY TO DCTU'S CONNECTED TO 5ESS SWITCHES THAT ARE RUNNING UNDER GENERIC 5E2(1) OR HIGHER SOFTWARE. THE SOFTWARE MUST BE INSTALLED BEFORE OPTION ① IS APPLIED. OPTION ③ IS TO BE APPLIED IN ALL OTHER CASES AND SHALL BE RATED 4W ONLY.
313. PRIOR TO ISSUE 15A, COLUMNS HEADED "STD", "MD", ETC., CONVEYED APPLICATION INFORMATION. AT ISSUE 15A, COLUMNS HEADED "AVAIL" AND "DA" NOW INDICATE THE AVAILABILITY OF THE PRODUCT.

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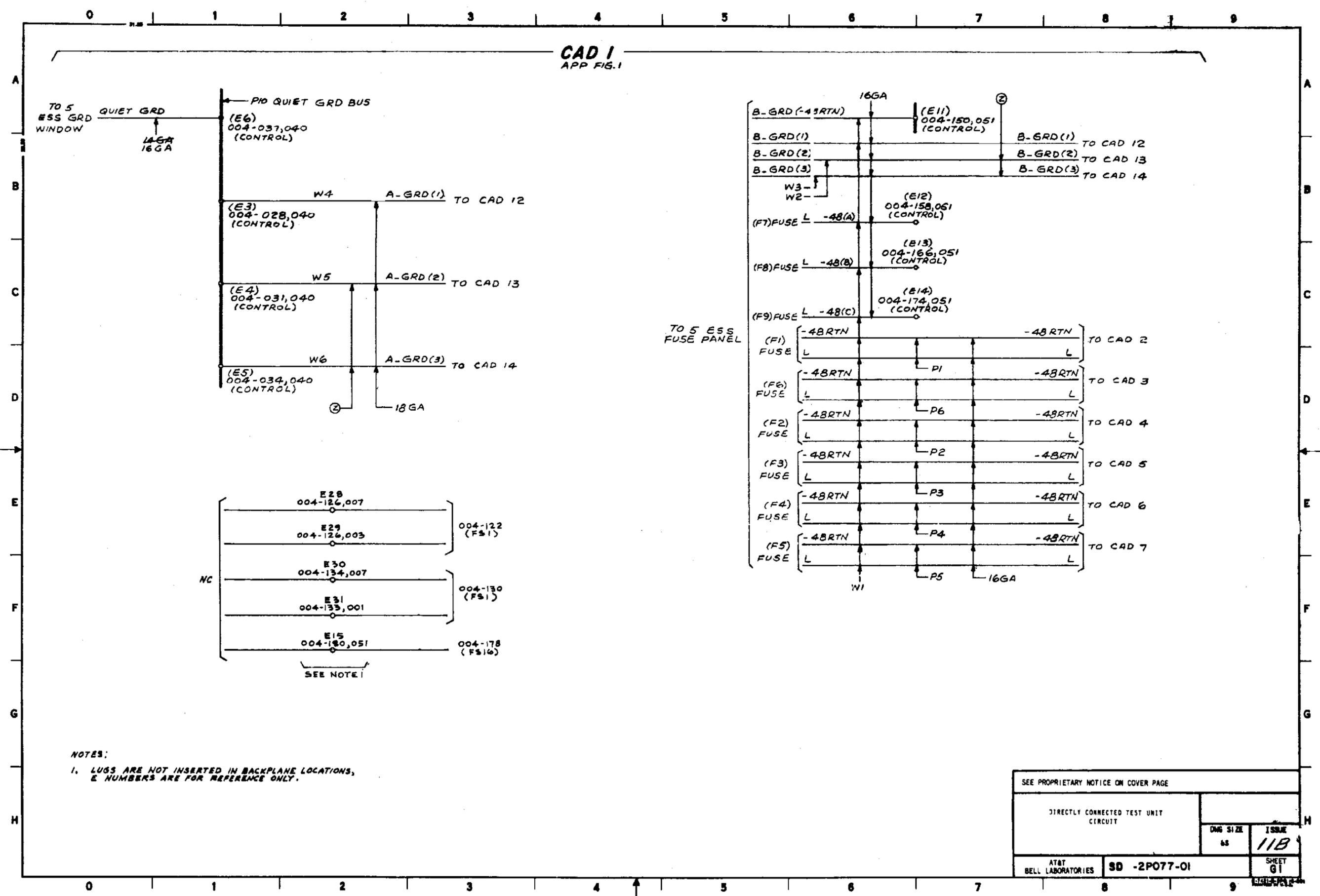
DIRECTLY CONNECTED TEST UNIT
CIRCUIT

DWG SIZE: 65
ISSUE: 15A

AT&T BELL LABORATORIES
SD -2P077-01

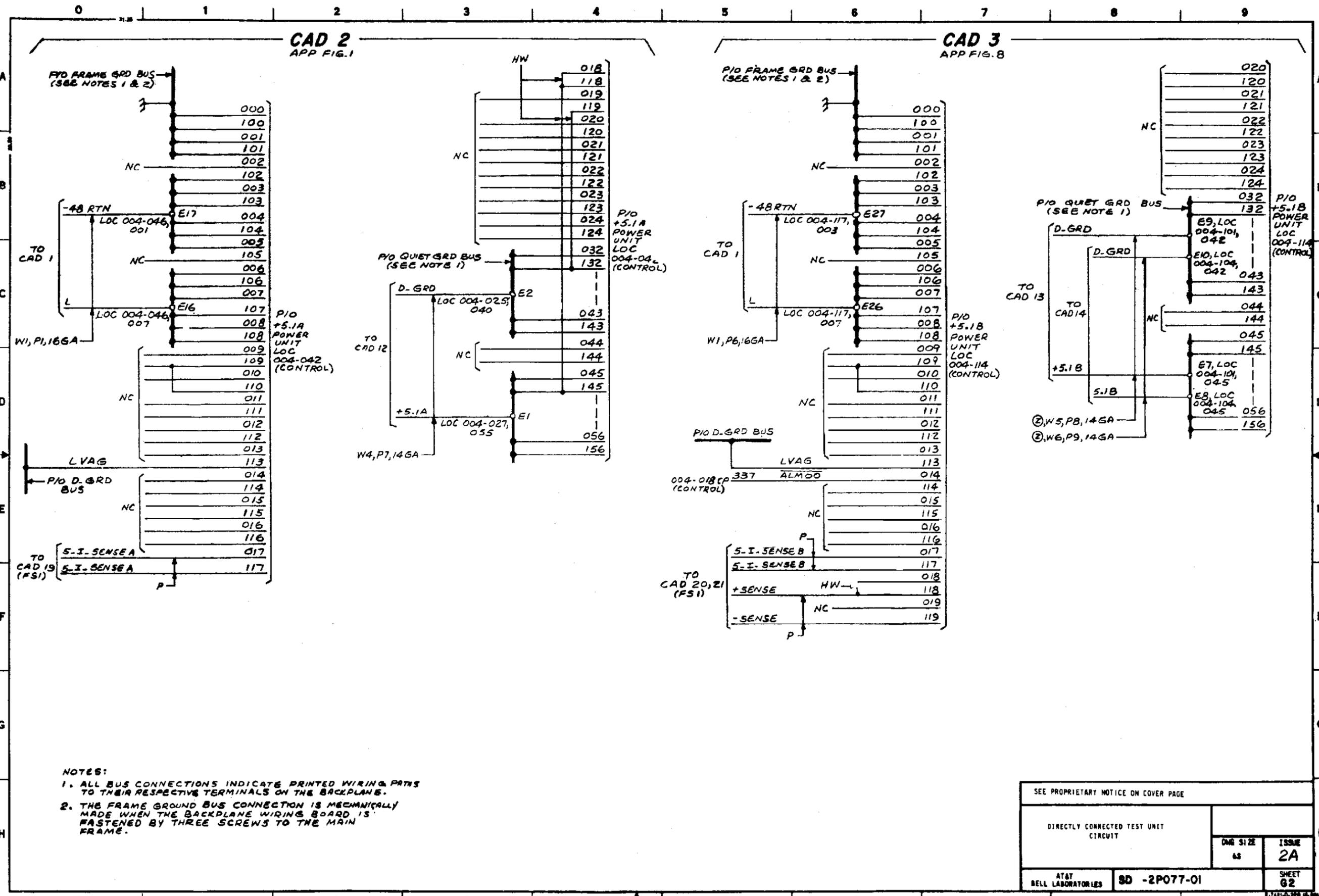
SHEET: 03

CAD 1
APP FIG. 1



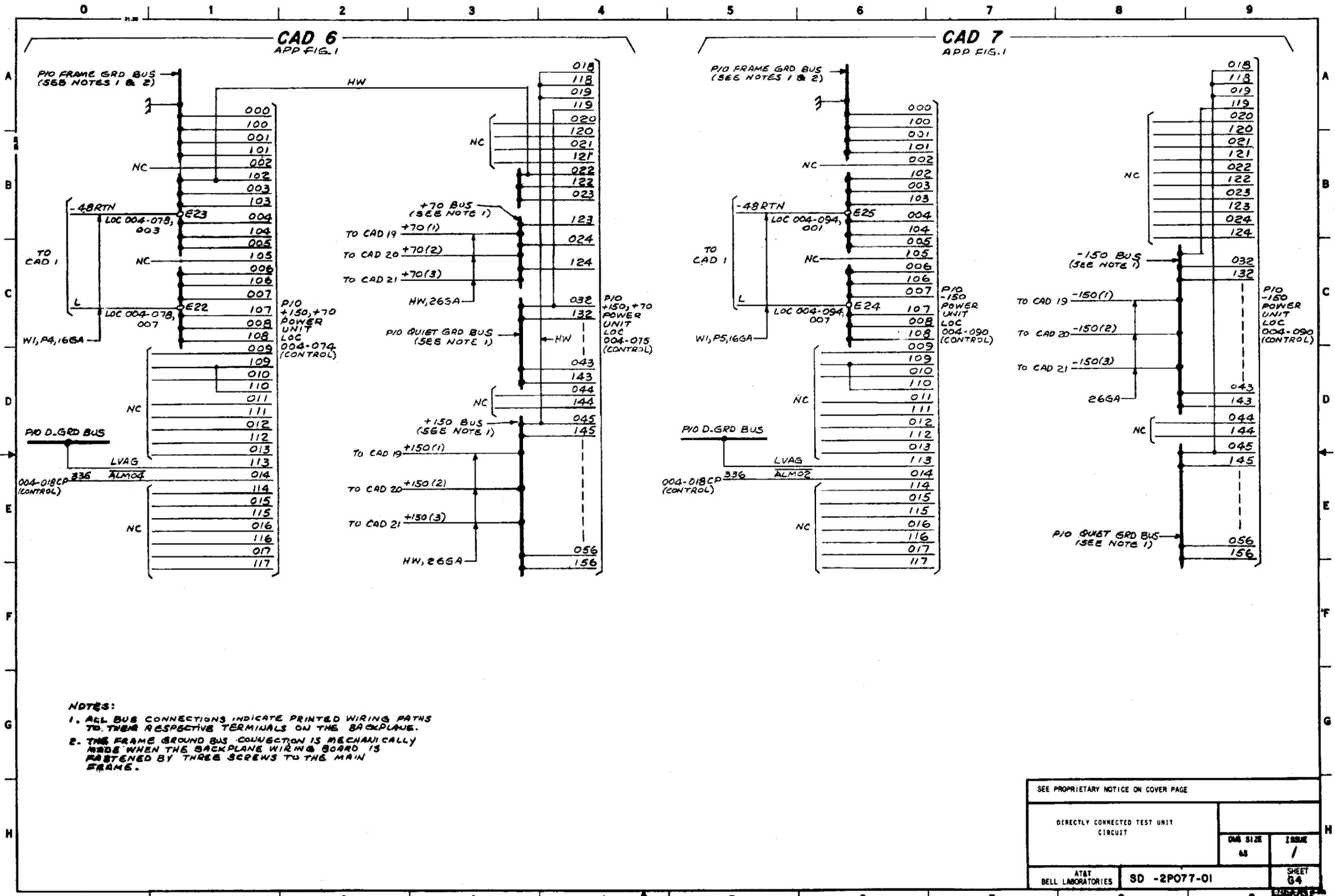
NOTES:
1. LUGS ARE NOT INSERTED IN BACKPLANE LOCATIONS, E NUMBERS ARE FOR REFERENCE ONLY.

SEE PROPRIETARY NOTICE ON COVER PAGE	
DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWG SIZE 65
AT&T BELL LABORATORIES	ISSUE 11B
SD -2P077-01	SHEET G1

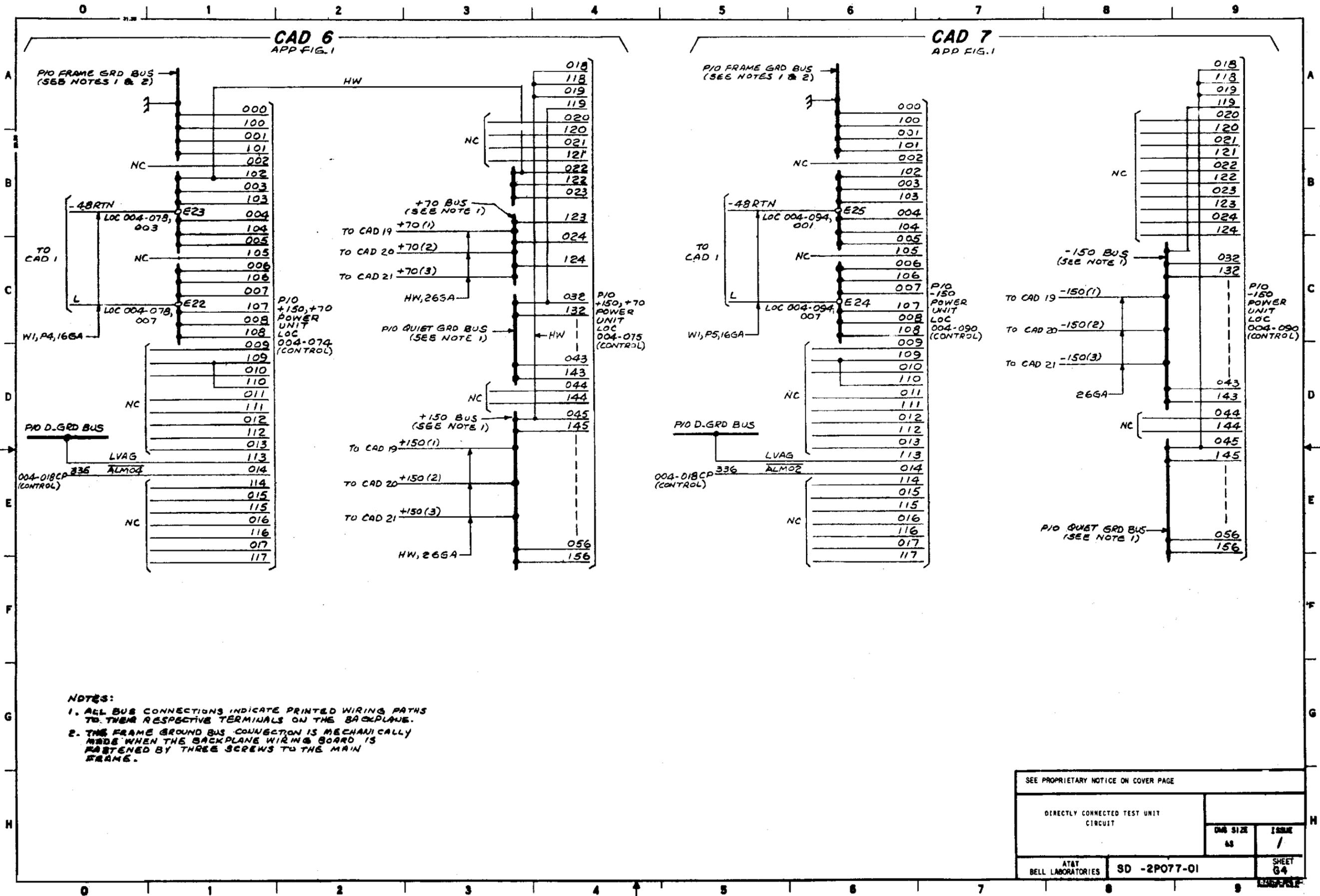


NOTES:
 1. ALL BUS CONNECTIONS INDICATE PRINTED WIRING PATHS TO THEIR RESPECTIVE TERMINALS ON THE BACKPLANE.
 2. THE FRAME GROUND BUS CONNECTION IS MECHANICALLY MADE WHEN THE BACKPLANE WIRING BOARD IS FASTENED BY THREE SCREWS TO THE MAIN FRAME.

SEE PROPRIETARY NOTICE ON COVER PAGE		
DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWG SIZE	ISSUE
	4S	2A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 02



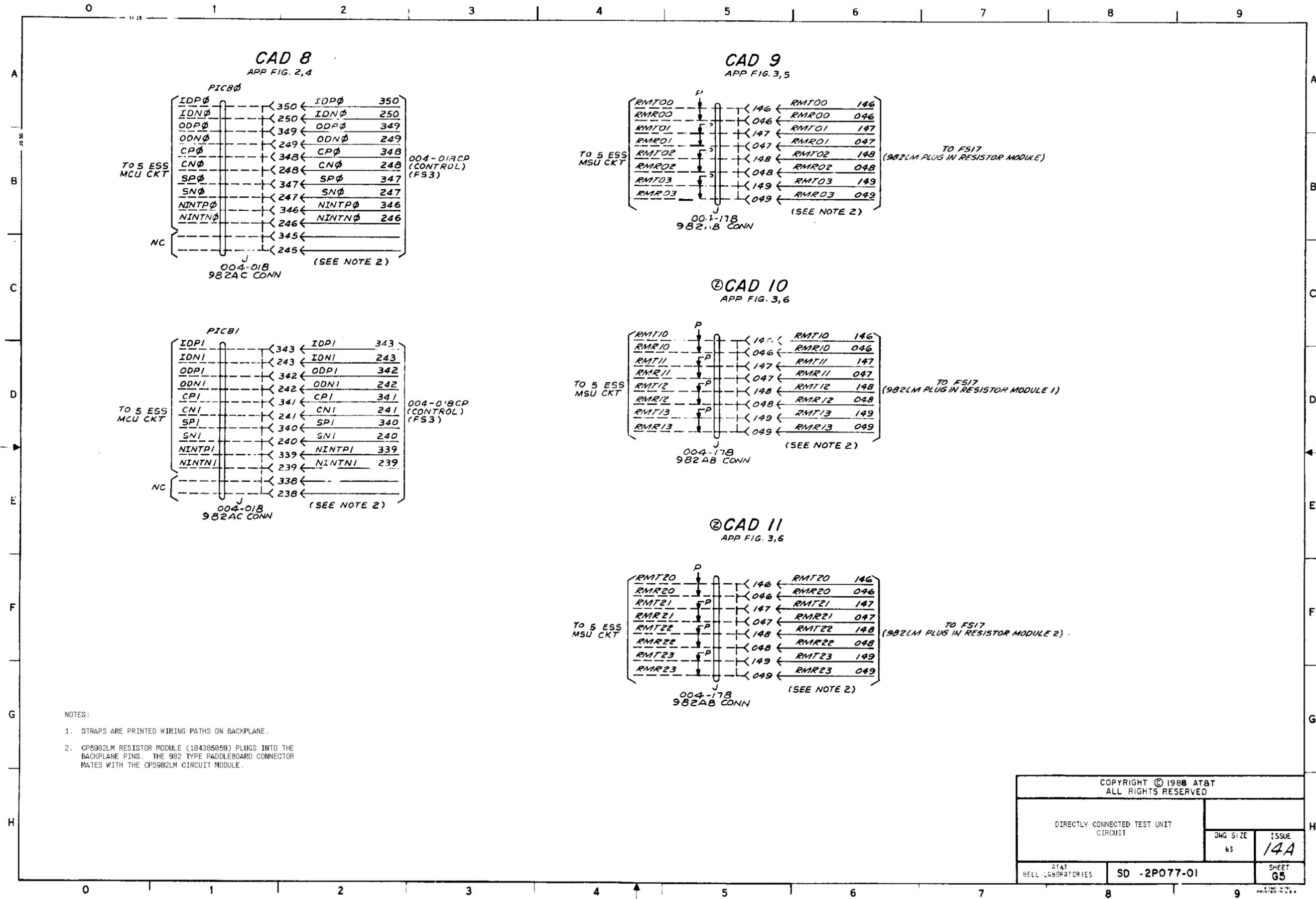
SEE PROPRIETARY NOTICE ON COVER PAGE		
DIRECTLY CONNECTED TEST UNIT CIRCUIT		DATE /
AT&T BELL LABORATORIES		SD -2P077-01
		SHEET 64



NOTES:

1. ALL BUS CONNECTIONS INDICATE PRINTED WIRING PATHS TO THEIR RESPECTIVE TERMINALS ON THE BACKPLANE.
2. THE FRAME GROUND BUS CONNECTION IS MECHANICALLY MADE WHEN THE BACKPLANE WIRING BOARD IS FASTENED BY THREE SCREWS TO THE MAIN FRAME.

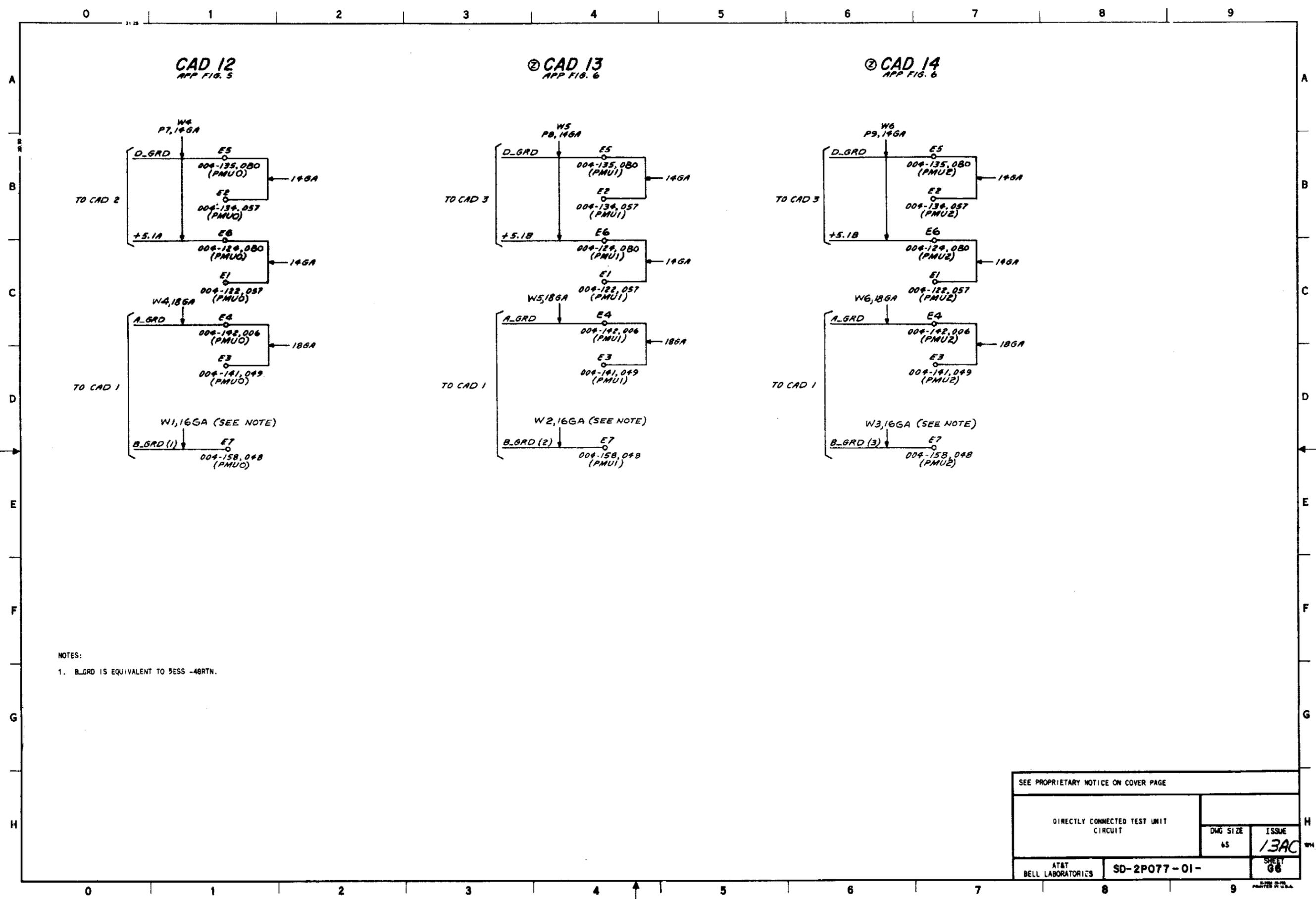
SEE PROPRIETARY NOTICE ON COVER PAGE			
DIRECTLY CONNECTED TEST UNIT CIRCUIT		DRG SIZE	ISSUE
		AS	/
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 64	



NOTES:

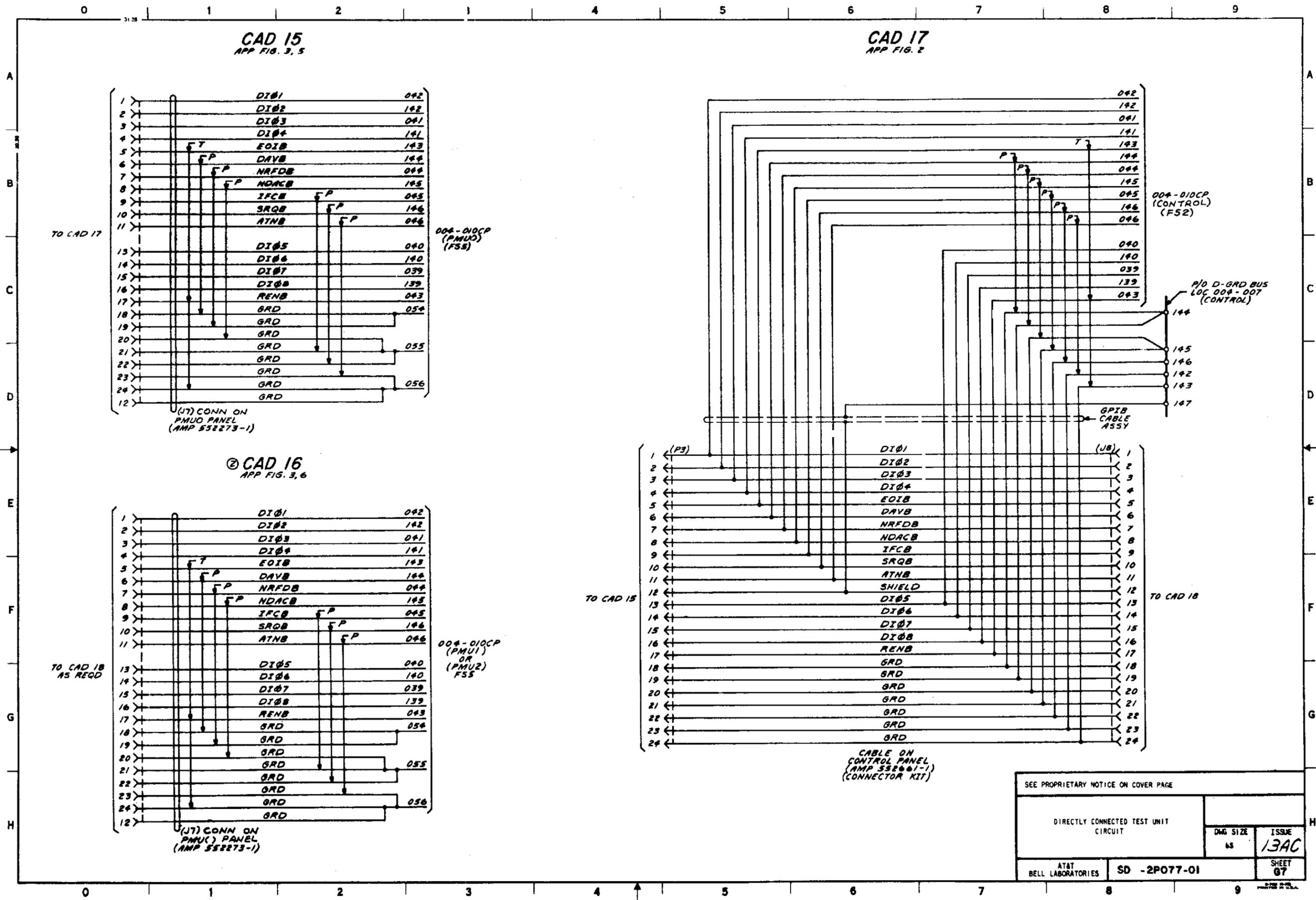
- STRAPS ARE PRINTED WIRING PATHS ON BACKPLANE.
- CP5982LM RESISTOR MODULE (184385859) PLUGS INTO THE BACKPLANE PINS. THE 982 TYPE PADDLEBOARD CONNECTOR MATES WITH THE CP5982LM CIRCUIT MODULE.

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DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWG SIZE	ISSUE
	65	14A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 65



NOTES:
 1. B_GRD IS EQUIVALENT TO 3ESS -48RTN.

SEE PROPRIETARY NOTICE ON COVER PAGE		
DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 65
AT&T BELL LABORATORIES		ISSUE 13AC SHEET 66
SD-2P077-01-		



CAD 15
APP FIG. 3, 5

CAD 17
APP FIG. 2

CAD 16
APP FIG. 3, 6

TO CAD 17

004-DIOCP
(PMU2)
(F55)

004-DIOCP
(CONTROL)
(F52)

P/O D-GRD BUS
LOC 004-007
(CONTROL)

(J7) CONN ON
PMU0 PANEL
(AMP 552273-1)

GP1B
CABLE
ASSY

TO CAD 15

TO CAD 18

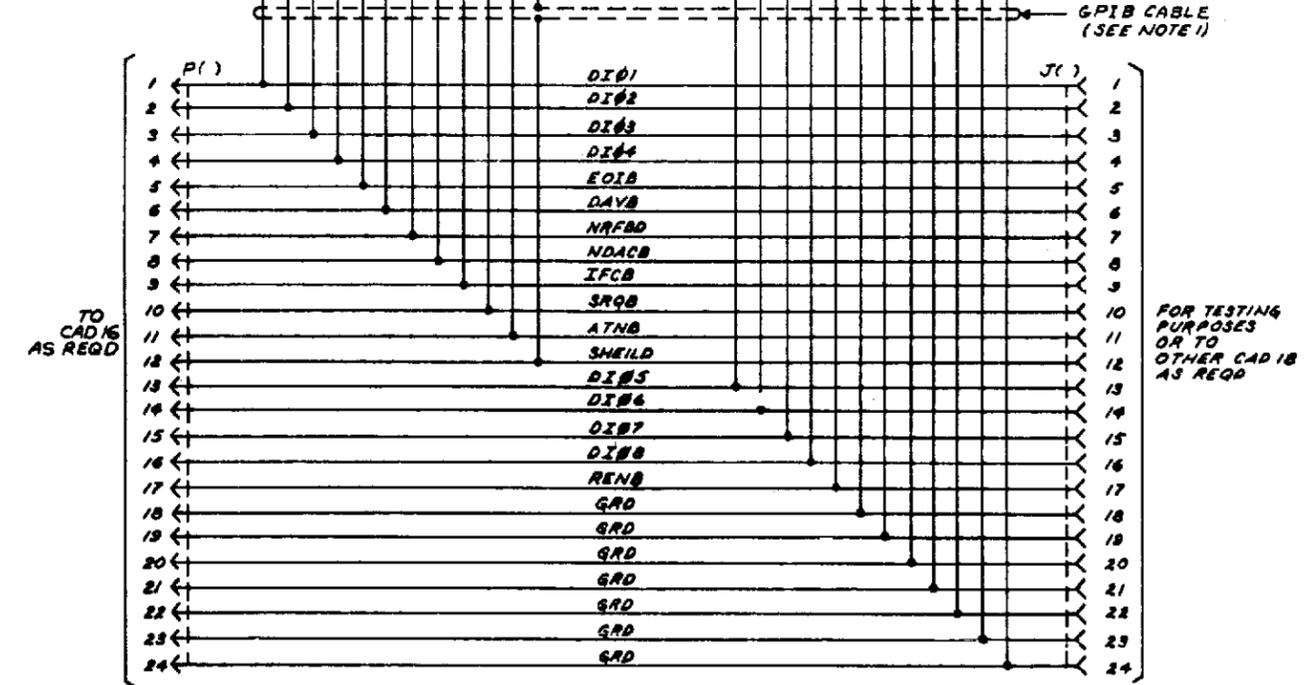
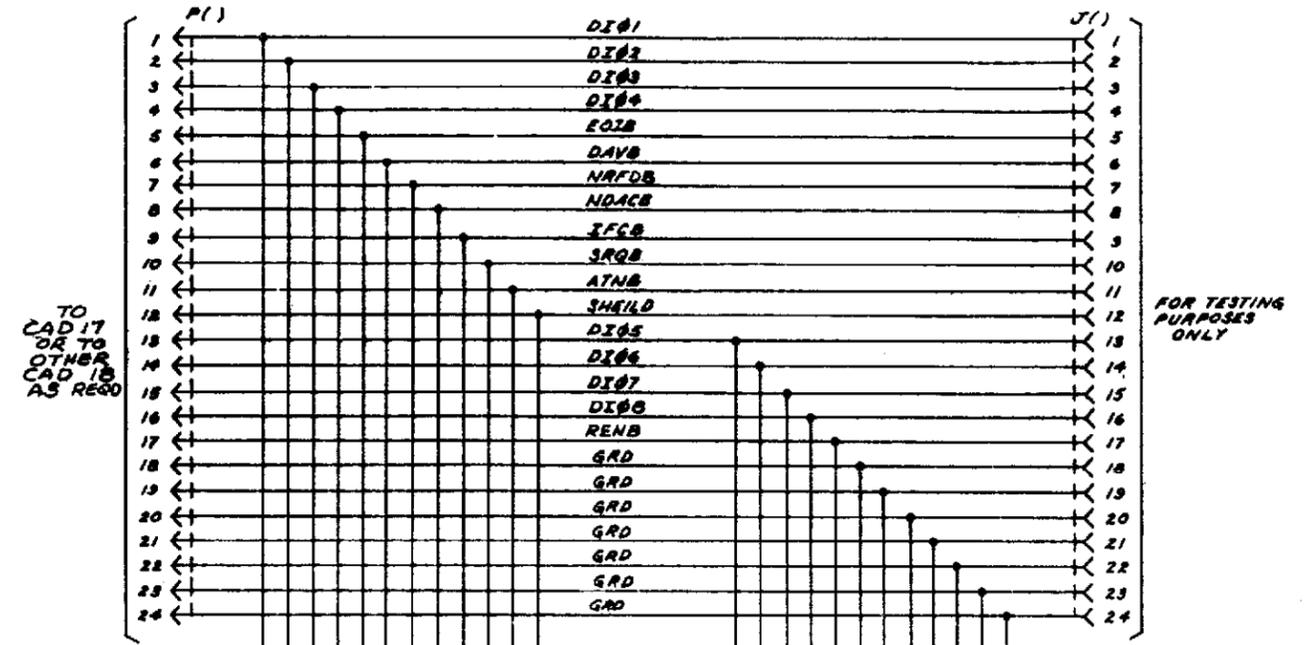
TO CAD 18
AS REQD

004-DIOCP
(PMU1)
OR
(PMU2)
F55

CABLE ON
CONTROL PANEL
(AMP 552001-1)
(CONNECTOR KIT)

SEE PROPRIETARY NOTICE ON COVER PAGE			
DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE 45	ISSUE 13AC
AT&T BELL LABORATORIES		SD -2P077-01	SHEET 07

② CAD 18
APP FIG. 5, 6

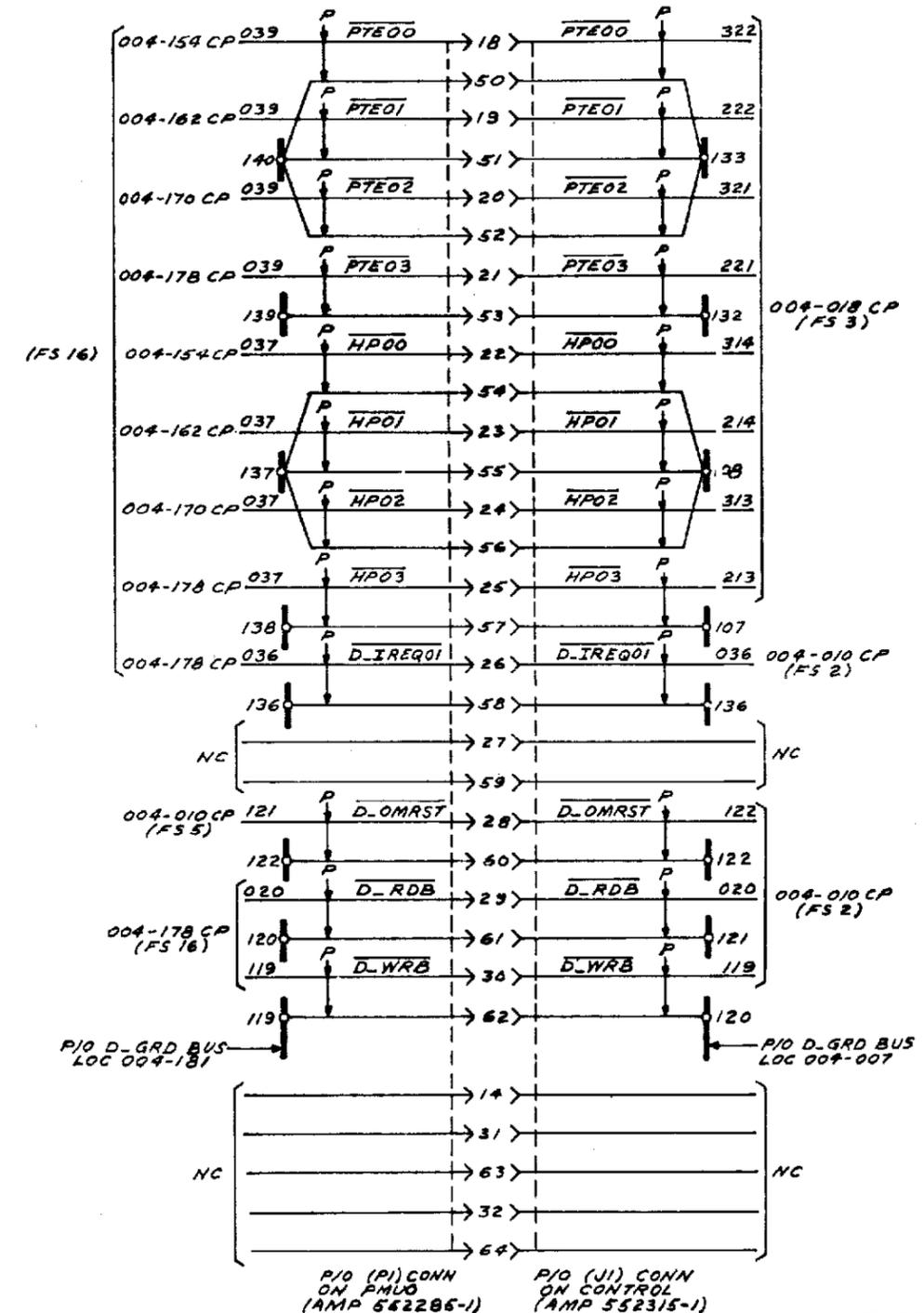
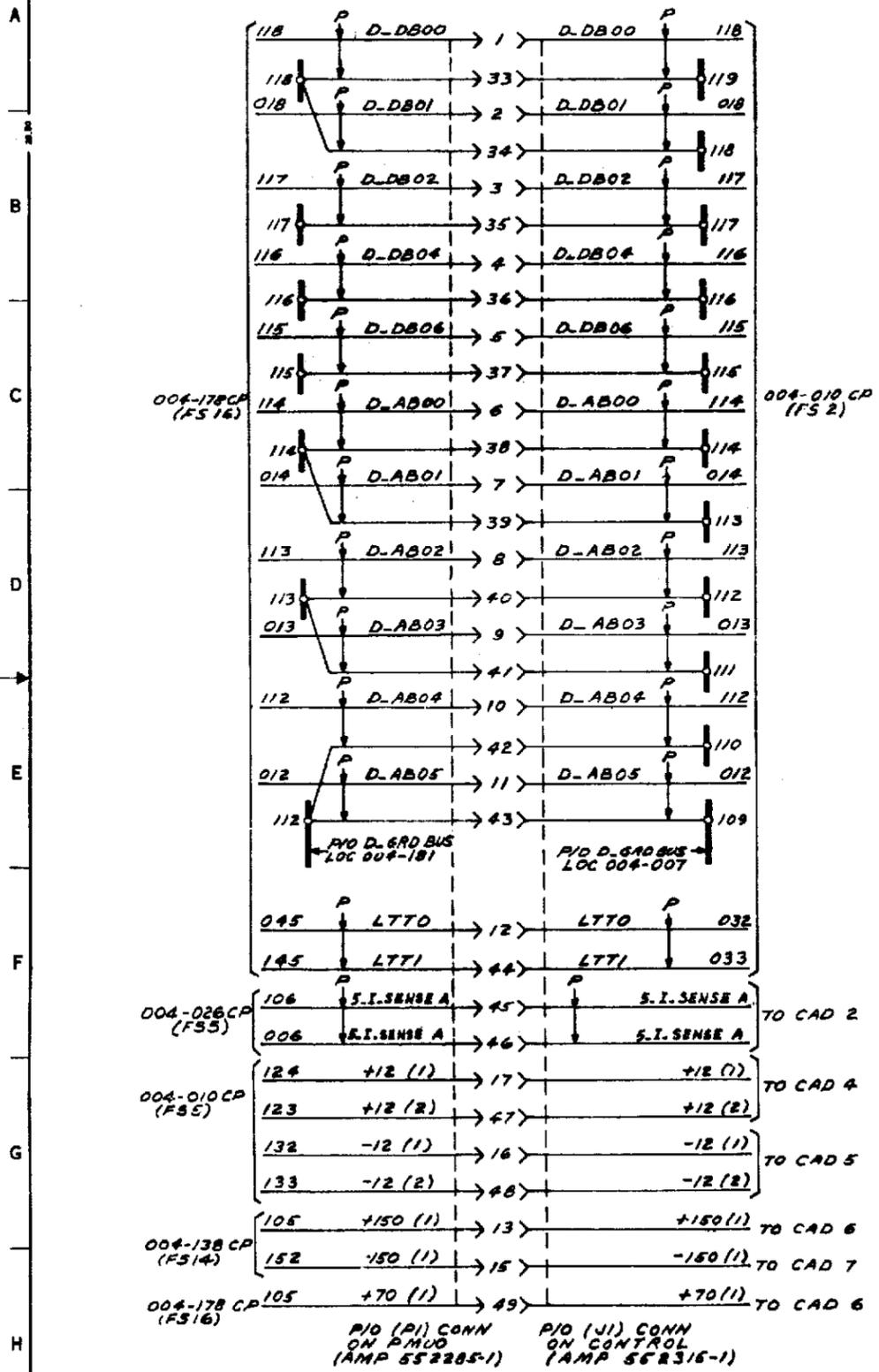


NOTES:
1. THE FOLLOWING DESIGNATIONS SHALL BE STAMPED ON THE CONNECTORS:

CAD	LOC	PLUG	CONNECTOR	GROUP NO.
1ST CAD 18	TOP	P4	J9	3
	BOTTOM	P5	J10	
2ND CAD 18	TOP	P6	J11	4
	BOTTOM	P7	J12	

SEE PROPRIETARY NOTICE ON COVER PAGE			
DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	2A
AT&T BELL LABORATORIES		SD -2P077-01	SHEET 08

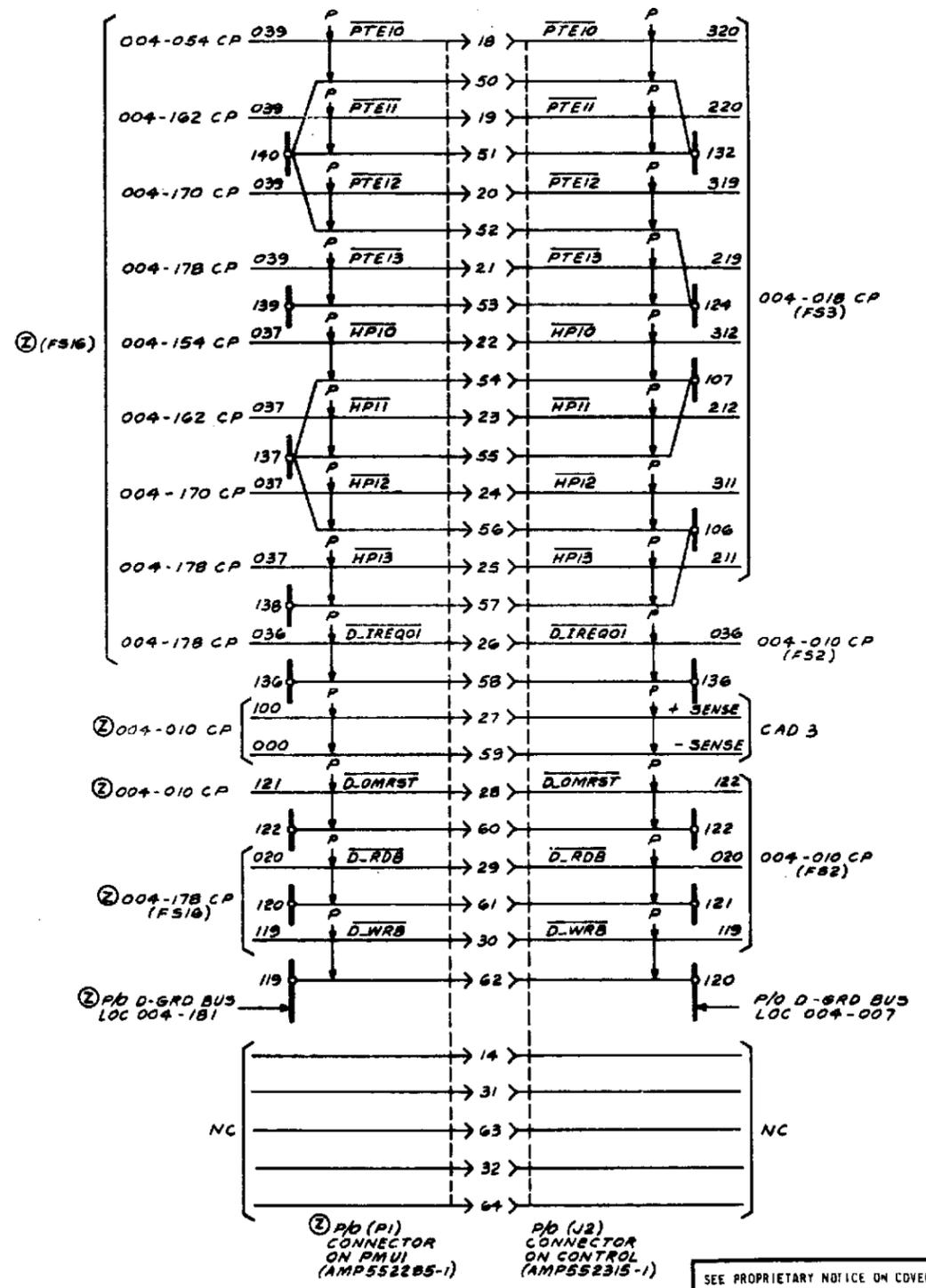
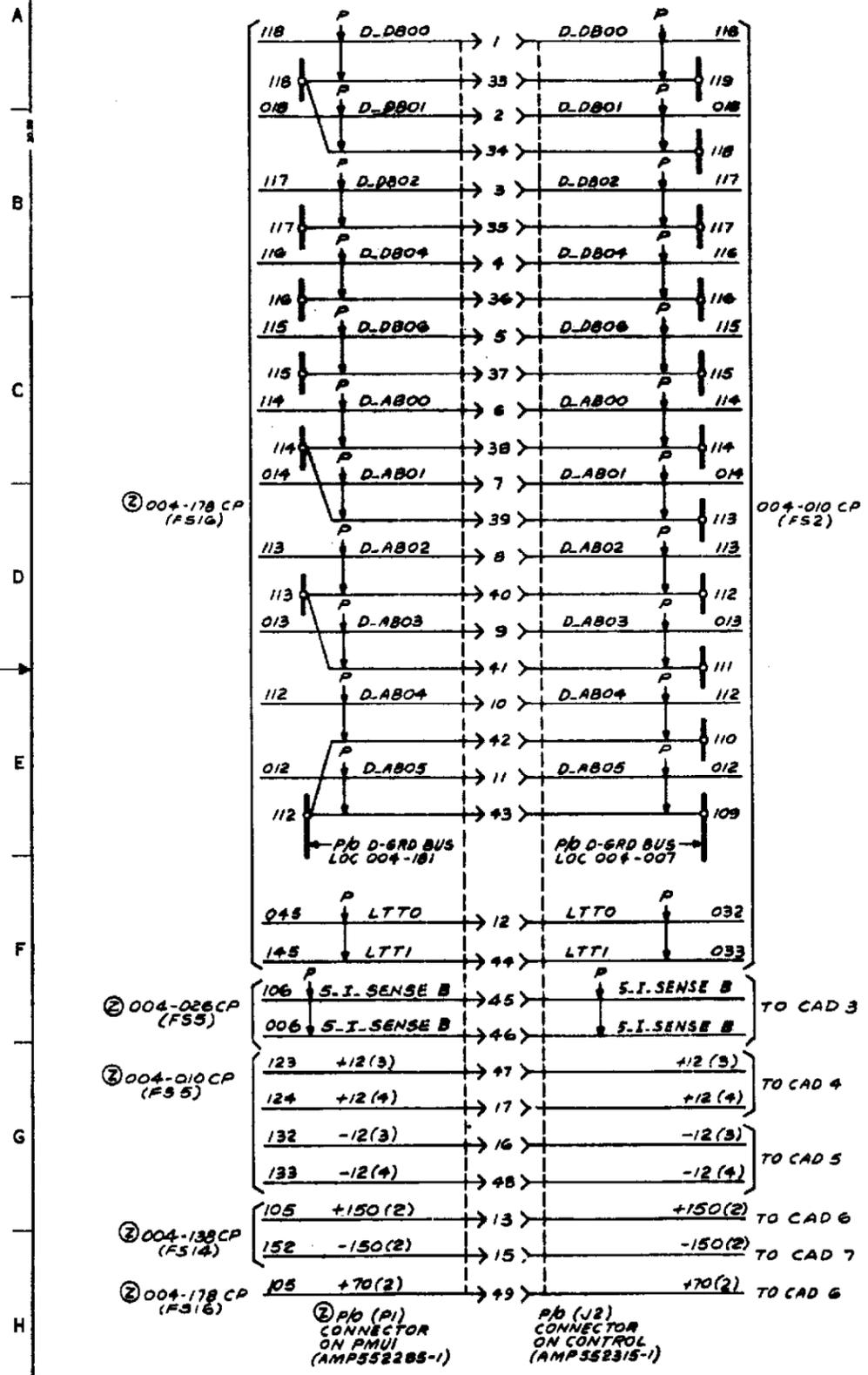
CAD 19
APP FIG. 2, 3, 5
QUIET SIDE



SEE PROPRIETARY NOTICE ON COVER PAGE

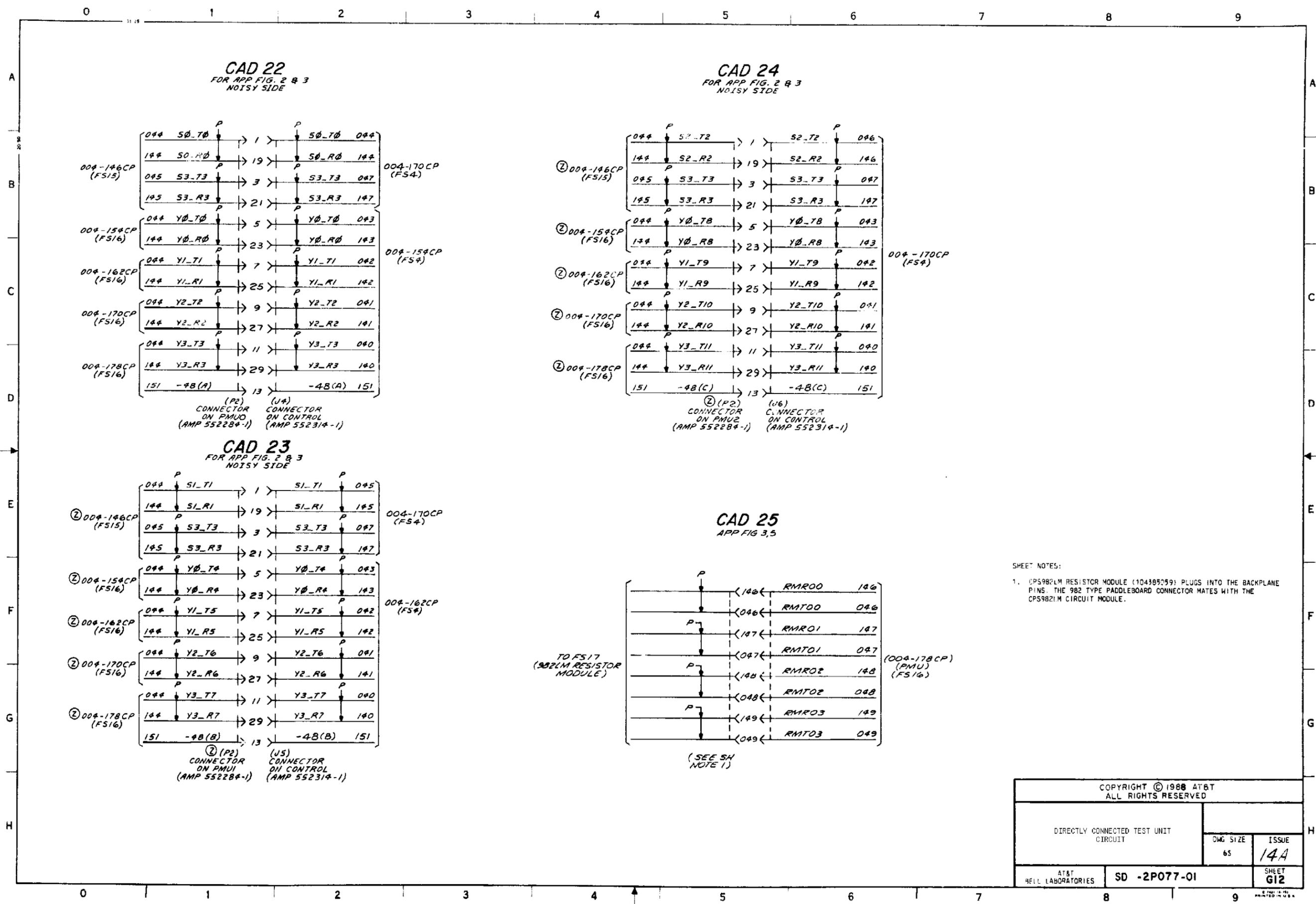
DIRECTLY CONNECTED TEST UNIT CIRCUIT		OMG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 69	

CAD 20
APP FIG. 2, 3, & 6
QUIET SIDE



SEE PROPRIETARY NOTICE ON COVER PAGE

DIRECTLY CONNECTED TEST UNIT CIRCUIT		DWG SIZE	ISSUE
		65	13AC
AT&T BELL LABORATORIES	SD -2P077-01	SHEET 610	



CAD 22
FOR APP FIG. 2 & 3
NOISY SIDE

CAD 24
FOR APP FIG. 2 & 3
NOISY SIDE

CAD 23
FOR APP FIG. 2 & 3
NOISY SIDE

CAD 25
APP FIG 3,5

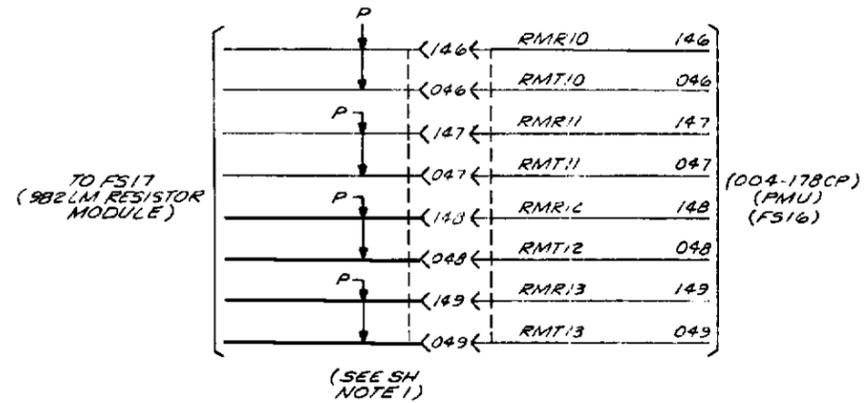
SHEET NOTES:
1. CPS982LM RESISTOR MODULE (104385259) PLUGS INTO THE BACKPLANE PINS. THE 982 TYPE PADDLEBOARD CONNECTOR MATES WITH THE CPS982LM CIRCUIT MODULE.

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DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWG SIZE 65	ISSUE 14A
AT&T BELL LABORATORIES	SD -2P077-01	SHEET G12

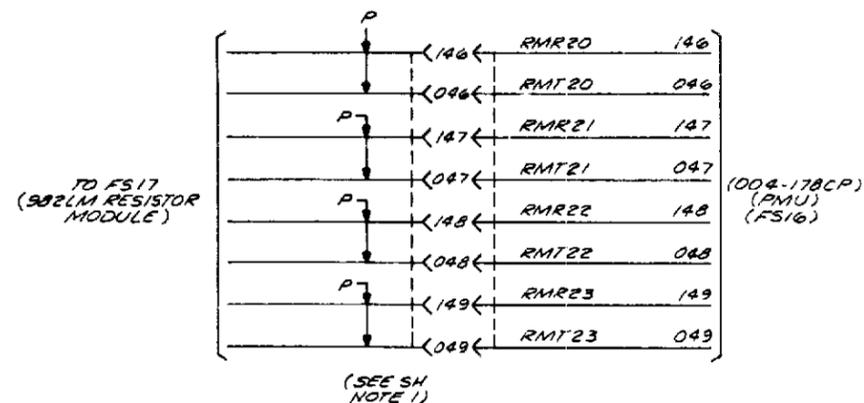
0 1 2 3 4 5 6 7 8 9

A
B
C
D
E
F
G
H

② CAD 26
APP FIG. 3,6



② CAD 27
APP FIG. 3,6



SHEET NOTES:
1. CPS982LM RESISTOR MODULE (1104385059) PLUGS INTO THE BACKPLANE PINS. THE 982 TYPE PADDLEBOARD CONNECTOR MATES WITH THE CPS982LM CIRCUIT MODULE.

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DIRECTLY CONNECTED TEST UNIT CIRCUIT	DWG SIZE	ISSUE
	8S	14A
AT&T BELL LABORATORIES	SD-2P077-01	SHEET G13

0 1 2 3 4 5 6 7 8 9