OPTION INDEX

APP OR WRG	RATED ON ISSUE	REF NOTES	LOCATION

DWG ISS	CD ISS	DATE ISSD	DRN	APP
1	1 APPX –	7-29-93		
2B	1 APPX 1B	10-11-95		

SUPPORTING INFORMATION

SYSTEM USED ON	DESIGN CONTROL	CATEGORY	NO.
3B21D	IH	EQUIPMENT DRAWING	J3T061A-1

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

RN98

COMMON SYSTEMS

3B21D PROCESSOR
COMPUTER SYSTEMS
CIRCUIT

DWG SIZE C2 | ISSUE 2B

AT&T | SD-3T015-01 | SHEET A1 50

PRINTED IN U.S.A

DESIGNATION MNEMONICS

MNEMONIC	LOC	DEFINITION
0C0CLK0[N,P]	B4D5	DMAC 0: CH11 DEV0 DSCH TRANSMIT CLOCK
0C0CLK1[N,P]	B5D7	DMAC 0: CH11 DEV1 DSCH TRANSMIT CLOCK
0C0CLK2[N,P]	B3D5	DMAC 0: CH11 DEV2 DSCH TRANSMIT CLOCK
0C0DAH0[N,P]	B4D5	DMAC 0: CH11 DEV0 DSCH DATA HIGH BYTE
0C0DAH1[N,P]	B5D7	DMAC 0: CH11 DEV1 DSCH DATA HIGH BYTE
0C0DAH2[N,P]	B3D5	DMAC 0: CH11 DEV2 DSCH DATA HIGH BYTE
0C0DAL0[N,P]	B4D5	DMAC 0: CH11 DEV0 DSCH DATA LOW BYTE
0C0DAL1[N,P]	B5D7	DMAC 0: CH11 DEV1 DSCH DATA LOW BYTE
0C0DAL2[N,P]	B3D5	DMAC 0: CH11 DEV2 DSCH DATA LOW BYTE
0C0REQ0[N,P]	B4D5	DMAC 0: CH11 DEV0 DSCH INTERRUPT
0C0REQ1[N,P]	B5D7	DMAC 0: CH11 DEV1 DSCH INTERRUPT
0C0REQ2[N,P]	B3D5	DMAC 0: CH11 DEV2 DSCH INTERRUPT
0C0XCK0[N,P]	B4D5	DMAC 0: CH11 DEV0 DSCH RECEIVE CLOCK
0C0XCK1[N,P]	B5D7	DMAC 0: CH11 DEV1 DSCH RECEIVE CLOCK
0C0XCK2[N,P]	B3D5	DMAC 0: CH11 DEV2 DSCH RECEIVE CLOCK
0C2CLK0[N,P]	B4D5	DMAC 0: CH13 DEV0 DSCH TRANSMIT CLOCK
0C2CLK1[N,P]	B5D6	DMAC 0: CH13 DEV1 DSCH TRANSMIT CLOCK
0C2CLK2[N,P]	B3D6	DMAC 0: CH13 DEV2 DSCH TRANSMIT CLOCK
0C2CLK3[N,P]	B6D5	DMAC 0: CH13 DEV3 DSCH TRANSMIT CLOCK
0C2DAH0[N,P]	B4D5	DMAC 0: CH13 DEV0 DSCH DATA HIGH BYTE
0C2DAH1[N,P]	B5D6	DMAC 0: CH13 DEV1 DSCH DATA HIGH BYTE
0C2DAH2[N,P]	B3D6	DMAC 0: CH13 DEV2 DSCH DATA HIGH BYTE
0C2DAH3[N,P]	B6D5	DMAC 0: CH13 DEV3 DSCH DATA HIGH BYTE
0C2DAL0[N,P]	B4D5	DMAC 0: CH13 DEV0 DSCH DATA LOW BYTE
0C2DAL1[N,P]	B5D6	DMAC 0: CH13 DEV1 DSCH DATA LOW BYTE
0C2DAL2[N,P]	B3D6	DMAC 0: CH13 DEV2 DSCH DATA LOW BYTE
0C2DAL3[N,P]	B6D5	DMAC 0: CH13 DEV3 DSCH DATA LOW BYTE
0C2REQ0[N,P]	B4D5	DMAC 0: CH13 DEV0 DSCH INTERRUPT
0C2REQ1[N,P]	B5D6	DMAC 0: CH13 DEV1 DSCH INTERRUPT
0C2REQ2[N,P]	B3D6	DMAC 0: CH13 DEV2 DSCH INTERRUPT
0C2REQ3[N,P]	B6D5	DMAC 0: CH13 DEV3 DSCH INTERRUPT
0C2XCK0[N,P]	B4D5	DMAC 0: CH13 DEV0 DSCH RECEIVE CLOCK
0C2XCK1[N,P]	B5D6	DMAC 0: CH13 DEV1 DSCH RECEIVE CLOCK
0C2XCK2[N,P]	B3D6	DMAC 0: CH13 DEV2 DSCH RECEIVE CLOCK
0C2XCK3[N,P]	B6D5	DMAC 0: CH13 DEV3 DSCH RECEIVE CLOCK
3BRST10	B11E7	COOLING UNIT: RESET FAN ALARM FROM CU0
3BRST11	B11D7	COOLING UNIT: RESET FAN ALARM FROM CU1
3BSCAN00	B11E7	COOLING UNIT: FAN ALARM TO CU0
3BSCAN01	B11D7	COOLING UNIT: FAN ALARM TO CU1
BSCAN1-1	B9F4	IOP0 PONL0 INPUT, + PHASE
BSCAN1-10	B9F4	IOP0 TDI INPUT, - PHASE
BSCAN1-2	B9F4	IOP0 TDO OUTPUT, + PHASE
BSCAN1-3	B9F4	IOP0 TMS INPUT, + PHASE
BSCAN1-4	B9F4	IOP0 TCK INPUT, + PHASE
BSCAN1-5	B9F4	IOP0 TDI INPUT, + PHASE
BSCAN1-6	B9F4	IOP0 PONL0 INPUT, - PHASE
BSCAN1-7	B9F4	IOP0 TDO OUTPUT, - PHASE
BSCAN1-8	B9F4	IOP0 TMS INPUT, - PHASE
BSCAN1-9	B9F4	IOP0 TCK INPUT, - PHASE
BSCAN2-1	B9C4	IOP1 PONL0 INPUT, + PHASE
BSCAN2-10	B9C4	IOP1 TDI INPUT, - PHASE
BSCAN2-2	B9C4	IOP1 TDO OUTPUT, + PHASE
BSCAN2-3	B9C4	IOP1 TMS INPUT, + PHASE
BSCAN2-4	B9C4	IOP1 TCK INPUT, + PHASE
BSCAN2-5	B9C4	IOP1 TDI INPUT, + PHASE
BSCAN2-6	B9C4	IOP1 PONL0 INPUT, - PHASE
BSCAN2-7	B9C4	IOP1 TDO OUTPUT, - PHASE
BSCAN2-8	B9C4	IOP1 TMS INPUT, - PHASE
BSCAN2-9	B9C4	IOP1 TCK INPUT, - PHASE
BSCAN3-1	B9F3	IOP2 GROWTH PONL0 INPUT, + PHASE
BSCAN3-10	B9F3	IOP2 GROWTH TDO OUTPUT, - PHASE
BSCAN3-2	B9F3	IOP2 GROWTH TDI INPUT, + PHASE
BSCAN3-3	B9F3	IOP2 GROWTH TMS INPUT, + PHASE
BSCAN3-4	B9F3	IOP2 GROWTH TCK INPUT, + PHASE
BSCAN3-5	B9F3	IOP2 GROWTH TDO OUTPUT, + PHASE
BSCAN3-6	B9F3	IOP2 GROWTH PONL0 INPUT, - PHASE
BSCAN3-7	B9F3	IOP2 GROWTH TDI INPUT, - PHASE
BSCAN3-8	B9F3	IOP2 GROWTH TMS INPUT, - PHASE
BSCAN3-9	B9F3	IOP2 GROWTH TCK INPUT, - PHASE
BSCAN4-1	B9C3	IOP3 GROWTH PONL0 INPUT, + PHASE
BSCAN4-10	B9C3	IOP3 GROWTH TDO OUTPUT, - PHASE
BSCAN4-2	B9C3	IOP3 GROWTH TDI INPUT, + PHASE
BSCAN4-3	B9C3	IOP3 GROWTH TMS INPUT, + PHASE
BSCAN4-4	B9C3	IOP3 GROWTH TCK INPUT, + PHASE
BSCAN4-5	B9C3	IOP3 GROWTH TDO OUTPUT, + PHASE
BSCAN4-6	B9C3	IOP3 GROWTH PONL0 INPUT, - PHASE
BSCAN4-7	B9C3	IOP3 GROWTH TDI INPUT, - PHASE
BSCAN4-8	B9C3	IOP3 GROWTH TMS INPUT, - PHASE
BSCAN4-9	B9C3	IOP3 GROWTH TCK INPUT, - PHASE
CLK000[N,P]	B4D3	IOP: DSCH 0, TRANSMIT CLOCK OUT
CLK010[N,P]	B4D4	IOP: DSCH 1, TRANSMIT CLOCK OUT
CLK210[N,P]	B4D4	IOP0 DSCH 1, TRANSMIT CLOCK OUT
CLKAN	B10D4	MCHL: TRANSMIT CLOCK OUT, - PHASE
CLKAP	B10D3	MCHL: TRANSMIT CLOCK OUT, + PHASE
DAH000[N,P]	B4D3	IOP: DSCH 0, DATA HI BYTES
DAH010[N,P]	B4D4	IOP0 DSCH 1, DATA HI BYTES
DAH010[N,P]	B4D4	IOP: DSCH 1, DATA HI BYTES
DAHAN	B10D4	MCHL: HIGH DATA BYTES, - PHASE
DAHAP	B10D3	MCHL: HIGH DATA BYTES, + PHASE
DAL000[N,P]	B4D3	IOP: DSCH 0, DATA LO BYTES
DAL010[N,P]	B4D4	IOP0 DSCH 1, DATA LO BYTES
DAL010[N,P]	B4D4	IOP: DSCH 1, DATA LO BYTES
DALAN	B10D4	MCHL: LOW DATA BYTES, - PHASE
DALAP	B10D3	MCHL: LOW DATA BYTES, + PHASE.
DFC0-1	B3F3	DFC1 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
DFC0-10	B3F3	DFC1 DSCH 0, INTERRUPT, - PHASE
DFC0-11	B3F4	DFC1 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
DFC0-12	B3F4	DFC1 DSCH 1, RECEIVE CLOCK IN, + PHASE
DFC0-13	B3F4	DFC1 DSCH 1, DATA HI BYTES, + PHASE
DFC0-14	B3F4	DFC1 DSCH 1, DATA LO BYTES, + PHASE
DFC0-15	B3F4	DFC1 DSCH 1, INTERRUPT, + PHASE
DFC0-16	B3F4	DFC1 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
DFC0-17	B3F4	DFC1 DSCH 1, RECEIVE CLOCK IN, - PHASE
DFC0-18	B3F4	DFC1 DSCH 1, DATA HI BYTES, - PHASE
DFC0-19	B3F4	DFC1 DSCH 1, DATA LO BYTES, - PHASE
DFC0-2	B3F3	DFC1 DSCH 0, RECEIVE CLOCK IN, + PHASE
DFC0-3	B3F3	DFC1 DSCH 0, DATA HI BYTES, + PHASE
DFC0-4	B3F3	DFC1 DSCH 0, DATA LO BYTES, + PHASE
DFC0-5	B3F3	DFC1 DSCH 0, INTERRUPT, + PHASE
DFC0-6	B3F3	DFC1 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
DFC0-7	B3F3	DFC1 DSCH 0, RECEIVE CLOCK IN, - PHASE[
DFC0-8	B3F3	DFC1 DSCH 0, DATA HI BYTES, - PHASE
DFC0-9	B3F3	DFC1 DSCH 0, DATA LO BYTES, - PHASE
DFC1-1	B3C3	DFC1 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
DFC1-10	B3C3	DFC1 DSCH 0, INTERRUPT, - PHASE
DFC1-11	B3C4	DFC1 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
DFC1-12	B3C4	DFC1 DSCH 1, RECEIVE CLOCK IN, + PHASE
DFC1-13	B3C4	DFC1 DSCH 1, DATA HI BYTES, + PHASE
DFC1-14	B3C4	DFC1 DSCH 1, DATA LO BYTES, + PHASE
DFC1-15	B3C4	DFC1 DSCH 1, INTERRUPT, + PHASE
DFC1-16	B3C4	DFC1 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
DFC1-17	B3C4	DFC1 DSCH 1, RECEIVE CLOCK IN, - PHASE
DFC1-18	B3C4	DFC1 DSCH 1, DATA HI BYTES, - PHASE
DFC1-19	B3C4	DFC1 DSCH 1, DATA LO BYTES, - PHASE
DFC1-2	B3C3	DFC1 DSCH 0, RECEIVE CLOCK IN, + PHASE
DFC1-20	B3C4	DFC1 DSCH 1, INTERRUPT, - PHASE
DFC1-3	B3C3	DFC1 DSCH 0, DATA HI BYTES, + PHASE
DFC1-4	B3C3	DFC1 DSCH 0, DATA LO BYTES, + PHASE
DFC1-5	B3C3	DFC1 DSCH 0, INTERRUPT, + PHASE
DFC1-6	B3C3	DFC1 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
DFC1-7	B3C3	DFC1 DSCH 0, RECEIVE CLOCK IN, - PHASE[
DFC1-8	B3C3	DFC1 DSCH 0, DATA HI BYTES, - PHASE
DFC1-9	B3C3	DFC1 DSCH 0, DATA LO BYTES, - PHASE
DFC2-1	B6C2	DFC2 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
DFC2-10	B6C2	DFC2 DSCH 0, INTERRUPT, - PHASE
DFC2-11	B6C3	DFC2 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
DFC2-12	B6C3	DFC2 DSCH 1, RECEIVE CLOCK IN, + PHASE
DFC2-13	B6C3	DFC2 DSCH 1, DATA HI BYTES, + PHASE
DFC2-14	B6C3	DFC2 DSCH 1, DATA LO BYTES, + PHASE
DFC2-15	B6C3	DFC2 DSCH 1, INTERRUPT, + PHASE
DFC2-16	B6C3	DFC2 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
DFC2-17	B6C3	DFC2 DSCH 1, RECEIVE CLOCK IN, - PHASE
DFC2-18	B6C3	DFC2 DSCH 1, DATA HI BYTES, - PHASE
DFC2-19	B6C3	DFC2 DSCH 1, DATA LO BYTES, - PHASE
DFC2-2	B6C2	DFC2 DSCH 0, RECEIVE CLOCK IN, + PHASE
DFC2-20	B6C3	DFC2 DSCH 1, INTERRUPT, - PHASE
DFC2-3	B6C2	DFC2 DSCH 0, DATA HI BYTES, + PHASE
DFC2-4	B6C2	DFC2 DSCH 0, DATA LO BYTES, + PHASE
DFC2-5	B6C2	DFC2 DSCH 0, INTERRUPT, + PHASE
DFC2-6	B6C2	DFC2 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
DFC2-7	B6C2	DFC2 DSCH 0, RECEIVE CLOCK IN, - PHASE[
DFC2-8	B6C2	DFC2 DSCH 0, DATA HI BYTES, - PHASE
DFC2-9	B6C2	DFC2 DSCH 0, DATA LO BYTES, - PHASE
EAI1-1	B8F3	PROC 0 EAI PORT 0 TRANSMIT DATA OUT, - PHASE
EAI1-2	B8F3	PROC 0 EAI PORT 0 RECEIVE DATA INPUT, - PHASE
EAI1-3	B8F3	PROC 0 EAI PORT 0 RTS OUTPUT, - PHASE
EAI1-4	B8F3	PROC 0 EAI PORT 0 TRANSMIT DATA OUT, + PHASE
EAI1-5	B8F3	PROC 0 EAI PORT 0 RECEIVE DATA INPUT, + PHASE
EAI1-6	B8F3	PROC 0 EAI PORT 0 RTS OUTPUT, + PHASE
EAI2-1	B8F3	PROC 0 EAI PORT 0 TRANSMIT DATA OUT, - PHASE
EAI2-2	B8F3	PROC 0 EAI PORT 0 RECEIVE DATA INPUT, - PHASE
EAI2-3	B8F3	PROC 0 EAI PORT 0 RTS OUTPUT, - PHASE
EAI2-4	B8F3	PROC 0 EAI PORT 0 TRANSMIT DATA OUT, + PHASE
EAI2-5	B8F3	PROC 0 EAI PORT 0 RECEIVE DATA INPUT, + PHASE
EAI2-6	B8F3	PROC 0 EAI PORT 0 RTS OUTPUT, + PHASE
EAI3-1	B8C3	PROC 1 EAI PORT 0 TRANSMIT DATA OUT, - PHASE
EAI3-2	B8C3	PROC 1 EAI PORT 0 RECEIVE DATA INPUT, - PHASE
EAI3-3	B8C3	PROC 1 EAI PORT 0 RTS OUTPUT, - PHASE
EAI3-4	B8C3	PROC 1 EAI PORT 0 TRANSMIT DATA OUT, + PHASE
EAI3-5	B8C3	PROC 1 EAI PORT 0 RECEIVE DATA INPUT, + PHASE
EAI4-1	B8C3	PROC 1 EAI PORT 0 TRANSMIT DATA OUT, - PHASE
EAI4-2	B8C3	PROC 1 EAI PORT 0 RECEIVE DATA INPUT, - PHASE
EAI4-3	B8C3	PROC 1 EAI PORT 0 RTS OUTPUT, - PHASE
EAI4-4	B8C3	PROC 1 EAI PORT 0 TRANSMIT DATA OUT, + PHASE
EAI4-5	B8C3	PROC 1 EAI PORT 0 RECEIVE DATA INPUT, + PHASE
EAI4-6	B8C3	PROC 1 EAI PORT 0 RTS OUTPUT, + PHASE
EAI4-6	B8C3	PROC 1 EAI PORT 0 RTS OUTPUT, + PHASE
FALM0	B11E2	FUSE ALARM TO PROC 0
FALM1	B11D2	FUSE ALARM TO PROC 1
IOP0-1	B4F3	IOP0 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
IOP0-10	B4F4	IOP0 DSCH 0, INTERRUPT, - PHASE
IOP0-11	B4F4	IOP0 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
IOP0-12	B4F4	IOP0 DSCH 1, RECEIVE CLOCK IN, + PHASE
IOP0-13	B4F4	IOP0 DSCH 1, DATA HI BYTES, + PHASE
IOP0-14	B4F4	IOP0 DSCH 1, DATA LO BYTES, + PHASE
IOP0-15	B4F4	IOP0 DSCH 1, INTERRUPT, + PHASE
IOP0-16	B4F4	IOP0 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
IOP0-17	B4F4	IOP0 DSCH 1, RECEIVE CLOCK IN, - PHASE
IOP0-18	B4F4	IOP0 DSCH 1, DATA HI BYTES, - PHASE
IOP0-19	B4F4	IOP0 DSCH 1, DATA LO BYTES, - PHASE
IOP0-2	B4F3	IOP0 DSCH 0, RECEIVE CLOCK IN, + PHASE
IOP0-20	B4F4	IOP0 DSCH 1, INTERRUPT, - PHASE
IOP0-3	B4F3	IOP0 DSCH 0, DATA HI BYTES, + PHASE
IOP0-4	B4F3	IOP0 DSCH 0, DATA LO BYTES, + PHASE
IOP0-5	B4F3	IOP0 DSCH 0, INTERRUPT, + PHASE
IOP0-6	B4F3	IOP0 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
IOP0-7	B4F3	IOP0 DSCH 0, RECEIVE CLOCK IN, - PHASE
IOP0-8	B4F3	IOP0 DSCH 0, DATA HI BYTES, - PHASE

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE: C2 | ISSUE: 1

AT&T | SD-3T015-01 | SHEET: A2

PRINTED IN U.S.A

DESIGNATION MNEMONICS

MNEMONIC	LOC	DEFINITION
IOP0-9	B4F3	IOP0 DSCH 0, DATA LO BYTES, - PHASE
IOP1-1	B4C3	IOP1 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
IOP1-10	B4C4	IOP1 DSCH 0, INTERRUPT, - PHASE
IOP1-11	B4C4	IOP1 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
IOP1-12	B4C4	IOP1 DSCH 1, RECEIVE CLOCK IN, + PHASE
IOP1-13	B4C4	IOP1 DSCH 1, DATA HI BYTES, + PHASE
IOP1-14	B4C4	IOP1 DSCH 1, DATA LO BYTES, + PHASE
IOP1-15	B4C4	IOP1 DSCH 1, INTERRUPT, + PHASE
IOP1-16	B4C4	IOP1 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
IOP1-17	B4C4	IOP1 DSCH 1, RECEIVE CLOCK IN, - PHASE
IOP1-18	B4C4	IOP1 DSCH 1, DATA HI BYTES, - PHASE
IOP1-19	B4C4	IOP1 DSCH 1, DATA LO BYTES, - PHASE
IOP1-2	B4C3	IOP1 DSCH 0, RECEIVE CLOCK IN, + PHASE
IOP1-20	B4C4	IOP1 DSCH 1, INTERRUPT, - PHASE
IOP1-3	B4C3	IOP1 DSCH 0, DATA HI BYTES, + PHASE
IOP1-4	B4C3	IOP1 DSCH 0, DATA LO BYTES, + PHASE
IOP1-5	B4C3	IOP1 DSCH 0, INTERRUPT, + PHASE
IOP1-6	B4C3	IOP1 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
IOP1-7	B4C3	IOP1 DSCH 0, RECEIVE CLOCK IN, - PHASE
IOP1-8	B4C3	IOP1 DSCH 0, DATA HI BYTES, - PHASE
IOP1-9	B4C3	IOP1 DSCH 0, DATA LO BYTES, - PHASE
IOP2-1	B5E2	IOP2 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
IOP2-10	B5F4	IOP2 DSCH 0, INTERRUPT, - PHASE
IOP2-11	B5F4	IOP2 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
IOP2-12	B5F4	IOP2 DSCH 1, RECEIVE CLOCK IN, + PHASE
IOP2-13	B5F4	IOP2 DSCH 1, DATA HI BYTES, + PHASE
IOP2-14	B5F4	IOP2 DSCH 1, DATA LO BYTES, + PHASE
IOP2-15	B5F4	IOP2 DSCH 1, INTERRUPT, + PHASE
IOP2-16	B5F4	IOP2 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
IOP2-17	B5F4	IOP2 DSCH 1, RECEIVE CLOCK IN, - PHASE
IOP2-18	B5F4	IOP2 DSCH 1, DATA HI BYTES, - PHASE
IOP2-19	B5F4	IOP2 DSCH 1, DATA LO BYTES, - PHASE
IOP2-2	B5E2	IOP2 DSCH 0, RECEIVE CLOCK IN, + PHASE
IOP2-20	B5F4	IOP2 DSCH 1, INTERRUPT, - PHASE
IOP2-3	B5E2	IOP2 DSCH 0, DATA HI BYTES, + PHASE
IOP2-4	B5E2	IOP2 DSCH 0, DATA LO BYTES, + PHASE
IOP2-5	B5E2	IOP2 DSCH 0, INTERRUPT, + PHASE
IOP2-6	B5E2	IOP2 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
IOP2-7	B5E2	IOP2 DSCH 0, RECEIVE CLOCK IN, - PHASE
IOP2-8	B5E2	IOP2 DSCH 0, DATA HI BYTES, - PHASE
IOP2-9	B5E2	IOP2 DSCH 0, DATA LO BYTES, - PHASE
IOP3-1	B5C2	IOP2 DSCH 0, TRANSMIT CLOCK OUT, + PHASE
IOP3-10	B5C4	IOP2 DSCH 0, INTERRUPT, - PHASE
IOP3-11	B5C4	IOP2 DSCH 1, TRANSMIT CLOCK OUT, + PHASE
IOP3-12	B5C4	IOP2 DSCH 1, RECEIVE CLOCK IN, + PHASE
IOP3-13	B5C4	IOP2 DSCH 1, DATA HI BYTES, + PHASE
IOP3-14	B5C4	IOP2 DSCH 1, DATA LO BYTES, + PHASE
IOP3-15	B5C4	IOP2 DSCH 1, INTERRUPT, + PHASE
IOP3-16	B5C4	IOP2 DSCH 1, TRANSMIT CLOCK OUT, - PHASE
IOP3-17	B5C4	IOP2 DSCH 1, RECEIVE CLOCK IN, - PHASE
IOP3-18	B5C4	IOP2 DSCH 1, DATA HI BYTES, - PHASE
IOP3-19	B5C4	IOP2 DSCH 1, DATA LO BYTES, - PHASE
IOP3-2	B5C2	IOP2 DSCH 0, RECEIVE CLOCK IN, + PHASE
IOP3-20	B5C2	IOP2 DSCH 1, INTERRUPT, - PHASE
IOP3-3	B5C2	IOP2 DSCH 0, DATA HI BYTES, + PHASE
IOP3-4	B5C2	IOP2 DSCH 0, DATA LO BYTES, + PHASE
IOP3-5	B5C2	IOP2 DSCH 0, INTERRUPT, + PHASE
IOP3-6	B5C2	IOP2 DSCH 0, TRANSMIT CLOCK OUT, - PHASE
IOP3-7	B5C2	IOP2 DSCH 0, RECEIVE CLOCK IN, - PHASE
IOP3-8	B5C2	IOP2 DSCH 0, DATA HI BYTES, - PHASE
IOP3-9	B5C2	IOP2 DSCH 0, DATA LO BYTES, - PHASE
MJ-0	B11E3	PROC 1 MAJOR ALARM -POWER OR FUSE FAULT
MJ-1	B11C3	PROC 0 MAJOR ALARM -POWER OR FUSE FAULT
MJ-DFC2	B6F1	DFC2 MAJOR ALARM -POWER OR FUSE FAULT
MJ-IOP2	B5F1	IOP2 MAJOR ALARM -POWER OR FUSE FAULT
MJ-IOP3	B5C1	IOP3 MAJOR ALARM -POWER OR FUSE FAULT
MJR-0	B11E3	PROC 1 MAJOR ALARM RETURN
MJR-1	B11C3	PROC 0 MAJOR ALARM RETURN
MJR-DFC2	B6F1	DFC2 MAJOR ALARM RETURN
MJR-IOP2	B5F1	IOP2 MAJOR ALARM RETURN
MJR-IOP3	B5C1	IOP3 MAJOR ALARM RETURN
PA-0	B11E3	PROC 1 POWER ALARM -POWER FAULT
PA-1	B11C3	PROC 0 POWER ALARM -POWER FAULT
PA-DFC2	B6F1	DFC2 POWER ALARM -POWER FAULT
PA-IOP2	B5F1	IOP2 POWER ALARM -POWER FAULT
PA-IOP3	B5C1	IOP3 POWER ALARM -POWER FAULT
PAR-0	B11E3	PROC 1 POWER ALARM RETURN
PAR-1	B11C3	PROC 0 POWER ALARM RETURN
PAR-DFC2	B6F1	DFC2 POWER ALARM RETURN
PAR-IOP2	B5F1	IOP2 POWER ALARM RETURN
PAR-IOP3	B5C1	IOP3 POWER ALARM RETURN
PODISAN	B12D6	PP14 DATA FROM PROC 1, - PHASE
PODISAP	B12D6	PP14 DATA FROM PROC 1, + PHASE
PODISBN	B12D6	PP15 DATA FROM PROC 1, - PHASE
PODISBP	B12D6	PP15 DATA FROM PROC 1, + PHASE
PUDISAN	B12D6	PP14 DATA TO PROC 1, - PHASE
PUDISAP	B12D6	PP14 DATA TO PROC 1 + PHASE
PUDISBN	B12D6	PP15 DATA TO PROC 1, - PHASE
PUDISBP	B12D6	PP15 DATA TO PROC 1, + PHASE
REQ00O[N,P]	B4D3	IOP: DSCH 0, INTERRUPT
REQ01O[N,P]	B4D4	IOP0 DSCH 1, INTERRUPT
REQ01O[N,P]	B4D4	IOP: DSCH 1, INTERRUPT
REQAN	B10D4	MCHL: REQUESTS SLAVE CC TO PULSE MRF0, - PHASE
REQAP	B10D3	MCHL: REQUESTS SLAVE CC TO PULSE MRF0, + PHASE
ROP-DCD	B7B4	DCD FROM PRINTER TO 3B21D
ROP-RET	B7B4	RS232 RETURN FROM PRINTER
ROP-RTS	B7B4	RTS FROM PRINTER TO 3B21D
ROP-RXD	B7B4	RXD FROM PRINTER TO 3B21D
ROP-TXD	B7B4	TXD TO PRINTER FROM 3B21D
ROP0-1	B7F2	ROP RS232 CTS OUTPUT TO IOP0
ROP0-2	B7F2	ROP RS232 RXD OUTPUT TO IOP0
ROP0-3	B7F2	ROP RS232 DSR OUTPUT TO IOP0
ROP0-4	B7F2	ROP RS232 DCD OUTPUT TO IOP0
ROP0-5	B7F2	ROP RS232 TXD INPUT FROM IOP0
ROP0-6	B7F2	ROP RS232 DTR INPUT FROM IOP0
ROP0-7	B7F2	ROP RS232 RTS INPUT FROM IOP0
ROP0-8	B7F2	ROP RS232 RETURN (TIED TO GRD)
ROP1-1	B7C2	ROP RS232 CTS OUTPUT TO IOP1
ROP1-2	B7C2	ROP RS232 RXD OUTPUT TO IOP1
ROP1-3	B7C2	ROP RS232 DSR OUTPUT TO IOP1
ROP1-4	B7C2	ROP RS232 DCD OUTPUT TO IOP1
ROP1-5	B7C2	ROP RS232 TXD INPUT FROM IOP1
ROP1-6	B7C2	ROP RS232 DTR INPUT FROM IOP1
ROP1-7	B7C2	ROP RS232 RTS INPUT FROM IOP1
ROP1-8	B7C2	ROP RS232 RETURN (TIED TO GRD)
RSTR0	B11E7	COOLING UNIT: 3BRST10 RETURN
RSTR1	B11D7	COOLING UNIT: 3BRST11 RETURN
SCAN0-1	B11E4	ACTIVATES REQUEST IN PROGRESS LED IN IOP0, + PHASE
SCAN0-10	B11E4	INDICATES STATE OF FUSE ALARM INPUT TO IOP0, - PHASE
SCAN0-2	B11E4	LIGHTS OUT OF SERVICE LED IN IOP0, + PHASE
SCAN0-3	B11E4	USED WITH SCAN0-4 TO ENCODE IOP0 POWER STATUS, + PHASE
SCAN0-4	B11E4	USED WITH SCAN0-3 TO ENCODE IOP0 POWER STATUS, + PHASE
SCAN0-5	B11E4	INDICATES STATE OF FUSE ALARM INPUT TO IOP0, POSTIVE PHASE
SCAN0-6	B11E4	ACTIVATES REQUEST IN PROGRESS LED IN IOP0, - PHASE
SCAN0-7	B11E4	LIGHTS OUT OF SERVICE LED IN IOP0, - PHASE
SCAN0-8	B11E4	USED WITH SCAN0-8 TO ENCODE IOP0 POWER STATUS, - PHASE
SCAN0-9	B11E4	USED WITH SCAN0-7 TO ENCODE IOP0 POWER STATUS, - PHASE
SCAN1-1	B11C4	ACTIVATES REQUEST IN PROGRESS LED IN IOP1, + PHASE
SCAN1-10	B11C4	INDICATES STATE OF FUSE ALARM INPUT TO IOP1, - PHASE
SCAN1-2	B11C4	LIGHTS OUT OF SERVICE LED IN IOP1, + PHASE
SCAN1-3	B11C4	USED WITH SCAN0-4 TO ENCODE IOP1 POWER STATUS, + PHASE
SCAN1-4	B11C4	USED WITH SCAN0-3 TO ENCODE IOP1 POWER STATUS, + PHASE
SCAN1-5	B11C4	INDICATES STATE OF FUSE ALARM INPUT TO IOP1, POSTIVE PHASE
SCAN1-6	B11C4	ACTIVATES REQUEST IN PROGRESS LED IN IOP1, - PHASE
SCAN1-7	B11C4	LIGHTS OUT OF SERVICE LED IN IOP1, - PHASE
SCAN1-8	B11C4	USED WITH SCAN0-8 TO ENCODE IOP1 POWER STATUS, - PHASE
SCAN1-9	B11C4	USED WITH SCAN0-7 TO ENCODE IOP1 POWER STATUS, - PHASE
SCAN2-1	B5E4	ACTIVATES REQUEST IN PROGRESS LED IN IOP3, + PHASE
SCAN2-2	B5E4	LIGHTS OUT OF SERVICE LED IN IOP3, + PHASE
SCAN2-3	B5E4	USED WITH SCAN1-4 TO ENCODE IOP2 POWER STATUS, + PHASE
SCAN2-4	B5E4	USED WITH SCAN1-3 TO ENCODE IOP2 POWER STATUS, + PHASE
SCAN2-5	B5E4	ACTIVATES REQUEST IN PROGRESS LED IN IOP2, - PHASE
SCAN2-6	B5E4	LIGHTS OUT OF SERVICE LED IN IOP2, - PHASE
SCAN2-7	B5E4	USED WITH SCAN1-8 TO ENCODE IOP2 POWER STATUS, - PHASE
SCAN2-8	B5E4	USED WITH SCAN1-7 TO ENCODE IOP2 POWER STATUS, - PHASE
SCAN3-1	B5C4	ACTIVATES REQUEST IN PROGRESS LED IN IOP3, + PHASE
SCAN3-2	B5C4	LIGHTS OUT OF SERVICE LED IN IOPPS, + PHASE
SCAN3-3	B5C4	USED WITH SCAN0-4 TO ENCODE IOP3 POWER STATUS, + PHASE
SCAN3-4	B5C4	USED WITH SCAN0-3 TO ENCODE IOP3 POWER STATUS, + PHASE
SCAN3-5	B5C4	ACTIVATES REQUEST IN PROGRESS LED IN IOP3, - PHASE
SCAN3-6	B5C4	LIGHTS OUT OF SERVICE LED IN IOP3, - PHASE
SCAN3-7	B5C4	USED WITH SCAN0-8 TO ENCODE IOP3 POWER STATUS, - PHASE
SCAN3-8	B5C4	USED WITH SCAN0-7 TO ENCODE IOP3 POWER STATUS, - PHASE
SCAN5-1	B6E4	ACTIVATES REQUEST IN PROGRESS LED IN DFC2, + PHASE
SCAN5-2	B6E4	LIGHTS OUT OF SERVICE LED IN DFC2, + PHASE
SCAN5-3	B6E4	USED WITH SCAN5-4 TO ENCODE DFC2 POWER STATUS, + PHASE
SCAN5-4	B6E4	USED WITH SCAN5-3 TO ENCODE DFC2 POWER STATUS, + PHASE
SCAN5-5	B6E4	ACTIVATES REQUEST IN PROGRESS LED IN DFC2, - PHASE
SCAN5-6	B6E4	LIGHTS OUT OF SERVICE LED IN DFC2, - PHASE
SCAN5-7	B6E4	USED WITH SCAN5-8 TO ENCODE DFC2 POWER STATUS, - PHASE
SCAN5-8	B6E4	USED WITH SCAN5-7 TO ENCODE DFC2 POWER STATUS, - PHASE

3B21D PROCESSOR COMPUTER SYSTEMS	DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01	SHEET A3

DESIGNATION MNEMONICS

MNEMONIC	LOC	DEFINITION
SCANR0	B11E7	COOLING UNIT: 3BSCAN00 RETURN
SCANR1	B11D7	COOLING UNIT: 3BSCAN01 RETURN
SUABUSN	B14D2	UPDATE ENABLE ADDRESS BUS, - PHASE
SUABUSP	B14D5	UPDATE ENABLE ADDRESS BUS, + PHASE
SUA[00-27]N	B13,14	UPDATE ADDRESS BITS 00-27, - PHASE
SUA[00-27]P	B13,14	UPDATE ADDRESS BITS 00-27, + PHASE
SUA[32-35]N	B13,14	UPDATE ADDR PARITY BITS 3-0, - PHASE
SUA[32-35]P	B13,14	UPDATE ADDR PARITY BITS 3-0, + PHASE
SUBYTEN	B14D3	UPDATE BUS IN BYTE MODE, - PHASE
SUBYTEP	B14D5	UPDATE BUS IN BYTE MODE, + PHASE
SUCMPN	B12D4	UPDATE STORE COMPLETE, - PHASE
SUCMPP	B12D6	UPDATE STORE COMPLETE, + PHASE
SUCOMPN	B16D2	UPDATE BUS COMMAND PARITY, - PHASE
SUCOMPP	B16D6	UPDATE BUS COMMAND PARITY, + PHASE
SUDBUSN	B14D2	UPDATE ENABLE DATA, - PHASE
SUDBUSP	B14D5	UPDATE ENABLE DATA, + PHASE
SUDSN	B14D2	UPDATE BUS DS0 (QUAD WORD TRANSFER), - PHASE
SUDSP	B14D5	UPDATE BUS DS0 (QUAD WORD TRANSFER), + PHASE
SUD[00-31]P	B15,16	UPDATE DATA BITS 00-31, + PHASE
SUD[00-31]P	B15,16	UPDATE DATA BITS 00-31, + PHASE
SUD[32-35]N	B15,16	UPDATE DATA PARITY BITS 3-0, - PHASE
SUD[32-35]N	B15,16	UPDATE DATA PARITY BITS 3-0, - PHASE
SUERAN	B12D5	MY STORE ERROR A TO OTHER MM, - PHASE
SUERAP	B12D5	MY STORE ERROR A TO OTHER MM, + PHASE
SUERBN	B12D5	MY STORE ERROR B TO OTHER MM, - PHASE
SUERBP	B12D5	MY STORE ERROR B TO OTHER MM, + PHASE
SUERCN	B12D3	MY STORE ERROR C TO OTHER MM, - PHASE
SUERCP	B12D3	MY STORE ERROR C TO OTHER MM, + PHASE
SUERDN	B12D3	MY STORE ERROR D TO OTHER MM, - PHASE
SUERDP	B12D3	MY STORE ERROR D TO OTHER MM, + PHASE
SUGON	B12D4	UPDATE STORE GO COMMAND, - PHASE
SUGOP	B12D6	UPDATE STORE GO COMMAND, + PHASE
SUHALFN	B14D3	UPDATE BUS IN HALF WORD MODE, - PHASE
SUHALFP	B14D5	UPDATE BUS IN HALF WORD MODE, + PHASE
SUMAINTN	B14D3	UPDATE BUS IN MAINTENANCE MODE, + PHASE
SUMAINTP	B14D5	UPDATE BUS IN MAINTENANCE MODE, + PHASE
SUOERRAN	B12D5	STORE ERROR A FROM OTHER MM, - PHASE
SUOERRAP	B12D5	STORE ERROR A FROM OTHER MM, + PHASE
SUOERRBN	B12D5	STORE ERROR B FROM OTHER MM, - PHASE
SUOERRBP	B12D5	STORE ERROR B FROM OTHER MM, + PHASE
SUOERRCN	B12D3	STORE ERROR C FROM OTHER MM, - PHASE
SUOERRCP	B12D3	STORE ERROR C FROM OTHER MM, + PHASE
SUOERRDN	B12D3	STORE ERROR D FROM OTHER MM, - PHASE
SUOERRDP	B12D3	STORE ERROR D FROM OTHER MM, + PHASE
SUOFONLN	B12D5	OTHER PROCESSOR ONLINE, - PHASE
SUOFONLP	B12D3	OTHER PROCESSOR ONLINE, + PHASE
SUOFUPDN	B12D5	OTHER CU IS IN UPDATE MODE, - PHASE
SUOFUPDP	B12D5	OTHER CU IS IN UPDATE MODE, + PHASE
SUPONLN	B12D5	PROCESSOR ONLINE TO OTHER CU, - PHASE
SUPONLP	B12D5	PROCESSOR ONLINE TO OTHER CU, + PHASE
SUPUPDN	B12D5	SEND UPDATE MODE TO OTHER CU, - PHASE
SUPUPDP	B12D5	SEND UPDATE MODE TO OTHER CU, + PHASE
SUQUADN	B14D3	UPDATE BUS IN QUAD WORD ACCESS MODE, - PHASE
SUQUADP	B14D5	UPDATE BUS IN QUAD WORD ACCESS MODE, + PHASE
SURWMN	B14D3	READ-MODIFY-WRITE MODE, - PHASE
SURWMP	B14D5	READ-MODIFY-WRITE MODE, + PHASE
SUWRTN	B14D3	UPDATE BUS IN WRITE MODE, - PHASE
SUWRTP	B14D5	UPDATE BUS IN WRITE MODE, + PHASE
TTY-DCD	B7B4	DCD FROM DISPLAY CONSOLE TO 3B21D
TTY-RET	B7B4	RS232 RETURN FROM DISPLAY CONSOLE
TTY-RTS	B7B4	RTS FROM DISPLAY CONSOLE TO 3B21D
TTY-RXD	B7B4	RXD FROM DISPLAY CONSOLE TO 3B21D
TTY-TXD	B7B4	TXD TO PRINTER FROM DISPLAY CONSOLE TO 3B21D
TTY0-1	B7F1	MTTY RS232 CTS OUTPUT TO IOP0
TTY0-2	B7F1	MTTY RS232 RXD OUTPUT TO IOP0
TTY0-3	B7F1	MTTY RS232 DSR OUTPUT TO IOP0
TTY0-4	B7F1	MTTY RS232 DCD OUTPUT TO IOP0
TTY0-5	B7F1	MTTY RS232 TXD INPUT FROM IOP0
TTY0-6	B7F1	MTTY RS232 DTR INPUT FROM IOP0
TTY0-7	B7F1	MTTY RS232 RTS INPUT FROM IOP0
TTY0-8	B7F1	MTTY RS232 RETURN (TIED TO GRD)
TTY1-1	B7C1	MTTY RS232 CTS OUTPUT TO IOP1
TTY1-2	B7C1	MTTY RS232 RXD OUTPUT TO IOP1
TTY1-3	B7C1	MTTY RS232 DSR OUTPUT TO IOP1
TTY1-4	B7C1	MTTY RS232 DCD OUTPUT TO IOP1
TTY1-5	B7C1	MTTY RS232 TXD INPUT FROM IOP1
TTY1-6	B7C1	MTTY RS232 DTR INPUT FROM IOP1
TTY1-7	B7C1	MTTY RS232 RTS INPUT FROM IOP1
TTY1-8	B7C1	MTTY RS232 RETURN (TIED TO GRD)
XCK00O[N,P]	B4D3	IOP: DSCH 0, RECEIVE CLOCK IN
XCK01O[N,P]	B4D4	IOP0 DSCH 1, RECEIVE CLOCK IN
XCK01O[N,P]	B4D4	IOP: DSCH 1, RECEIVE CLOCK IN
XCKAN	B10D4	MCHL: RECEIVE CLOCK IN, - PHASE
XCKAP	B10D4	MCHL: RECEIVE CLOCK IN, + PHASE

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE: C2 | ISSUE: 1

AT&T | SD-3T015-01 | SHEET: A4

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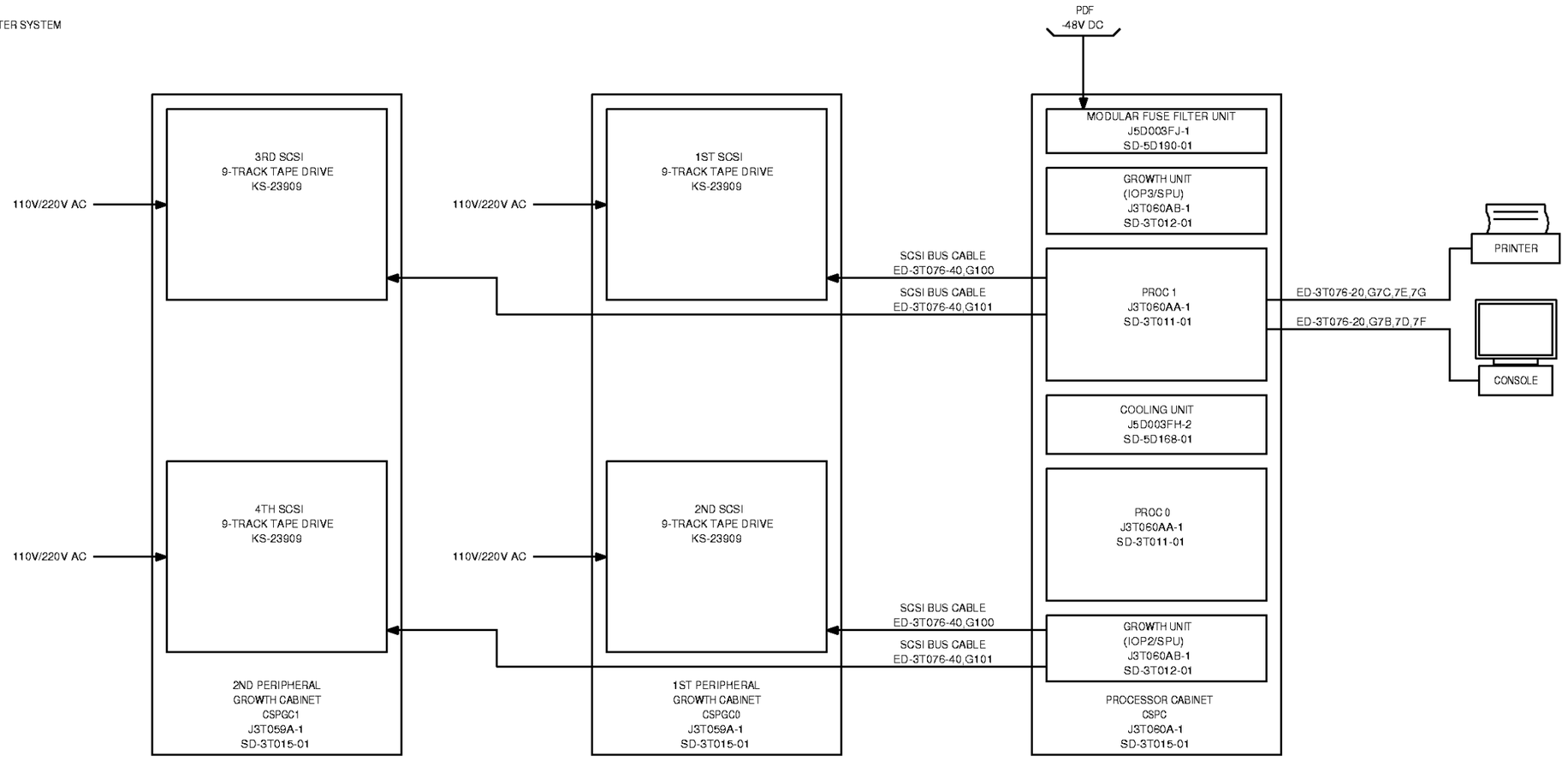
PART OF FS 1

3B21D COMPUTER SYSTEM
FIXED FLOOR PLAN
(MAXIMUM CONFIGURATION)

TOP VIEW
(FRONT)

(REAR)
FLOOR PLAN LAYOUT FOR 3B21D COMPUTER SYSTEM



REAR VIEW

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET B1

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PART OF FS 2

3B21D PROCESSOR CABINET

GROWTH CABINET J3T059A-1 SD-3T015-01 — FS 3

PROCESSOR CABINET J3T060A-1 SD-3T015-01 — FS 2

(REAR)

FLOOR PLAN LAYOUT FOR 3B21D COMPUTER SYSTEM

MODULAR FUSE FILTER UNIT (MMFU) J5D003FJ-1 SD-5D190-01

IOP 3 SCAN & SIGNAL DISTRIBUTOR ED-3T076-20,G18A

GROWTH UNIT (IOP3/SPU) J3T060AB-1 SD-3T012-01

SCSI OPT 2 ED3T076-40,G4E

SCSI OPT 2 ED3T076-40,G4D

FUSE & ALARM ED-3T076-50,G2

GROWTH BOUNDARY SCAN ED3T076-20,G6A

SCSI OPT 1 ED3T076-40,G4B,G4C

MAJOR ALARM
POWER ALARM
APPLICATION DEPENDENT

PROCESSOR UNIT (PROC 1) J3T060AA-1 SD-3T011-01

(16)

(13)

(8)

MTTY-ROP CABLES (2) ED-3T076-20,G2,G2A,G2D-G2G,G7B-G7G,G33,G33A,G34,G34A

BOUNDARY SCAN ED-3T076-20,G4,4A

DSCH CABLES ED-3T076-20,G1A-1N

MCH CABLE ED-3T076-20,G5

COOLING UNIT J5D003FH-2 SD-5D168-01

SCAN & SIGNAL DISTR. ED-3T076-20,G14A

SCAN & SIGNAL DISTR. ED-3T076-20,G14

EAI INTERCONNECTION ED-3T076-20,G3A,3C

IOP SCAN & SIGNAL DISTRIBUTOR ED-3T076-20,G15A,15D

MEMORY UPDATE ED-3T076-40,G1

SPU SCAN & SIGNAL DISTRIBUTOR ED-3T076-20,G17C,17E,17G,17J,17L

FUSE & ALARM ED-3T076-50,G1

PROCESSOR UNIT (PROC 0) J3T060AA-1 SD-3T011-01

(2)

(5)

SPU, IOP 2 AND DFC 2 SCAN & SIGNAL DISTRIBUTOR ED-3T076-20,G17B,17D,17F, G17H,17K,G18

(6)

MAJOR ALARM
POWER ALARM
APPLICATION DEPENDENT

GROWTH BOUNDARY SCAN ED3T076-20,G6

SCSI OPT 1 ED3T076-40,G4,G4A

GROWTH UNIT (IOP2/SPU) J3T060AB-1 SD-3T012-01

PROCESSOR CABINET J3T060A-1 SD-3T015-01

3B21D PROCESSOR COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	2B

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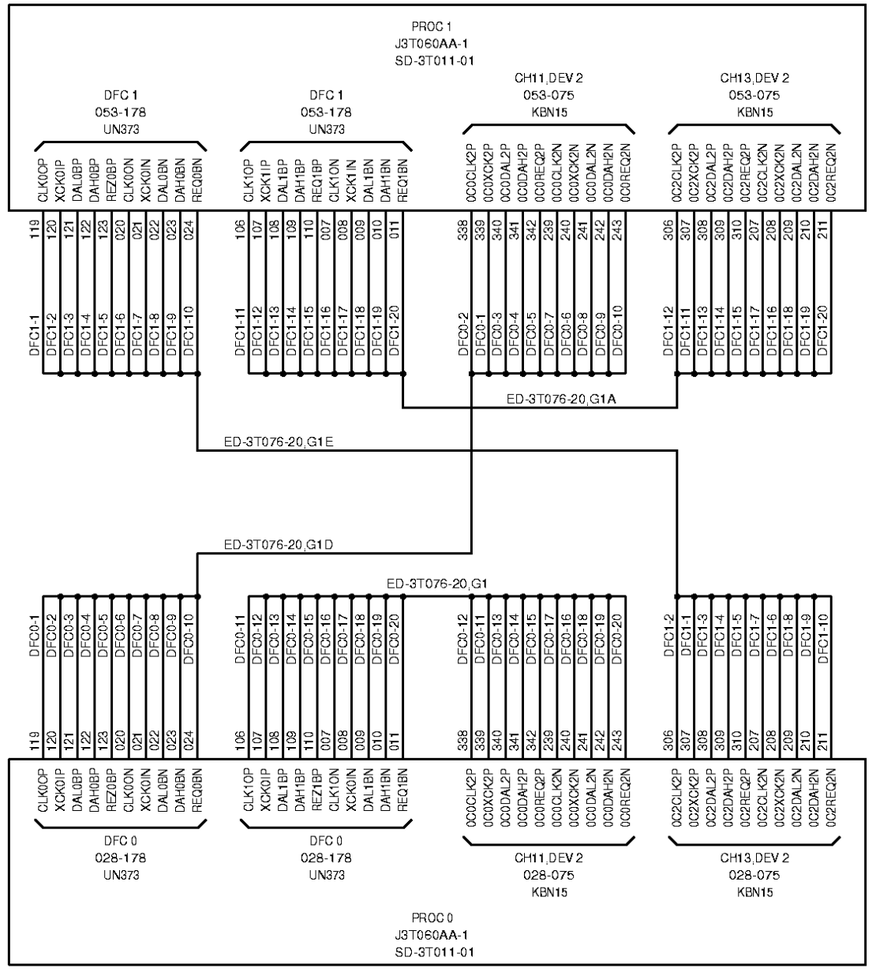
PART OF FS 2

DFC DSCH INTERCONNECTION



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01	SHEET B3	

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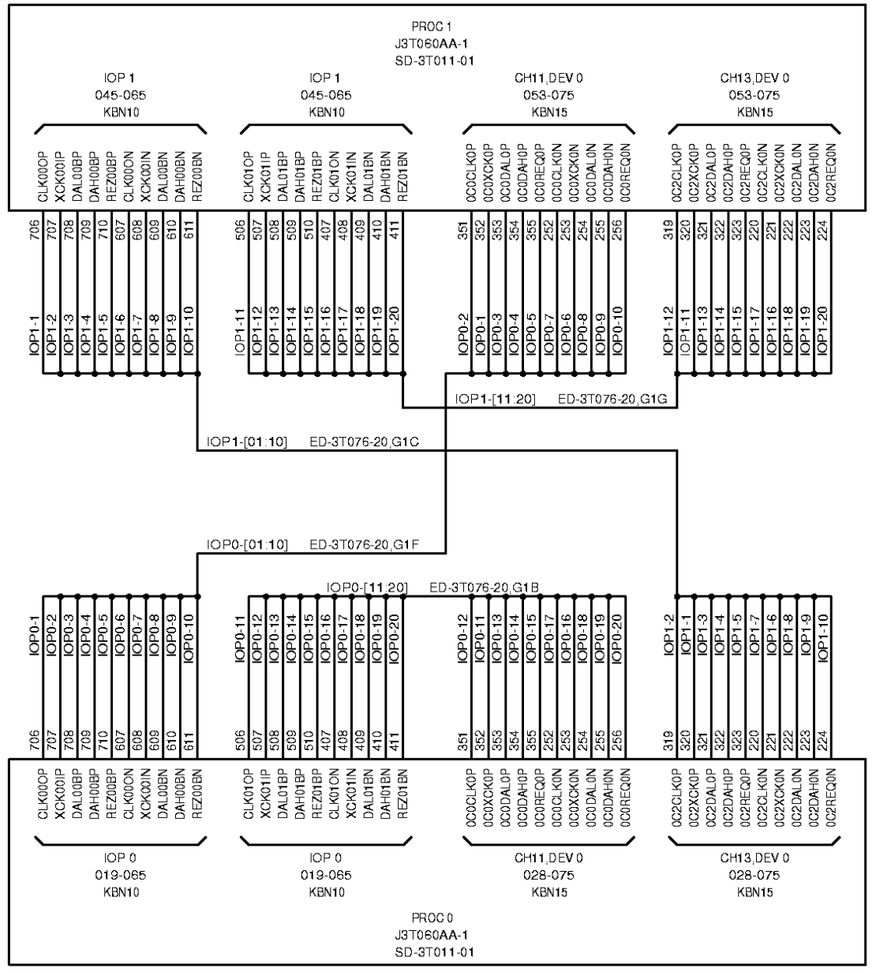
PART OF FS 2

IOP DSCH INTERCONNECTION



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE	ISSUE
		C2	1
AT&T	SD-3T015-01	SHEET	B4

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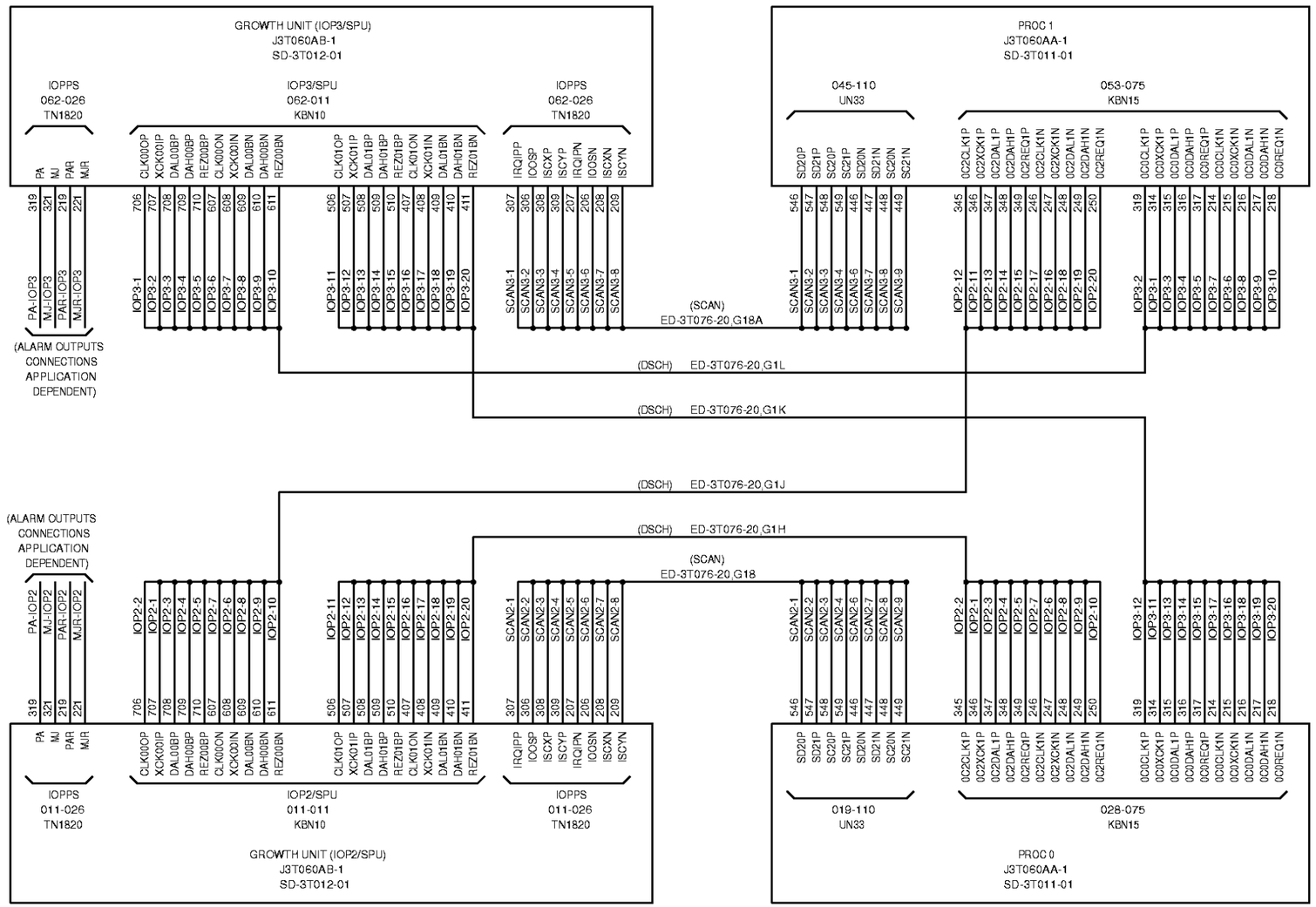
PART OF FS 2

GROWTH IOP DSCH & SCAN INTERCONNECTION



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
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PART OF FS 2

GROWTH DFC 2 DSCH & SCAN INTERCONNECTION

PROC 1
J3T060AA-1
SD-3T011-01

DMA 0,
CH13,DEV 3
053-075
KBN15

0C2CLK3P
0C2XCK3P
0C2DAL3P
0C2DAH3P
0C2REQ3P
0C2CLK3N
0C2XCK3N
0C2DAL3N
0C2DAH3N
0C2REQ3N

345 346 347 348 349 246 247 248 249 250

DFC2-12 DFC2-11 DFC2-13 DFC2-14 DFC2-15 DFC2-17 DFC2-16 DFC2-18 DFC2-19 DFC2-20

(DSCH) ED-3T076-20,G1N

(DSCH) ED-3T076-20,G1M

(SCAN) ED-3T076-20,G18B

(DFC 2 ALARM CONNECTIONS APPLICATION DEPENDENT)

PA-DFC2
MJ-DFC2
PAR-DFC2
MJR-DFC2

555 554 455 454

PA MJ PAR MJR

106 DFC2-1
107 DFC2-2
108 DFC2-3
109 DFC2-4
110 DFC2-5
DFC2-6
007 DFC2-7
008 DFC2-8
009 DFC2-9
010 DFC2-10
011 DFC2-11

CLK0OP XCK0IP DALOBP DAH0BP REQ0BP CLK0ON XCK0IN DALOBN DAH0BN REQ0BN

118 DFC2-12
120 DFC2-13
121 DFC2-14
122 DFC2-15
123 DFC2-16
020 DFC2-17
021 DFC2-18
022 DFC2-19
023 DFC2-20
024

CLK1OP XCK1IP DAL1BP DAH1BP REQ1BP CLK1ON XCK1IN DAL1BN DAH1BN REQ1BN

307 SCAN5-1
306 SCAN5-2
308 SCAN5-3
309 SCAN5-4
207 SCAN5-5
206 SCAN5-6
208 SCAN5-7
209 SCAN5-8

RQIPN OOSP SCXP SCYP RQIPN OOSN SCXN SCYN

DFC 2
011-180
UN373

GROWTH UNIT (IOP2/SPU)
J3T060AB-1
SD-3T012-01

332 DFC2-2
333 DFC2-1
334 DFC2-3
335 DFC2-4
336 DFC2-5
233 DFC2-7
234 DFC2-6
235 DFC2-8
236 DFC2-9
237 DFC2-10

0C2CLK3P 0C2XCK3P 0C2DAL3P 0C2DAH3P 0C2REQ3P 0C2CLK3N 0C2XCK3N 0C2DAL3N 0C2DAH3N 0C2REQ3N

DMA 0
CH13,DEV 1
028-075
KBN15

PROC 0
J3T060AA-1
SD-3T011-01

546 SCAN5-1
547 SCAN5-2
548 SCAN5-3
549 SCAN5-4
446 SCAN5-5
447 SCAN5-6
448 SCAN5-7
449 SCAN5-8

SD20P SD21P SC20P SC21P SD20N SD21N SC20N SC21N

PC-30
028-130
UN33

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	1

AT&T	SD-3T015-01	SHEET
		B6

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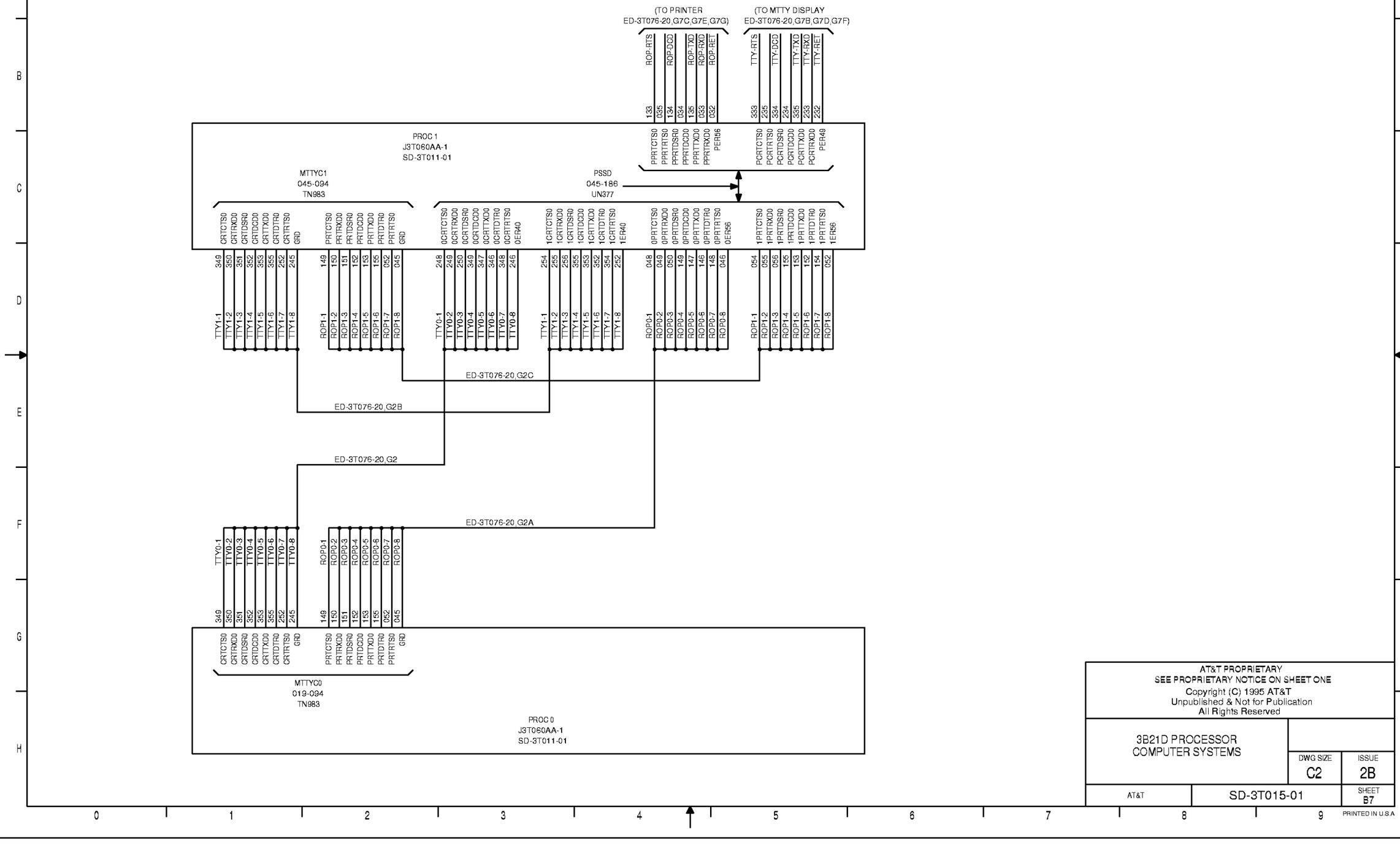
PART OF FS 2

PORTSWITCH INTERCONNECTION



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 2B
AT&T	SD-3T015-01	SHEET B7	

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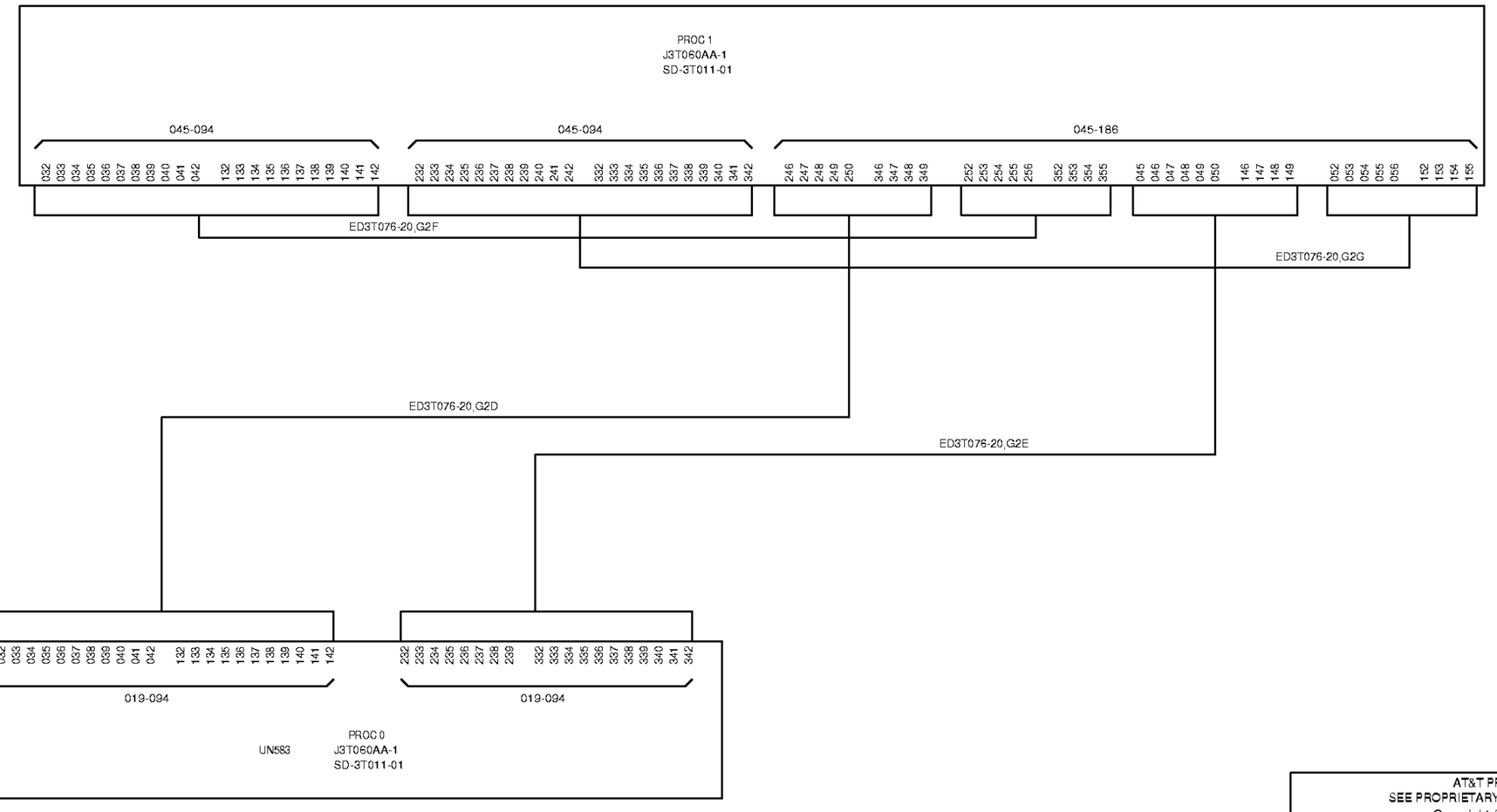
PART OF FS 2

PORTSWITCH INTERCONNECTION



3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	2B

AT&T	SD-3T015-01	SHEET
		B7A

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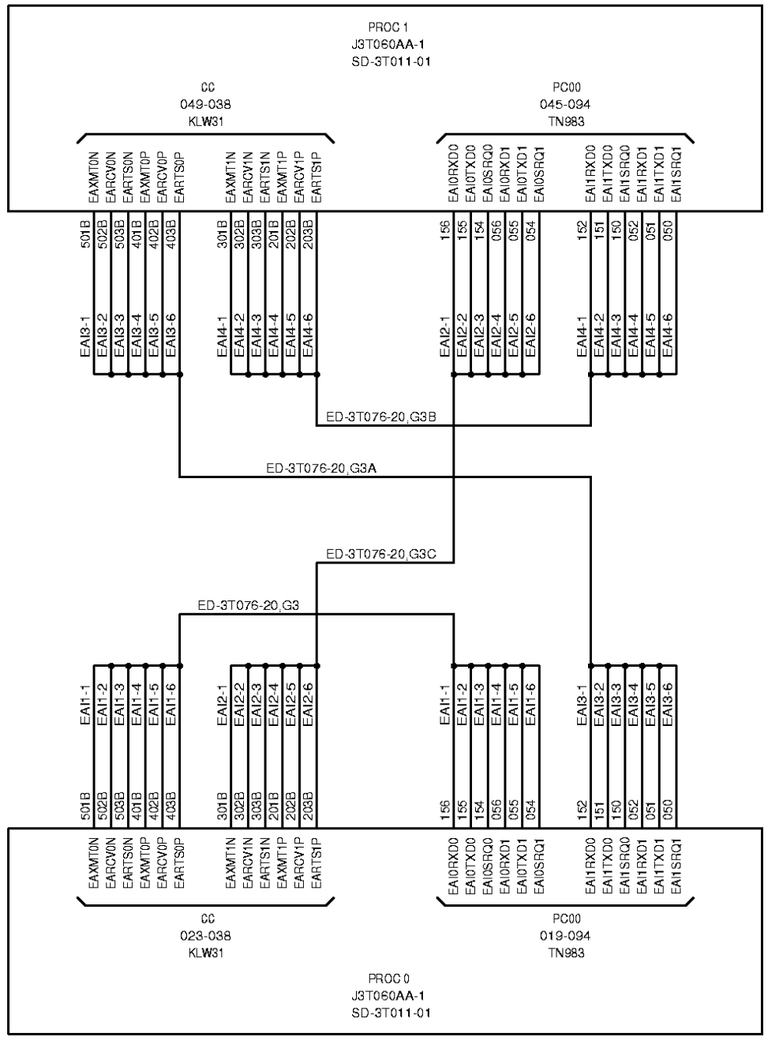
EAI INTERCONNECTION



3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	1

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		B8

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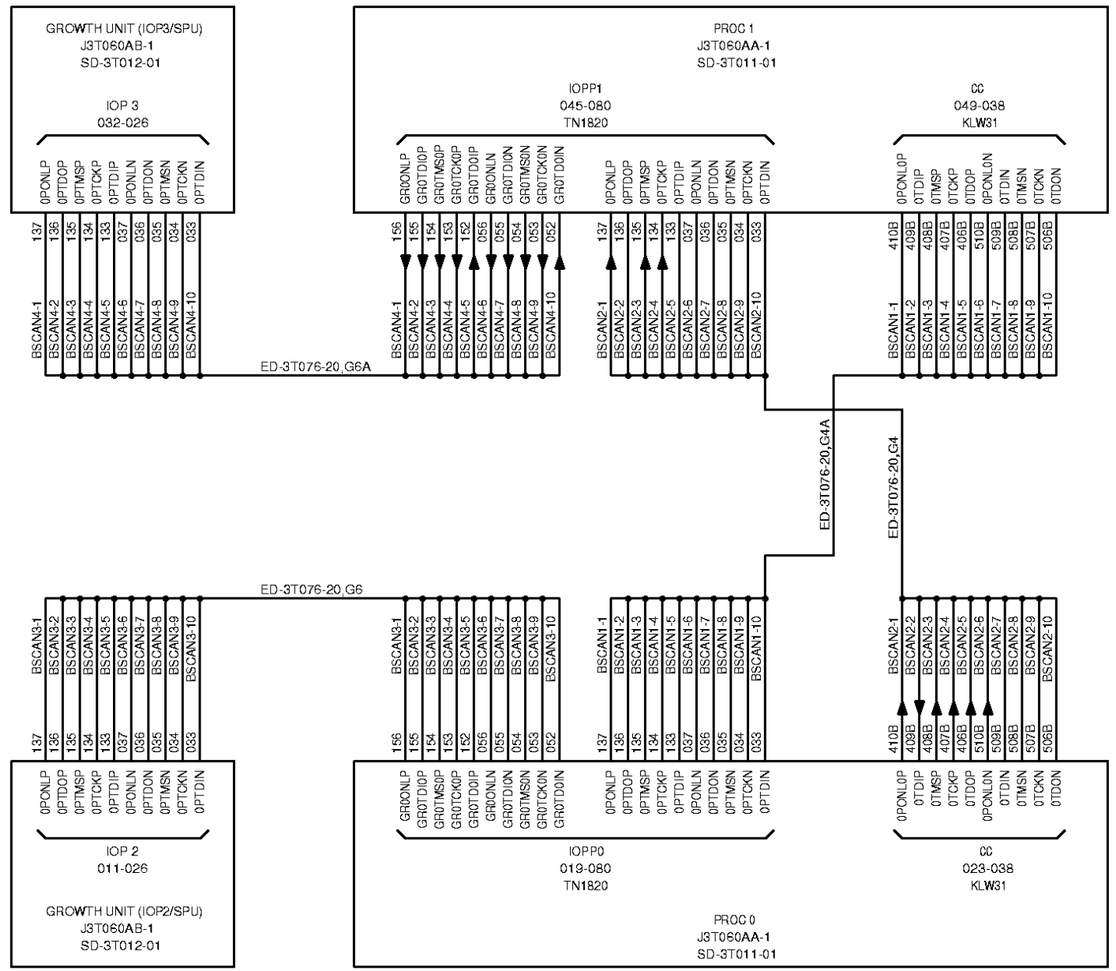
PART OF FS 2

BOUNDARY SCAN INTERCONNECTION

NOTES:

1. BOUNDARY SCAN CROSSOVER CABLES.
2. BOUNDARY SCAN EXTENSION CABLES TO GROWTH IOP2 OR IOP3.



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET B9

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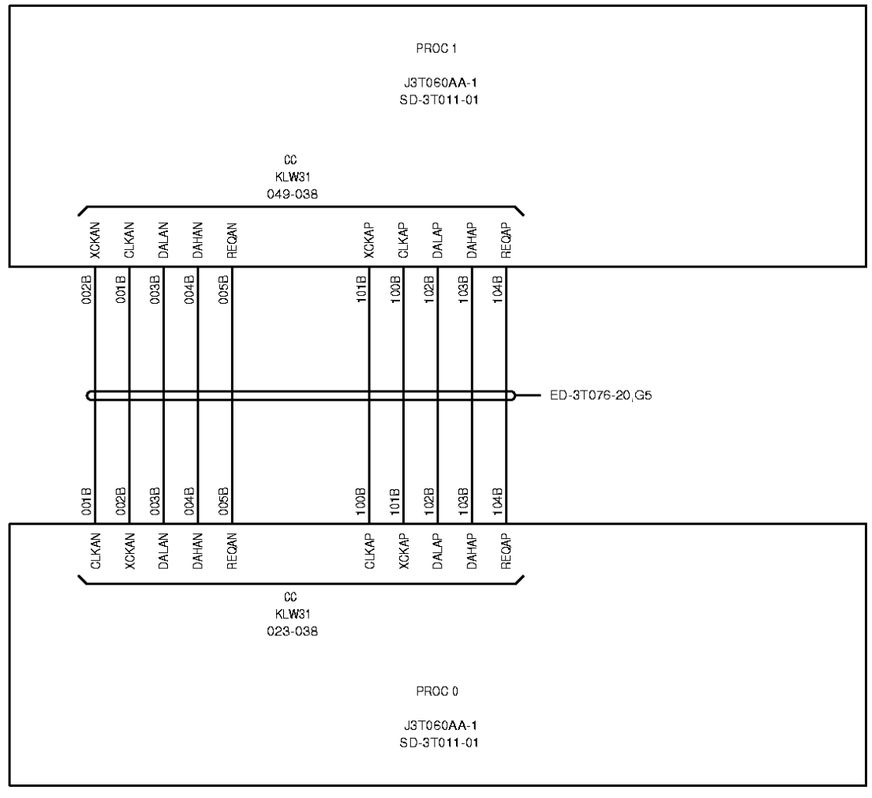
PART OF FS 2

MAINTENANCE CHANNEL INTERCONNECTION
1 CABLE



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
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PART OF FS 2

IOP SCAN, FUSE & FAN

NOTE:

1. THIS SHEET CONTAINS:
   - A. SCAN CABLES FOR IOP0 AND IOP1.
   - B. FUSE ALARM CABLE FROM FUSE UNIT.
   - C. COOLING UNIT SCAN CABLE.
   - D. CONNECTING POINT FOR MAJOR AND POWER ALARMS, WHICH ARE CONNECTED TO ALL 3B21D POWER CONTROLLERS.

PROC 1
J3T060AA-1
SD-3T011-01

CUPS
053-060
TN1821

IOPPS
045-080
TN1820

PC02
045-110
UN33

FALM1 317
PA 319
MJ 321
PAR 219
MJR 221

FALM0
PA-1 319
MJ-1 321
PAR-1 219
MJR-1 221

TO APPLICATION CKT

IRQIPP 307
ICOSP 306
ISCXP 308
ISCYP 309
ISCZP 310
IRQIPN 207
ICOSN 206
ISCXN 208
ISCYN 209
ISCZN 210

SCAN1-1 307
SCAN1-2 306
SCAN1-3 308
SCAN1-4 309
SCAN1-5 310
SCAN1-6 207
SCAN1-7 206
SCAN1-8 208
SCAN1-9 209
SCAN1-10 210

SD22P 550
SD23P 551
SC22P 552
SC23P 553
SC42P 554
SD22N 450
SD23N 451
SC22N 452
SC23N 453
SC42N 454

SCAN0-1 550
SCAN0-2 551
SCAN0-3 552
SCAN0-4 553
SCAN0-5 554
SCAN0-6 450
SCAN0-7 451
SCAN0-8 452
SCAN0-9 453
SCAN0-10 454

SD08P 333
SC08P 335
SD08N 233
SC08N 235

3BRST11 333
3BSCAN01 335
RSTR1 233
SCANR1 235

ED-3T076-20,G14A

SCANR1 300
RSTR1 302
3BSCAN01 301
3BRST11 312

SCANR
RSTR
3BSCAN0
3BRST1
036-011

COOLING UNIT
J5D003FH-2
SD-5D168-01

3BRST10 202
3BSCAN00 211
RSTR0 212
SCANR0 210

3BRST1
3BSCAN0
RSTR
SCANR
036-011

ED-3T076-20,G14

ED-3T076-20,G15D

ED-3T076-20,G15A

060-100 103
ED-3T076-50,G2

069-100 106
ED-3T076-50,G1

MODULAR FUSE FILTER UNIT
J5D003FJ-1
SD-5D190-01

PROC 0
J3T060AA-1
SD-3T011-01

CUPS
028-060
TN1821

IOPPS
019-080
TN1820

PC02
019-110
UN33

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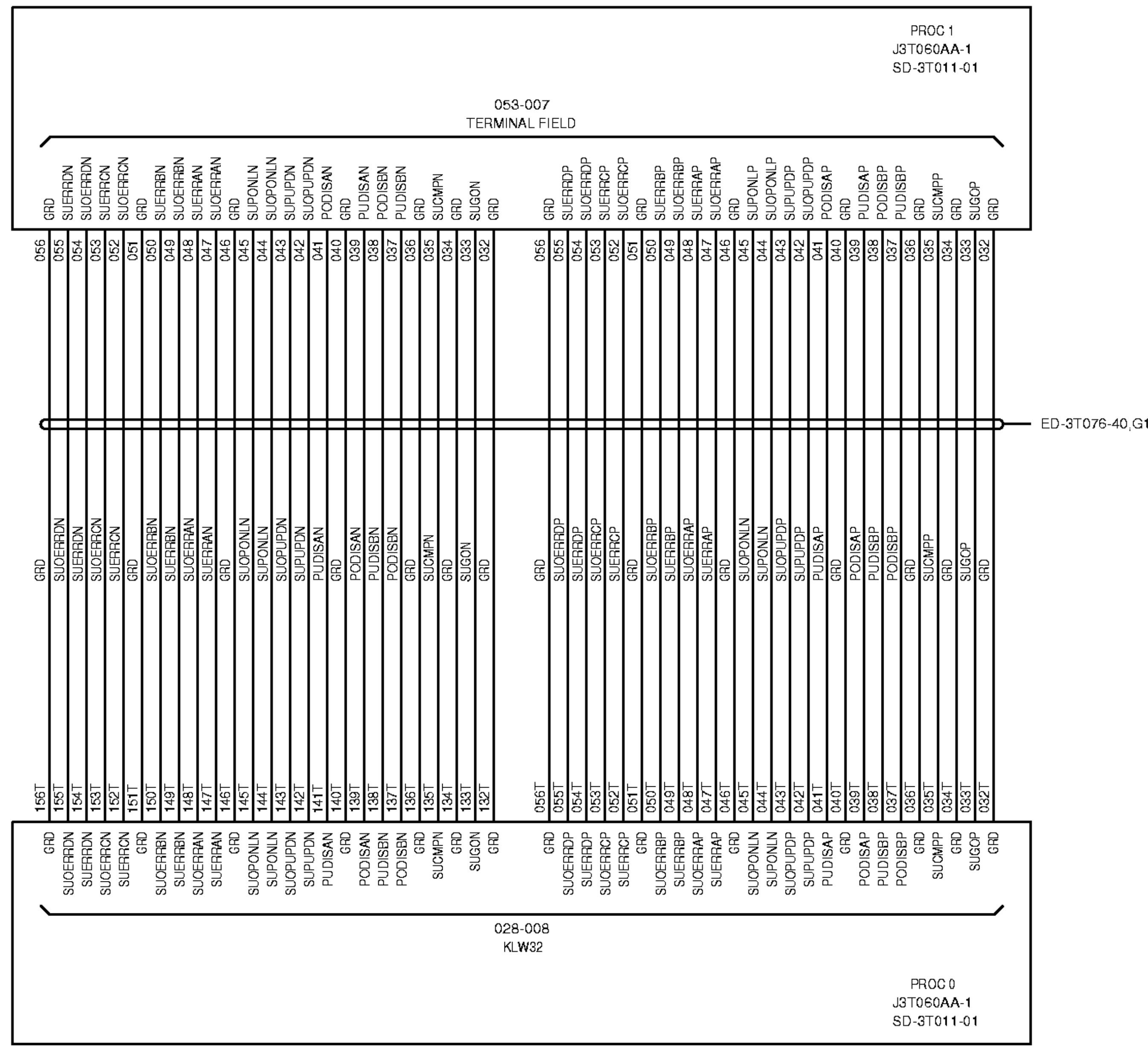
PART OF FS 2

MEMORY UPDATE INTERCONNECTION
1 OF 5 CABLES



3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	1

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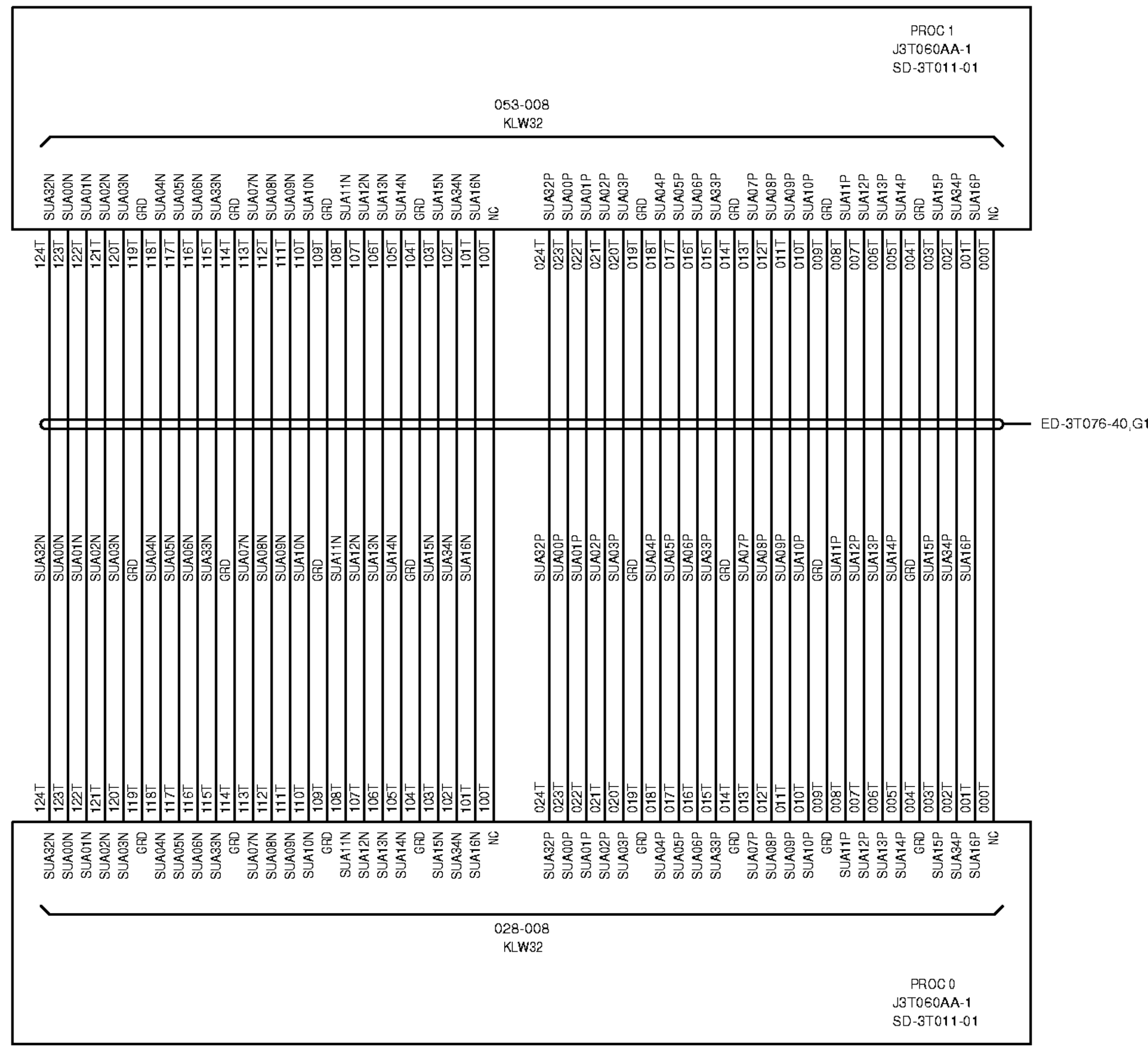
PART OF FS 2

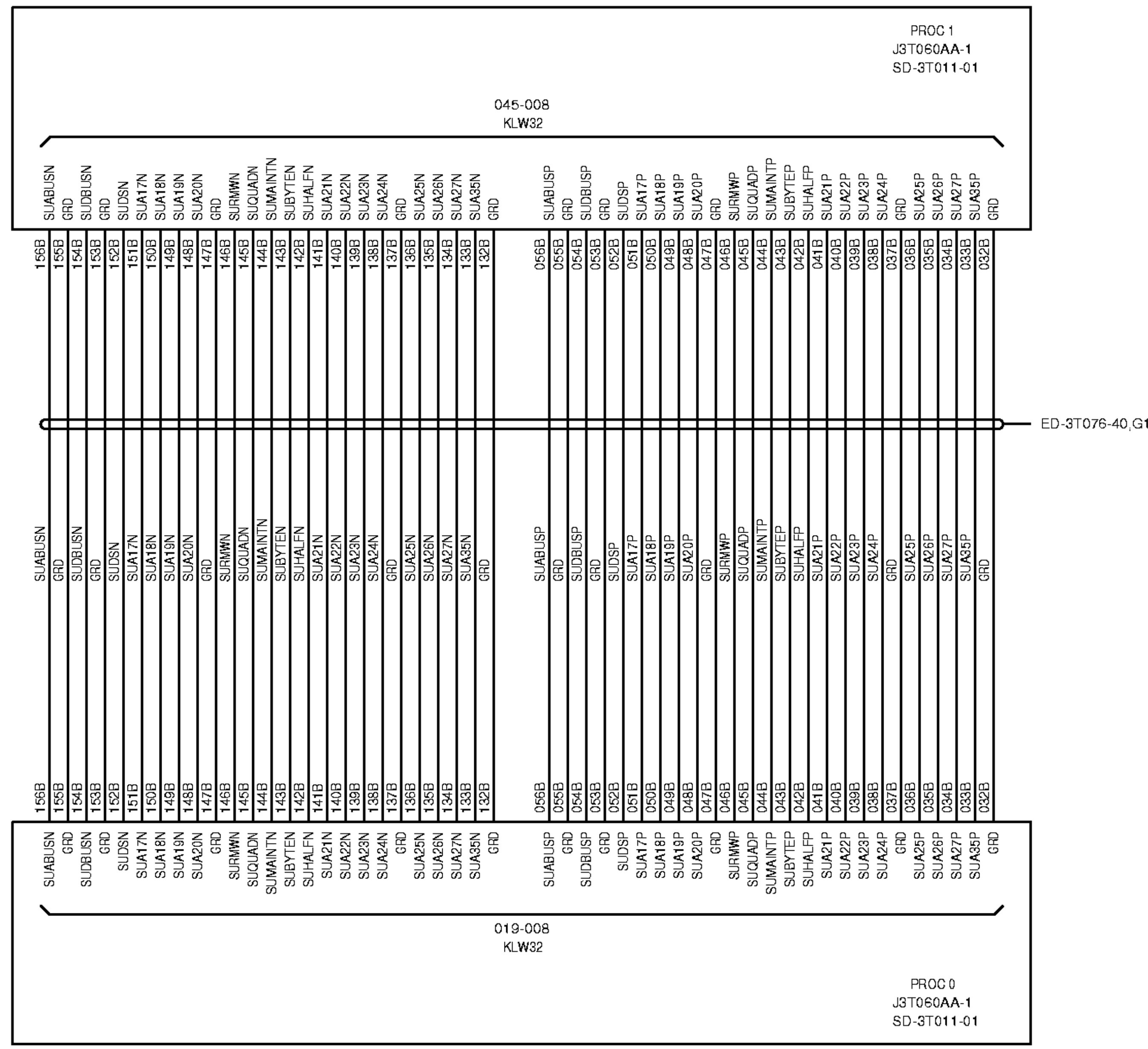
MEMORY UPDATE INTERCONNECTION
2 OF 5 CABLES



3B21D PROCESSOR COMPUTER SYSTEMS	DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01	SHEET B13

PART OF FS 2

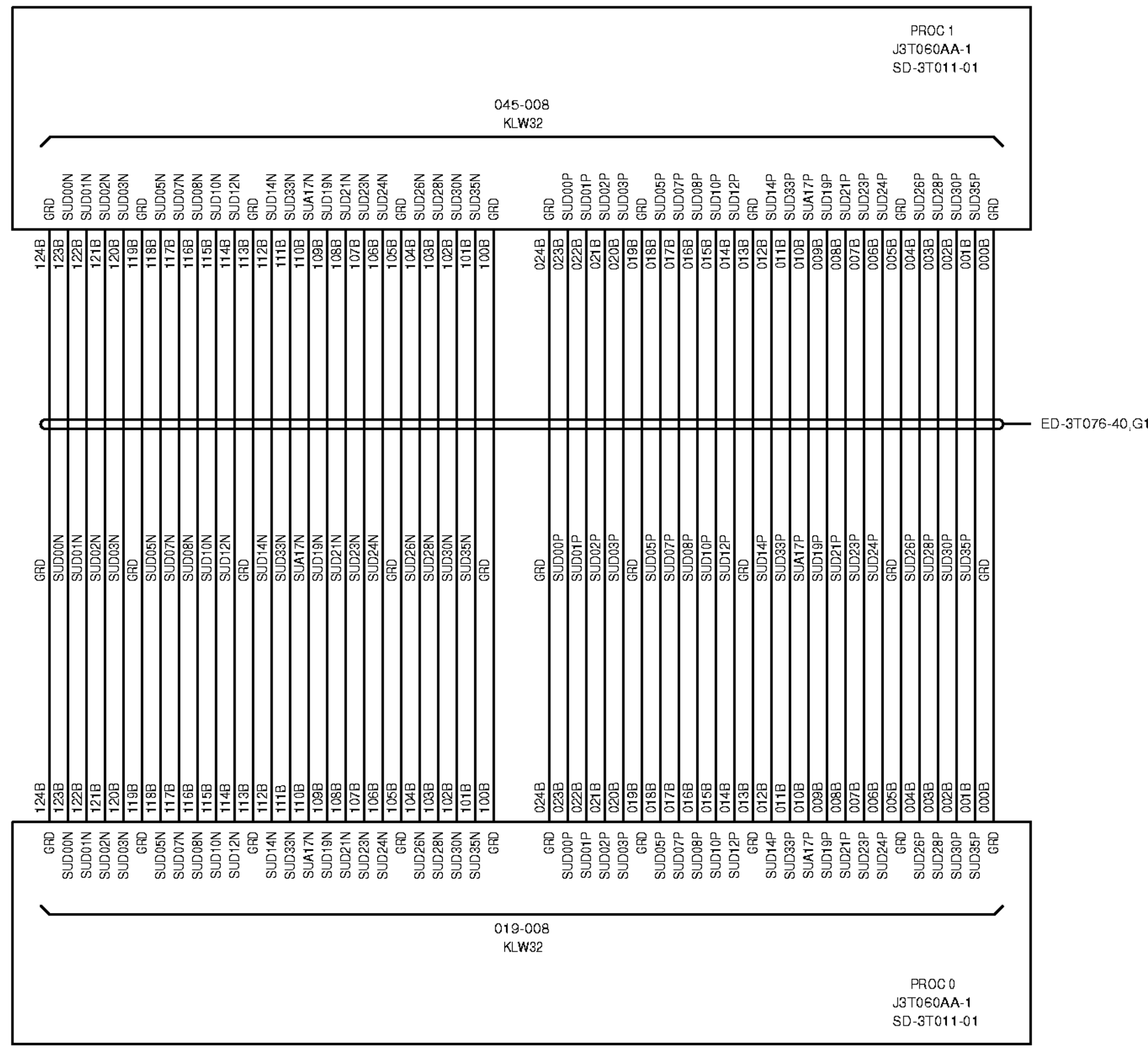
MEMORY UPDATE INTERCONNECTION
3 OF 5 CABLES



3B21D PROCESSOR COMPUTER SYSTEMS	DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01	SHEET B14

PART OF FS 2

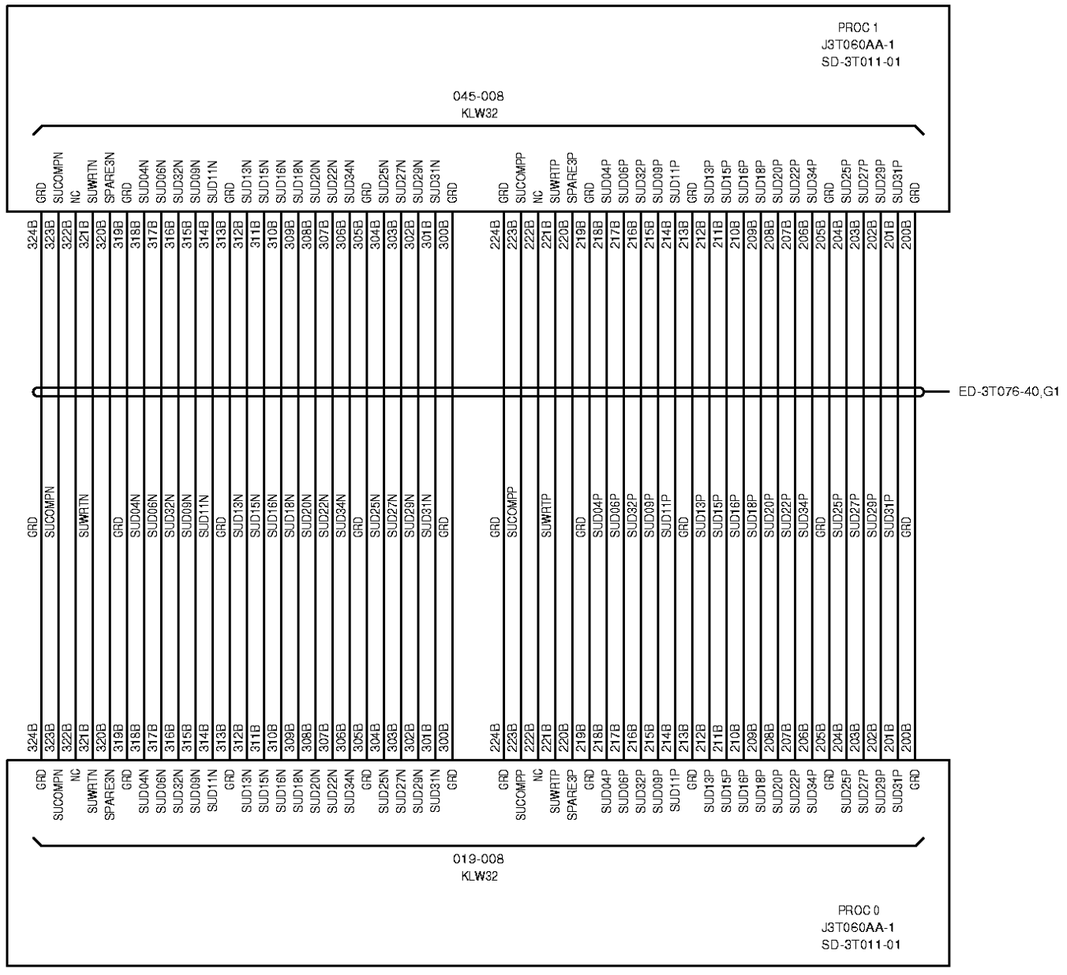
MEMORY UPDATE INTERCONNECTION
4 OF 5 CABLES



3B21D PROCESSOR COMPUTER SYSTEMS	DWG SIZE C2	ISSUE 1
AT&T SD-3T015-01		SHEET B15

PART OF FS 2

MEMORY UPDATE INTERCONNECTION
5 OF 5 CABLES



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
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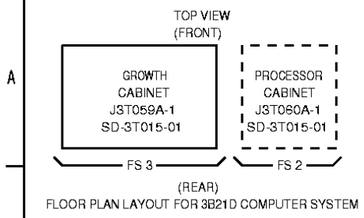
PART OF FS 3



FLOOR PLAN LAYOUT FOR 3B21D COMPUTER SYSTEM

3B21D COMPUTER SYSTEM
GROWTH CABINET
(CSPGC0 OR CSPGC1)

SCSI
9-TRACK TAPE DRIVE
KS-23909
(1ST OR 3RD UNIT)

SCSI BUS CABLE
ED-3T076-40 (SEE FS 1)

TO
PROCESSOR CABINET

SCSI
9-TRACK TAPE DRIVE
KS-23909
(2ND OR 4TH UNIT)

SCSI BUS CABLE
ED-3T076-40 (SEE FS 1)

TO
PROCESSOR CABINET

1ST OR 2ND PERIPHERAL
GROWTH CABINET
J3T059A-1
SD-3T015-01
(CSPGC0 OR CSPGC1)

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET B17

APPARATUS FIGURE SUMMARY

FEATURE OR OPTION	APP FIG.	QUANTITY	UNIT EQUIP DATA	CABINET EQUIP DATA	SYSTEM EQUIP DATA
3B21D COMPUTER PROCESSOR CABINET ARRANGED FOR: UP TO 48MB OF MAIN MEMORY, 3 DISK FILE CONTROLLERS (DFC0-2), DIRECT MEMORY ACCESS 0 AND 1 (DMA0 & DMA1), 2 I/O PROCESSORS (IOP0 & IOP1), EACH WITH 4 PC COMMUNITIES (COMM0 - COMM3); (COMM0 - COMM2) ARRANGED FOR UP TO 4 PERIPHERAL CONTROL (PC) CIRCUIT PACKS AND (COMM3) ARRANGED FOR 3 (PC) CIRCUIT PACKS OR 1 (PC) CIRCUIT PACK AND 1 SCSI PERIPHERAL UNIT; 1 UNILITY CIRCUIT(UC), EQUIPPED WITH DIRECT MEMORY ACCESS 0 (DMA0); 2 DISK FILE CONTROLLERS (DFC0 & DFC1), DISKS 0 AND 1; ONE PORT SWITCH SCANNER DISTRIBUTOR; IOP0 AND IOP1 COMMUNITY 0 E/W PC00 (MTTY) AND PC02 (SCSD).	1	2	J3T060AA-1,L1, LWA	J3T060A-1,L1	J3T061A-1,L1
		1	J5D003FH-2,L1		
		1	J5D003FJ-1,L105		
		1	ED-5D471-70,G1		
IOP2-SPU GROWTH UNIT ARRANGED FOR IOP2 WITH 4 COMMUNITIES OR MAXIMUM 5 SCSI PERIPHERAL UNITS (SPU) AND 2 COMMUNITIES OR DFC2, MAXIMUM 4 SPU'S AND 2 COMMUNITIES; EACH COMMUNITY ARRANGED FOR 4 PC SLOTS.	2	1	J3T060AB-1	J3T060A-1,L2	J3T061A-1,L2
IOP3-SPU GROWTH UNIT ARRANGED FOR IOP3 WITH 4 COMMUNITIES OR MAXIMUM 5 SCSI PERIPHERAL UNITS (SPU) AND 2 COMMUNITIES; EACH COMMUNITY ARRANGED FOR 4 PC SLOTS.	3	1	J3T060AB-1	J3T060A-1,L3	J3T061A-1,L3
DIRECT MEMORY ACCESS 1 (DMA1) OPTION, DUPLICATED.	5	2	KBN15		J3T060A-1,L5
UTILITY CIRCUIT (UC) OPTION, DUPLICATED.	6	2	UN379		J3T060A-1,L6
5V POWER, DUPLICATED, (MAX. 2)	9	2	410AA		J3T060A-1,L9
5V POWER FOR IOP 0 & 1 COMMUNITIES 2 & 3. (1 PER IOP, MAX 2.)	10	1	410AA		J3T061A-1,L10
60HZ MAINTENANCE COLOR VIDEO TERMINAL (MTTY)	11	1	KS-23996,L1		J3T061A-1,L11
50HZ MAINTENANCE COLOR VIDEO TERMINAL (MTTY)	12	1	KS-23996,L5		J3T061A-1,L12
ADDITIONAL 60HZ MAINTENANCE TERMINAL WITH 100 FT. OF CABLE.	13	1	KS-23996,L1		J3T061A-1,L13
ADDITIONAL 50HZ MAINTENANCE TERMINAL WITH 100 FT. OF CABLE.	14	1	KS-23996,L5		J3T061A-1,L14
60HZ 577 READ ONLY PRINTER (ROP)	15	1			J3T061A-1,L15
50HZ 577 READ ONLY PRINTER (ROP)	16	1			J3T061A-1,L16
DUAL SERIAL CHANNEL, BOUNDARY SCAN AND SCAN/SD CABLES FOR IOP2	17	1	ED-3T076-20,G1H, G1J,G6,G18	J3T060A-1,LN	J3T061A-1,L17
5V POWER FOR COMMUNITIES 2 AND 3 PC SLOTS 20-23 AND 30-33. (MAX. 1) FOR GROWTH UNIT 0 (IOP2)	18	1	410AA		J3T061A-1,L18
DUAL SERIAL CHANNEL, BOUNDARY SCAN AND SCAN/SD CABLES FOR IOP3	19	1	ED-3T076-20,G1K, G1L,G6A,G18A	J3T060A-1,LP	J3T061A-1,L19
5V POWER FOR COMMUNITIES 2 AND 3 PC 5 SLOTS 20-23 AND 30-33. (MAX. 1) FOR GROWTH UNIT 1 (IOP3)	20	1	410AA		J3T061A-1,L20
32MB OF MAIN MEMORY (DUPLICATED).	21	2	KLW32		J3T061A-1,L21
40MB OF MAIN MEMORY (DUPLICATED).	22	2	KLW40		J3T061A-1,L22
48MB OF MAIN MEMORY (DUPLICATED).	23	2	KLW48		J3T061A-1,L23

FEATURE OR OPTION		APP FIG.	QUANTITY	UNIT EQUIP DATA	CABINET EQUIP DATA	SYSTEM EQUIP DATA
DUAL SERIAL CHANNEL, AND SCAN/SD CABLES FOR DFC2		24	1	J3T076-20,G1M, G1N,G18B	J3T060A-1,LS	J3T061A-1,L24
SCANNER SIGNAL DISTRIBUTOR PERIPHERAL CONTROLLER (PC) CIRCUIT PACK, NOT DUPLICATED.		100	1	UN33D		J3T061A-1,L100
TTY/ROP (PC) CIRCUIT PACK, NOT DUPLICATED.		101	1	MC4C011-A1B/ TN74B		J3T061A-1,L101
SYNCHRONOUS LINK (PC) CIRCUIT PACK.		102	1	TN1839		J3T061A-1,L102
BX.25 HIGH SPEED 56KPS DATA LINK (PC) CIRCUIT PACK, NOT DUPLICATED.		103	1	MC4C052-A1E/ TN82B		J3T061A-1,L103
MAGNETIC TAPE UNIT CIRCUIT PACK.		104	1	UN376		J3T061A-1,L104
1GB SCSI DISK UNIT CIRCUIT PACK.		105	1	UN375		J3T061A-1,L105
SYNCHRONOUS LINK (PC) CIRCUIT PACK FOR U.S. APPLICATIONS, NOT DUPLICATED.		106	1	MC4C048-A1B/ TN75C		J3T061A-1,L106
64K BIT/SEC INTERFACE CONTROLLER CIRCUIT PACK, NOT DUPLICATED.		107	1	TN1420		J3T061A-1,L107
1ST GROWTH PIC CABINET ARRANGED FOR 1ST & 2ND SCSI TAPE UNITS.	1 PERIPHERAL GROWTH CABINET ARR. FOR 1 OR 2 9 TRACK SCSI TAPE UNITS.	200	1	ED-5D471-70,G1	J3T059A-1,L1	J3T061A-1,L200
	1 60HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2).	201	1	KS-23909,L10	J3T059A-1,L3	J3T061A-1,L201
2ND GROWTH PIC CABINET ARRANGED FOR 3RD & 4TH SCSI TAPE UNITS.	1 50HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2).	202	1	KS-23909,L10	J3T059A-1,L4	J3T061A-1,L202
SCAN/SD CABLE AND SCSI BUS JUMPER FOR SPU04.		B	1	ED-3T076-20,G17	J3T060A-1,LA	J3T061A-1,LB
SCAN/SD CABLE AND SCSI BUS JUMPER FOR SPU05.		C	1	ED-3T076-20,G17A	J3T060A-1,LB	J3T061A-1,LC
SCAN/SD CABLE CABLE FOR SPU18.		D	1	ED-3T076-20,G17B	J3T060A-1,LC	J3T061A-1,LD
SCAN/SD CABLE CABLE FOR SPU19.		E	1	ED-3T076-20,G17C	J3T060A-1,LD	J3T061A-1,LE

(CONT.)

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE C2 | ISSUE 2B

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APPARATUS FIGURE SUMMARY

(CONT.)

FEATURE OR OPTION	APP FIG.	QUANTITY	UNIT EQUIP DATA	CABINET EQUIP DATA	SYSTEM EQUIP DATA
SCAN/SD CABLE AND SCSI BUS 0 JUMPER FOR SPU20.	F	1	ED-3T076-20,G17D	J3T060A-1,LE	J3T061A-1,LF
SCAN/SD CABLE AND SCSI BUS 1 JUMPER FOR SPU21.	G	1	ED-3T076-20,G17E	J3T060A-1,LF	J3T061A-1,LG
SCAN/SD CABLE AND SCSI BUS 2 JUMPER FOR SPU22.	H	1	ED-3T076-20,G17F	J3T060A-1,LG	J3T061A-1,LH
SCAN/SD CABLE AND SCSI BUS 3 JUMPER FOR SPU23.	J	1	ED-3T076-20,G17G	J3T060A-1,LH	J3T061A-1,LJ
SCAN/SD CABLE AND SCSI BUS 0 JUMPER FOR SPU24.	K	1	ED-3T076-20,G17H	J3T060A-1,LJ	J3T061A-1,LK
SCAN/SD CABLE AND SCSI BUS 1 JUMPER FOR SPU25.	L	1	ED-3T076-20,G17J	J3T060A-1,LK	J3T061A-1,LL
SCAN/SD CABLE AND SCSI BUS 2 JUMPER FOR SPU26.	M	1	ED-3T076-20,G17K	J3T060A-1,LL	J3T061A-1,LM
SCAN/SD CABLE AND SCSI BUS 3 JUMPER FOR SPU27.	N	1	ED-3T076-20,G17L	J3T060A-1,LM	J3T061A-1,LN
SCSI BUS EXT. CABLE WHEN SPU19, SPU23 & SPU27 ARE CONNECTED TO SCSI BUS 1 (DFC-1).	R	1	ED-3T076-40,G4E		J3T061A-1,LR
SCSI BUS EXT. CABLE WHEN SPU18, SPU22 & SPU26 ARE CONNECTED TO SCSI BUS 2 (DFC-0).	S	1	ED-3T076-40,G4A		J3T061A-1,LS
SCSI BUS EXT. CABLE WHEN SPU19, SPU23 & SPU27 ARE CONNECTED TO SCSI BUS 3 (DFC-1).	T	1	ED-3T076-40,G4C		J3T061A-1,LT
SCSI BUS EXT. CABLE WHEN SPU20 & SPU24 ARE CONNECTED TO SCSI BUS 0 (DFC-0).	U	1	ED-3T076-40,G4		J3T061A-1,LU
SCSI BUS EXT. CABLE WHEN SPU21 & SPU25 ARE CONNECTED TO SCSI BUS 1 (DFC-1).	V	1	ED-3T076-40,G4B		J3T061A-1,LV
SCSI BUS EXT. CABLE WHEN SPU21 & SPU25 ARE CONNECTED TO SCSI BUS 0 (DFC-0).	W	1	ED-3T076-40,G4D		J3T061A-1,LW
TAPE UNIT CABLE FOR (CSPGC0) CABINET.	X	1	ED-3T076-40,G100		J3T061A-1,LX
TAPE UNIT CABLE FOR (CSPGC1) CABINET.	Y	1	ED-3T076-40,G101		J3T061A-1,LY
INTERRUPT SOURCE BIT WIRING FOR 5ESS®	AM	1	J3T060AA-1,LWB	J3T060AA-1,LT	J3T061A-1,LAM
INTERRUPT SOURCE BIT WIRING FOR STP/1NCP.	AN	1	J3T060AA-1,LWC	J3T060AA-1,LU	J3T061A-1,LAN
1 50FT. CABLE BETWEEN PORT SWITCH AND MAINTENANCE TERMINAL (MTTY).	CA	1	ED-3T076-20,G7B		J3T061A-1,LCA
1 100FT. CABLE BETWEEN PORT SWITCH AND MAINTENANCE TERMINAL (MTTY).	CB	1	ED-3T076-20,G7D		J3T061A-1,LCB
1 250FT. CABLE BETWEEN PORT SWITCH AND MAINTENANCE TERMINAL (MTTY).	CC	1	ED-3T076-20,G7F		J3T061A-1,LCC
1 50FT. CABLE BETWEEN PORT SWITCH AND THE PRINTER (ROP).	CD	1	ED-3T076-20,G7C		J3T061A-1,LCD
1 100FT. CABLE BETWEEN PORT SWITCH AND THE PRINTER (ROP).	CE	1	ED-3T076-20,G7E		J3T061A-1,LCE
1 250FT. CABLE BETWEEN PORT SWITCH AND THE PRINTER (ROP).	CF	1	ED-3T076-20,G7G		J3T061A-1,LCF

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE: C2 | ISSUE: 2B

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CIRCUIT NOTES:

101.

DESIG	FUSE AMP	POTENTIAL	ONE PER
BATTERY SYMBOL			VOLTAGE RANGE

CIRCUIT NOTES: (CONT.)

102. UN33B SCANNER/SIGNAL DISTRIBUTOR CONTROLLER CIRCUIT PACK.

CONSISTS OF CIRCUITRY FOR MONITORING 48 SCAN POINTS AND CONTROLLING 32 DISTRIBUTE POINTS. CONNECTION TO OTHER CIRCUITS IS LIMITED TO 1000 FEET. CONNECTION FROM THE UN33B TO NON-3B S/D POINTS SHOULD BE MADE THROUGH AN S/D INTERFACE IN THE PORT SWITCH UNIT (UN377).
THIS IS AN ISOLATED PC.

PC UN33B SCSD TERMINAL STRIP CABLING OPTIONS:

2 SD POINTS, 2 SCAN POINTS
USE 2X4 982AB

133,333,533,0(7)33
137,337,537,0(7)37
146,346,546,0(7)46
150,350,550,0(7)50

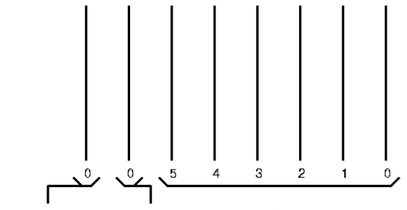
2 SD POINTS, 4 SCAN POINTS
USE 2X6 982AC

137,337,537,0(7)37
150,350,550,0(7)50

4 SCAN POINTS
USE 2X4 982AB

139,339,539,0(7)39
152,352,552,0(7)52

NUMBERING OF PC SLOTS



HORZ. LOCATION TYP.

IF PC SLOT IS 125
TERM. STRIP 0(6) IS 131
TERM. STRIP 0(7) IS 132

SCAN POINT ASSIGNMENTS AVAILABLE ON EACH UN33D CIRCUIT PACK

	0	0	5	4	3	2	1	0	
56			*	*					56
55	SC47P	SC47N	SC43P	SC43N	SC39P	SC39N	SC35P	SC35N	55
54	SC46P	SC46N	SC42P	SC42N	SC38P	SC38N	SC34P	SC34N	54
53	SC31P	SC31N	SC23P	SC23N	SC15P	SC15N	SC07P	SC07N	53
52	SC30P	SC30N	SC22P	SC22N	SC14P	SC14N	SC06P	SC06N	52
51	SD31P	SD31N	SD23P	SD23N	SD15P	SD15N	SD07P	SD07N	51
50	SD30P	SD30N	SD22P	SD22N	SD14P	SD14N	SD06P	SD06N	50
49	SC29P	SC29N	SC21P	SC21N	SC13P	SC13N	SC05P	SC05N	49
48	SC28P	SC28N	SC20P	SC20N	SC12P	SC12N	SC04P	SC04N	48
47	SD29P	SD29N	SD21P	SD21N	SD13P	SD13N	SD05P	SD05N	47
46	SD28P	SD28N	SD20P	SD20N	SD12P	SD12N	SD04P	SD04N	46
45			-48V	-48R	GRD	GRD	GRD	GRD	45
44			-48V3	-48R	+12E	+12E	-12E	-12E	44
43			*	*					43
42	SC45P	SC45N	SC41P	SC41N	SC37P	SC37N	SC33P	SC33N	42
41	SC44P	SC44N	SC40P	SC40N	SC36P	SC36N	SC32P	SC32N	41
40	SC27P	SC27N	SC19P	SC19N	SC11P	SC11N	SC03P	SC03N	40
39	SC26P	SC26N	SC18P	SC18N	SC10P	SC10N	SC02P	SC02N	39
38	SD27P	SD27N	SD19P	SD19N	SD11P	SD11N	SD03P	SD03N	38
37	SD26P	SD26N	SD18P	SD18N	SD10P	SD10N	SD02P	SD02N	37
36	SC25P	SC25N	SC17P	SC17N	SD09P	SD09N	SC01P	SC01N	36
35	SC24P	SC24N	SC16P	SC16N	SC08P	SC08N	SC00P	SC00N	35
34	SD25P	SD25N	SD17P	SD17N	SD09P	SD09N	SD01P	SD01N	34
33	SD24P	SD24N	SD16P	SD16N	SD08P	SD08N	SD00P	SD00N	33
32			*	GRD	GRD	GRD	GRD	GRD	32
	0(7)	0(6)	5	4	3	2	1	0	

* RESERVED FOR BOUNDARY SCAN ACCESS

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE C2 | ISSUE 1

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CIRCUIT NOTES (CONT):

103. FOR THE SCAN-SD POINTS THAT ARE NOT FIXED FOR 3B21D OPERATION CODE UN33D, SEE TABLES AS FOLLOWS:

TABLE	DESCRIPTION	CABINET	EQL
A	ASSIGNED SCAN POINTS FOR 3B21D	PROCESSOR	19-110
B	ASSIGNED SCAN POINTS FOR 3B21D	PROCESSOR	45-110
C	ASSIGNED SCAN POINTS FOR 3B21D	PROCESSOR	28-130

TABLE A

J3T060A-1, IOP 0; PC SLOT 02; EQL 19-110

	0 (7)	0 (6)	5	4	3	2	1	0	
56	---	---	---	---	---	---	---	---	56
55									55
54	PROC0 Z	PROC0 Z	IOP1 Z	IOP1 Z					54
53	PROC0 X	PROC0 X	IOP1 X	IOP1 X					53
52	PROC0 Y	PROC0 Y	IOP1 Y	IOP1 Y					52
51	PROC0 RQIP	PROC0 RQIP	IOP1 RQIP	IOP1 RQIP					51
50	PROC0 OOS	PROC0 OOS	IOP1 OOS	IOP1 OOS					50
49	DFC0 Y	DFC0 Y	IOP2 X	IOP2 X					49
48	DFC0 X	DFC0 X	IOP2 Y	IOP2 Y					48
47	DFC0 RQIP	DFC0 RQIP	IOP2 RQIP	IOP2 RQIP					47
46	DFC0 OOS	DFC0 OOS	IOP2 OOS	IOP2 OOS					46
45	---	---	---	---	---	---	---	---	45
44									44
43	---	---	---	---	---	---	---	---	43
42									42
41									41
40	SPU00 Y	SPU00 Y	SPU04 Y	SPU04 Y					40
39	SPU00 X	SPU00 X	SPU04 X	SPU04 X					39
38	SPU00 RQIP	SPU00 RQIP	SPU04 RQIP	SPU04 RQIP					38
37	SPU00 OOS	SPU00 OOS	SPU04 OOS	SPU04 OOS					37
36	SPU02 Y	SPU02 Y	SPU54 Y	SPU54 Y					36
35	SPU02 X	SPU02 X	SPU54 X	SPU54 X	3BFAN FAN	3BFAN FAN			35
34	SPU02 RQIP	SPU02 RQIP	SPU54 RQIP	SPU54 RQIP	+	+			34
33	SPU02 OOS	SPU02 OOS	SPU54 OOS	SPU54 OOS	3BFAN RST	3BFAN RST			33
32	---	---	---	---	---	---	---	---	32
	0(7)	0(6)	5	4	3	2	1	0	

+ = INACCESSIBLE
SPU = SCSI PERIPHERAL UNIT

TABLE B

J3T060A-1, IOP 1; PC SLOT 02; EQL 45-110

	0 (7)	0 (6)	5	4	3	2	1	0	
56	---	---	---	---	---	---	---	---	56
55	MTTY A	MTTY A	ROP A	ROP A					55
54	PROC1 Z	PROC1 Z	IOP0 Z	IOP0 Z					54
53	PROC1 X	PROC1 X	IOP0 X	IOP0 X					53
52	PROC1 Y	PROC1 Y	IOP0 Y	IOP0 Y					52
51	PROC1 RQIP	PROC1 RQIP	IOP0 RQIP	IOP0 RQIP					51
50	PROC1 OOS	PROC1 OOS	IOP0 OOS	IOP0 OOS					50
49	DFC1 Y	DFC1 Y	IOP3 X	IOP3 X					49
48	DFC1 X	DFC1 X	IOP3 Y	IOP3 Y					48
47	DFC1 RQIP	DFC1 RQIP	IOP3 RQIP	IOP3 RQIP					47
46	DFC1 OOS	DFC1 OOS	IOP3 OOS	IOP3 OOS					46
45	---	---	---	---	---	---	---	---	45
44									44
43	---	---	---	---	---	---	---	---	43
42	MTTY B	MTTY B	ROP B	ROP B					42
41	MTTY C	MTTY C	ROP C	ROP C					41
40	SPU01 Y	SPU01 Y	SPU05 Y	SPU05 Y					40
39	SPU01 X	SPU01 X	SPU05 X	SPU05 X					39
38	SPU01 RQIP	SPU01 RQIP	SPU05 RQIP	SPU05 RQIP					38
37	SPU01 OOS	SPU01 OOS	SPU05 OOS	SPU05 OOS					37
36	SPU03 Y	SPU03 Y							36
35	SPU03 X	SPU03 X			3BFAN FAN	3BFAN FAN			35
34	SPU03 RQIP	SPU03 RQIP			+	+			34
33	SPU03 OOS	SPU03 OOS			3BFAN RST	3BFAN RST			33
32	---	---	---	---	---	---	---	---	32
	0(7)	0(6)	5	4	3	2	1	0	

+ = INACCESSIBLE
SPU = SCSI PERIPHERAL UNIT

TABLE C

J3T060A-1, IOP 0; PC SLOT 30; EQL 28-130

	0 (7)	0 (6)	5	4	3	2	1	0	
56									56
55									55
54									54
53					SPU22 Y	SPU22 Y	SPU25 Y	SPU25 Y	53
52					SPU22 X	SPU22 X	SPU25 X	SPU25 X	52
51					SPU22 RQIP	SPU22 RQIP	SPU25 RQIP	SPU25 RQIP	51
50					SPU22 OOS	SPU22 OOS	SPU25 OOS	SPU25 OOS	50
49			DFC2 Y	DFC2 Y	SPU20 Y	SPU20 Y	SPU23 Y	SPU23 Y	49
48			DFC2 X	DFC2 X	SPU20 X	SPU20 X	SPU23 X	SPU23 X	48
47			DFC2 RQIP	DFC2 RQIP	SPU20 RQIP	SPU20 RQIP	SPU23 RQIP	SPU23 RQIP	47
46			DFC2 OOS	DFC2 OOS	SPU20 OOS	SPU20 OOS	SPU23 OOS	SPU23 OOS	46
45	---	---	---	---	---	---	---	---	45
44									44
43	---	---	---	---	---	---	---	---	43
42									42
41									41
40			SPU26 Y	SPU26 Y	SPU18 Y	SPU18 Y	SPU21 Y	SPU21 Y	40
39			SPU26 X	SPU26 X	SPU18 X	SPU18 X	SPU21 X	SPU21 X	39
38			SPU26 RQIP	SPU26 RQIP	SPU18 RQIP	SPU18 RQIP	SPU21 RQIP	SPU21 RQIP	38
37			SPU26 OOS	SPU26 OOS	SPU18 OOS	SPU18 OOS	SPU21 OOS	SPU21 OOS	37
36			SPU24 Y	SPU24 Y	SPU27 Y	SPU27 Y	SPU19 Y	SPU19 Y	36
35			SPU24 X	SPU24 X	SPU27 X	SPU27 X	SPU19 X	SPU19 X	35
34			SPU24 RQIP	SPU24 RQIP	SPU27 RQIP	SPU27 RQIP	SPU19 RQIP	SPU19 RQIP	34
33			SPU24 OOS	SPU24 OOS	SPU27 OOS	SPU27 OOS	SPU19 OOS	SPU19 OOS	33
32	---	---	---	---	---	---	---	---	32
	0(7)	0(6)	5	4	3	2	1	0	

SPU = SCSI PERIPHERAL UNIT

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET D2

PRINTED IN U.S.A

INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS,
CAPACITANCE VALUES ARE IN MICROFARADS,
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.

302.

FEATURE OR OPTION		PROVIDE		
		APP FIG	APP OR WRG	QUANTITY
3B21D PROCESSOR CABINET ARRANGED FOR 2 PROCESSOR UNITS AND 2 GROWTH UNITS	PROCESSOR CABINET	1		1
	PROCESSOR UNIT CU 0			
	PROCESSOR UNIT CU 1			
	GROWTH UNIT CU 0	2		
	GROWTH UNIT CU 1	3		
	DIRECT MEMORY ACCESS 1 (DMA1) OPTION DUPLICATED (KBN15)	5		2
	UTILITY CIRCUIT (UC) OPTION DUPLICATED (UN379)	6		
	5V POWER DUPLICATED (410AA)	9		
	5V POWER FOR COMM 2 & 3 (PC SLOTS 20-23, 30-32) PROCESSOR UNIT (410AA)	10		1
	60 HZ MTCE TTY TERM. COLOR (KS-23996,L1)	11		
	50 HZ MTCE TTY TERM. COLOR (KS-23996,L5)	12		
	ADDITIONAL 60 HZ MTCE TTY WITH 100 FT. CABLE (KS-23996,L1)	13		
	ADDITIONAL 50 HZ MTCE TTY WITH 100 FT. CABLE (KS-23996,L5)	14		
	60 HZ READ ONLY PRINTER (ROP) (577)	15		
	50 HZ READ ONLY PRINTER (ROP) (577)	16		
	5V POWER FOR COMM 2 & 3 (PC SLOTS 20-23, 30-33) FOR GROWTH UNIT 0 (IOP 2) (MAX. 1) (410AA)	18		
	5V POWER FOR COMM 2 & 3 (PC SLOTS 20-23, 30-33) FOR GROWTH UNIT 1 (IOP 3) (MAX. 1) (410AA)	20		

INFORMATION NOTES: (CONT.)

302. (CONT.)

FEATURE OR OPTION			PROVIDE		
			APP FIG	APP OR WRG	QUANTITY
3B21D PROCESSOR CABINET ARRANGED FOR 2 PROCESSOR UNITS AND 2 GROWTH UNITS (CONT.)	CIRCUIT PACKS	32 MB OF MAIN MEMORY DUPLICATED (KLW32)	21		2
		40 MB OF MAIN MEMORY DUPLICATED (KLW40)	22		
		48 MB OF MAIN MEMORY DUPLICATED (KLW48)	23		
		SCANNER SIGNAL DISTRIBUTOR PERIPHERAL CONTROLLER (PC) (UN33D)	100		1
		TTY/ROP PC (MC4C011A1B/TN74B)	101		
		SYNC LINK PC (TN1839)	102		
		BX.25 HIGH SPEED 56 KPS DATA LINK PC (MC4C052A1E/TN82B)	103		
		MAGNETIC TAPE UNIT (UN376)	104		
		1 GB SCSI DISC UNIT (UN375)	105		
		SYNC LINK PC FOR U.S. APPLICATION (MC4C048A1B/TN75C)	106		
		64 BIT/SEC. INTERFACE CONTROLLER (TN1420)	107		
	INTERRUPT SOURCE BIT WIRING FOR 5ESS		AM		1
	INTERRUPT SOURCE BIT WIRING FOR STP/1 NCP		AN		

INFORMATION NOTES: (CONT.)

302. (CONT.)

FEATURE OR OPTION		PROVIDE		
		APP FIG	APP OR WRG	QUANTITY
3B21D 1ST GROWTH PIC CABINET ARRANGED FOR 1ST AND 2ND SCSI TAPE UNITS	ONE GROWTH CABINET ARRANGED FOR 1 OR 2 9-TRACK SCSI TAPE UNITS (ED-5D471-70,G1)	200		1
	ONE 60 HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2) (KS-23909,L10)	201		
	ONE 50 HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2) (KS-23909,L10)	202		
3B21D 2ND GROWTH PIC CABINET ARRANGED FOR 3RD AND 4TH SCSI TAPE UNITS	ONE GROWTH CABINET ARRANGED FOR 1 OR 2 9-TRACK SCSI TAPE UNITS (ED-5D471-70,G1)	200		1
	ONE 60 HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2) (KS-23909,L10)	201		
	ONE 50 HZ 1600/6250 BPI, 125 IPS TAPE UNIT WITH SCSI INTERFACE (MAX. 2) (KS-23909,L10)	202		

INFORMATION NOTES: (CONT.)

303.

RECORD OF FIGURES, WIRING AND APPARATUS CHANGES						
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT		
				STD	A&M	MD

304.

		FROM			TO				
TITLE	FUNCTION	CABINET OR UNIT	UNIT SD	EQL - TERM	CABINET OR UNIT	EQL - TERM	UNIT SD	CABLE DRAWING NO.	J3T061A-1 LIST NO.
PROCESSOR CABINET 48V POWER AND FUSE ALARM (FORMED CABLES)	POWER & ALARM	PROC 0	SD-3T011-01	(NOTE 1)	FUSE UNIT	(NOTE 1)	SD-5D190-01	ED-3T076-50,G1	,L1
		PROC 1						ED-3T076-50,G2	
		GROWTH - IOP2/SPU	SD-3T012-01					ED-3T076-50,G3	
		GROWTH - IOP3/SPU						ED-3T076-50,G4	

NOTE:

1. ED3T076-50,G1,G2,G3 & G4 ARE FORMED CABLE ASSEMBLIES. TO IDENTIFY EQL AND PIN NO./LUG NAME, SEE TCJ3T060A-1 DRAWING. SEE NOTE 313 FOR POWER CABLE LEADS BETWEEN FUSE AND UNIT LUGS.

INFORMATION NOTES: (CONT.)

305.

		FROM			TO					
TITLE	FUNCTION	CABINET OR UNIT	UNIT SD	EQL - TERM	CABINET OR UNIT	EQL - TERM	UNIT SD	CABLE DRAWING NO.	J3T061A-1 LIST NO.
3B21D PROCESSOR CABINET DUAL SERIAL CHANNEL CABLES	PROC 0/1 UNIT DSCH	PROC 0, DFC 0	SD-3T011-01	028-178-106	PROC 0, DMA 0	028-075-338	SD-3T011-01	ED-3T076-20,G1	
		PROC 1, DFC 1		053-178-106	PROC 0, DMA 0	028-075-306		ED-3T076-20,G1A	
		PROC 0, IOP 0		019-065-506	PROC 0, DMA 0	028-075-351		ED-3T076-20,G1B	
		PROC 1, IOP 1		045-065-506	PROC 0, DMA 0	028-075-319		ED-3T076-20,G1C	
		PROC 0, DFC 0		028-178-119	PROC 1, DMA 0	053-075-338		ED-3T076-20,G1D	
		PROC 1, DFC 1		053-178-119	PROC 1, DMA 0	053-075-306		ED-3T076-20,G1E	
		PROC 0, IOP 0		019-065-706	PROC 1, DMA 0	053-075-351		ED-3T076-20,G1F	
		PROC 1, IOP 1		045-065-706	PROC 1, DMA 0	053-075-319		ED-3T076-20,G1G	
	GROWTH UNITS IOP 2 & 3	IOP 2 - SPU	SD-3T012-01	011-011-506	PROC 0, DMA 0	028-075-345		ED-3T076-20,G1H	,L17
		IOP 2 - SPU		011-011-706	PROC 1, DMA 0	053-075-345		ED-3T076-20,G1J	,L17
		IOP 3 - SPU		062-011-506	PROC 0, DMA 0	028-075-313		ED-3T076-20,G1K	,L19
		IOP 3 - SPU		062-011-706	PROC 1, DMA 0	053-075-313		ED-3T076-20,G1L	,L19
		IOP 2 - DFC 2		011-180-106	PROC 0, DMA 0	028-075-332		ED-3T076-20,G1M	,L24
		IOP 2 - DFC 2		011-180-119	PROC 1, DMA 0	053-075-332		ED-3T076-20,G1N	,L24
MTTY-ROP CONTROL CABLES	TN983 MTTYC	PROC 0, PC00	SD-3T011-01	019-094-345	PROC 1, UN377	045-186-345		ED-3T076-20,G2	
		PROC 0, PC00		019-094-132		045-186-145		ED-3T076-20,G2A	
		PROC 1, PC00		045-094-345		045-186-351		ED-3T076-20,G2B	
		PROC 1, PC00		045-094-132		045-186-151		ED-3T076-20,G2C	
EMERGENCY ACTION INTERFACE (EAI)		PROC 0, PC00		019-094-153	PROC 0, KLW31	019-038-500		ED-3T076-20,G3	
		PROC 0, PC00		019-094-149	PROC 1, KLW31	045-038-500		ED-3T076-20,G3A	
		PROC 1, PC00		045-094-149	PROC 1, KLW31	045-038-300		ED-3T076-20,G3B	
		PROC 1, PC00		045-094-153	PROC 0, KLW31	019-038-300		ED-3T076-20,G3C	
3B21D PROCESSOR CABINET CABLES	BOUNDARY SCAN	PROC 0, KLW31	SD-3T011-01	019-038-506	PROC 1, TN1820	045-080-132		ED-3T076-20,G4	
		PROC 1, KLW31		045-038-506	PROC 0, TN1820	019-080-132		ED-3T076-20,G4A	
	MAINT. CH.	PROC 0, KLW31		019-038-100	PROC 1, KLW31	045-038-100		ED-3T076-20,G5	
	BOUNDARY SCAN	PROC 0, TN1820		019-080-151	IOP 2, TN1820	011-026-132	SD-3T012-01	ED-3T076-20,G6	,L17
		PROC 1, TN1820		045-080-151	IOP 3, TN1820	062-026-132		ED-3T076-20,G6A	,L19
	MTTY-ROP CABLES 50 FEET	PROC 1, UN377		045-186-332	MTTY	—	—	ED-3T076-20,G7B	,LCA
	50 FEET	PROC 1, UN377		045-186-132	ROP	—	—	ED-3T076-20,G7C	,LCD
	100 FEET	PROC 1, UN377		045-186-332	MTTY	—	—	ED-3T076-20,G7D	,LCB
	100 FEET	PROC 1, UN377		045-186-132	ROP	—	—	ED-3T076-20,G7E	,LCE
	250 FEET	PROC 1, UN377		045-186-332	MTTY	—	—	ED-3T076-20,G7F	,LCC
	250 FEET	PROC 1, UN377		045-186-132	ROP	—	—	ED-3T076-20,G7G	,LCF
MTTY-ROP CONTROL CABLES	UN583 MTTYC	PROC 0, PC0D	SD-3T011-01	019-094-132	PROC 1,UN377	045-186-345	SD-3T011-01	ED-3T076-20,G2D	
		PROC 0, PC0D		019-094-332		045-186-145		ED-3T076-20,G2E	
		PROC 1, PC0D		045-094-132		045-186-351		ED-3T076-20,G2F	
		PROC 1, PC0D		045-094-332		045-186-151		ED-3T076-20,G2G	
EMERGENCY ACTION INTERFACE (EAI)		PROC 0, PC0D		019-094-317	PROC 0,KLW31	019-038-500		ED-3T076-20,G33	
		PROC 0, PC0D		045-094-117	PROC 1,KLW31	045-038-300		ED-3T076-20,G33A	
		PROC 1, PC0D		019-094-120	PROC 1,KLW31	045-038-500		ED-3T076-20,G34	
		PROC 1, PC0D		045-094-320	PROC 0,KLW31	019-038-300		ED-3T076-20,G34A	

INFORMATION NOTES: (CONT.)

306.

		FROM			TO				
TITLE	FUNCTION	CABINET OR UNIT	UNIT SD	EQL - TERM	CABINET OR UNIT	EQL - TERM	UNIT SD	CABLE DRAWING NO.	J3T061A-1 LIST NO.
3B21D PROCESSOR CABINET CABLES	SCAN AND SIGNAL DISTRIBUTOR (SCSD) UN33D	PROC 0, PC02	SD-3T011-01	019-110-333	FAN UNIT 0	036-011-200	—	ED-3T076-20,G14	
		PROC 1, PC02		045-110-333	FAN UNIT 1	036-011-300	—	ED-3T076-20,G14A	
		PROC 0, PC02		019-110-550	PROC 1, TN1820	045-080-306	SD-3T011-01	ED-3T076-20,G15A	
		PROC 1, PC02		045-110-550	PROC 0, TN1820	019-080-306		ED-3T076-20,G15D	
		PROC 0, PC02		019-110-537	PROC 0, SPU 04	028-146-539		ED-3T076-20,G17	,LB
		PROC 1, PC02		045-110-537	PROC 1, SPU 05	053-146-539		ED-3T076-20,G17A	,LC
		PROC 0, PC30		028-130-337	IOP 2, SPU18	011-180-539	SD-3T012-01	ED-3T076-20,G17B	,LD
		PROC 0, PC30		028-130-133	IOP 3, SPU19	062-180-539		ED-3T076-20,G17C	,LE
		PROC 0, PC30		028-130-346	IOP 2, SPU20	011-164-539		ED-3T076-20,G17D	,LF
		PROC 0, PC30		028-130-137	IOP 3, SPU21	062-164-539		ED-3T076-20,G17E	,LG
		PROC 0, PC30		028-130-350	IOP 2, SPU22	011-148-539		ED-3T076-20,G17F	,LH
		PROC 0, PC30		028-130-146	IOP 3, SPU23	062-148-539		ED-3T076-20,G17G	,LJ
		PROC 0, PC30		028-130-533	IOP 2, SPU24	011-132-539		ED-3T076-20,G17H	,LK
		PROC 0, PC30		028-130-150	IOP 3, SPU25	062-132-539		ED-3T076-20,G17J	,LL
		PROC 0, PC30		028-130-537	IOP 2, SPU26	011-116-539		ED-3T076-20,G17K	,LM
		PROC 0, PC30		028-130-333	IOP 3, SPU27	062-116-539		ED-3T076-20,G17L	,LN
		PROC 0, PC02		019-110-546	IOP 2, TN1820	011-026-306		ED-3T076-20,G18	,L17
		PROC 1, PC02		045-110-546	IOP 3, TN1820	062-026-306		ED-3T076-20,G18A	,L19

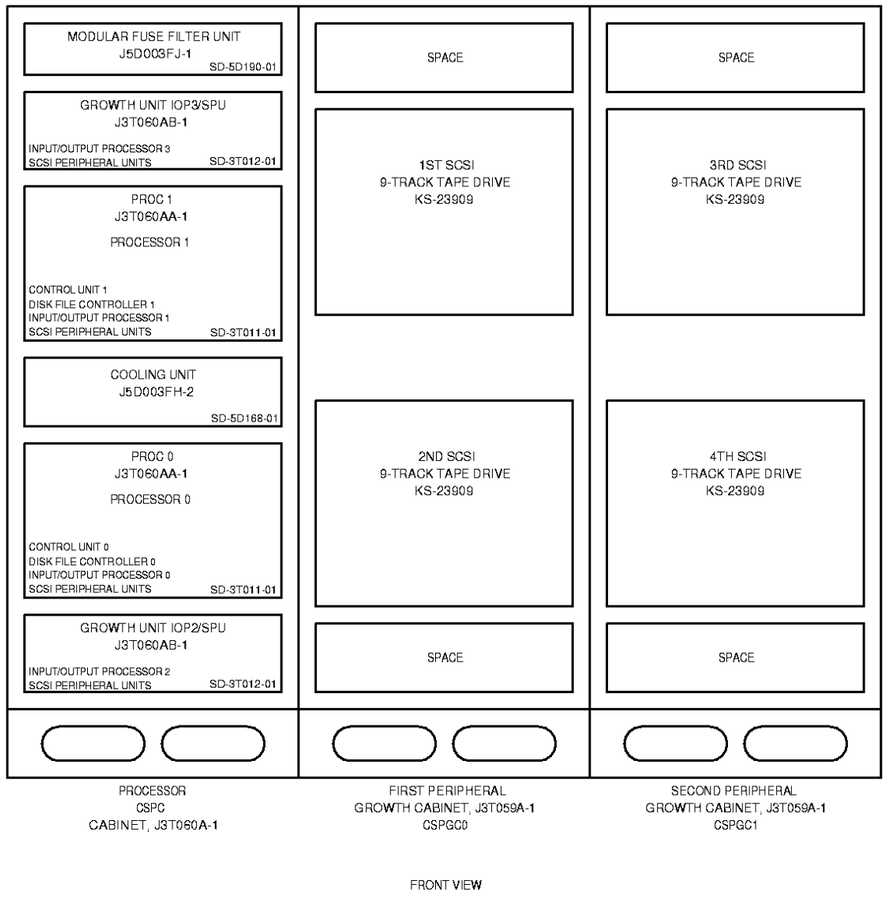
INFORMATION NOTES: (CONT.)

307.

		FROM			TO				
TITLE	FUNCTION	CABINET OR UNIT	UNIT SD	EQL - TERM	CABINET OR UNIT	EQL - TERM	UNIT SD	CABLE DRAWING NO.	J3T061A-1 LIST NO.
3B21D PROCESSOR CABINET	MAINSTORE UPDATE BUS CABLE	PROC 0, KLW32	SD-3T011-01	019-008-100B	PROC 1, KLW32	045-008-100B	SD-3T011-01	ED-3T076-40,G1	
				019-008-132		045-008-132			
				019-008-300		045-008-300			
				028-008-100		053-008-100			
				028-008-132		053-007-032			
	SCSI BUS JUMPER CABLES	IOP 3	SD-3T012-01	62-180-500	IOP 3	62-180-500	SD-3T012-01	ED-3T076-40,G3	
				62-180-300		62-180-300			
		PROC 1	SD-3T011-01	53-178-300	PROC 1	53-178-300	SD-3T011-01		
				53-101-000		53-101-000			
				45-186-500		45-186-500			
				45-101-000		45-101-000			
		PROC 0		28-178-300	PROC 0	28-178-300			
				28-101-000		28-101-000			
				19-186-500		19-186-500			
				19-101-000		19-101-000			
		IOP 2	SD-3T012-01	11-180-300	IOP 2	11-180-300	SD-3T012-01		
				11-180-500		11-180-500			
	SCSI BUS EXTENSION CABLES	PROC 0, BUS 0	SD-3T011-01	28-101-000	IOP 2, BUS A	11-063-000		ED-3T076-40,G4	,LU
		PROC 0, BUS 2		19-101-000	IOP 2, BUS B	11-047-000		ED-3T076-40,G4A	,LS
		PROC 1, BUS 1		53-101-000	IOP 3, BUS A	62-063-000		ED-3T076-40,G4B	,LV
		PROC 1, BUS 3		45-101-000	IOP 3, BUS B	62-047-000		ED-3T076-40,G4C	,LT
		PROC 0, BUS 0		28-101-000	IOP 3, BUS A	62-063-000		ED-3T076-40,G4D	,LW
		PROC 0, BUS 1		53-101-000	IOP 3, BUS B	62-047-000		ED-3T076-40,G4E	,LR
		PROC 0		19-186-500	9-TRACK DR. 0	—	—	ED-3T076-40,G100	,LX
		PROC 1		45-186-500	9-TRACK DR. 1	—	—		
		PROC 0		28-186-300	9-TRACK DR. 2	—	—	ED-3T076-40,G101	,LY
		PROC 1		53-178-300	9-TRACK DR. 3	—	—		

INFORMATION NOTES: (CONT.)

308. 3B21D PROCESSOR COMPUTER SYSTEM (MAXIMUM CONFIGURATION).



FRONT VIEW

3B21D PROCESSOR COMPUTER SYSTEMS			
		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET D8

INFORMATION NOTES: (CONT.)

309. PROCESSOR CABINET - J3T060A-1, CONFIGURATION

CONFIGURATION FOR THE PROCESSOR CABINET CONTAINS THE FOLLOWING MAJOR UNITS:

- ONE MODULAR FILTER AND FUSE PANEL UNIT, J5D003FJ-1.
- ONE BIDIRECTIONAL COOLING UNIT, J5D003FH-2.
- TWO PROCESSOR UNITS, J3T060AA-1.
- TWO GROWTH UNITS, J3T060AB-1.

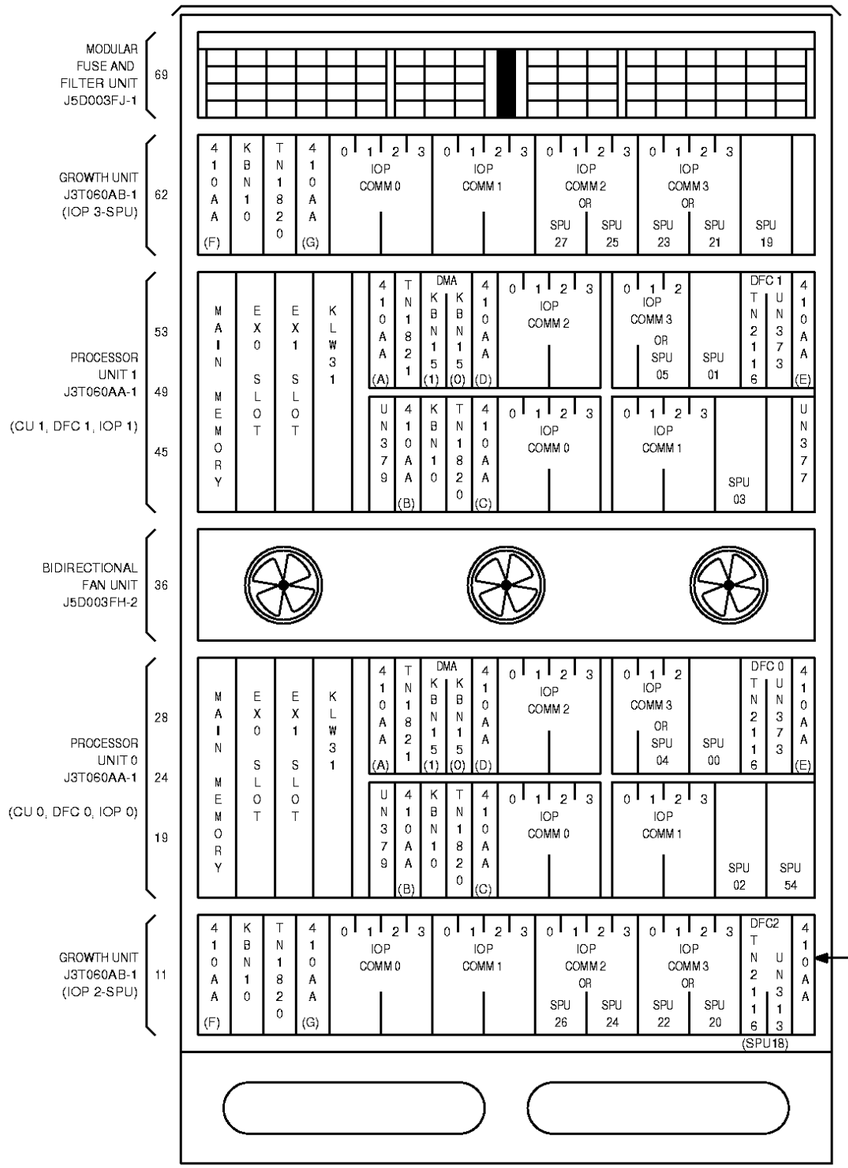
THE GROWTH UNITS CAN BE OPTIONALLY EQUIPPED TO PROVIDE PERIPHERAL COMMUNITY 2, PERIPHERAL COMMUNITY 3, OR SPU'S. THIS CONFIGURATION PROVIDES THE FOLLOWING EQUIPMENT:

- PROC 0 AND PROC 1.
- DMA 0 IS PART OF THE BASIC SYSTEM. DMA 1 IS OPTIONAL.
- DFC0 AND DFC1 TOGETHER CAN SUPPORT UP TO 21 SCSI PERIPHERAL UNITS (SPU'S). THE PROCESSOR CABINET MAY HAVE UP TO 17 SPU POSITIONS, WHEN FULLY EQUIPPED. FOUR ADDITIONAL SPU POSITIONS (SCSI 9 TRACK UNITS) MAY BE EQUIPPED EXTERNAL TO THE PROCESSOR CABINET. EACH DFC HAS 2 SCSI BUSSES, NAMED SBUS0 AND SBUS2 FOR DFC0, AND SBUS1 AND SBUS3 FOR DFC1.

  POSITIONS SPU00 AND SPU01 ARE ALWAYS EQUIPPED WITH A UN375 MHD CIRCUIT PACK. SPU54 IS ALWAYS EQUIPPED WITH A UN376 DAT CIRCUIT PACK. THE REMAINING SPU POSITIONS ARE GROWTH POSITIONS. SPU02 AND SPU03 ARE DEDICATED FOR SPU CIRCUIT PACKS. THE OTHER SPU SLOTS ARE MULTI-PURPOSE POSITIONS, WHICH ACCEPT EITHER ONE SPU CIRCUIT PACK OR TWO IOP CONTROLLER PACKS. WITHIN PROCESSOR UNIT 0 AND PROCESSOR UNIT 1, THE SPU POSITIONS ARE ASSIGNED TO A SPECIFIC SCSI BUS. SCSI BUS ASSIGNMENTS IN THE GROWTH POSTITIONS ARE DEPENDENT ON THE PARTICULAR GROWTH CONFIGURATION.

  FIVE SPU'S CAN BE EQUIPPED IN EACH GROWTH UNIT. FIVE OF THE GROWTH UNIT SPU'S ARE CONNECTED TO DFC 1; FIVE OF THE GROWTH UNIT SPU'S ARE CONNECTED TO DFC 0. REFER TO NOTE 310 FOR SPU CONTROLLER AND BUS ASSIGNMENTS.
- IOP 0 WITH PERIPHERAL COMMUNITIES 0, 1, 2, AND 3.
- IOP 1 WITH PERIPHERAL COMMUNITIES 0, 1, 2, AND 3.
- IOP 2 WITH PERIPHERAL COMMUNITIES 0 AND 1.
- IOP 3 WITH PERIPHERAL COMMUNITIES 0 AND 1.
- DFC2 IS A GROWTH OPTION FOR THE LOWER GROWTH UNIT, IN PLACE OF SPU18. A TN2116, UN373, AND 410AA COMPRISE THE DFC2 CONTROLLER. THIS DFC THEN USED THE TWO SBUSSED WITHIN THE GROWTH UNIT.

PROCESSOR CABINET EQUIPMENT OVERVIEW - FRONT VIEW



PROCESSOR CABINET, J3T060A-1

INFORMATION NOTES: (CONT.)

310. SCSI PERIPHERAL UNIT CONTROLLER AND BUS ASSIGNMENTS

SCSI PERIPHERAL UNIT			PROCESSOR CABINET CONFIGURATION			ADDITIONAL GROWTH (WITH REDUCED IOP CAPABILITY)
	EQUIPMENT LOCATION		BASIC	EXAMPLE 1 WITH GROWTH UNIT AT EQL 57	EXAMPLE 2 WITH GROWTH UNITS AT EQL'S 57 AND 06	
DESCRIPTION	PROCESSOR CABINET	PERIPHERAL GROWTH CABINET	DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS	DFC/SCSI BUS
SPU00	28-162		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU01	53-162		DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU02	19-170		DFC 0/SBUS 2	DFC 0/SBUS 2	DFC 0/SBUS 2	
SPU03	45-170		DFC 1/SBUS 3	DFC 1/SBUS 3	DFC 1/SBUS 3	
SPU04	28-146		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU05	53-146		DFC 1/SBUS 1	DFC 1/SBUS 1	DFC 1/SBUS 1	
SPU06	19-154					DFC 0/SBUS 2
SPU07	45-154					DFC 1/SBUS 3
SPU08	28-118					DFC 0/SBUS 0
SPU09	53-118					DFC 1/SBUS 1
SPU10	19-138					DFC 0/SBUS 2
SPU11	45-138					DFC 1/SBUS 3
SPU12	28-102					DFC 0/SBUS 0
SPU13	53-102					DFC 1/SBUS 1
SPU14	19-118					DFC 0/SBUS 2
SPU15	45-118					DFC 1/SBUS 3
SPU16	19-102					DFC 0/SBUS 2
SPU17	45-102					DFC 1/SBUS 3
SPU18	11-180				DFC 0/SBUS 2	
SPU19	62-180			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU20	11-164				DFC 0/SBUS 0	
SPU21	62-164			DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU22	11-148				DFC 0/SBUS 2	
SPU23	62-148			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU24	11-132				DFC 0/SBUS 0	
SPU25	62-132			DFC 0/SBUS 0	DFC 1/SBUS 1	
SPU26	11-116				DFC 0/SBUS 2	
SPU27	62-116			DFC 1/SBUS 1	DFC 1/SBUS 3	
SPU28	11-096					DFC 0/SBUS 0
SPU29	62-096					DFC 1/SBUS 1
SPU30	11-080					DFC 0/SBUS 2
SPU31	62-080					DFC 1/SBUS 3
SPU32	11-064					DFC 0/SBUS 0
SPU33	62-064					DFC 1/SBUS 1
SPU34	11-048					DFC 0/SBUS 2
SPU35	62-048					DFC 1/SBUS 3
SPU54 (MT)	19-186		DFC 0/SBUS 0	DFC 0/SBUS 0	DFC 0/SBUS 0	
SPU56 (9-TRACK1)		17-000	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	
SPU57 (9-TRACK0)		42-000	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	
SPU58 (9-TRACK3)		17-000	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	
SPU59 (9-TRACK2)		42-000	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	DFC 0-1/SBUS 0-3	

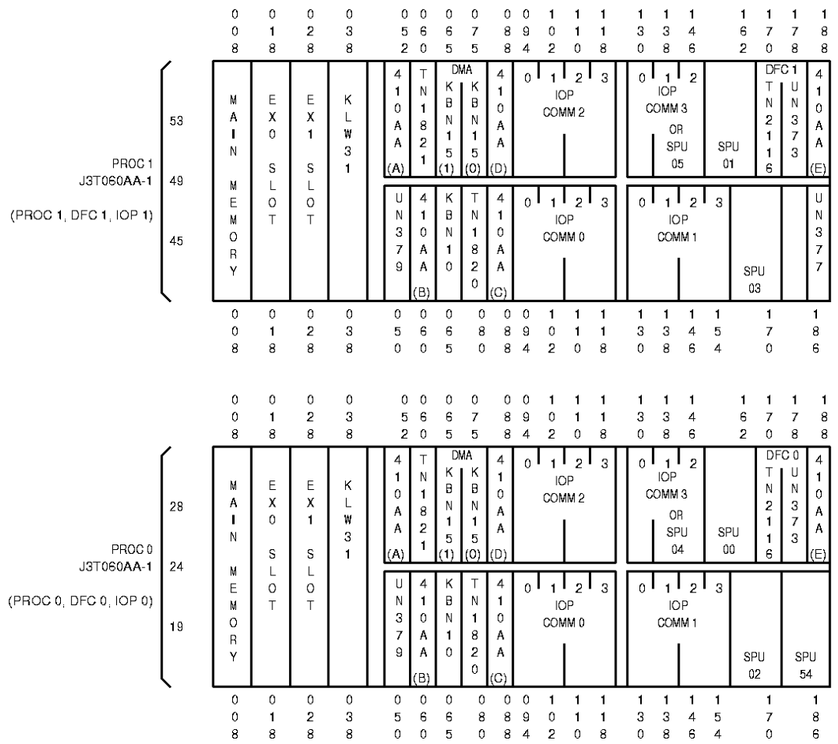
INFORMATION NOTES: (CONT.)

311. PROCESSOR CABINET ARRANGEMENT

PROCESSOR UNIT, J3T060AA-1

THE PROCESSOR UNIT, J3T060AA-1, SUPPORTS THE CENTRAL CONTROL (CC), DIRECT MEMORY ACCESS (DMA), MAIN MEMORY (MM), DISK FILE CONTROLLER (DFC), SCSI PERIPHERAL UNITS (SPU'S), DC-TO-DC POWER CONVERTER, POWER CONTROL, PORT SWITCH WITH RS-232 INTERFACE, AND IOP/PC FUNCTIONS. THE SPU'S INCLUDE THE UN375 CIRCUIT PACK, UN376 CIRCUIT PACKS, AND 9-TRACK TAPE. THE MM CAN BE A KLW32, KLW40, OR KLW48 CIRCUIT PACK. THE PROCESSOR UNIT ALSO PROVIDES TWO KLW-SIZE SLOTS (EX 0 AND EX 1) FOR FUTURE EXPANSION CAPABILITY. VIEW BELOW SHOWS APPARATUS HOUSING LAYOUT DETAILS FOR THE PROCESSOR UNIT 0 AND 1. CIRCUIT PACK TABLE IDENTIFIES THE EQUIPAGE OF THE PROCESSOR UNIT 0 AND PROCESSOR UNIT 1 IN THE PROCESSOR CABINET.

PROCESSOR UNIT, J3T060AA-1, EQUIPMENT LAYOUT - FRONT VIEW



PROCESSOR UNIT 0 AND 1 CIRCUIT PACKS

CIRCUIT PACK	PANEL DESIGNATION	PROCESSOR UNIT 0 EQL	PROCESSOR UNIT 1 EQL
410AA POWER CONVERTER	PWRA (RED) 410AA	28-052	53-052
410AA POWER CONVERTER	PWRB (BLUE) 410AA	19-060	45-060
410AA POWER CONVERTER	PWRC (BLACK) 410AA	19-088	45-088
410AA POWER CONVERTER	PWRD (GREEN) 410AA	28-088	53-088
410AA POWER CONVERTER	PWRE (PURPLE) 410AA	28-188	53-188
KBN10 INPUT/OUTPUT PROCESSOR	IOP (BLACK) KBN10	19-065	45-065
KBN15 DIRECT MEMORY ACCESS	DMA0 (RED) KBN15	28-075	53-075
KBN15 DIRECT MEMORY ACCESS	DMA1 (BLUE) KBN15	28-065	53-065
KLW31 CENTRAL CONTROL	CC (RED) KLW31	24-038	49-038
MAIN MEMORY (KLW32, KLW40, OR KLW48)	MM (RED) KLW32	24-008	49-008
KLW__ EXPANSION SLOT	EX0 (BLUE)	28-018	53-018
KLW__ EXPANSION SLOT	EX1 (BLUE)	24-028	49-028
TN1820 INPUT/OUTPUT PROCESSOR POWER SWITCH	IOPPS (GREEN AND BLACK) TN1820	19-080	45-080
TN1821 CONTROL UNIT POWER SWITCH	CUPS (RED) TN1821	28-060	53-060
TN2116 SCSI HOST ADAPTER	DFC0 (PURPLE)	28-170	
TN2116 SCSI HOST ADAPTER	DFC1 (PURPLE)		53-170
TN983 MTTY CONTROLLER	PC00 (BLACK)	19-094	45-094
	PC01 (BLACK)	19-102	
	PC01 (BLACK)		45-102
UN33D SCAN AND SIGNAL DISTRIBUTOR POINT CONTROLLER	PC02 (BLACK)	19-110	45-110
	PC03 (BLACK)	19-118	45-118
	PC10 (BLACK)	19-130	45-130
	PC11 (BLACK)	19-138	45-138
	PC12 (BLACK)	19-146	45-146
	PC13 (BLACK)	19-154	45-154
	PC20 (GREEN)	28-094	53-094
	PC21 (GREEN)	28-102	53-102
	PC22 (GREEN)	28-110	53-110
	PC23 (GREEN)	28-118	53-118
	PC30 (GREEN)	28-130	53-130
	PC31 (GREEN)	28-138	53-138
	PC32 (GREEN)	28-146	53-146
UN373 DDSBS/DSCH INTERFACE	DFC0 (PURPLE) UN373	28-178	
UN373 DDSBS/DSCH INTERFACE	DFC1 (PURPLE) UN373		53-178
UN375 SCSI DISK	SPU 00 UN375	28-162	
UN375 SCSI DISK	SPU 01 UN375		53-162
UN375 SCSI DISK	SPU 02	19-170	
UN375 SCSI DISK	SPU 03		45-170
UN376 SCSI TAPE (MT)	SPU 54 UN376	19-186	
UN377 PORT SWITCH AND SCANNER-DISTRIBUTOR BUFFER	PSSD (BLACK)		45-186
UN379 UTILITY CIRCUIT	UC (RED)	19-050	45-050

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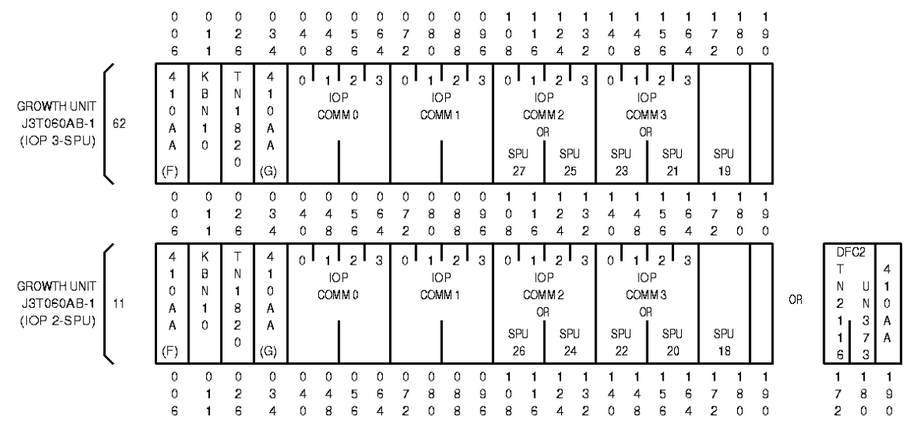
INFORMATION NOTES: (CONT.)

312. GROWTH UNIT ARRANGEMENT

GROWTH UNIT, J3T060AB-1

THE GROWTH UNIT, J3T060AB-1 SUPPORTS THE EQUIPAGE OF ADDITIONAL SCSI PERIPHERAL UNITS (SPU'S) AND IOP/PC CIRCUIT PACKS TO PROVIDE A SYSTEM GROWTH CAPABILITY. TWO GROWTH UNITS CAN BE EQUIPPED IN THE PROCESSOR CABINET. VIEW BELOW SHOWS APPARATUS HOUSING LAYOUT DETAILS FOR THE GROWTH UNITS. CIRCUIT PACK TABLE IDENTIFIES THE EQUIPAGE OF THE IOP 2-SPU AND IOP 3-SPU GROWTH UNITS IN THE PROCESSOR CABINET.

GROWTH UNIT, J3T060AB-1, EQUIPMENT LAYOUT - FRONT VIEW



GROWTH UNIT CIRCUIT PACKS

CIRCUIT PACK	PANEL DESIGNATION	PROCESSOR CABINET	
		IOP 2-SPU GROWTH UNIT EQL	IOP 3-SPU GROWTH UNIT EQL
410AA POWER CONVERTER	PWRF (RED) 410AA	11-006	62-006
410AA POWER CONVERTER	PWRG (BLACK) 410AA	11-034	62-034
KBN10 INPUT/OUTPUT PROCESSOR	IOP (RED) KBN10	11-011	
KBN10 INPUT/OUTPUT PROCESSOR	IOP (RED) KBN10		62-011
TN1820 INPUT/OUTPUT PROCESSOR POWER SWITCH	IOPPS (RED AND BLACK) TN1820	11-026	62-026
EQUIPAGE IS APPLICATION DEPENDENT AND INCLUDES PERIPHERAL CONTROLLERS.	PC00 (RED)		62-040
	PC01 (RED)		62-048
	PC00 (RED)	11-040	
	PC01 (RED)	11-048	
	PC02 (RED)		62-056
	PC03 (RED)		62-064
	PC02 (RED)	11-056	
	PC03 (RED)	11-064	
EQUIPAGE IS APPLICATION DEPENDENT AND INCLUDES PERIPHERAL CONTROLLERS.	PC10 (RED)		62-072
	PC11 (RED)		62-080
	PC10 (RED)	11-072	
	PC11 (RED)	11-080	
	PC12 (RED)		62-088
	PC13 (RED)		62-096
	PC12 (RED)	11-088	
	PC13 (RED)	11-096	
IOP COMMUNITY 2 OR SPU'S 24 THROUGH 27. EQUIPAGE IS APPLICATION DEPENDENT AND INCLUDES PERIPHERAL CONTROLLERS AND/OR SCSI PERIPHERAL UNITS.	PC20 (BLACK)		62-108
	PC21 (BLACK)		62-116
	SPU 27		62-116
	PC20 (BLACK)	11-108	
	PC21 (BLACK)	11-116	
	SPU 26	11-116	
	PC22 (BLACK)		62-124
	PC23 (BLACK)		62-132
	SPU 25		62-132
	PC22 (BLACK)	11-124	
	PC23 (BLACK)	11-132	
	SPU 24	11-132	
EQUIPAGE IS APPLICATION DEPENDENT AND INCLUDES PERIPHERAL CONTROLLERS AND/OR SCSI PERIPHERAL UNITS.	PC30 (BLACK)		62-140
	PC31 (BLACK)		62-148
	SPU 23		62-148
	PC30 (BLACK)	11-140	
	PC31 (RED)	11-148	
	SPU 22	11-148	
	PC32 (RED)		62-156
	PC33 (RED)		62-164
	SPU 21		62-164
	PC32 (RED)	11-156	
	PC33 (RED)	11-164	
	SPU 20	11-164	
SPU 18	SPU 18	11-180	
SPU 19	SPU 19		62-180
DFC2: EQUIPAGE IS APPLICATION DEPENDENT AND INCLUDES SCSI PERIPHERAL UNITS.	UN373 DDSBS/DSCH INTERFACE	11-180	
	TN2116 HOST ADAPTER	11-172	
	410AA POWER CONVERTER	11-190	

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INFORMATION NOTES: (CONT.)

313. POWER DISTRIBUTION OVERVIEW.

FIGURE 1 SHOWS THE TYPICAL -48 V DC DISTRIBUTION ARRANGEMENT FOR THE 3B21D COMPUTER PROCESSOR CABINET. THE PRIMARY POWER SOURCE FOR THE 3B21D COMPUTER IS -48 V DC FROM A LOCAL BATTERY PLANT. POWER IS DISTRIBUTED TO THE COMPUTER VIA POWER FEEDERS FROM A POWER DISTRIBUTION CABINET (PDC). IN INTERNATIONAL APPLICATIONS, THE POWER FEEDERS CONNECT TO DEDICATED POWER LINE ELECTRO-MAGNETIC INTERFERENCE (EMI) FILTERS ABOVE THE COMPUTER CABINET. THE EMI FILTER OUTPUTS ARE ROUTED TO THE FUSE AND FILTER UNIT (FFU) WHERE THEY ARE SPLIT INTO BRANCHES TO THE EQUIPMENT UNITS AND COOLING FANS. IN DOMESTIC APPLICATIONS THE POWER FEEDERS FROM THE PDC CONNECT DIRECTLY TO THE FFU. IN THE EQUIPMENT UNITS, DC-TO-DC CONVERTERS GENERATE THE VOLTAGES USED BY THE CIRCUIT PACKS. THE COOLING FANS AND A FEW CIRCUIT PACKS DIRECTLY USE -48 V DC. THE DC-TO-DC CONVERTERS ARE -48 V DC TO +5 V DC SUPPLIES THAT PLUG INTO THE BACKPLANE OR ARE BOARD-MOUNTED POWER MODULES (BMPM'S) THAT PROVIDE POWER DIRECTLY TO THE CIRCUIT PACK ON WHICH THEY ARE MOUNTED.

THE 3B21D COMPUTER COMPLIES WITH THE EUROPEAN TELECOMMUNICATION STANDARDIZATION INSTITUTE (ETSI) EXTENDED VOLTAGE LIMITS.

PROCESSOR CABINET POWER DISTRIBUTION

▲ CAUTION 1:

EQUIPMENT DAMAGE CAN RESULT IF THE PDC FUSES ARE INSTALLED WITHOUT FIRST UNSEATING THE ASSOCIATED 3B21D COMPUTER CIRCUIT PACKS THAT DRAW -48 V CURRENT. TO PREVENT EQUIPMENT DAMAGE, UNSEAT THE CIRCUIT PACKS ASSOCIATED WITH THE PDC FEEDER BEFORE INSTALLING THE PDC FUSE FOR THAT FEEDER. THESE PACKS ARE:

ALL 410AA
ALL UN377
ALL TN1820
ALL TN1821

▲ CAUTION 2:

FUSE FAILURE WILL RESULT IF THE 3B21D COMPUTER FFU FUSE FOR ANY OF THE ABOVE CIRCUIT PACKS IS INSTALLED WITHOUT FIRST UNSEATING THE CIRCUIT PACK. TO PREVENT FUSE FAILURE WHEN IT IS BEING REPLACED, UNSEAT THE CIRCUIT PACK BEFORE INSTALLING ITS FUSE IN THE FFU. REINSTALL THE CIRCUIT PACK AFTER THE FUSE HAS BEEN INSTALLED.

FIGURE 2 IS A REAR VIEW OF THE FFU IN THE PROCESSOR CABINET SHOWING HOW BLOCKS OF FUSES SPLIT THE FEEDERS INTO BRANCHES TO THE INTERNAL UNITS. TABLE 1 IDENTIFIES THE -48 V DC LOADS FOR ASSOCIATED POWER FEEDER, FUSE, AND BRANCH.

POWER FEEDERS ORIGINATING FROM PDC BUS 0 AND 1 TERMINATE IN THE FFU IN THE 3B21D COMPUTER PROCESSOR CABINET. NOTE THAT SOME 3B20D COMPUTER APPLICATIONS REFER TO THESE BUSES AS BUS A AND BUS B, RESPECTIVELY. THE LEFT HALF OF THE FFU DISTRIBUTES POWER FROM PDC BUS 0 (6 FEEDERS) TO PROCESSOR UNIT 0; THE RIGHT HALF DISTRIBUTES POWER FROM PDC BUS 1 (6 FEEDERS) TO PROCESSOR UNIT 1.

IN THE FFU, BLOCKS OF FUSES SPLIT THE FEEDERS INTO BRANCHES TO THE INTERNAL UNITS. EACH BRANCH IS PROTECTED WITH A SINGLE FAST-BLOW FUSE. THE FUSE BLOCKS CONTAIN A "FUSE-ALARM" LED ASSOCIATED WITH EACH FUSE POSITION AND TWO ALARM OUTPUTS THAT SIGNAL A FUSE BLOWING EVENT. THE FAILURE OF ANY FUSE IS INDICATED VIA A LED INDICATOR ON THE INDICATOR STRIPS ABOVE THE CABINET DOORS AT THE FRONT AND REAR OF THE PROCESSOR CABINET. FUSE BLOWING TRANSIENTS ARE MINIMIZED BY CAPACITORS (ONE PER FEEDER). EACH 4700 µF CAPACITOR HAS A 10 K OHM BLEEDER RESISTOR. EACH PROCESSOR CAN REQUIRE UP TO 33 BRANCHES (2 TO 9 BRANCHES PER FEEDER).

SINCE THE 3B21D COMPUTER FFU HAS ELECTROLYTIC FILTER CAPACITORS ON THE INPUT POWER FEEDERS, A CHARGING TOOL MUST BE USED WHEN INSTALLING 3B21D COMPUTER FUSES AT THE POWER DISTRIBUTION CABINET (PDC). SEE CAUTION 1.

ALSO NOTE THAT WHEN INSTALLING A FUSE IN THE 3B21D COMPUTER FFU THAT PROTECTS A UN377, 410AA, TN1820, OR TN1821 CIRCUIT PACK, THAT PACK IS FIRST UNSEATED BEFORE INSTALLING THE FUSE. AFTER REPLACING THE FUSE, THE CIRCUIT PACK MAY BE RESEATED AND THEN TURNED ON. SEE CAUTION 2. IN ADDITION, THIS SAME RESTRICTION APPLIES WHEN REPLACING A FUSE IN THE PDC CABINET. IN THAT CASE, ALL AFFECTED UN377, 410AA, TN1820, AND TN1821 CIRCUIT PACKS IN THE CIRCUIT PROTECTED BY THAT FUSE MUST BE REMOVED. SEE CAUTION 1.

INFORMATION NOTES: (CONT.)

313. (CONT.)

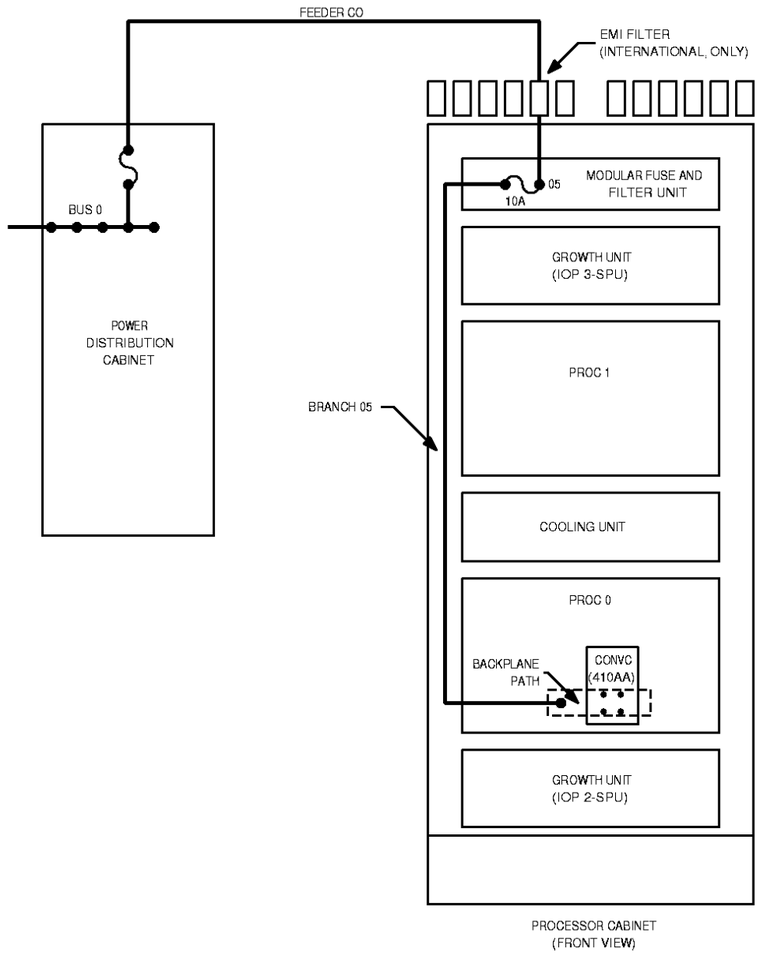


FIG. 1

PROCESSOR CABINET -48 V DC LOADS

POWER FEEDER	FUSE LOCATION {1ST UNIT,2ND UNIT} POSITION	FUSE LOCATION {1ST UNIT,2ND UNIT} EQL	LOAD	BRANCH	CURRENT @ 40.5 V (AMPERES)	FUSE RATING (AMPERES)	WIRE SIZE (AWG)	
A(0,1)	D{1,19}	014D,186D	PWR A	N48V02	6.7	10	14	PROCESSOR UNIT
	C{1,19}	014C,186C	CUPS	N48V01	0.2	3.0	16	
	B{1,19}	014B,186B	PC00-01	N48V07	0.1	3.0	16	
	A{1,19}	014A,186A	PC02-03	N48V08	0.1	3.0	16	
					7.1			
B(0,1)	D{2,18}	023D,177D	PWR B	N48V03	6.4	10	14	
	C{2,18}	023C,177C	PC10-11	N48V09	0.1	3.0	16	
	B{2,18}	023B,177B	FAN A, FAN G	N48VF{A,G}	0.8	3.0	16	
	A{2,18}	023A,177A	PC22-23	N48V12	0.1	3.0	16	
					7.4			
C(0,1)	D{3,17}	032D,168D	PWR C	N48V05	3.1	10	14	
	C{3,17}	032C,168C	IOPPS	N48V04	2.0	5.0	16	
	B{3,17}	032B,168B	FAN B, FAN F	N48VF{B,F}	0.8	3.0	16	
	A{3,17}	032A,168A	PC12-13	N48V10	0.1	3.0	16	
					6.0			
D(0,1)	D{4,16}	041D,159D	PWR D	N48V06	3.1	10	14	
	C{4,16}	041C,159C	PC20-21	N48V11	0.1	3.0	16	
	B{4,16}	041B,159B	FAN C, FAN E	N48VF{C,E}	0.8	3.0	16	
	A{4,16}	041A,159A	PC30-32 [SPU04, SPU05]	N48V13	0.15[1.3]	3.0	16	
					5.13[5.3]			
E(0,1)	D{5,15}	050D,150D	PWR E	N48V15	1.5	10	14	GROWTH UNIT
	C{5,15}	050C,150C	DFC 0, DFC 1	N48V14	0.2	3.0	16	
	B{5,15}	050B,150B	SPU00, SPU01	N48V16	1.3	3.0	16	
	A{5,15}	050A,150A	SPU02, SPU03	N48V17	1.3	3.0	16	
	D{6,14}	059D,141D	SPU54, PSSDB	N48V18	1.0	3.0	16	
	C{6,14}	059C,141C	PWR H*	N48V19	1.5	10	16	
E(0,1)	B{6,14}	059B,141B	SPU18, SPU19* [DFC 2,*]	N48V20	0.2[1.3]	3.0	16	
	A{6,14}	059A,141A	PC32-33* [SPU20, SPU21]*	N48V21	0.1[1.3]	3.0	16	
					7.1[9.4]			
F(0,1)	D{7,13}	073D,127D	PWR F*	N48V22	3.1	10	14	
	C{7,13}	073C,127C	IOPPS*	N48V23	2.0	5.0	16	
	B{7,13}	073B,127B	PC00-01*	N48V24	0.1	3.0	16	
	A{7,13}	073A,127A	PC02-03*	N48V25	0.1	3.0	16	
F(0,1)	D{8,12}	082D,118D	SPARE	N48V26				
	C{8,12}	082C,118C	SPARE	N48V27				
	B{8,12}	082B,118B	PC10-11*	N48V28	0.1	3.0	16	
	A{8,12}	082A,118A	PC12-13*	N48V29	0.2	3.0	16	
F(0,1)	D{9,11}	091D,109D	PWR G* [SPARE] (NOTE 4)	N48V30	3.1[0.0]	10	16	
	C{9,11}	091C,109C	PC20-21* [SPU26, SPU27]*	N48V31	0.1[1.3]	3.0	16	
	B{9,11}	091B,109B	PC22-23* [SPU24, SPU25]*	N48V32	0.1[1.3]	3.0	16	
	A{9,11}	091A,109A	PC30-32* [SPU22, SPU23]*	N48V33	0.1[1.3]	3.0	16	
					9.0[9.5]			

NOTES:

1. THE POWER FEEDER DESIGNATION "{0,1}" CONNECTS TO PROC 0 & 1 FROM PDC BUS 0 & BUS 1, RESPECTIVELY.
2. LOADS IN THE GROWTH UNIT ARE IDENTIFIED WITH AN ASTERISK (*).
3. ALTERNATE LOADS ARE IN BRACKETS ([]).
4. PWR G (410AA) IS OMITTED IF N48V21, N48V31, N48V31, AND N48V33 FEED SPU'S.
5. AN SPU CAN BE A UN375 MHD OR UN376 MT CIRCUIT PACK.

TABLE 1

NOTES:

1. THE POWER FEEDER DESIGNATION "{0,1}" CONNECTS TO PROCESSOR 0 AND 1 FROM PDC BUS 0 AND BUS 1, RESPECTIVELY.
2. LOADS IN THE GROWTH UNIT ARE IDENTIFIED WITH AN ASTERISK (*).
3. ALTERNATE LOADS ARE IN BRACKETS ([ ]).
4. THE MAXIMUM ALLOWABLE FEEDER CURRENT IS 13 AMPERES. THE WORST CASE CURRENT IN FEEDER F EXCEEDS 13 AMPERES. THEREFORE, THE PC CIRCUIT PACKS AND/OR SPU'S IN THE GROWTH UNIT MUST BE DISTRIBUTED BETWEEN FEEDERS E AND F TO KEEP THE FEEDER F CURRENT WITHIN LIMITS.
5. AN SPU CAN BE A UN375 MHD OR UN376 MT CIRCUIT PACK.

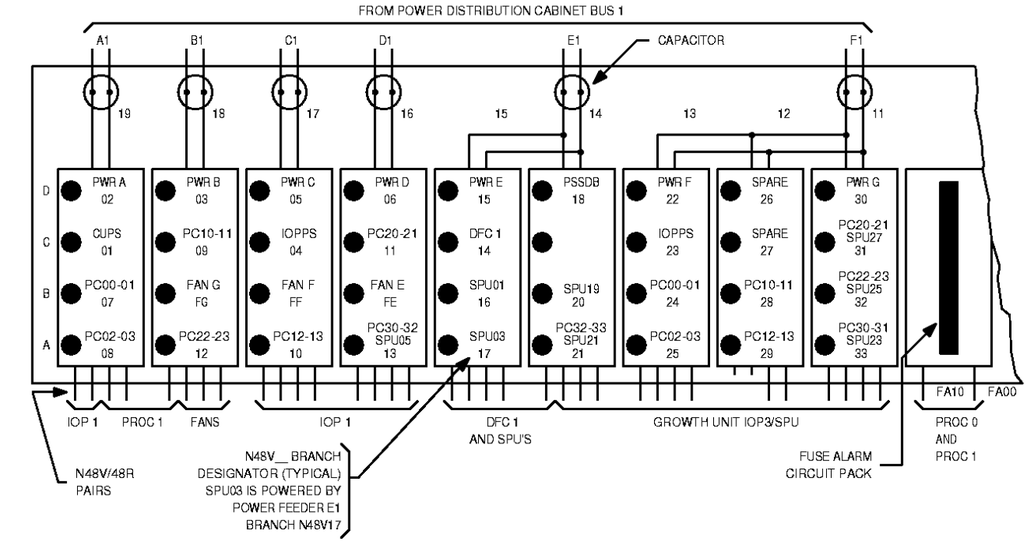
INFORMATION NOTES: (CONT.)

313. (CONT.)

NOTE:

1. SEE TABLE 1 FOR FUSE RATINGS.

PROCESSOR CABINET FUSE AND FILTER UNIT -48 V DC DISTRIBUTION (REAR VIEW)



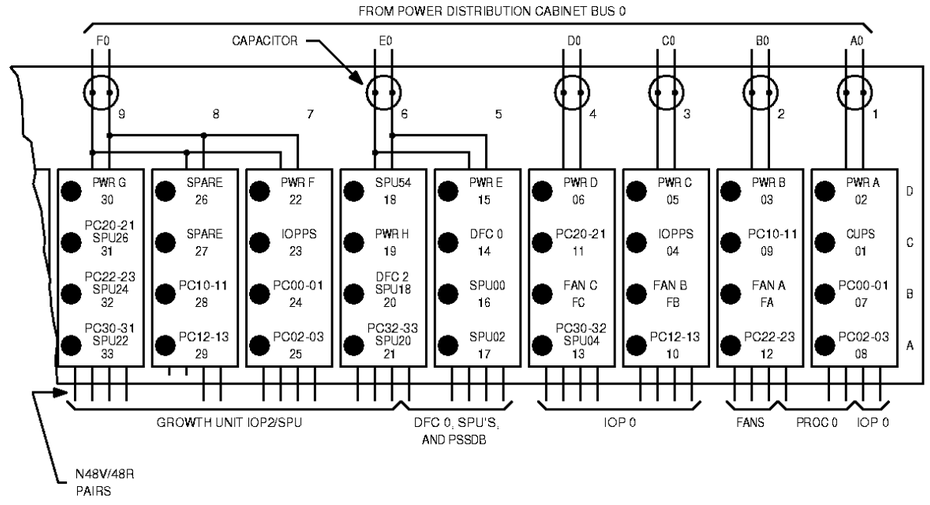


FIG. 2

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET D15

INFORMATION NOTES: (CONT.)

314. PROCESSOR UNIT POWER DISTRIBUTION

THE 3B21D COMPUTER PROCESSOR UNIT CAN CONTAIN UP TO FIVE POWER CONVERTERS (CONVA THROUGH CONVE). THREE OF THE CONVERTERS, CONVA, CONVC, AND CONVE, ARE ALWAYS EQUIPPED. CONVB AND CONVD ARE OPTIONALLY EQUIPPED. CONTROL FOR THE POWER CONVERTERS IS IN THE TN1821 (CUPS), TN1820 (IOPPS), AND THE UN373 (DFCA) CIRCUIT PACKS. THE POWER CONVERTERS AND THEIR CONTROLLERS REQUIRE -48 V DC AS A SUPPLY VOLTAGE. DFCA (UN373) IS UNLIKE THE OTHER TWO POWER CONTROL CIRCUIT PACKS IN THAT POWER CONTROL IS ONLY A SMALL PART OF ITS FUNCTIONALITY. DFCA ALSO USES THE 5 V FROM THE CONVERTER IT CONTROLS TO SUPPLY ITS OTHER INTERNAL LOGIC.

THIS VIEW SHOWS THERE ARE 18 SEPARATE -48 V BRANCHES TO THE PROCESSOR UNIT BACKPLANE. EACH CONVERTER AND POWER SWITCH HAS A FUSED POWER INPUT. LIKEWISE, EACH SCSI PERIPHERAL HAS A FUSED INPUT. IN PC COMMUNITIES 0, 1, AND 2, TWO -48 V BRANCHES ARE PROVIDED PER COMMUNITY, WITH ONE BRANCH PER SLOT PAIR. THE PRIMARY PURPOSE OF THESE -48 V FEEDS ARE TO POWER OPTIONAL SCSI UNITS IN THE PC COMMUNITY. THE ONLY CURRENT PC CARD SUPPORTED BY THE 3B21D REQUIRING -48 V IS THE THE UN33, BUT -48 VOLTS IS ALWAYS PROVIDED AT EVERY PC POSITION. IN PC COMMUNITY 3, ONE -48 V BRANCH SUPPLIES ALL THREE SLOTS. FINALLY, 5 V FROM CONVC IS ROUTED TO THE SPU54/PSSD POSITION FOR USE BY THE PSSD. THE PSSDB USES -48 V FROM THE BACKPLANE AND 5 V FROM CONVC. THE SPU54 USES ONLY -48 V FROM THE BACKPLANE.

THE PC COMMUNITIES ALSO REQUIRE +/-12 V AND -5 V WHICH ARE PROVIDED BY THE IOPPS. THE +/-12 V SUPPLIES ON THE IOPPS ARE RATED AT 50 WATTS EACH. AS INDICATED HERE, THE -48 V RETURN IS ISOLATED FROM THE FRAME AND LOGIC GROUND. ALL OTHER SUPPLY VOLTAGES HAVE THEIR RETURNS TIED TO LOGIC AND FRAME GROUND.

THE CIRCUIT PACK DESIGNATION STRIPS ON THE UNIT ARE COLOR-CODED TO SHOW WHICH DC-TO-DC CONVERTERS SUPPLY POWER TO THE VARIOUS CIRCUIT PACK POSITIONS. FIGURE 3 IDENTIFIES THIS COLOR-CODING FOR EACH OF THE CONVERTERS.

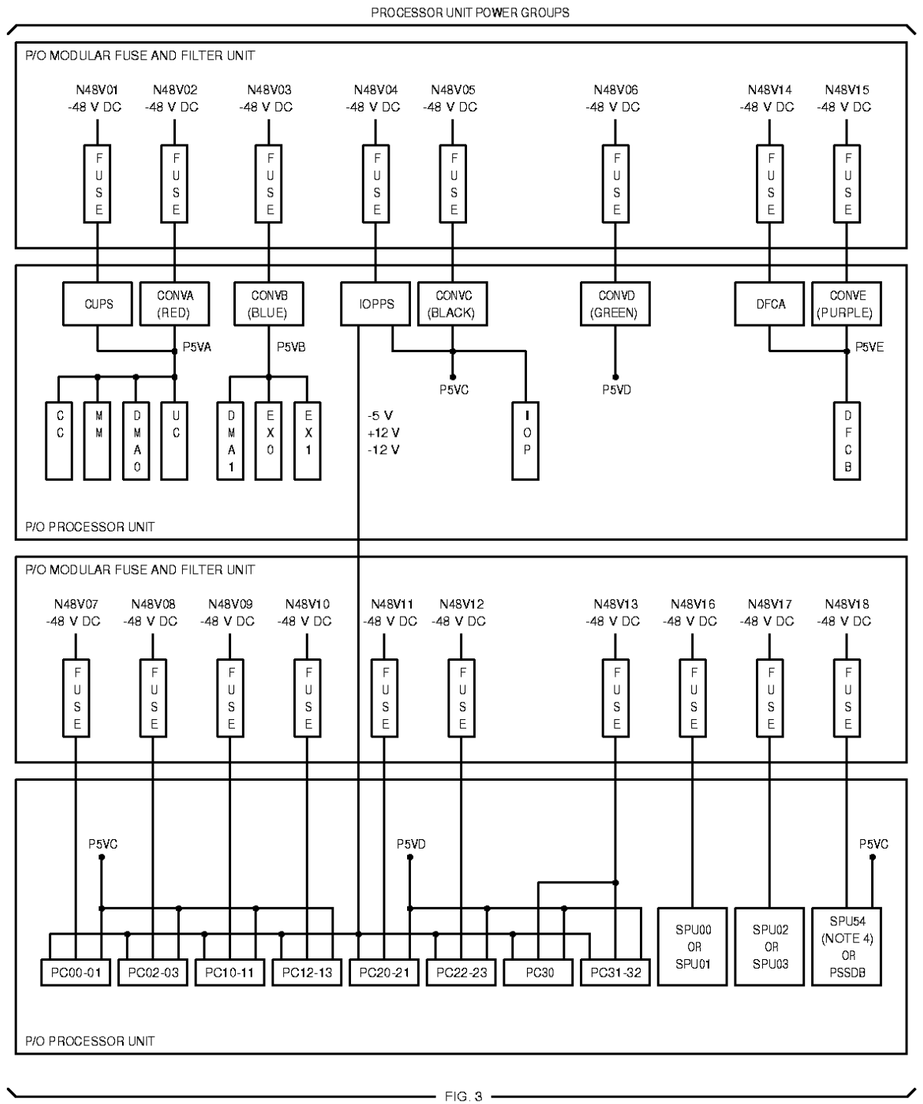


FIG. 3

NOTES:

1. +5 V RETURNS TIED TO GND, WHICH IS ALSO FROM GROUND.
2. -48 V RETURNS ARE TIED TO 48R, WHICH IS ISOLATED FROM LOGIC GROUND AND FROM FRAME GROUND IN THE CABINET.
3. -48 V RETURNS ARE INDIVIDUALLY ROUTED TO EACH CONVERTER.
4. THE SPU54 USES ONLY -48 V, IT DOES NOT USE P5VC.

3B21D PROCESSOR COMPUTER SYSTEMS		
	DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01	SHEET D16

INFORMATION NOTES: (CONT.)

315. GROWTH UNIT POWER DISTRIBUTION

THE 3B21D COMPUTER GROWTH UNIT CAN CONTAIN UP TO THREE POWER CONVERTERS (CONVF, CONVG, CONVH). FIGURE 4 ILLUSTRATES THESE THREE CONVERTERS AND THE CIRCUIT PACKS THEY SERVE. CONTROL FOR THE POWER CONVERTERS IS IN THE TN1820 (IOPPS) AND THE UN373 (DFCA) CIRCUIT PACKS. THE POWER CONVERTERS AND THEIR CONTROLLERS REQUIRE -48 V DC AS A SUPPLY VOLTAGE. DFCA (UN373) IS UNLIKE THE OTHER TWO POWER CONTROL CIRCUIT PACKS IN THAT POWER CONTROL IS ONLY A SMALL PART OF ITS FUNCTIONALITY. DFCA ALSO USES THE 5 V FROM THE CONVERTER IT CONTROLS TO SUPPLY ITS OTHER INTERNAL LOGIC.

FIGURE 4 SHOWS THERE ARE 13 SEPARATE -48 V BRANCHES TO THE GROWTH BACKPLANE. EACH CONVERTER AND POWER SWITCH HAS A FUSED POWER INPUT. LIKEWISE, EACH SCSI PERIPHERAL HAS A FUSED INPUT. IN PC COMMUNITIES 0, 1, 2, AND 3, TWO -48 V BRANCHES ARE PROVIDED PER COMMUNITY, WITH ONE FEED PER SLOT PAIR. THE PRIMARY PURPOSE OF THESE -48 V FEEDS ARE TO POWER OPTIONAL SCSI UNITS IN THE PC COMMUNITY. THE ONLY CURRENT PC CIRCUIT PACK SUPPORTED BY THE 3B21D COMPUTER REQUIRING -48 V IS THE UN33 CIRCUIT PACK, BUT -48 VOLTS IS PROVIDED AT EVERY PC POSITION.

CONVF SUPPLIES +5 V TO THE PC COMMUNITIES 0 AND 1. CONVG SUPPLIES +5 V TO THE PC COMMUNITIES 2 AND 3. THE PC COMMUNITIES ALSO REQUIRE +/-12 V AND -5 V WHICH ARE PROVIDED BY THE IOPPS. THE +/-12 V SUPPLIES ON THE IOPPS ARE RATED AT 50 WATTS EACH. AS INDICATED HERE, THE -48 V RETURN IS ISOLATED FROM FRAME AND LOGIC GROUND. ALL OTHER SUPPLY VOLTAGES HAVE THEIR RETURNS TIED TO LOGIC AND FRAME GROUND.

THE CIRCUIT PACK DESIGNATION STRIP ON THE UNIT IS COLOR-CODED TO SHOW WHICH DC-TO-DC CONVERTERS SUPPLY POWER TO THE VARIOUS CIRCUIT PACK POSITIONS. FIGURE 4 IDENTIFIES THIS COLOR-CODING FOR EACH OF THE DC-TO-DC CONVERTERS.

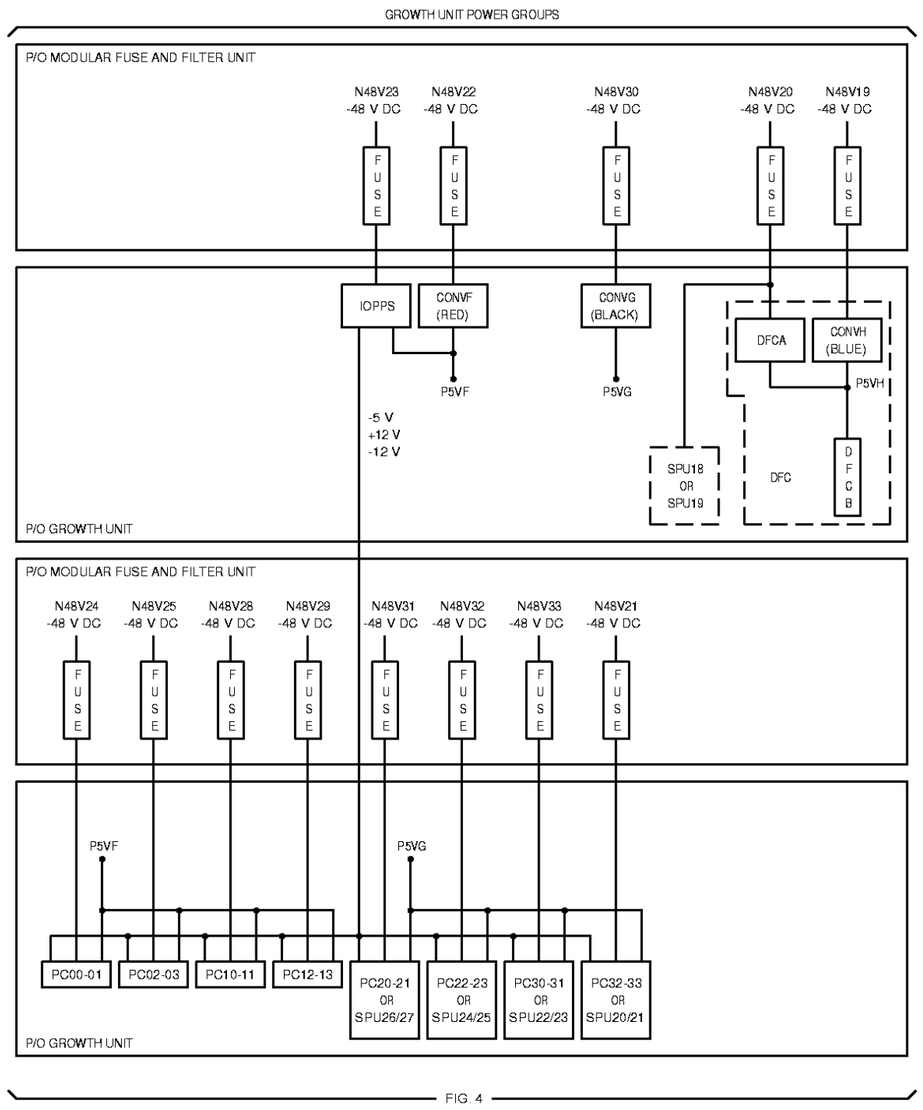


FIG. 4

NOTES:

1. +5 V RETURNS TIED TO GND, WHICH IS ALSO FROM GROUND.
2. -48 V RETURNS ARE TIED TO 48R, WHICH IS ISOLATED FROM LOGIC GROUND AND FROM FRAME GROUND IN THE CABINET.
3. -48 V RETURNS ARE INDIVIDUALLY ROUTED TO EACH CONVERTER.

3B21D PROCESSOR COMPUTER SYSTEMS		
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INFORMATION NOTES: (CONT.)

316. BIDIRECTIONAL COOLING UNIT

THE BIDIRECTIONAL COOLING UNIT IS EQUIPPED IN THE PROCESSOR CABINET. THE UNIT CONTAINS TWO GROUPS OF FANS. ONE GROUP BLOWS AIR UPWARD TO COOL PROCESSOR 1 AND IOP 3-SPU GROWTH UNIT; THE OTHER GROUP BLOWS AIR DOWNWARD TO COOL PROCESSOR 0 AND IOP 2-SPU GROWTH UNIT. FIGURE 5 IS A FUNCTIONAL BLOCK DIAGRAM OF THE BIDIRECTIONAL COOLING UNIT POWER AND ALARM CIRCUITS.

THE FAN MOTORS OPERATE ON -48 V. FAN GROUPS 0 AND 1 ARE SUPPLIED FROM FFU SIDE 0 AND 1 RESPECTIVELY. THE ALARM CIRCUIT IS POWERED BY N48VFANC AND N48VFANG THAT ARE ORED WITHIN THE ALARM CIRCUIT BOARD.

EACH FAN INCLUDES AN INTEGRAL FAN PERFORMANCE SENSOR (FPS) THAT OPERATES FROM +5 V OBTAINED FROM A BMPM IN THE ALARM CIRCUIT. IF ONE OR MORE FANS FAIL, THE CIRCUIT LATCHES AN ALARM STATE ON ITS SCAN POINT OUTPUT AND LIGHTS THE ASSOCIATED FAN INDICATOR (LED) ON THE COOLING UNIT. A FAN INDICATOR IS ON WHEN A FAN IS NOT RUNNING. THE SD POINT IS USED TO RETIRE THE ALARM. A SWITCH ON THE COOLING UNIT CAN ALSO BE USED TO MANUALLY RETIRE THE ALARM.

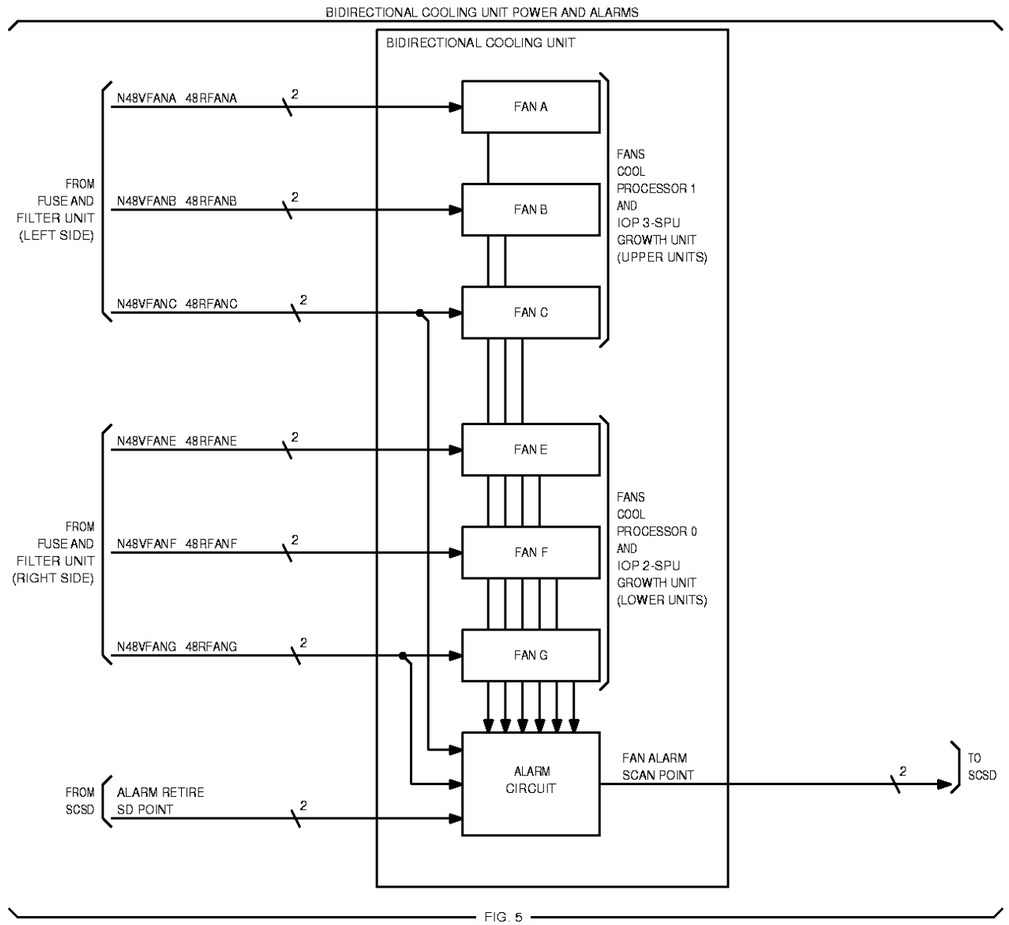

FIG. 5

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET D18

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INFORMATION NOTES: (CONT.)

317. ED-3T076-40,G3 SCSI BUS TERMINATORS

THIS TABLE IDENTIFIES THE SCSI BUS TERMINATORS. TERMINATION RESISTORS FOR THE SCSI BUSES ARE MOUNTED EXTERNAL TO THE BACKPLANE AND CIRCUIT PACKS, BUT NOT ON PADDLEBOARDS. A SCSI BUS TERMINATOR CONSISTS OF A RESISTOR ASSEMBLY WHICH PLUGS INTO A CONNECTOR THAT IS CABLED TO THE BACKPLANE. THERE ARE FOUR OF THESE ASSEMBLIES, TWO FOR EACH END OF THE TWO SCSI BUSES. THIS TABLE IDENTIFIES ALL POSSIBLE LOCATIONS FOR THE SCSI BUS TERMINATORS.

ED-3T076-40,G3
SCSI BUS TERMINATORS

UNIT	EQL
IOP3-SPU GROWTH UNIT	62-180-300 62-180-500
PROCESSOR UNIT 1	53-178-300 53-101-000 45-186-500 45-101-000
PROCESSOR UNIT 0	28-178-300 28-101-000 19-186-500 19-101-000
IOP2-SPU GROWTH UNIT	11-180-300 11-180-500

SCSI BUS TERMINATIONS ARE ALWAYS PROVIDED AT THE FOUR LOCATIONS IN PROCESSOR UNITS 0 AND 1. IF THE SCSI BUSSES ARE GROWN, THEN A SCSI EXTENDER IS ATTACHED AT THE APPROPRIATE END OF THE BUS AND THE TERMINATION IS REMOVED.

317.1 9824A PADDLEBOARD ASSEMBLIES

THIS TABLE IDENTIFIES THE PADDLEBOARD ASSEMBLIES USED ON THE PROCESSOR UNIT BACKPLANE. ALL PADDLEBOARDS CONTAIN A NETWORK OF SERIES RC TERMINATIONS TO GROUND. THE RESISTANCE VALUE IS 56 OHMS, AND THE CAPACITANCE IS 47 PF. THIS MATCHES THE LINE IMPEDANCE OF 65 OHMS, AND ASSUMES A SERIES IMPEDANCE OF 10 OHMS IN THE DRIVING ELEMENTS. PADDLEBOARD ASSEMBLY BTR1 ALSO CONTAINS PULLUP RESISTORS TO VCC FOR THE CCIO DATA BUS, CCIO ADDRESSES, AND CCIO COMMANDS. THE PULLUP RESISTANCE IS 1000 OHMS. THE PULLUP RESISTORS ARE ON THE SAME POWER BOUNDARY (P5VA) AS THE CC AND DMA 0 CIRCUIT PACKS.

9824A PADDLEBOARD ASSEMBLIES

NAME	EQL	NUMBER	DESCRIPTION
BTR1	13-075-732	9824AP	CCIO BUS TERMINATIONS AND PULLUPS, DMA 0 END
BTR2	13-075-700	9824AR	MAS DATA AND ADDRESS TERMINATIONS, DMA 0 END
BTR3	13-018-532	9824AS	CCIO BUS TERMINATIONS, EX 0 END

INFORMATION NOTES: (CONT.)

317.2 9824AN SCSI BUS JUMPERS

THIS TABLE LISTS THE SCSI BUS JUMPER LOCATIONS.

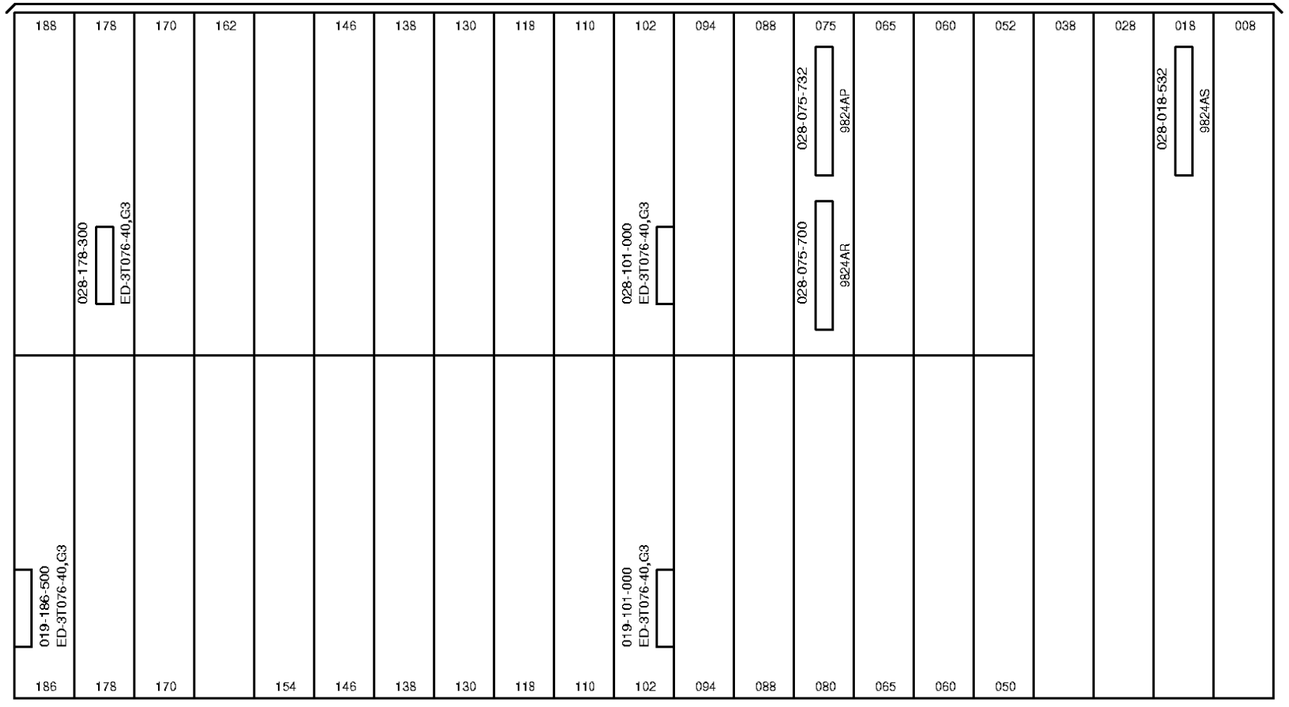
9824AN SCSI BUS JUMPER LOCATIONS

UNIT	EQL	NOTES
IOP3-SPU GROWTH UNIT	62-171-000 62-155-000 62-139-000 62-123-000	SPU21 SPU23 SPU25 SPU27
PROCESSOR UNIT 1	53-153-000	SPU05
PROCESSOR UNIT 0	28-153-000	SPU04
IOP2-SPU GROWTH UNIT	11-171-000 11-155-000 11-139-000 11-123-000	SPU20 SPU22 SPU24 SPU26

INFORMATION NOTES: (CONT.)

318.

BUS TERMINATION RESISTORS - PROCESSOR 0



REAR VIEW

3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE: C2
ISSUE: 1

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INFORMATION NOTES: (CONT.)

319.

BUS TERMINATION RESISTORS - PROCESSOR 1

188	178	170	162		146	138	130	118	110	102	094	088	075	065	060	052	038	028	018	008
	053-178-300 ED-3T076-40,G3									053-101-000 ED-3T076-40,G3			053-075-732 9824AP 053-075-700 9824AR						053-018-532 9824AS	

186	178	170		154	146	138	130	118	110	102	094	088	080	065	060	050				
045-186-500 ED-3T076-40,G3										045-101-000 ED-3T076-40,G3										

REAR VIEW

INFORMATION NOTES: (CONT.)

320. LISTS SHOWN BELOW MAY BE USED TO CONNECT CH 11/13, CH 12/14, CH 16/18, AND CH 17/19 TO SIS100/SIS110 INTERRUPT PINS FOR BASIC PROCESSOR UNIT (J3T060AA-1) (SD3T011-01, NOTE 313).

THE OFFICE ENGINEER SHOULD BE AWARE OF THE SYSTEM INTERRUPT BITS THAT WILL BE USED IN HIS/HER OFFICE APPLICATIONS. IF A GROWTH DMAC IS EQUIPPED, THE OFFICE SHOULD SPECIFY WHAT DMAC CHANNELS WILL BE USED AND WHAT SYSTEM INTERRUPT BITS WILL BE USED. THE 3B21D DOCUMENTS CANNOT SPECIFY THIS INFORMATION BECAUSE IT IS DEPENDENT ON THE USER.

LIST BELOW SHOWS THE CHANNEL INTERRUPT OUTPUTS AVAILABLE FROM THE DMACS AND THE POSSIBLE PROCESSOR SYSTEM INTERRUPT INPUTS THAT CAN BE CHOSEN.

SIGNAL	EQL	DESCRIPTION
D0INT00	13-037-053	INTERRUPT OUTPUT FROM DMA0, CHANNELS 11 & 13
D0INT10	13-037-052	INTERRUPT OUTPUT FROM DMA0, CHANNELS 12 & 14
D1INT00	13-037-050	INTERRUPT OUTPUT FROM DMA1, CHANNELS 16 & 18
D1INT10	13-037-049	INTERRUPT OUTPUT FROM DMA1, CHANNELS 17 & 19

THESE ARE OUTPUTS THAT SIGNAL WHEN A DMAC CHANNEL HAS A MESSAGE. DMA0 IS ALWAYS EQUIPPED, AND SO THE FIRST TWO PINS MUST ALWAYS BE SPECIFIED. WHEN DMA1 IS EQUIPPED, THE LAST TWO PINS MUST BE SPECIFIED.

LIST BELOW ALSO SHOWS THE POTENTIAL PROCESSOR INPUTS THAT RECEIVE THE ABOVE OUTPUTS. THESE ARE CALLED SYSTEM INTERRUPT SOURCE (SIS) BITS. WHILE THERE ARE 11 PINS, ONLY TWO ARE TYPICALLY USED AS INPUTS.

SIGNAL	EQL	DESCRIPTION
SIS100	08-038-049T	SYSTEM INTERRUPT BIT 10 INPUT
SIS110	08-038-048T	SYSTEM INTERRUPT BIT 11 INPUT

THE FOUR OUTPUT SIGNALS DESCRIBED ABOVE ARE WIRED TO EITHER OF THESE TWO INPUT PINS. IF ONLY DMA0 IS EQUIPED, THEN ONLY TWO OUTPUTS NEED TO BE WIRED.

THE OFFICE ENGINEER SHOULD HAVE INFORMATION THAT DESCRIBES:

1) HOW MANY DMAC'S ARE EQUIPPED? ONE OR TWO?
2) WHERE SHOULD THE DMAC CHANNELS BE CONNECTED?
   A) 3B21D ALWAYS CONNECTS CHANNEL 11/13 TO SIS BIT 10 (SIS100).
   B) WHERE DOES CHANNEL 12/14 GO? EITHER SIS BIT 10 OR BIT 11.
   C) IF DMA1, WHERE DOES CHANNEL 16/18 GO? EITHER SIS100 OR SIS110.
   D) IF DMA1, WHERE DOES CHANNEL 17/19 GO? EITHER SIS100 OR SIS110.

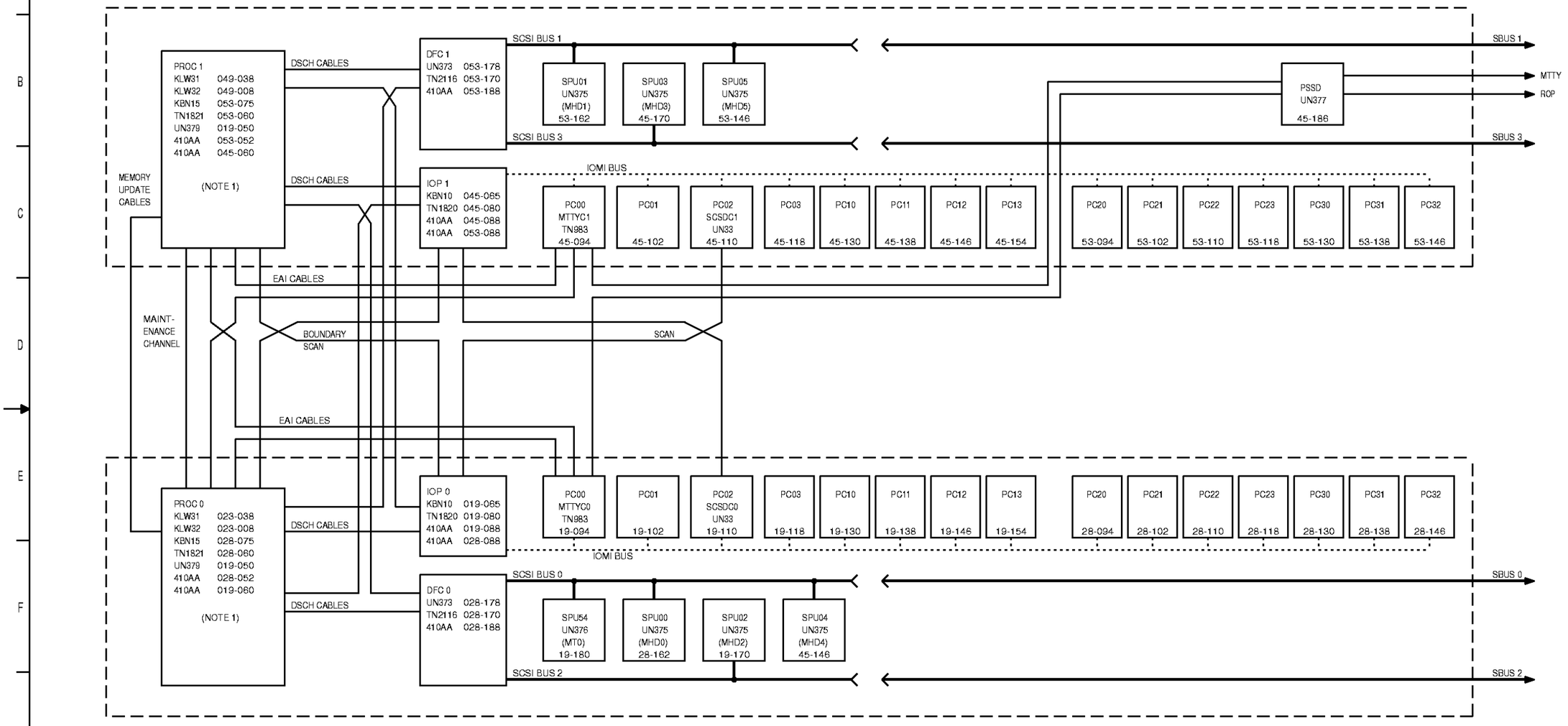
WE HAVE FOUND THAT DIFFERENT APPLICATIONS HAVE DIFFERENT NEEDS. SOME CUSTOMERS DO NOT HAVE DMA1. OTHERS HOOK CHANNEL 12/14 TO SIS100 WHILE OTHERS HOOK CHANNEL 12/14 TO SIS110. WE CANNOT TABULATE ALL THESE BECAUSE THEY CAN BE CHANGED BY THE CUSTOMER.

BD 1

SCSI BUS 0-3 AND MISC. CABLES

NOTE:

1. SEE NOTE 311 FOR CIRCUIT PACK EQL'S.



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
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BD 2

SCSI BUSES
BASIC UNIT

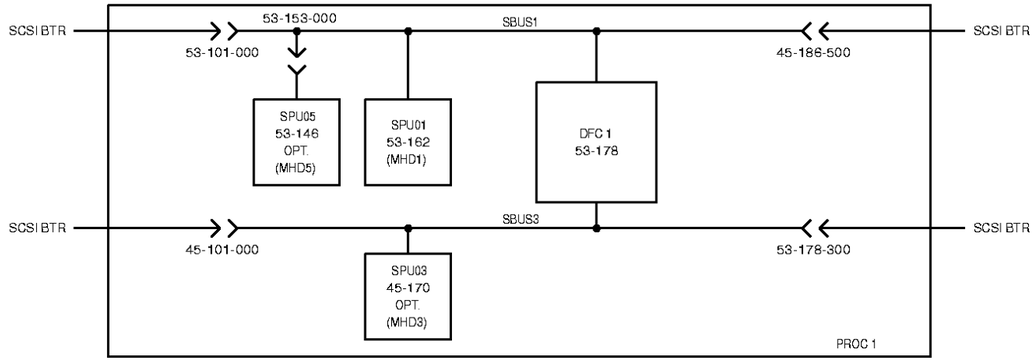
NOTES:

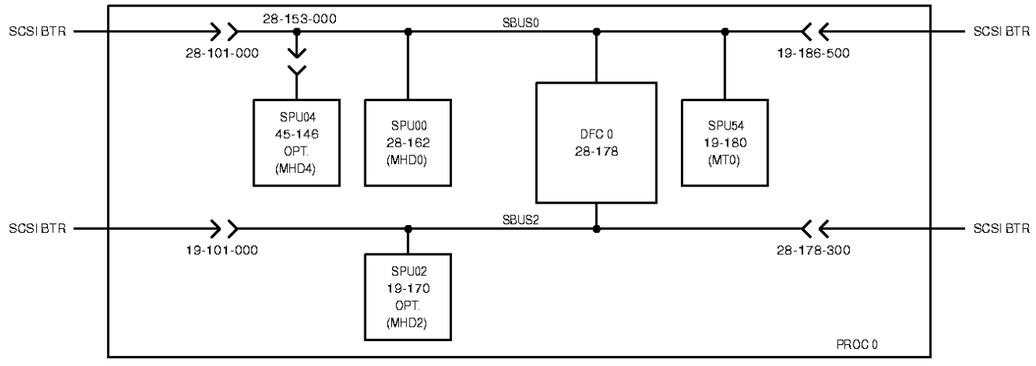
1. SCSI BUSES ARE SELF CONTAINED IN PROCESSOR 0 AND PROCESSOR 1.
2. SCSI BTR'S ARE ED-3T076-40,G3.
3. 9824AN CONNECTS SPU04 AND SPU05 TO SCSI BUSES. SEE DETAIL.

* DETAIL FOR SPU 04

28-146		9824AN		28-153	
GRD	524		024	GRD	
ION	523		023	IOAN	
REQN	522		022	REQAN	
CDN	521		021	CDAN	
SELN	520		020	SELAN	
MSGN	519		019	MSGAN	
RSTN	518		018	RSTAN	
ACKN	517		017	ACKAN	
BSYN	516		016	BSYAN	
GRD	515		015	GRD	
ATN	514		014	ATAN	
GRD	513		013	GRD	
TERMPWR	512		012	TRMPWRA	
GRD	511		011	GRD	
GRD	510		010	GRD	
SDPN	509		009	SDAPN	
SD7N	508		008	SDA7N	
SD6N	507		007	SDA6N	
SD5N	506		006	SDA5N	
SD4N	505		005	SDA4N	
SD3N	504		004	SDA7N	
SD2N	503		003	SDA6N	
SD1N	502		002	SDA5N	
SD0N	501		001	SDA4N	
GRD	500		000	GRD	

28-146		9824AN		28-152	
GRD	424		024	GRD	
IOP	423		023	IOAP	
REQP	422		022	REQAP	
CDP	421		021	CDAP	
SELP	420		020	SELAP	
MSGP	419		019	MSGAP	
RSTP	418		018	RSTAP	
ACKP	417		017	ACKAP	
BSYP	416		016	BSYAP	
GRD	415		015	GRD	
ATN	414		014	ATN	
GRD	413		013	GRD	
TERMPWR	412		012	TRMPWRA	
GRD	411		011	GRD	
GRD	410		010	GRD	
SDP	409		009	SDAPP	
SD7P	408		008	SDA7P	
SD6P	407		007	SDA6P	
SD5P	406		006	SDA5P	
SD4P	405		005	SDA4P	
SD3P	404		004	SDA7P	
SD2P	403		003	SDA6P	
SD1P	402		002	SDA5P	
SD0P	401		001	SDA4P	
GRD	400		000	GRD	





3B21D PROCESSOR
COMPUTER SYSTEMS

DWG SIZE	ISSUE
C2	1

AT&T	SD-3T015-01	SHEET
		H2

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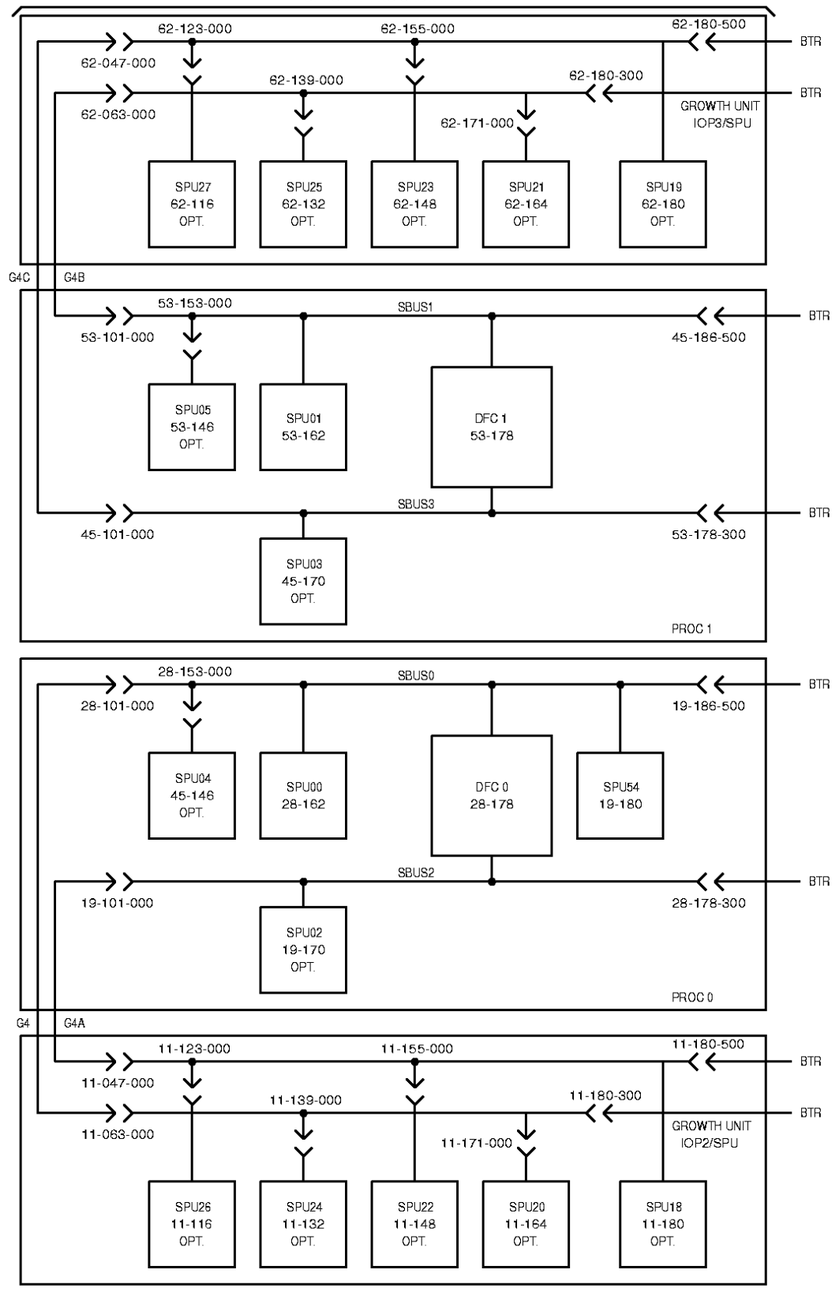
BD 3

SCSI CABLING/SPU GROWTH

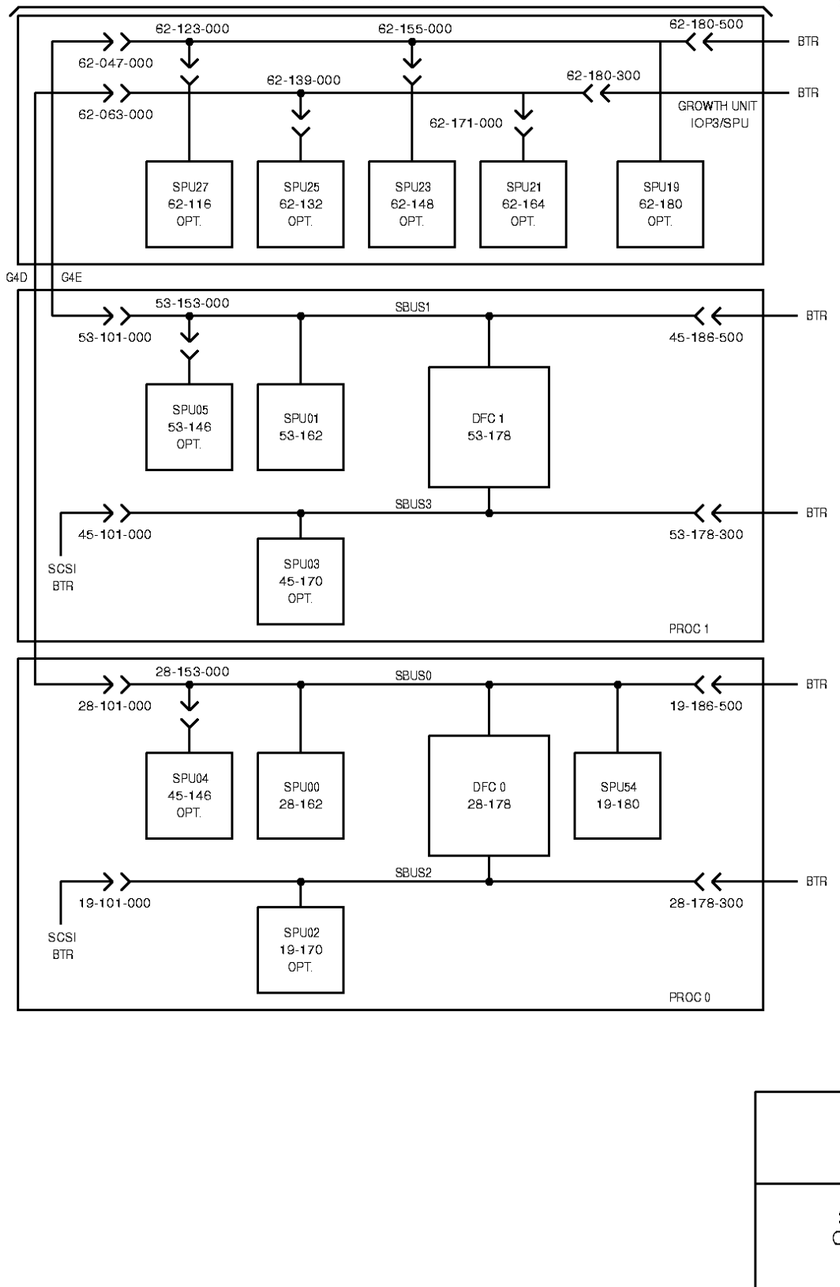
NOTES:

1. 9824AN REQUIRED WHEN BACKPLANE CONNECTION SHOWN.
2. ALL SCSI CABLE REFERENCES ARE ED-3T076-40.
3. REFER TO NOTE 306 FOR SCAN CABLE ASSIGNMENTS.

OPTION 1: TWO GROWTH UNITS



OPTION 2: SINGLE GROWTH UNIT



3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 2B
AT&T	SD-3T015-01	SHEET H3	

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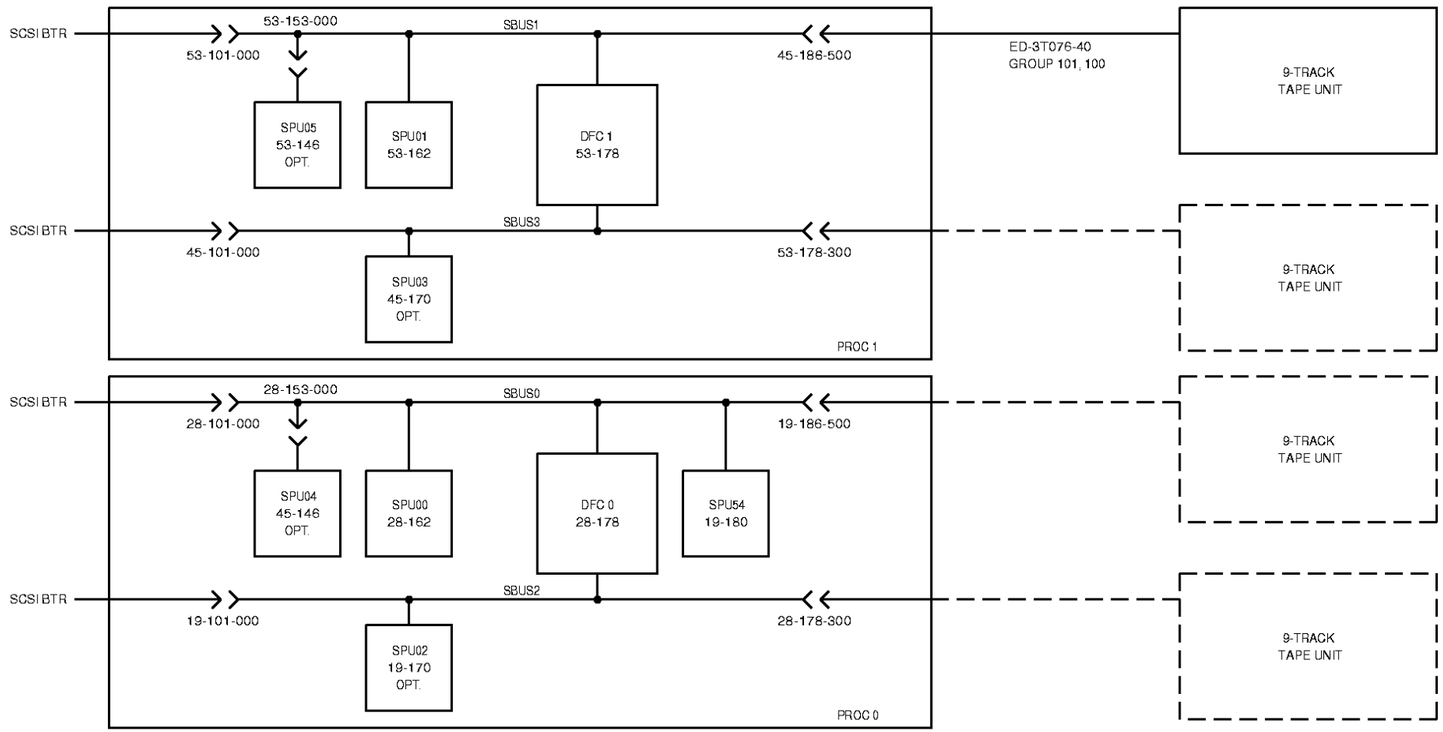
BD 4

SCSI CABLING
9-TRACK TAPE

NOTES:

1. THE SCSI 9-TRACK TAPE UNIT MAY BE CONNECTED TO ANY OF THESE FOUR POSITIONS.
2. ONE TO FOUR 9-TRACK UNITS MAY BE CONNECTED.
3. NO SCAN ASSIGNMENTS FOR THE SCSI 9-TRACK UNIT.



ED-3T076-40
GROUP 101, 100

9-TRACK
TAPE UNIT

9-TRACK
TAPE UNIT

9-TRACK
TAPE UNIT

9-TRACK
TAPE UNIT

3B21D PROCESSOR COMPUTER SYSTEMS		DWG SIZE C2	ISSUE 1
AT&T	SD-3T015-01		SHEET H4

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