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8B	1	6-11-93			

SUPPORTING INFORMATION			
SYSTEM USED ON	DESIGN CONTROL	CATEGORY	NO.
SESS	IH	EQUIPMENT DRAWING	J50003AP-02
		FRAME SD	SD-5D113-01 SD-5D119-01

SHEET INDEX NOTES

- ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
- FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
- THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

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BT13

SESS[®] SWITCHING EQUIPMENT

FACILITIES INTERFACE UNIT

MODEL 2

CIRCUIT

DWG SIZE	ISSUE
C2	8B

AT&T SD-5D401-01 SHEET A1
32 SHEETS

0 1 2 3 4 5 6 7 8 9 PRINTED IN U.S.A.

DESIGNATION MNEMONICS

MNEMONICS	FS/SYM	DEFINITION	MNEMONICS	FS/SYM	DEFINITION	MNEMONICS	FS/SYM	DEFINITION	MNEMONICS	FS/SYM	DEFINITION
GRD04(028-086)	1/2-16	SIDE 0 GROUND, EQL'S 04-026 THROUGH 04-086	Q(A,B)TPAR	1/4, 15	SIDE 0, GROUP A OR B, TRANSMIT PARITY ERROR	Q(0,1)DLIALM	1-2/1	SIDE 0 OR 1, ALARM	Q(0,1)NINTIP	1-2/10	SIDE 0, 0 OR 1 NEGATIVE INTERRUPT (POS)
GRD04(116-176)	2/2-16	SIDE 1 GROUND, EQL'S 04-116 THROUGH 04-176	Q(A,B)TPARIN	1/5	SIDE 0, GROUP A OR B, TRANSMIT PARITY INPUT	Q(0,1)DLIALMP	1-2/1	SIDE 0 OR 1, DLI ALARM LAMP	Q(0,1)ODN	1-2/10	SIDE 0, 0 OR 1 OUT DATA (NEG)
Q-CURPR	1/4	SIDE 0, PLUS CURRENT PROGRAMMING RESISTOR	Q(A,B)WA7	1/4, 15	SIDE 0, GROUP A OR B, WRITE ADDRESS BIT 7	Q(0,1)DLIINT	1-2/5	SIDE 0 OR 1, DLI INTERRUPT	Q(0,1)ODP	1-2/10	SIDE 0, 0 OR 1 OUT DATA (POS)
Q+12	1/2	SIDE 0, +12 VOLT POWER	Q(A,B)WRENO	1/4, 15	SIDE 0, GROUP A OR B, WRITE ENABLE, ACTIVE LOW	Q(0,1)DLIS1	1-2/1	SIDE 0 OR 1, DLI SHUTDOWN 1	Q(0,1)SN	1-2/10	SIDE 0, 0 OR 1 SYNC (NEG)
Q+5V	1/2	SIDE 0, +5 VOLT POWER	Q(A,B)WFIST	1/8, 8, 11, 13	SIDE 0, GROUP A OR B, DFI STATUS 0 THROUGH 8	Q(0,1)DLIS2	1-2/1	SIDE 0 OR 1, DLI SHUTDOWN 2	Q(0,1)SP	1-2/10	SIDE 0, 0 OR 1 SYNC (POS)
Q-CURPR	1/4	SIDE 0, MINUS CURRENT PROGRAMMING RESISTOR	Q(A,B)(0-9)DFIST	1/8, 8, 11, 13	SIDE 0, GROUP A OR B, DFI STATUS 0 THROUGH 9	Q(0,1)DLIS3	1-2/1	SIDE 0 OR 1, DLI SHUTDOWN 3	1-CURPR	2/4	SIDE 1, PLUS CURRENT PROGRAMMING RESISTOR
Q-48RTN	1/1	SIDE 0, -48 VOLT RETURN	Q(A,B)(0-9)PBIN	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (NEG)	Q(0,1)DOOS48	1-2/1	SIDE 0 OR 1, DLI OUT-OF-SERVICE (-48V)	1+12	2/2	SIDE 1, -12 VOLT POWER
Q-48V	1/1	SIDE 0, -48 VOLT POWER FEED	Q(A,B)(0-9)PBIP	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (POS)	Q(0,1)FREERUN	1-2/10	SIDE 0 OR 1, SELECT FREERUN	1+5V	2/2	SIDE 1, +5 VOLT POWER
Q(A,B)BUFFER	1/4, 15	SIDE 0, GROUP A OR B BUFFER	Q(A,B)(0-9)PBOP	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	Q(0,1)FRSQ	1-2/5	SIDE 0 OR 1, FRAME SEQUENCE	1-CURPR	2/4	SIDE 1, MINUS CURRENT PROGRAMMING RESISTOR
Q(A,B)CERAM0	1/4, 15	SIDE 0, GROUP A OR B, CHIP ENABLE RAM, ACTIVE LOW	Q(A,B)(0-9)PBON	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	Q(0,1)FRSQT3	1-2/5	SIDE 0 OR 1, FRAME SEQUENCE FROM T3 CARRIER	1-48RTN	2/1	SIDE 1, -48 VOLT RETURN
Q(A,B)CKCCI	1/5	SIDE 0, GROUP A OR B, CLOCK CENTRAL PROCESSOR INTERVENTION	Q(A,B)(0-9)PBOP	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	Q(0,1)GRD	1-2/10	SIDE 0 OR 1, GROUND	1-48V	2/1	SIDE 1, -48 VOLT POWER FEED
Q(A,B)CK16M	1/10	SIDE 0, GROUP A OR B, 16 MHZ CLOCK	Q(A,B)(0-9)PBOP	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	Q(0,1)MATEEN	1-2/5	SIDE 0 OR 1, MATE ENABLE	1(A,B)BUFFER	2/4, 15	SIDE 1, GROUP A OR B BUFFER
Q(A,B)CK2M1	1/4, 15	SIDE 0, GROUP A OR B, CLOCK 2 MHZ	Q(A,B)(0-9)PBOP	1/3, 16	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	Q(0,1)MCK4M0	1/5, 10	SIDE 0 OR 1, MATE CLOCK 4 MHZ, ACTIVE LOW	1(A,B)CERAM0	2/4, 15	SIDE 1, GROUP A OR B, CHIP ENABLE RAM, ACTIVE LOW
Q(A,B)CK32	1/5	SIDE 0, GROUP A OR B, 32 MHZ CLOCK	Q(A,B)(0-9)RESET	1/7, 9, 12, 14	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, RESET	Q(0,1)MPCK	1-2/10	SIDE 0 OR 1, MATE CONTROL INTERFACE CLOCK	1(A,B)CKCCI	2/5	SIDE 1, GROUP A OR B, CLOCK CENTRAL PROCESSOR INTERVENTION
Q(A,B)CK4K1	1/5	SIDE 0, GROUP A OR B, CLOCK 4 KHZ	Q(A,B)(0-9)RESET	1/7, 9, 12, 14	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, RESET	Q(0,1)MPOATA	1-2/10	SIDE 0 OR 1, MATE CONTROL DATA IN	1(A,B)CK16M	2/10	SIDE 1, GROUP A OR B, 16 MHZ CLOCK
Q(A,B)CK8MC	1/10	SIDE 0, GROUP A OR B, CLOCK 8 MHZ	Q(A,B)ORP	1/4, 15	SIDE 0, A OR B GROUP, RECEIVE PARITY	Q(0,1)MPG0	1-2/10	SIDE 0 OR 1, MATE CONTROL INTERFACE COMMAND ENABLE	1(A,B)CK2M1	2/4, 15	SIDE 1, GROUP A OR B, CLOCK 2 MHZ
Q(A,B)COND5	1/4, 15	SIDE 0, LINK CONDITIONED POWER	Q(A,B)ORP	1/4, 15	SIDE 0, A OR B GROUP, RECEIVE PARITY	Q(0,1)MPOUT	1-2/5	SIDE 0 OR 1, MATE CONTROL DATA OUT	1(A,B)CK32	2/5	SIDE 1, GROUP A OR B, 32 MHZ CLOCK
Q(A,B)DFRSQ	1/5	SIDE 0, GROUP A OR B, DISABLE FRAME SEQUENCE	Q(A,B)ORX	1/4, 15	SIDE 0, A OR B GROUP, RECEIVE DATA X	Q(0,1)PWR5	1-2/4, 15	SIDE 0 OR 1, +5 VOLT POWER	1(A,B)CK4K1	2/5	SIDE 1, GROUP A OR B, CLOCK 4 KHZ
Q(A,B)DSFBIT	1/5	SIDE 0, GROUP A OR B, ADD S AND F BIT	Q(A,B)ORY	1/4, 15	SIDE 0, A OR B GROUP, RECEIVE DATA Y	Q(0,1)RA(0-7)	1-2/5	SIDE 0 OR 1, RECEIVE ADDRESS BITS 0 THROUGH 7	1(A,B)CK8MC	2/10	SIDE 1, GROUP A OR B, CLOCK 8 MHZ
Q(A,B)ECTRIN	1/4, 15	SIDE 0, GROUP A OR B, ERROR COUNTER INPUT	Q(A,B)ORZ	1/4, 15	SIDE 0, A OR B GROUP, RECEIVE DATA Z	Q(0,1)REC	1-2/4, 15	SIDE 0 OR 1, RECEIVE FROM SWITCHING MODULE	1(A,B)COND5	2/4, 15	SIDE 1, LINK CONDITIONED POWER
Q(A,B)INFRIN	1/4, 15	SIDE 0, GROUP A OR B, INFRAME INPUT	Q(A,B)OTP	1/3, 16	SIDE 0, A OR B GROUP, TRANSMIT PARITY	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)DFRSQ	2/5	SIDE 1, GROUP A OR B, DISABLE FRAME SEQUENCE
Q(A,B)INT	1/1	SIDE 0, GROUP A OR B, INTERRUPT	Q(A,B)OTX	1/3, 16	SIDE 0, A OR B GROUP, TRANSMIT DATA X	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)DSFBIT	2/5	SIDE 1, GROUP A OR B, ADD S AND F BIT
Q(A,B)LOOP	1/5	SIDE 0, GROUP A OR B, LOOP LINK	Q(A,B)OTY	1/3, 16	SIDE 0, A OR B GROUP, TRANSMIT DATA Y	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)ECTRIN	2/4, 15	SIDE 1, GROUP A OR B, ERROR COUNTER INPUT
Q(A,B)MUXCR	1/10	SIDE 0, GROUP A OR B, MUX CONTROL REGISTER ENABLE	Q(A,B)OTZ	1/3, 16	SIDE 0, A OR B GROUP, TRANSMIT DATA Z	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)INFRIN	2/4, 15	SIDE 1, GROUP A OR B, INFRAME INPUT
Q(A,B)MUXDI	1/3, 16	SIDE 0, GROUP A OR B, MUX DATA IN	Q(A,B)T1 CLK	1/7, 9, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 CLOCK	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)INT	2/1	SIDE 1, GROUP A OR B INTERRUPT
Q(A,B)MUXDO	1/10	SIDE 0, GROUP A OR B, MUX DATA OUT	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)LOOP	2/5	SIDE 1, GROUP A OR B, LOOP LINK
Q(A,B)MUXER	1/10	SIDE 0, GROUP A OR B, MUX ERROR REGISTER ENABLE	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXCR	2/10	SIDE 1, GROUP A OR B, MUX CONTROL REGISTER ENABLE
Q(A,B)MUXINT	1/3, 16	SIDE 0, GROUP A OR B, MUX INTERRUPT	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXDI	2/3, 16	SIDE 1, GROUP A OR B, MUX DATA IN
Q(A,B)MUXRD	1/10	SIDE 0, GROUP A OR B, MUX READ	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXDO	2/10	SIDE 1, GROUP A OR B, MUX DATA OUT
Q(A,B)MUXSH	1/10	SIDE 0, GROUP A OR B, MUX SHIFT CLOCK	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXER	2/10	SIDE 1, GROUP A OR B, MUX ERROR REGISTER ENABLE
Q(A,B)MUXWR	1/10	SIDE 0, GROUP A OR B, MUX WRITE	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXINT	2/3, 16	SIDE 1, GROUP A OR B, MUX INTERRUPT
Q(A,B)RPAR	1/4, 15	SIDE 0, GROUP A OR B, RECEIVE PARITY ERROR	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXRD	2/10	SIDE 1, GROUP A OR B, MUX READ
Q(A,B)RPARIN	1/5	SIDE 0, GROUP A OR B, RECEIVE PARITY INPUT	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXSH	2/10	SIDE 1, GROUP A OR B, MUX SHIFT CLOCK
Q(A,B)SICCODE	1/5	SIDE 0, GROUP A OR B, SEND IDLE CODE	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE	1(A,B)MUXWR	2/10	SIDE 1, GROUP A OR B, MUX WRITE
Q(A,B)SYN2M0	1/5	SIDE 0, GROUP A OR B, SYNC 2 MHZ LOW	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE			
Q(A,B)SYN4K	1/10	SIDE 0, GROUP A OR B, SYNC 4 KHZ	Q(A,B)(0-9)T1 STA	1/6, 8, 10	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	Q(0,1)XMIT	1-2/4, 15	SIDE 0 OR 1 TRANSMIT TO SWITCHING MODULE			

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FACILITIES INTERFACE UNIT MODEL 2		DWG SIZE C2
AT&T		ISSUE 8B
SD-5D401-01		SHEET A2

DESIGNATION MNEMONICS

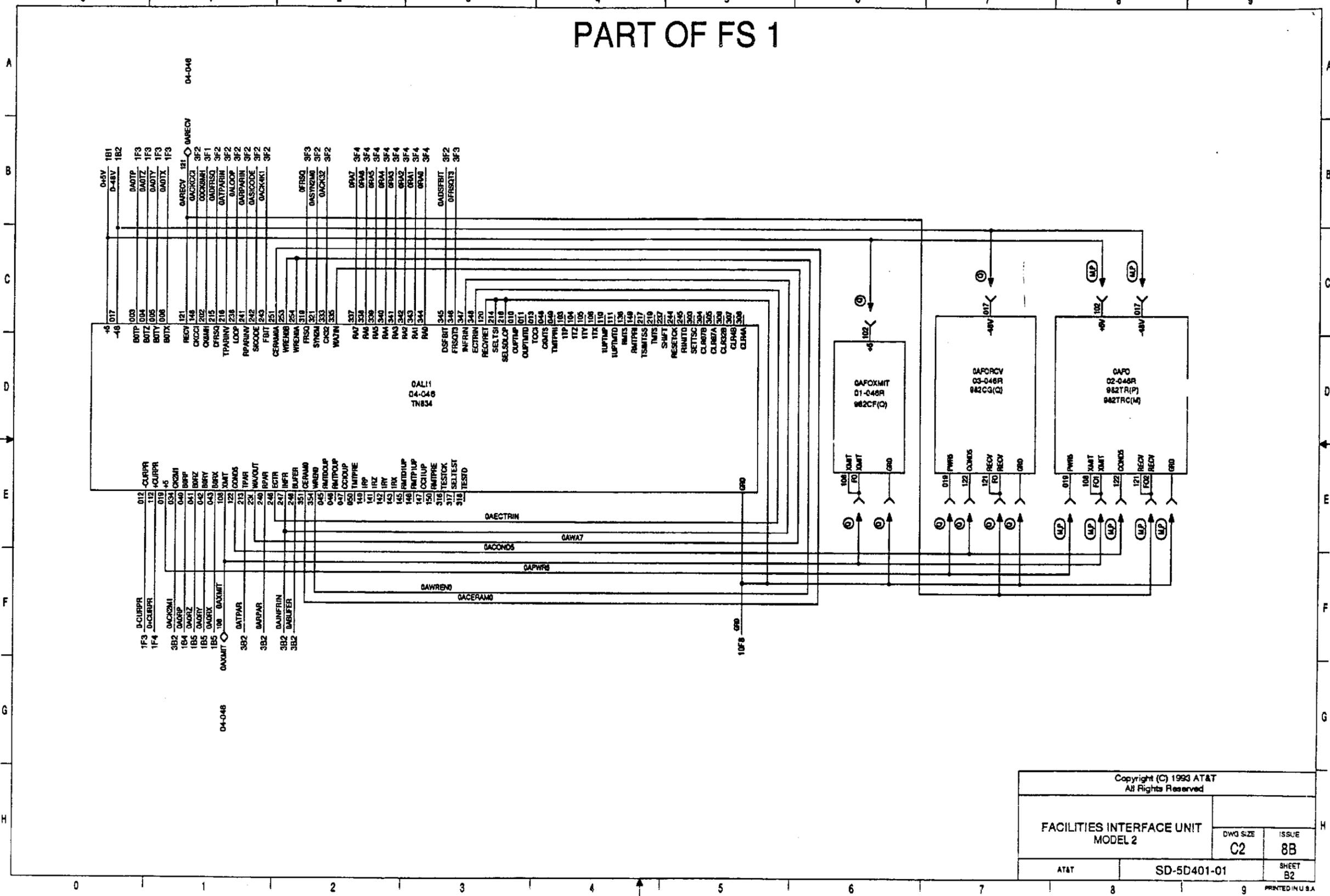
	MNEMONICS	FS/SYM	DEFINITION	MNEMONICS	FS/SYM	DEFINITION
A	1(A,B)RPAR	2/4,15	SIDE 1, GROUP A OR B, RECEIVE PARITY ERROR	1(A,B)(0-9)T1STA	2/6,8,10	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS
	1(A,B)RPARIN	2/5	SIDE 1, GROUP A OR B, RECEIVE PARITY INPUT	1(A,B)(0-9)4MCN	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (NEG)
	1(A,B)SICODE	2/5	SIDE 1, GROUP A OR B, SEND IDLE CODE	1(A,B)(0-9)4MCP	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (POS)
B	1(A,B)SYN2M0	2/5	SIDE 1, GROUP A OR B, SYNC 2 MHZ, ACTIVE LOW	1(A,B)(0-9)8KSN	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (NEG)
	1(A,B)SYN4K	2/10	SIDE 1, GROUP A OR B, SYNC 4 KHZ	1(A,B)(0-9)8KSP	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (POS)
	1(A,B)TPAR	2/4,15	SIDE 1, GROUP A OR B, TRANSMIT PARITY ERROR	1BBUF	2/16	SIDE 1 GROUP B, BUFFER
	1ATPARIN	2/5	SIDE 1, GROUP A TRANSMIT PARITY INPUT	10CKMH	2/5	SIDE 1, CLOCK 8 MHZ TO SWITCHING MODULE
	1(A,B)WA7	2/4,15	SIDE 1, GROUP A OR B, WRITE ADDRESS, BIT 7	1(0,1)CN	2/10	SIDE 1, 0 OR 1 CLOCK (NEG)
C	1(A,B)WRENO	2/4,15	SIDE 1, GROUP A OR B, WRITE ENABLE, ACTIVE LOW	1(0,1)CP	2/10	SIDE 1, 0 OR 1 CLOCK (POS)
	1(A,B)(0-9)DFIST	2/6,8 11,13	SIDE 1, GROUP A OR B, DFI STATUS 0 THROUGH 9	1(0,1)DN	2/10	SIDE 1, 0 OR 1 IN DATA (NEG)
	1(A,B)(0-9)PBIN	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (NEG)	1(0,1)DP	2/10	SIDE 1, 0 OR 1 IN DATA (POS)
D	1(A,B)(0-9)PBIP	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (POS)	1(0,1)NINTIN	2/10	SIDE 1, 0 OR 1 NEGATIVE INTERRUPT (NEG)
	1(A,B)(0-9)PBON	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	1(0,1)NINTIP	2/10	SIDE 1, 0 OR 1 NEGATIVE INTERRUPT (POS)
	1(A,B)(0-9)PBOP	2/3,16	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	1(0,1)ODN	2/10	SIDE 1, 0 OR 1 OUT DATA (NEG)
E	1(A,B)(0-9)RESET	2/7,8 12,14	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, RESET	1(0,1)ODP	2/10	SIDE 1, 0 OR 1 OUT DATA (POS)
	1(A,B)ORP	2/4,15	SIDE 1, A OR B GROUP, RECEIVE PARITY	1(0,1)SN	2/10	SIDE 1, 0 OR 1 SYNC (NEG)
	1(A,B)ORX	2/4,15	SIDE 1, A OR B GROUP, RECEIVE DATA X	1(0,1)SP	2/10	SIDE 1, 0 OR 1 SYNC (POS)
F	1(A,B)ORY	2/4,15	SIDE 1, A OR B GROUP, RECEIVE DATA Y	10SYNMS	2/5	SIDE 1, 0 SELECT SYNC 6 MHZ
	1(A,B)ORZ	2/4,15	SIDE 1, A OR B GROUP, RECEIVE DATA Z	11CKMH	2/5	SIDE 1, 1 CLOCK 8 MHZ
	1(A,B)OTP	2/3,16	SIDE 1, A OR B GROUP, TRANSMIT PARITY	14KOUT	2/10	SIDE 1, 4K OUTPUT
	1(A,B)OTX	2/3,16	SIDE 1, A OR B GROUP, TRANSMIT DATA X	16KIN0	2/10	SIDE 1, 8K INPUT FOR CIRCUIT 0
G	1(A,B)OTY	2/3,16	SIDE 1, A OR B GROUP, TRANSMIT DATA Y	16KIN1	2/10	SIDE 1, 8K INPUT FOR CIRCUIT 0
	1(A,B)OTZ	2/3,16	SIDE 1, A OR B GROUP, TRANSMIT DATA Z	16KREF	2/10	SIDE 1, 8K REFERENCE
	1(A,B)(0-9)T1CLK	2/7,9,10	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 CLOCK	16KRTN0	2/10	SIDE 1, 8K RETURN FOR CIRCUIT 0
				16KRTN1	2/10	SIDE 1, 8K RETURN FOR CIRCUIT 1

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FACILITIES INTERFACE UNIT MODEL 2	DWG SIZE C2	ISSUE 8B
AT&T	SD-5D401-01	SHEET A3

APPARATUS INDEX					LEAD INDEX
CODE	EQUIP LOC	SHEET LOC	APP FIG.	OPTION	SEE CAD 1
TN618	04-068	B4D4	2	(2)	
TN618	04-158	B11D4	2	(2)	
TN618B	04-068	B4E4	2	(3)	
TN618B	04-158	B11E4	2	(3)	
TN618C	04-068	B4E4	2	(3)	
TN618C	04-158	B11E4	2	(3)	
TN618D	04-068	B4E4	2	(3)	
TN618D	04-158	B11E4	2	(3)	
TN619	04-038	B1D8	2	(3)	
TN619	04-088	B8E8	2	(3)	
TN619	04-128	B8E8	2	(3)	
TN619	04-178	B13E8	2	(3)	
TN834	04-048	B2D3	2		
TN834	04-078	B5D3	2		
TN834	04-138	B9D3	2		
TN834	04-168	B12D3	2		
TN835	04-058	B3D4	2		
TN835	04-148	B10D4	2		
TN1039	04-038	B1C8	2	(3)	
TN1039	04-088	B8E8	2	(3)	
TN1039	04-128	B8E8	2	(3)	
TN1039	04-178	B13E8	2	(3)	
495KA	04-028	B1D2	2		
495KA	04-118	B8C2	2		
982CF	01-048R	B2D8	3	(3)	
982CF	01-078R	B5D8	3	(3)	
982CF	01-138R	B9D8	3	(3)	
982CF	01-168R	B12D8	3	(3)	
982CG	03-048R	B2D7	3	(3)	
982CG	03-078R	B5D7	3	(3)	
982CG	03-138R	B9D7	3	(3)	
982CG	03-168R	B12D7	3	(3)	
982TR	02-048R	B2D8	3	(3)	
982TR	02-078R	B5D8	3	(3)	
982TR	02-138R	B9D8	3	(3)	
982TR	02-168R	B12D8	3	(3)	
TN1802	04-038	B1D8	2	(3)	
TN1802	04-088	B8E8	2	(3)	
TN1802	04-128	B8E8	2	(3)	
TN1802	04-178	B13E8	2	(3)	
982TRC	02-048R	B2D8	3	(3)	
982TRC	02-078R	B5D8	3	(3)	
982TRC	02-138R	B9D8	3	(3)	
982TRC	02-168R	B12D8	3	(3)	

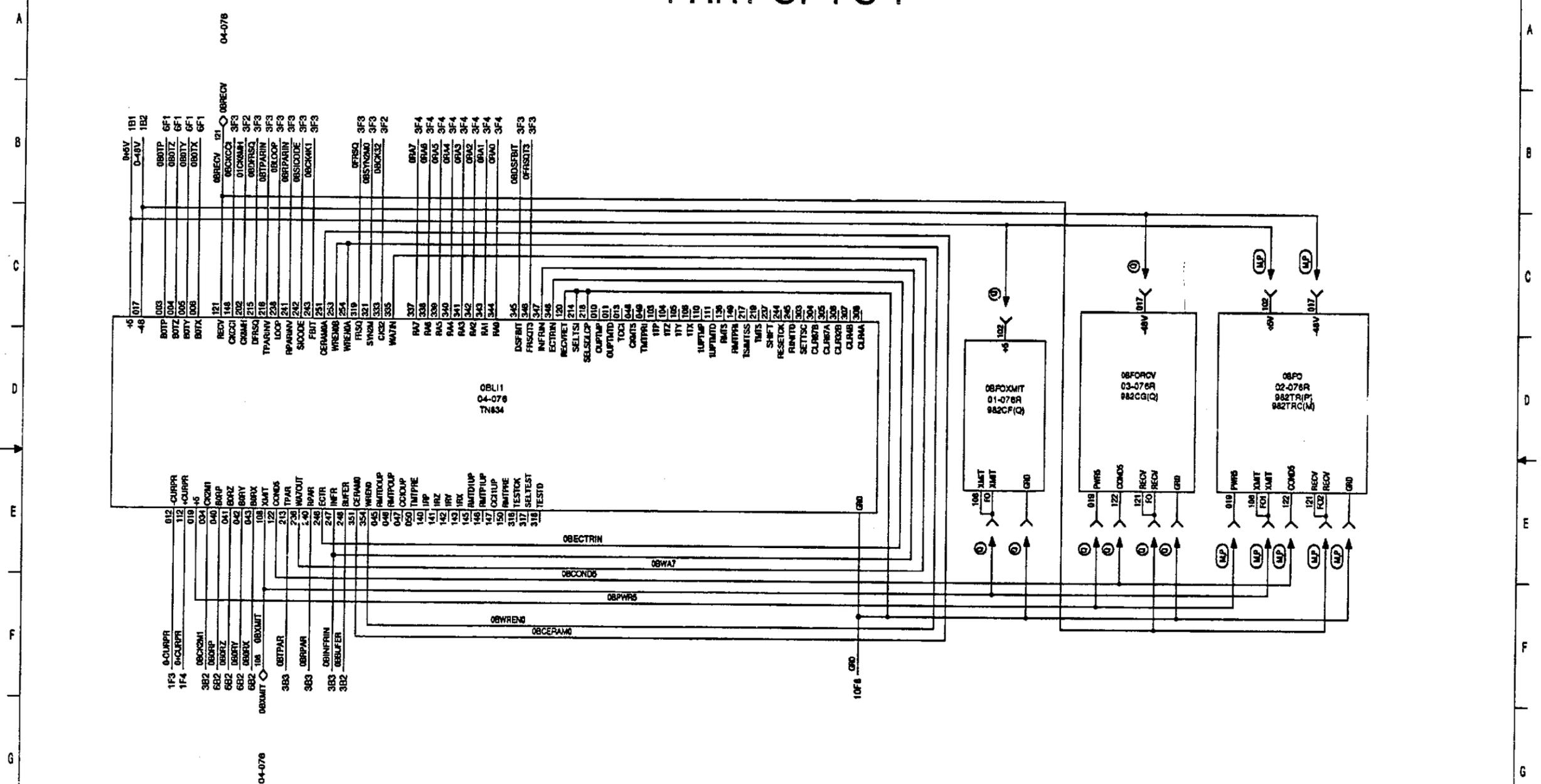
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003 TP	060TP	000	046Y	1B1	
004 TZ	060TZ	004			
005 TY	060TY	005			
006 TX	060TX	006			
012 RP1	060RP1	012			
017 RP2	060RP2	017			
018 TP4		018			
021 TP3		021			
022 TP5		022			
02	060MOUNT	02			
03	060MOUNT	03			
038 MUD01		038			
039 MUD02		039			
040 MUD03		040			
041 MUD04		041			
042 MUD05		042			
043 MUD06		043			
044 MUD07		044			
045 MUD08		045			
046 MUD09		046			
047 MUD10		047			
048 MUD11		048			
049 MUD12		049			
050 MUD13		050			
051 MUD14		051			
052 MUD15		052			
053 MUD16		053			
054 MUD17		054			
055 MUD18		055			
056 MUD19		056			
057 MUD20		057			
058 MUD21		058			
059 MUD22		059			
060 MUD23		060			
061 MUD24		061			
062 MUD25		062			
063 MUD26		063			
064 MUD27		064			
065 MUD28		065			
066 MUD29		066			
067 MUD30		067			
068 MUD31		068			
069 MUD32		069			
070 MUD33		070			
071 MUD34		071			
072 MUD35		072			
073 MUD36		073			
074 MUD37		074			
075 MUD38		075			
076 MUD39		076			
077 MUD40		077			
078 MUD41		078			
079 MUD42		079			
080 MUD43		080			
081 MUD44		081			
082 MUD45		082			
083 MUD46		083			
084 MUD47		084			
085 MUD48		085			
086 MUD49		086			
087 MUD50		087			
088 MUD51		088			
089 MUD52		089			
090 MUD53		090			
091 MUD54		091			
092 MUD55		092			
093 MUD56		093			
094 MUD57		094			
095 MUD58		095			
096 MUD59		096			
097 MUD60		097			
098 MUD61		098			
099 MUD62		099			
100 MUD63		100			

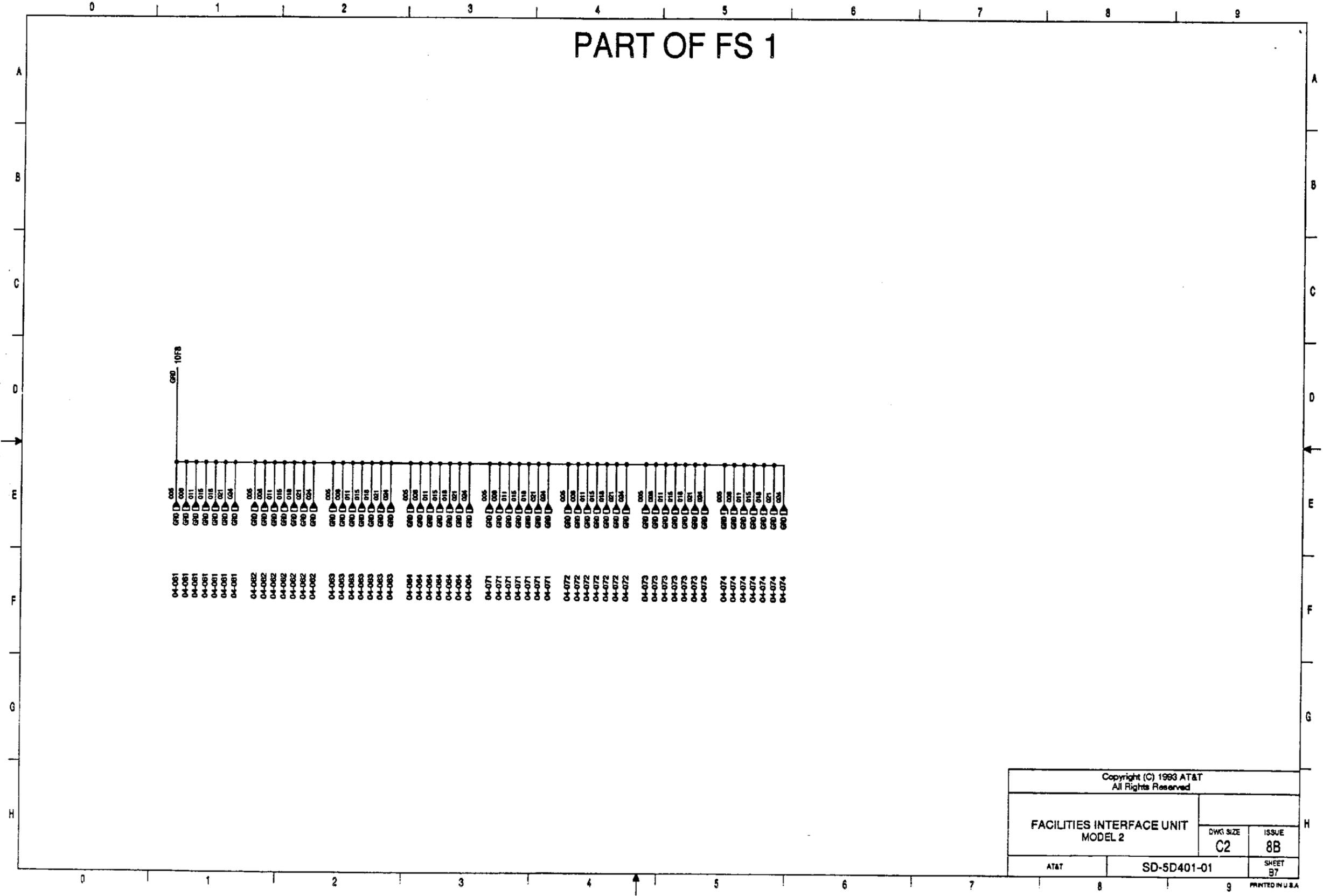
060MUD
04-088
TN1819(9)
TN1820(7)

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	C2	8B
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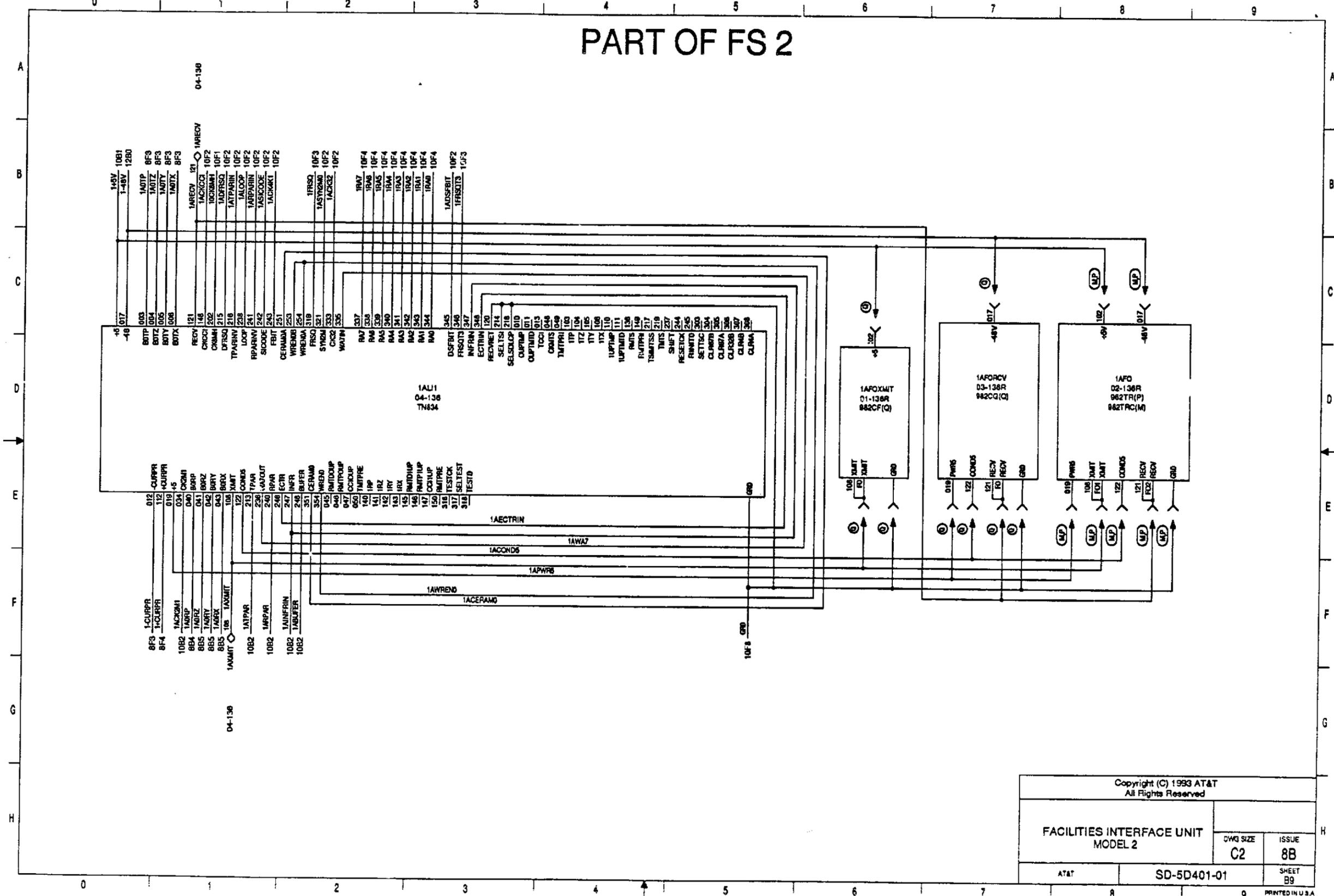
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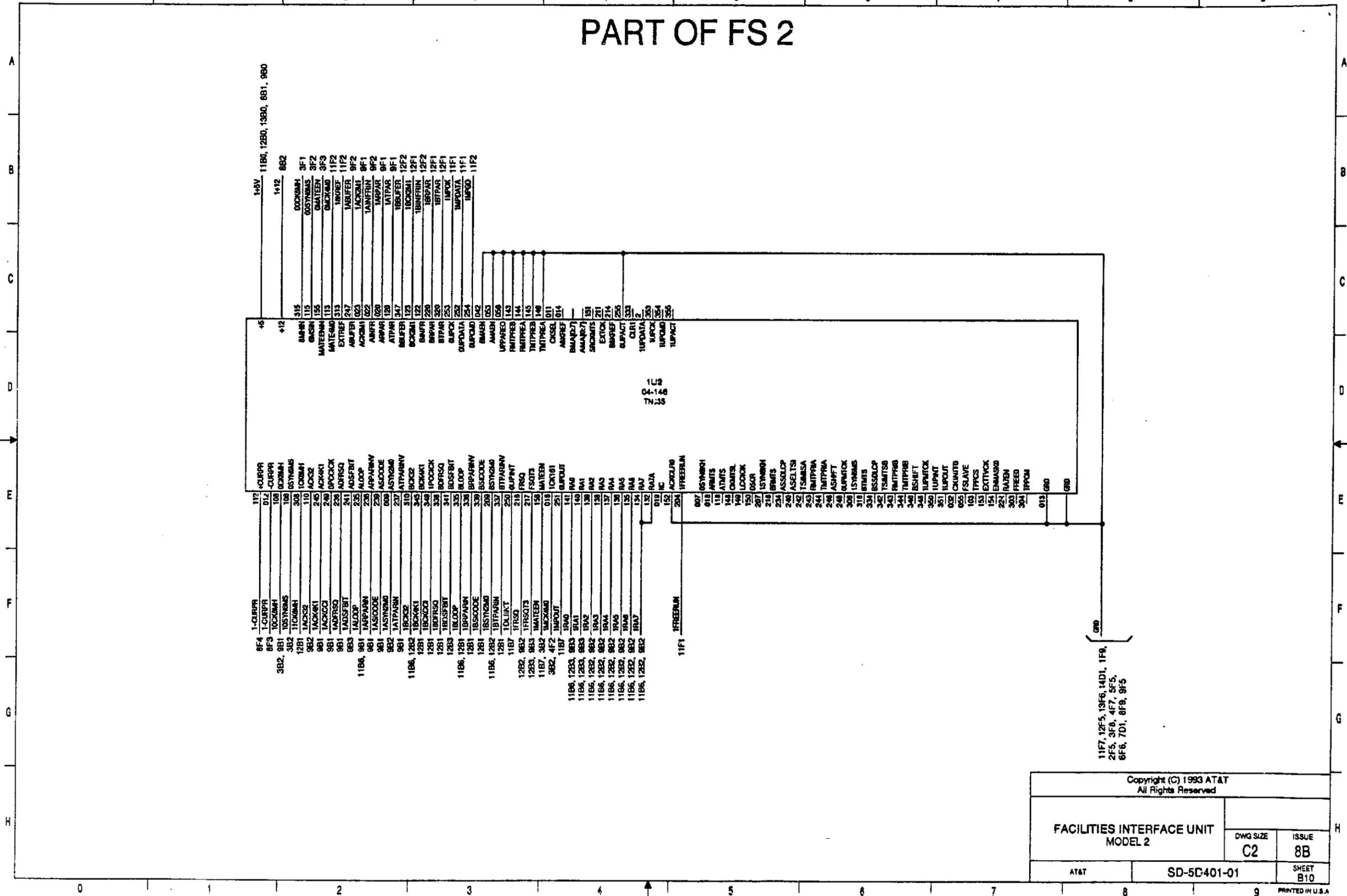
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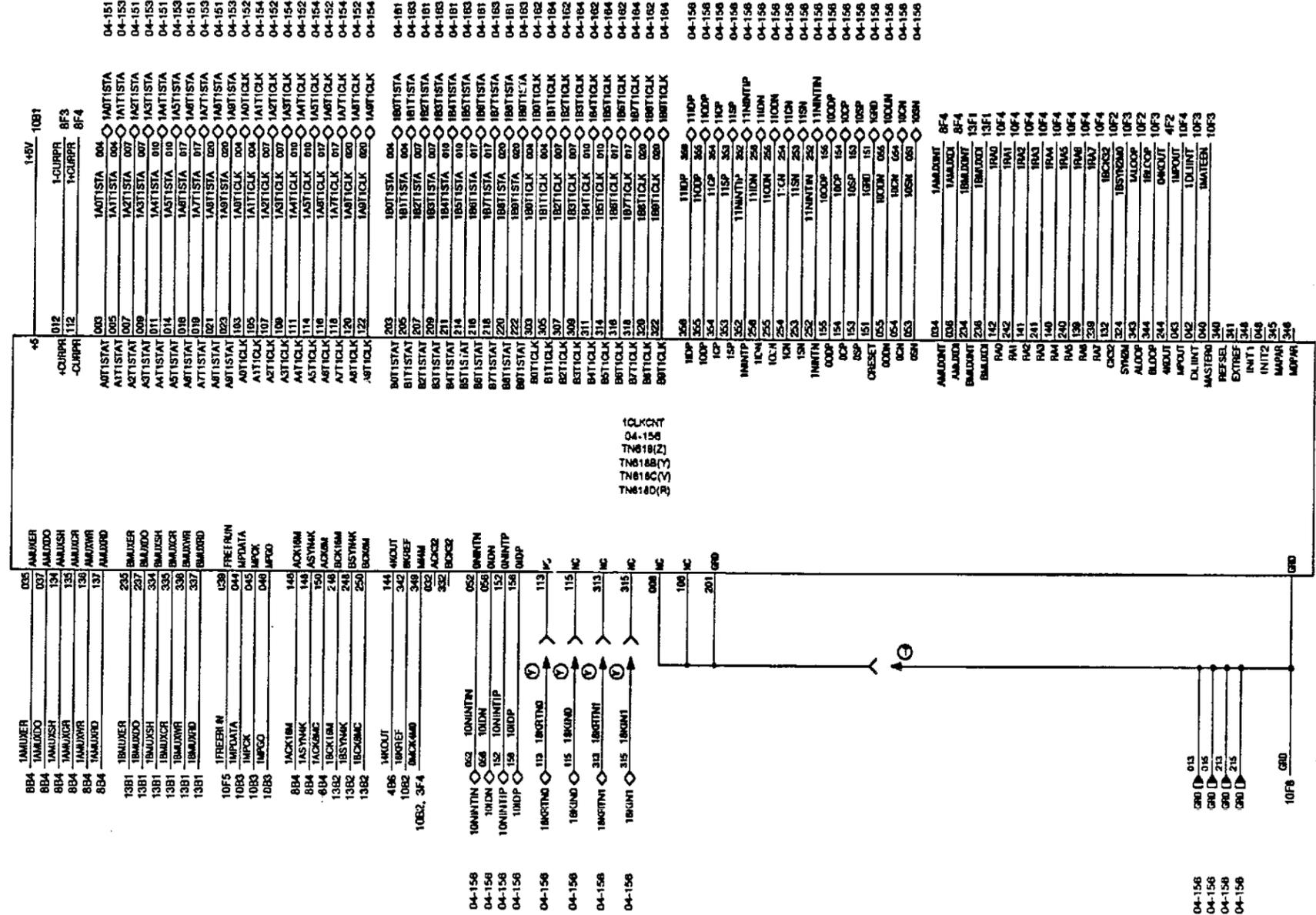
11F7, 12F5, 13F6, 14D1, 1F9,
2F5, 3F8, 4F7, 5F5,
6F6, 7D1, 8F9, 9F5

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		C2	8B
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1CLXGAT
04-156
7N618(Z)
7N618(B)(Y)
7N618(C)(Y)
7N618(C)(R)

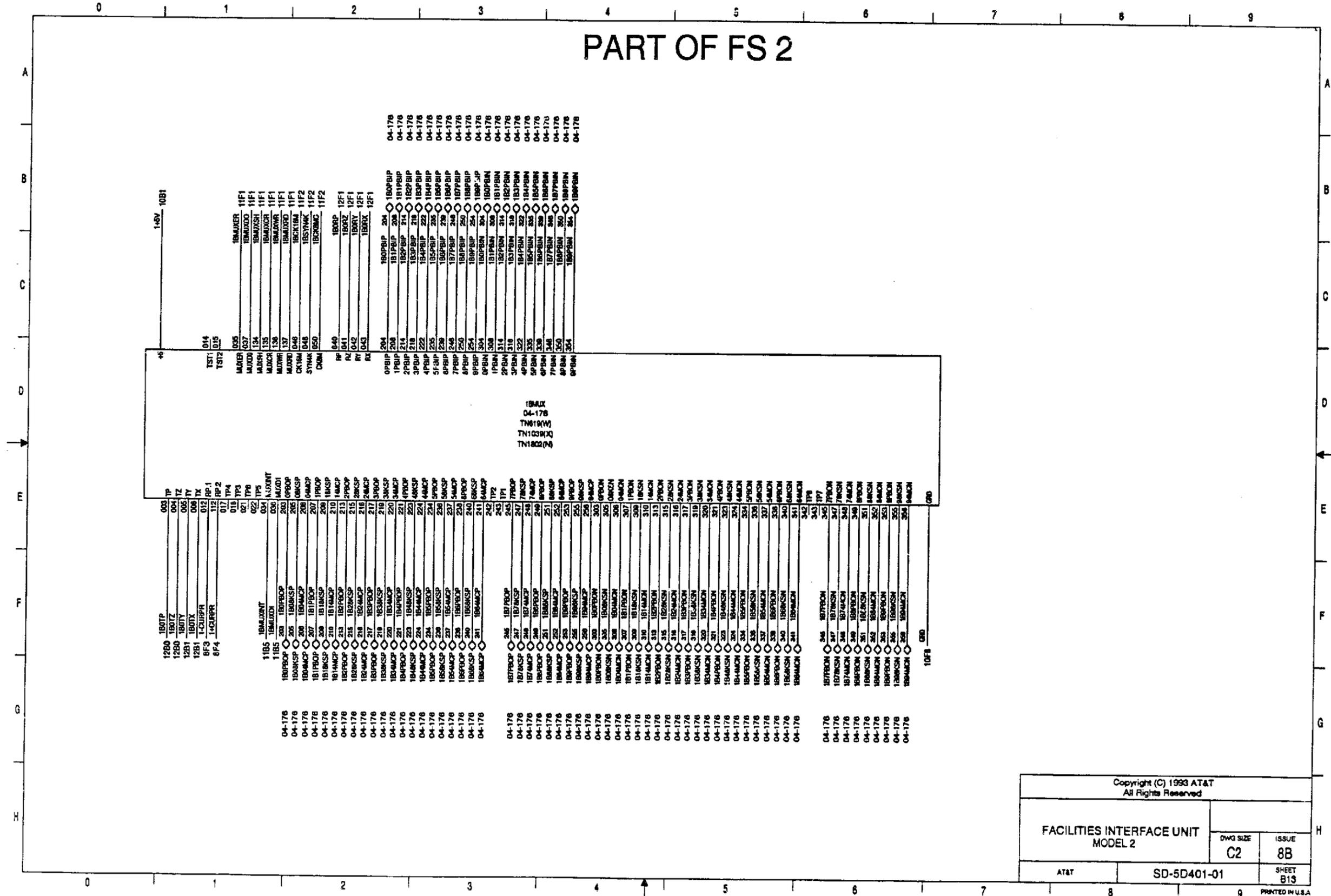
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FACILITIES INTERFACE UNIT
MODEL 2

DWG SIZE C2	ISSUE 8B
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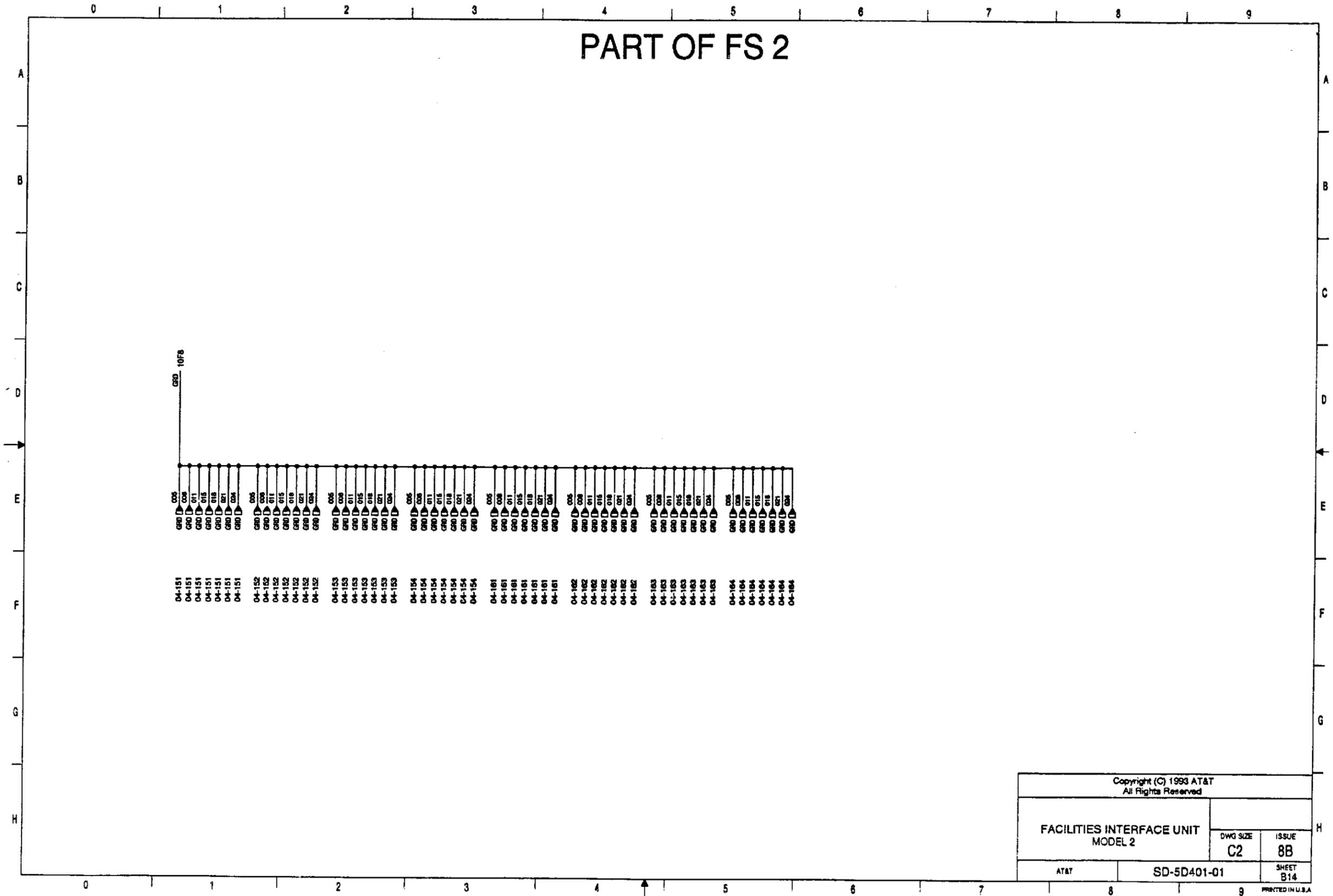
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		SHEET B14

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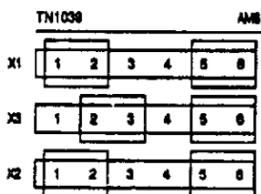
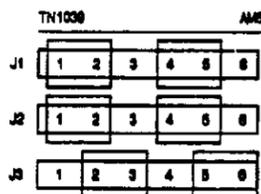
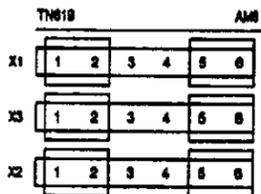
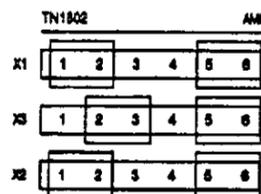
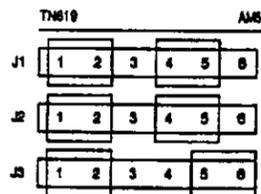
CIRCUIT NOTES:

DESIG	FUSE AMP	POTENTIAL	ONE PER
0-48V 1-48V	70C 3A	-48V	SIDE (0,1) TOTAL 2
BATTERY SYMBOL		VOLTAGE RANGE	
-48		-42.75 TO -52.50	

102. WHEN THE FACILITY INTERFACE UNIT IS USED IN A CABINET EQUIPPED WITH A MODULAR FUSE/FILTER UNIT THE FOLLOWING FUSE ARRANGEMENT IS REQUIRED:

DESIG	FUSE AMP	FUSE TYPE
0-48V	2A	WP 81768 L107
1-48V	2A	WP 81768 L107

103. THE FOLLOWING DIAGRAM PROVIDES PROGRAMMING PLUG POSITION INFORMATION:



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0 1 2 3 4 5 6 7 8 9

A
B
C
D
E
F
G
H

A
B
C
D
E
F
G
H

EQUIPMENT NOTES:

201. UNLESS OTHERWISE SPECIFIED, ALL BACKPLANE WIRING WILL BE AUTOMATIC MACHINE WIRING (A-D4) 30 GAUGE, WHICH HAS BEEN PROCESSED BY THE WESWRAP PROGRAMS.

202. ALL PRINTED WIRING CONNECTIONS ARE SPECIFIED BY ED-5D623-30.

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0 1 2 3 4 5 6 7 8 9

INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS,
CAPACITANCE VALUES ARE IN MICROFARADS,
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.

302.

FEATURE OR OPTION	PROVIDE		QUANTITY
	APP FIG	APP OR WRG	
BACKPLANE & WIRING	24 CHANNEL	S	1 PER SIDE
	30 CHANNEL	T	
MINIMUM EQUIPAGE	FACILITIES INTERFACE (TN834)		2 PER SIDE
	LINK INTERFACE (TN835)		
	POWER (485KA)		
CLOCK CONTROLLER	NO RCU (TN818)	Z	1 PER SIDE
	WITH RCU OR WITHOUT 24 CHANNEL (TN818B)	Y	
	24 CHANNEL WITH OR WITHOUT RCU (TN818C)	V	
	24 OR 30 CHANNEL WITH OR WITHOUT RCU (TN818D)	R	
MULTIPLEXER (SEE NOTE 305)	24 CHANNEL (TN819)	W	2 PER SIDE
	30 CHANNEL (TN1039)	X	
	24 CHANNEL (TN1802)	N	
NCT LINK FIBER OPTIC CONNECTORS	ODL40 TYPE (4) 982CF (4) 982CG	Q	2 PER SIDE
	ODL50 TYPE (4) 982TR	P	
	LDT TYPE (4) 982TRC (SEE NOTE 306)	M	

INFORMATION NOTES: (CONT)

303.

CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT		
				STD	ADM	MD
2B	Y	Y OR Z	Y		Z	
4A	W		W			
4A	X		X			
5AC		S,T,V	S,T,V			
				AVAIL	DA	
6A		R		R		
7M		P,Q		P,Q		
8B		M,N		M,N		

PRIOR TO ISSUE 6A, COLUMNS HEADED "STD", "MD", ETC., CONVEYED APPLICATION INFORMATION. AT ISSUE 6A, COLUMNS HEADED "AVAIL" AND "DA" NOW INDICATE THE AVAILABILITY OF THE PRODUCT.

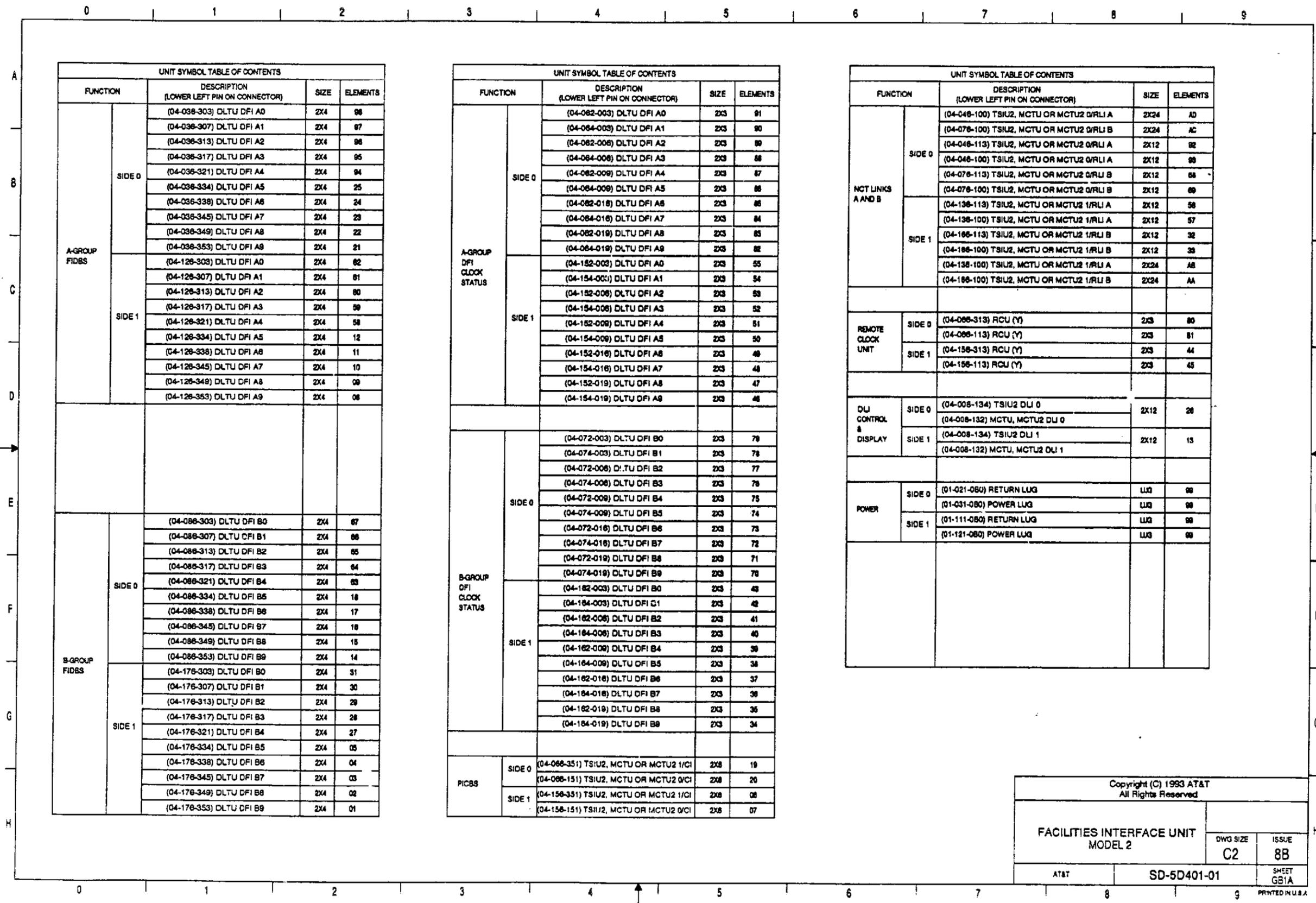
304.

CIRCUIT PACK CODE OR MICROCODE	COMMON LANGUAGE EQUIPMENT IDENTIFICATION CODE (CLEI)
TN818	ESPC218A0X
TN818B	ESPC218A0X
TN818C	ESPC218A0X
TN818D	ESPC218A0X
TN819	ESPC219A0X
TN834	ESPC287A0X
TN835	ESPC287A0X
TN1039	ESPC287A0X
485KA	PWPQ54EA0X
TN1802	ESPC287A0X

305. OPTIONS W AND X TO BE USED WHEN FIU INTERFACES WITH A DLTU. OPTION N TO BE USED WHEN FIU 2 OR 3 INTERFACES WITH A DLTU2.

306. THE 982TRC LDT PRODUCT MEETS THE INTERNATIONAL CIS PER 22 EMC REQUIREMENTS.

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FACILITIES INTERFACE UNIT MODEL 2		DWG SIZE C2
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UNIT SYMBOL TABLE OF CONTENTS			
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS
A-GROUP FIBRS	SIDE 0	(04-036-303) DLTU DFI A0	2X4 98
		(04-036-307) DLTU DFI A1	2X4 97
		(04-036-313) DLTU DFI A2	2X4 96
		(04-036-317) DLTU DFI A3	2X4 95
		(04-036-321) DLTU DFI A4	2X4 94
		(04-036-334) DLTU DFI A5	2X4 25
		(04-036-338) DLTU DFI A6	2X4 24
		(04-036-345) DLTU DFI A7	2X4 23
		(04-036-349) DLTU DFI A8	2X4 22
	(04-036-353) DLTU DFI A9	2X4 21	
	SIDE 1	(04-126-303) DLTU DFI A0	2X4 82
		(04-126-307) DLTU DFI A1	2X4 81
		(04-126-313) DLTU DFI A2	2X4 80
		(04-126-317) DLTU DFI A3	2X4 79
		(04-126-321) DLTU DFI A4	2X4 78
		(04-126-334) DLTU DFI A5	2X4 12
		(04-126-338) DLTU DFI A6	2X4 11
		(04-126-345) DLTU DFI A7	2X4 10
(04-126-349) DLTU DFI A8		2X4 99	
(04-126-353) DLTU DFI A9	2X4 98		
B-GROUP FIBRS	SIDE 0	(04-086-303) DLTU DFI B0	2X4 87
		(04-086-307) DLTU DFI B1	2X4 86
		(04-086-313) DLTU DFI B2	2X4 85
		(04-086-317) DLTU DFI B3	2X4 84
		(04-086-321) DLTU DFI B4	2X4 83
		(04-086-334) DLTU DFI B5	2X4 18
		(04-086-338) DLTU DFI B6	2X4 17
		(04-086-345) DLTU DFI B7	2X4 16
		(04-086-349) DLTU DFI B8	2X4 15
	(04-086-353) DLTU DFI B9	2X4 14	
	SIDE 1	(04-176-303) DLTU DFI B0	2X4 31
		(04-176-307) DLTU DFI B1	2X4 30
		(04-176-313) DLTU DFI B2	2X4 29
		(04-176-317) DLTU DFI B3	2X4 28
		(04-176-321) DLTU DFI B4	2X4 27
		(04-176-334) DLTU DFI B5	2X4 05
		(04-176-338) DLTU DFI B6	2X4 04
		(04-176-345) DLTU DFI B7	2X4 03
(04-176-349) DLTU DFI B8		2X4 02	
(04-176-353) DLTU DFI B9	2X4 01		

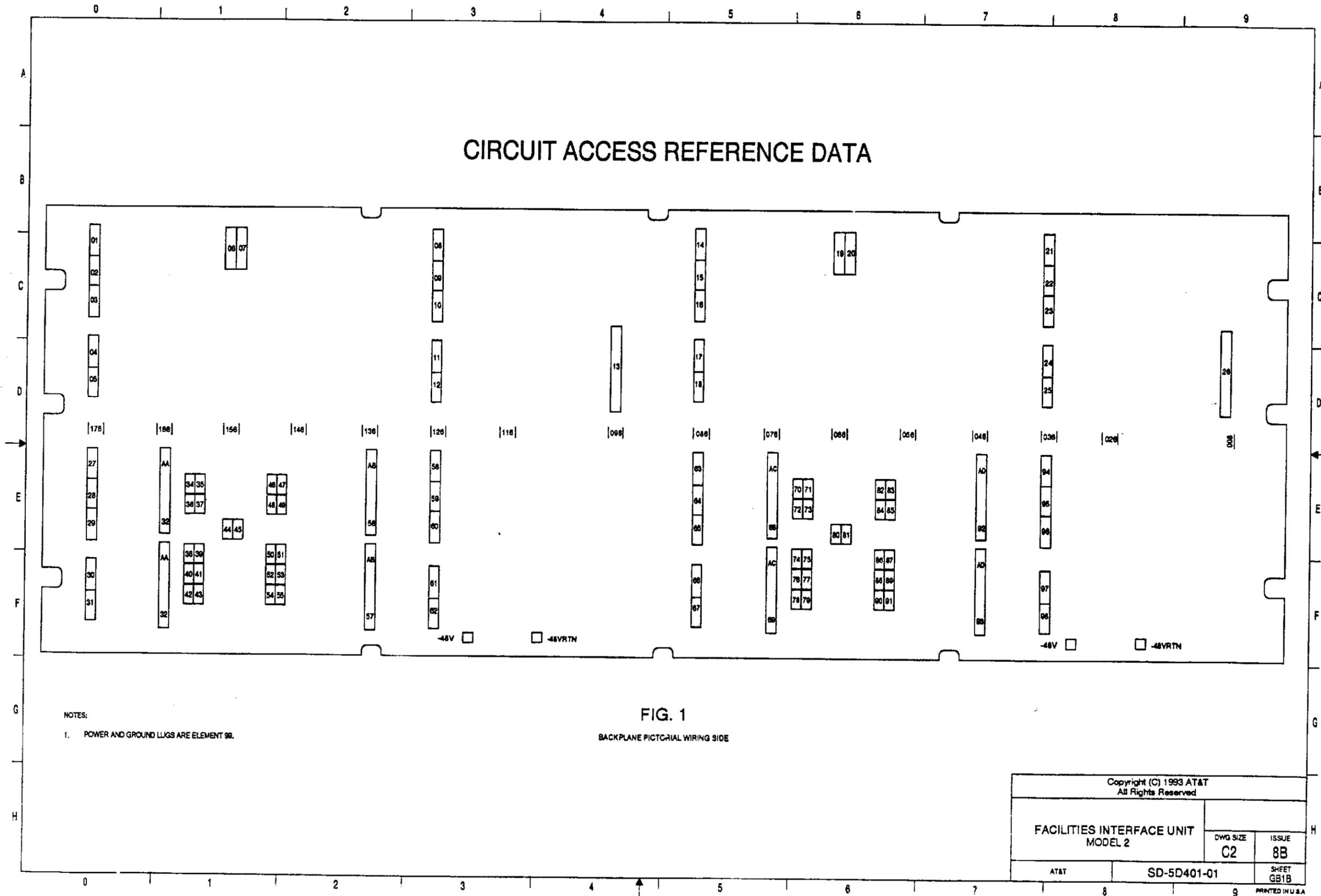
UNIT SYMBOL TABLE OF CONTENTS			
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS
A-GROUP DFI CLOCK STATUS	SIDE 0	(04-082-003) DLTU DFI A0	2X3 91
		(04-082-003) DLTU DFI A1	2X3 90
		(04-082-008) DLTU DFI A2	2X3 89
		(04-082-008) DLTU DFI A3	2X3 88
		(04-082-009) DLTU DFI A4	2X3 87
		(04-082-009) DLTU DFI A5	2X3 86
		(04-082-018) DLTU DFI A6	2X3 85
		(04-082-018) DLTU DFI A7	2X3 84
		(04-082-018) DLTU DFI A8	2X3 83
	(04-082-018) DLTU DFI A9	2X3 82	
	SIDE 1	(04-152-003) DLTU DFI A0	2X3 55
		(04-152-003) DLTU DFI A1	2X3 54
		(04-152-008) DLTU DFI A2	2X3 53
		(04-152-008) DLTU DFI A3	2X3 52
		(04-152-008) DLTU DFI A4	2X3 51
		(04-152-008) DLTU DFI A5	2X3 50
		(04-152-018) DLTU DFI A6	2X3 49
		(04-152-018) DLTU DFI A7	2X3 48
(04-152-018) DLTU DFI A8		2X3 47	
(04-152-018) DLTU DFI A9	2X3 46		
B-GROUP DFI CLOCK STATUS	SIDE 0	(04-072-003) DLTU DFI B0	2X3 79
		(04-072-003) DLTU DFI B1	2X3 78
		(04-072-008) DLTU DFI B2	2X3 77
		(04-072-008) DLTU DFI B3	2X3 76
		(04-072-008) DLTU DFI B4	2X3 75
		(04-072-008) DLTU DFI B5	2X3 74
		(04-072-018) DLTU DFI B6	2X3 73
		(04-072-018) DLTU DFI B7	2X3 72
		(04-072-018) DLTU DFI B8	2X3 71
	(04-072-018) DLTU DFI B9	2X3 70	
	SIDE 1	(04-182-003) DLTU DFI B0	2X3 43
		(04-182-003) DLTU DFI B1	2X3 42
		(04-182-008) DLTU DFI B2	2X3 41
		(04-182-008) DLTU DFI B3	2X3 40
		(04-182-008) DLTU DFI B4	2X3 39
		(04-182-008) DLTU DFI B5	2X3 38
		(04-182-018) DLTU DFI B6	2X3 37
		(04-182-018) DLTU DFI B7	2X3 36
(04-182-018) DLTU DFI B8		2X3 35	
(04-182-018) DLTU DFI B9	2X3 34		
PICBS	SIDE 0	(04-068-351) TSIU2, MCTU OR MCTU2 1/CI	2X8 19
		(04-068-151) TSIU2, MCTU OR MCTU2 0/CI	2X8 20
	SIDE 1	(04-158-351) TSIU2, MCTU OR MCTU2 1/CI	2X8 08
		(04-158-151) TSIU2, MCTU OR MCTU2 0/CI	2X8 07

UNIT SYMBOL TABLE OF CONTENTS			
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS
NCT LINKS A AND B	SIDE 0	(04-048-100) TSIU2, MCTU OR MCTU2 0/RLI A	2X24 AD
		(04-078-100) TSIU2, MCTU OR MCTU2 0/RLI B	2X24 AC
		(04-048-113) TSIU2, MCTU OR MCTU2 0/RLI A	2X12 92
		(04-048-100) TSIU2, MCTU OR MCTU2 0/RLI A	2X12 98
		(04-078-113) TSIU2, MCTU OR MCTU2 0/RLI B	2X12 88
		(04-078-100) TSIU2, MCTU OR MCTU2 0/RLI B	2X12 89
	SIDE 1	(04-138-113) TSIU2, MCTU OR MCTU2 1/RLI A	2X12 56
		(04-138-100) TSIU2, MCTU OR MCTU2 1/RLI A	2X12 57
		(04-168-113) TSIU2, MCTU OR MCTU2 1/RLI B	2X12 32
		(04-168-100) TSIU2, MCTU OR MCTU2 1/RLI B	2X12 38
		(04-138-100) TSIU2, MCTU OR MCTU2 1/RLI A	2X24 AB
		(04-168-100) TSIU2, MCTU OR MCTU2 1/RLI B	2X24 AA
REMOTE CLOCK UNIT	SIDE 0	(04-088-313) RCU (Y)	2X3 80
		(04-088-113) RCU (Y)	2X3 81
	SIDE 1	(04-158-313) RCU (Y)	2X3 44
		(04-158-113) RCU (Y)	2X3 45
DLI CONTROL & DISPLAY	SIDE 0	(04-008-134) TSIU2 DLI 0	2X12 28
		(04-008-132) MCTU, MCTU2 DLI 0	
	SIDE 1	(04-008-134) TSIU2 DLI 1	2X12 13
		(04-008-132) MCTU, MCTU2 DLI 1	
POWER	SIDE 0	(01-021-080) RETURN LUG	LUG 99
		(01-031-080) POWER LUG	LUG 99
	SIDE 1	(01-111-080) RETURN LUG	LUG 99
		(01-121-080) POWER LUG	LUG 99

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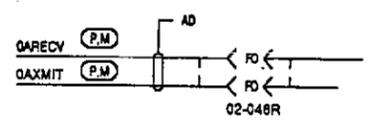
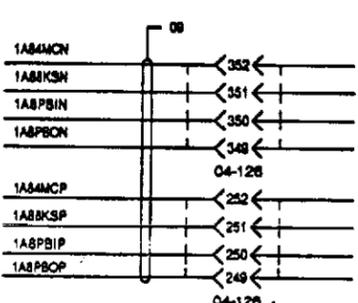
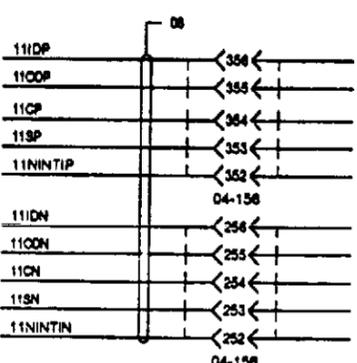
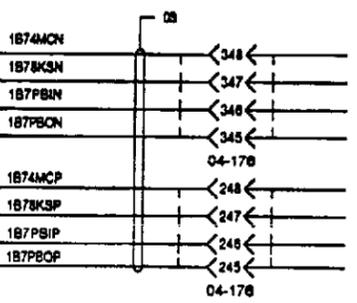
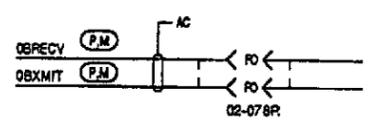
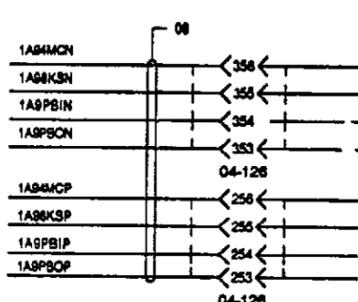
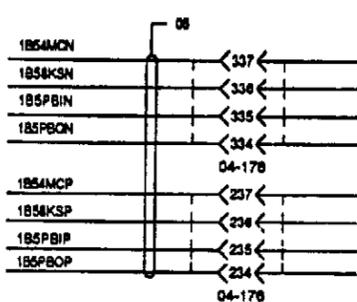
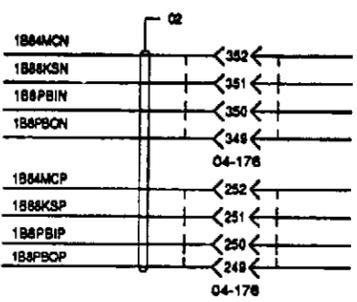
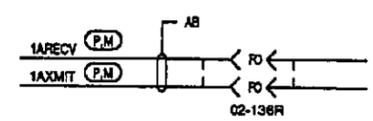
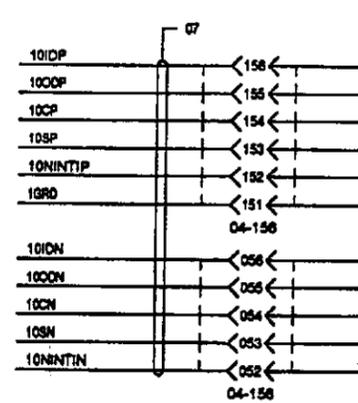
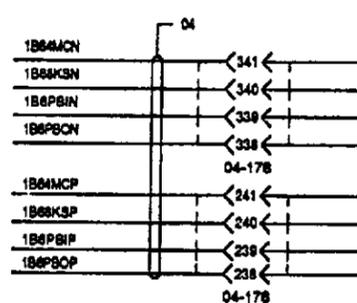
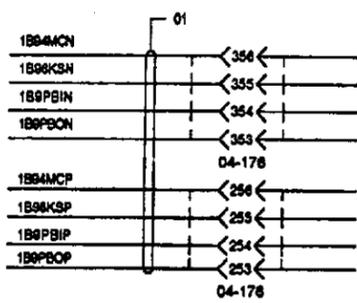
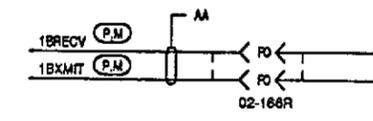
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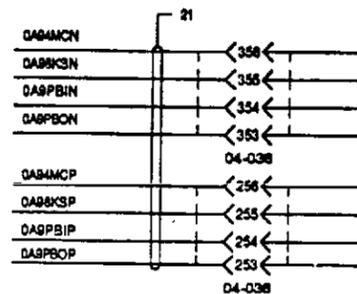
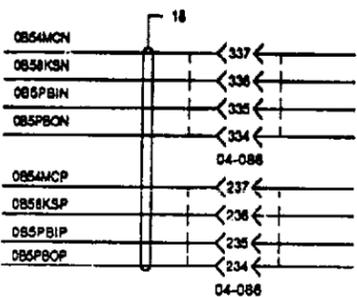
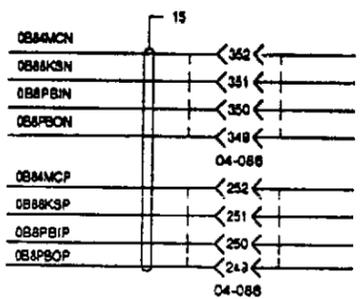
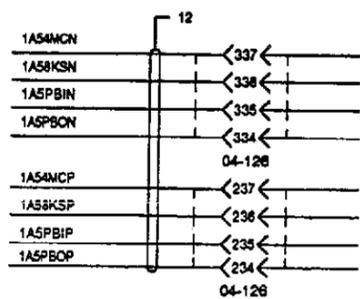
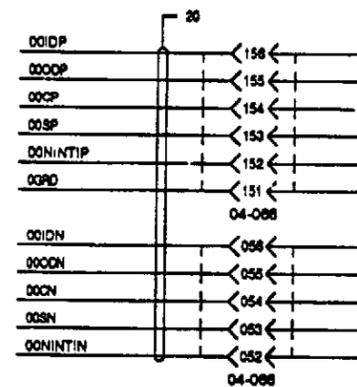
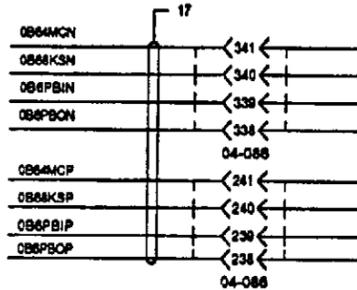
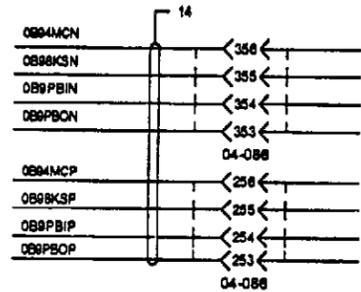
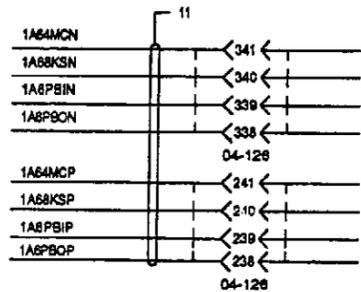
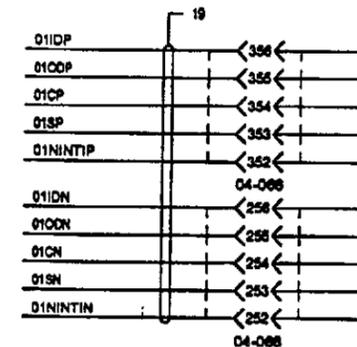
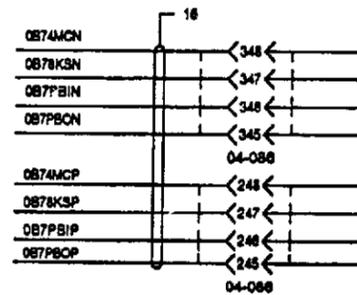
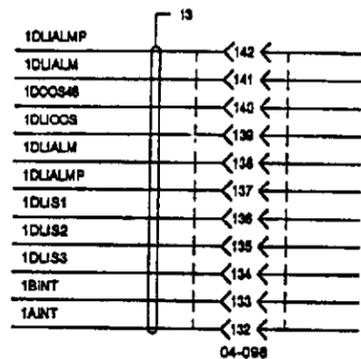
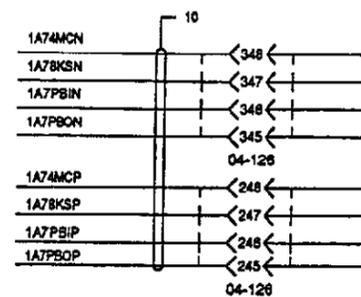


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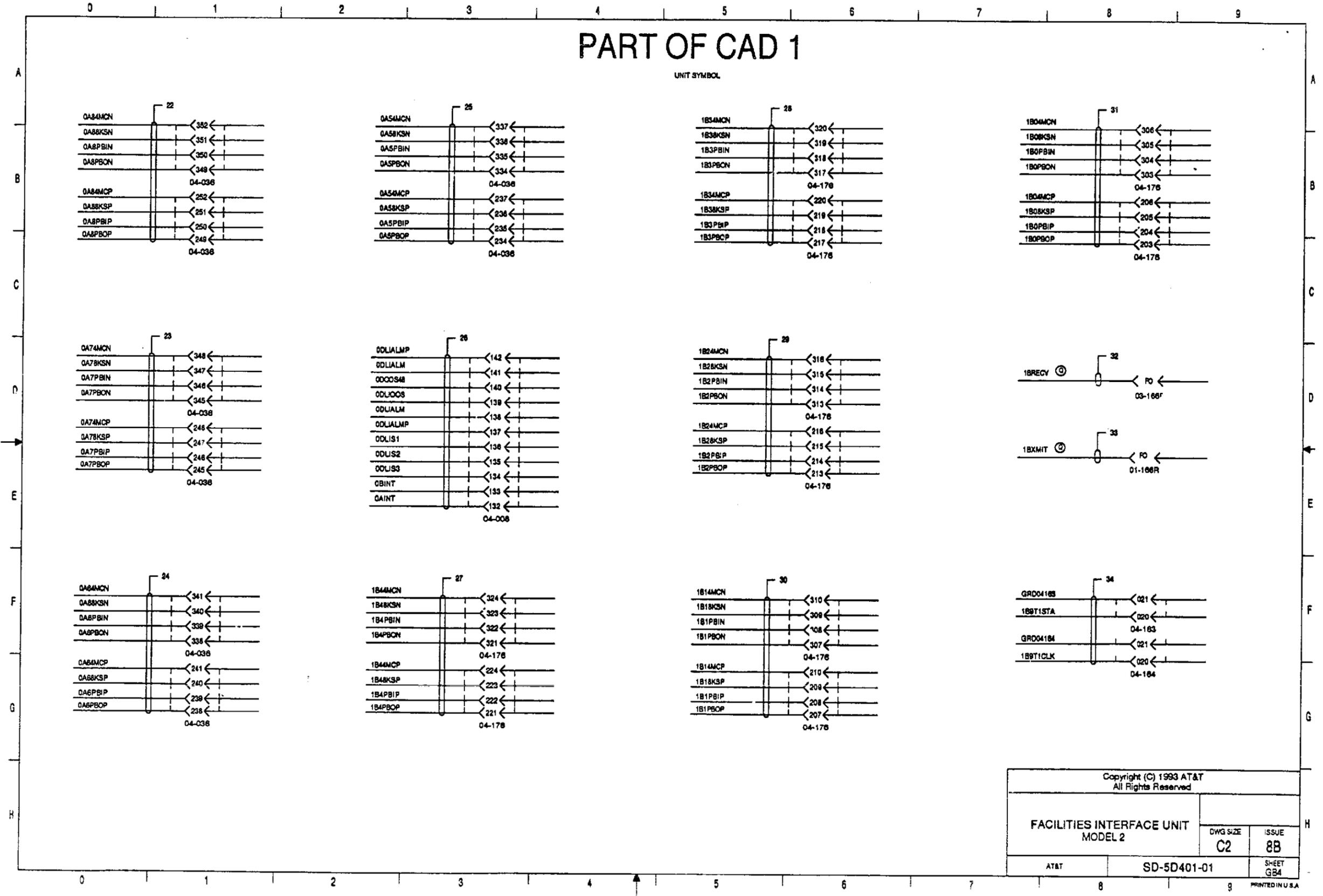
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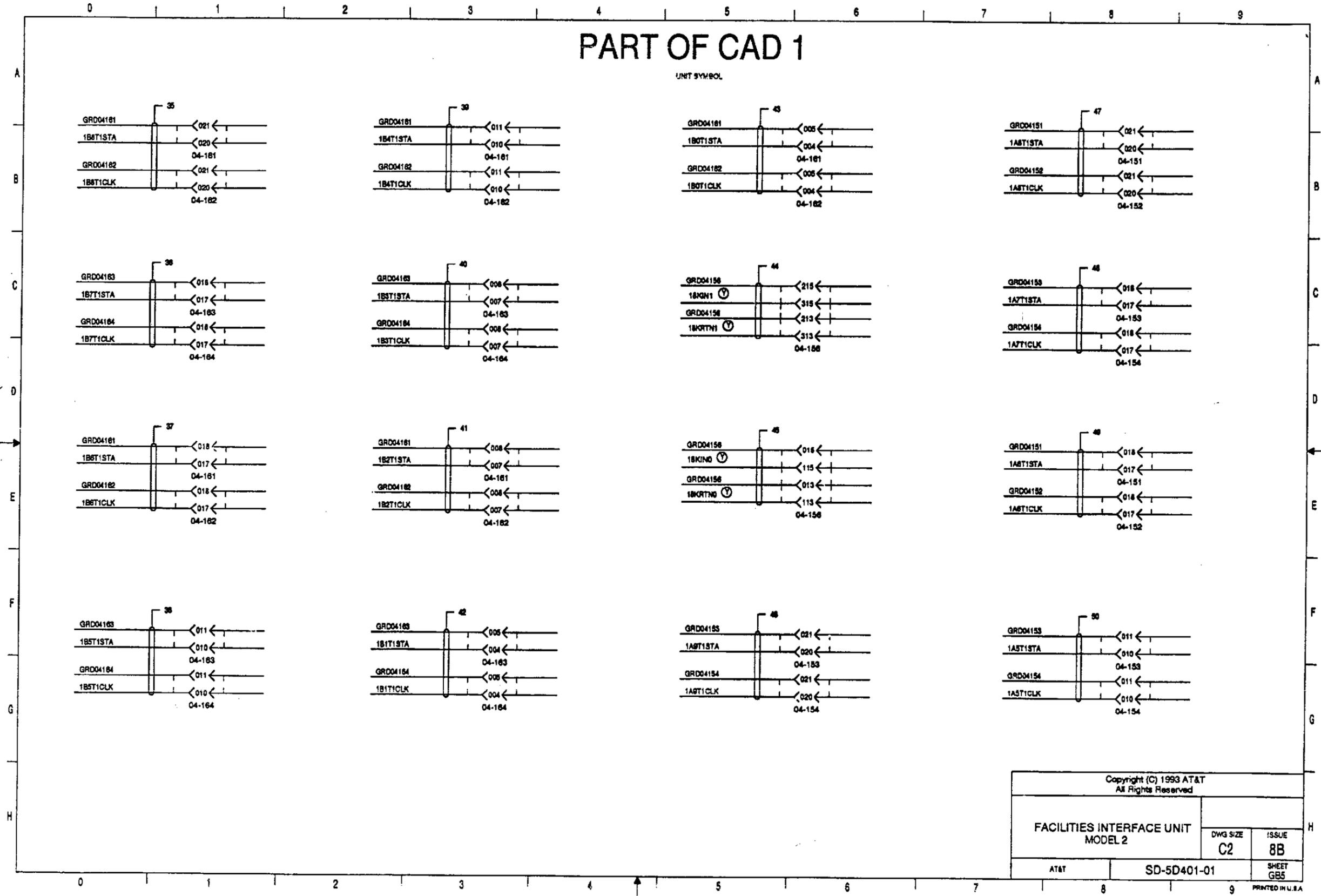
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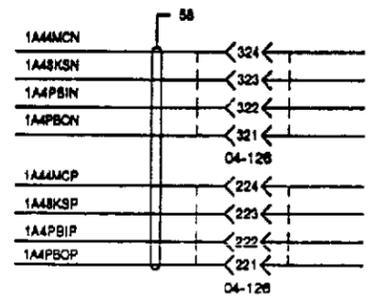
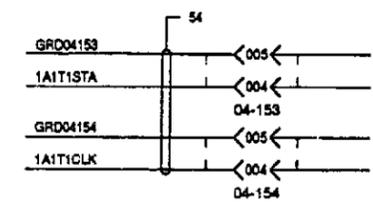
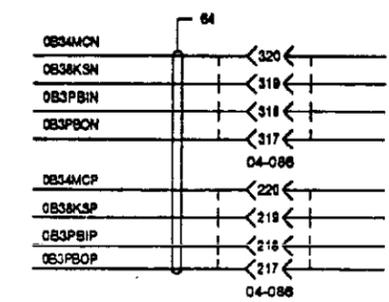
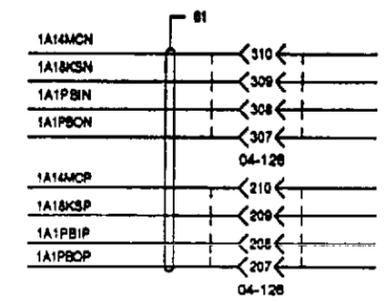
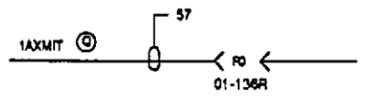
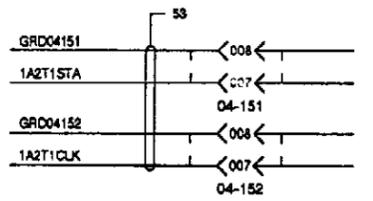
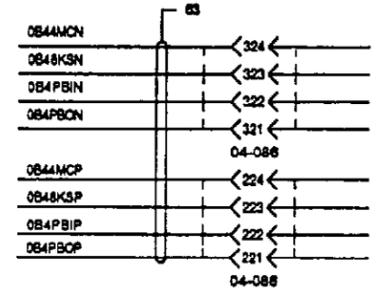
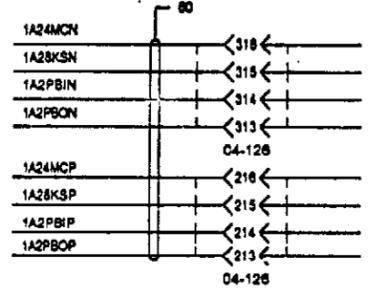
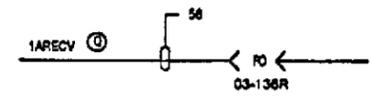
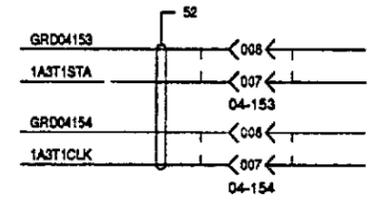
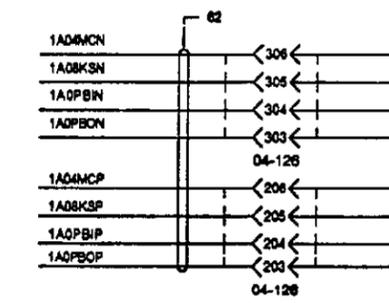
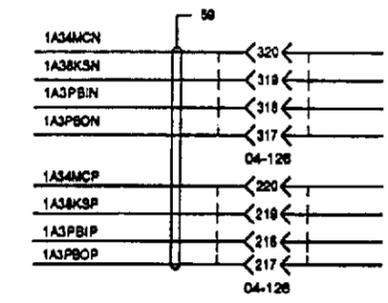
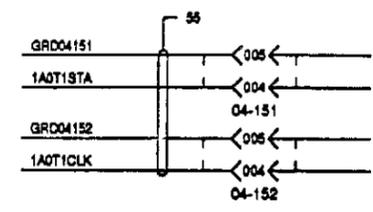
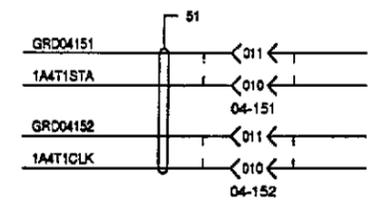
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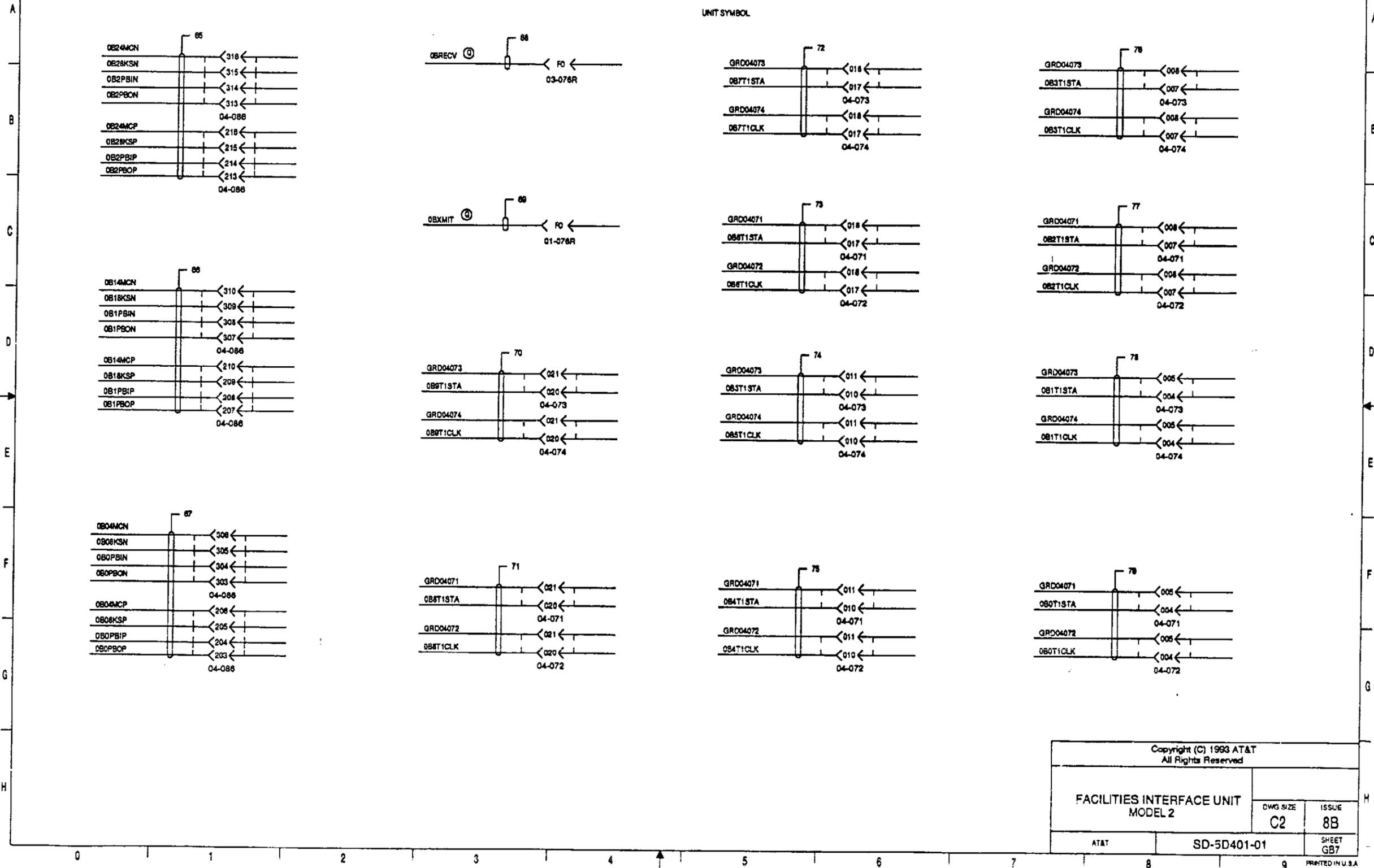
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0 1 2 3 4 5 6 7 8 9

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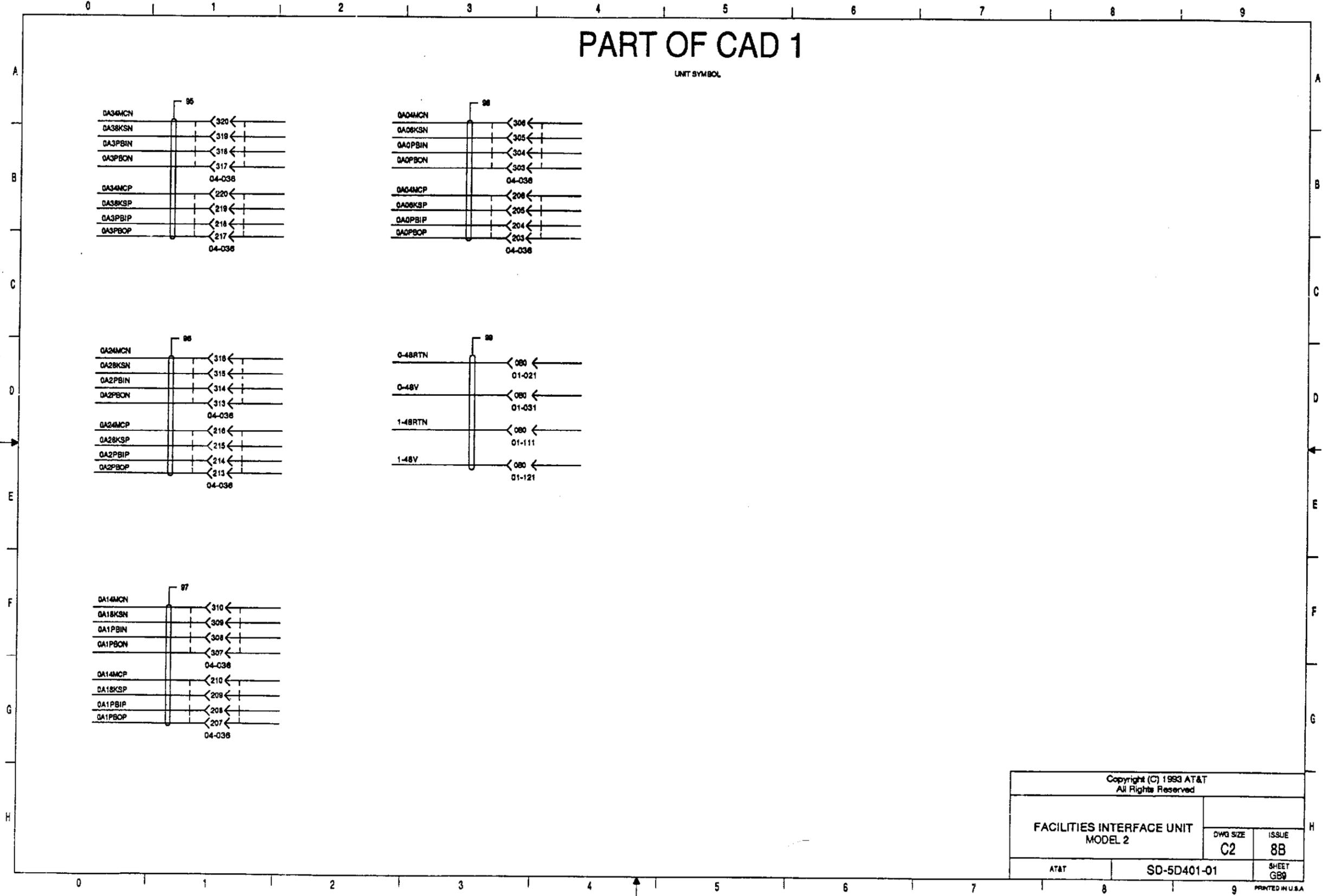
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