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DWG ISS	CD ISS	DWG ISS	CD ISS	DWG ISS	CD ISS
1	1	2M	1	2M	1
4A	1	3A			
5B	1	4B			

SUPPORTING INFORMATION			
SYSTEM USED ON	DESIGN CONTROL	CATEGORY	NO.
SESS	IH	EQUIPMENT DRAWING FRAME 50	JS003AP-03 3D-SD113-01 3D-SD119-01

SHEET INDEX NOTES

- ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
- FOR RE-ISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
- THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

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BT13

SESS[®] SWITCHING EQUIPMENT

FACILITIES INTERFACE UNIT

MODEL 3

CIRCUIT

DWG SIZE	ISSUE
C2	5B

AT&T SD-5D401-02 SHEET A1
28 SHEETS PRINTED IN U.S.A.

DESIGNATION MNEMONICS

MNEMONIC	FS/STM	DEFINITION	MNEMONIC	FS/STM	DEFINITION	MNEMONIC	FS/STM	DEFINITION	MNEMONIC	FS/STM	DEFINITION
GRD04(018-076)	1/2,1/3, 1/4, 1/5, 1/6,1/7, 1/8,1/9, 1/10,1/11, 1/12,1/13, 1/14	SIDE 0 GROUND, EQL'S 04-018 THROUGH 04-076	0(A,B)PWR5	1/4	SIDE 0, GROUP A OR B, RECEIVER +5 VOLT POWER	0(A,B)(0-9)8KSP	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (POS)	0(0,1)NINTIN	1/9	SIDE 0, 0 OR 1 NEGATIVE INTERRUPT (NEG)
GRD04(108-166)	2/2,2/3, 2/4,2/5, 2/6,2/7, 2/8,2/9, 2/10,2/11, 2/12,2/13, 2/14	SIDE 1 GROUND, EQL'S 04-108 THROUGH 04-166	0BSYN2M0	1/4	SIDE 0, SYNC 2 MHZ LOW	(0,1)DLIALM(P)	1/1	SIDE 0 OR 1, DLI ALARM LAMP	0(0,1)NINTIP	1/9	SIDE 0, 0 OR 1 NEGATIVE INTERRUPT (POS)
0+CURPR	1/2	SIDE 0, PLUS CURRENT PROGRAMMING RESISTOR	0(A,B)STM4K	1/3	SIDE 0, GROUP A OR B, SYNC 4 KHZ	(0,1)DLIINT	1/4	SIDE 0 OR 1, DLI INTERRUPT	0(0,1)ODN	1/9	SIDE 0, 0 OR 1 OUT DATA (NEG)
0+12V	1/2	SIDE 0, +12 VOLT POWER	0(A,B)XMIT	1/4	SIDE 0, GROUP A OR B, TRANSMIT TO SWITCH MODULE	(0,1)DLIOGS	1/1	SIDE 0 OR 1, DLI OUT-OF-SERVICE	0(0,1)ODP	1/9	SIDE 0, 0 OR 1 OUT DATA (POS)
0+5V	1/2	SIDE 0, +5 VOLT POWER	0(A,B)XPWR5	1/4	SIDE 0, GROUP A OR B, TRANSMIT +5 VOLT POWER	(0,1)DLIS1	1/1	SIDE 0 OR 1, DLI SHUTDOWN 1	0(0,1)SN	1/9	SIDE 0, 0 OR 1 SYNC (NEG)
0-CURPR	1/2	SIDE 0, MINUS CURRENT PROGRAMMING RESISTOR	0(A,B)(0-9)PBIN	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (NEG)	(0,1)DLIS2	1/1	SIDE 0 OR 1, DLI SHUTDOWN 2	0(0,1)SP	1/9	SIDE 0, 0 OR 1 SYNC (POS)
0-48VTRN	1/2	SIDE 0, -48 VOLT RETURN	0(A,B)(0-9)PBIP	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (POS)	(0,1)DLIS3	1/2	SIDE 0 OR 1, DLI SHUTDOWN 3	1+CURPR	2/2	SIDE 1, PLUS CURRENT PROGRAMMING RESISTOR
0-48V	1/2	SIDE 0, -48 VOLT POWER FEED	0(A,B)(0-9)PBOW	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	(0,1)DLIS3	1/2	SIDE 0 OR 1, DLI SHUTDOWN 3	1+12V	2/2	SIDE 1, +12 VOLT POWER
0(A,B)CK16M	1/3	SIDE 0, GROUP A OR B, 16 MHZ CLOCK	0(A,B)(0-9)PBOW	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	(0,1)DOOS48	1/1	SIDE 0 OR 1, DLI OUT-OF-SERVICE (-48V)	1+5V	2/2	SIDE 1, +5 VOLT POWER
0BCK32	1/4	SIDE 0, 32 MHZ CLOCK	0(A,B)(0-9)PBOP	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	(0,1)FREERUN	1/4	SIDE 0 OR 1, SELECT FREE	1-CURPR	2/2	SIDE 1, MINUS CURRENT PROGRAMMING RESISTOR
0(A,B)CK8MC	1/3	SIDE 0, GROUP A OR B, CLOCK 8 MHZ	0(A,B)ORP	1/3	SIDE 0, A OR B GROUP, RECEIVE PARITY	(0,1)MATEEN	1/4	SIDE 0 OR 1, MATE ENABLE	1-48VTRN	2/2	SIDE 1, -48 VOLT RETURN
(A,B)COND5	1/4	SIDE 0, GROUP A OR B, LINK CONDITIONED POWER	0(A,B)ORX	1/3	SIDE 0, A OR B GROUP, RECEIVE DATA X	(0,1)MCK4M0	1/4	SIDE 0, MATE CLOCK 4 MHZ, ACTIVE LOW	1-48V	2/2	SIDE 1, -48 VOLT POWER FEED
0(A,B)INT	1/1	SIDE 0, GROUP A OR B INTERRUPT	0(A,B)ORY	1/3	SIDE 0, A OR B GROUP, RECEIVE DATA Y	(0,1)CK8MH	1/4	SIDE 0, MATE CLOCK 8MHZ	1(A,B)CK16M	2/3	SIDE 1, GROUP A OR B, 16 MHZ CLOCK
0(A,B)LOOP	1/4	SIDE 0, GROUP A OR B, LOOP LINK	0(A,B)ORZ	1/3	SIDE 0, A OR B GROUP, RECEIVE DATA Z	(0,1)MPCK	1/4	SIDE 0 OR 1, MATE CONTROL INTERFACE CLOCK	1BCK32	2/4	SIDE 1, 32MHZ CLOCK
0(A,B)MUXCR	1/3	SIDE 0, GROUP A OR B, MUX CONTROL REGISTER ENABLE	0(A,B)OR2	1/3	SIDE 0, A OR B GROUP, RECEIVE DATA 2	(0,1)MPDATA	1/4	SIDE 0 OR 1, MATE CONTROL DATA IN	1(A,B)CK8MC	2/3	SIDE 1, GROUP A OR B, CLOCK 8 MHZ
0(A,B)MUXDI	1/3	SIDE 0, GROUP A OR B, MUX DATA IN	0(A,B)OTP	1/4	SIDE 0, GROUP, TRANSMIT PARITY	(0,1)MPGO	1/4	SIDE 0 OR 1, MATE CONTROL INTERFACE COMMAND ENABLE	1(A,B)INT	2/1	SIDE 1, GROUP A OR B INTERRUPT
0(A,B)MUXDO	1/3	SIDE 0, GROUP A OR B, MUX DATA OUT	0(A,B)OTX	1/4	SIDE 0, GROUP, TRANSMIT DATA X	(0,1)MPOUT	1/4	SIDE 0 OR 1, MATE CONTROL DATA OUT	1(A,B)LOOP	2/4	SIDE 1, GROUP A OR B, LOOP LINK
0(A,B)MUXER	1/3	SIDE 0, GROUP A OR B, MUX ERROR REGISTER ENABLE	0(A,B)OTY	1/3	SIDE 0, A OR B GROUP, TRANSMIT DATA Y	(0,1)MPDI	1/4	SIDE 0 OR 1, MATE CONTROL DATA IN	0(A,B)MUXCR	1/3	SIDE 0, GROUP A OR B, MUX CONTROL REGISTER ENABLE
0(A,B)MUXINT	1/3	SIDE 0, GROUP A OR B, MUX INTERRUPT	0(A,B)OTZ	1/3	SIDE 0, TRANSMIT DATA Z	(0,1)RA(0-7)	1/4	SIDE 0 OR 1, RECEIVE ADDRESS BITS 0 THROUGH 7	0(A,B)MUXDI	1/3	SIDE 0, GROUP A OR B, MUX DATA IN
0(A,B)MUXRD	1/3	SIDE 0, GROUP A OR B, MUX READ	0(A,B)(0-9)T1CLK	1/6	SIDE 0, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 CLOCK	(0,1)OBSYN6M8	1/4	SIDE 0 OR 1, SELECT SYNC 6 MS	0(A,B)MUXDO	1/3	SIDE 0, GROUP A OR B, MUX DATA OUT
0(A,B)MUXSH	1/3	SIDE 0, GROUP A OR B, MUX SHIFT CLOCK	0(A,B)(0-9)T1STA	1/5	SIDE 0, GROUP A OR B PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	04KOUT	1/9	SIDE 0 4K OUTPUT	0(A,B)MUXDI	1/3	SIDE 0, GROUP A OR B, MUX DATA IN
0(A,B)MUXWR	1/3	SIDE 0, GROUP A OR B, MUX WRITE	0(A,B)(0-9)4MCH	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (NEG)	08KIN0	1/9	SIDE 0, 8K INPUT FOR CIRCUIT 0	0(A,B)MUXDO	1/3	SIDE 0, GROUP A OR B, MUX DATA OUT
0(A,B)R-48	1/4	SIDE 0, GROUP A OR B, RECEIVE -48 VOLT POWER	0(A,B)(0-9)4MCP	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (POS)	08KIN1	1/9	SIDE 0, 8K INPUT FOR CIRCUIT 1	0(A,B)MUXER	1/3	SIDE 0, GROUP A OR B, MUX ERROR REGISTER ENABLE
0(A,B)RECV	1/4	SIDE 0, GROUP A OR B, RECEIVE FROM SWITCHING MODULE	0(A,B)(0-9)8KSN	1/3	SIDE 0, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (NEG)	08KREF	1/4	SIDE 0, 8K REFERENCE	0(A,B)MUXINT	1/3	SIDE 0, GROUP A OR B, MUX INTERRUPT
						08KRTN0	1/9	SIDE 0, 8K RETURN FOR CIRCUIT 0	0(A,B)MUXRD	1/3	SIDE 0, GROUP A OR B, MUX READ
						08KRTN1	1/9	SIDE 0, 8K RETURN FOR CIRCUIT 1	0(A,B)MUXSH	1/3	SIDE 0, GROUP A OR B, MUX SHIFT CLOCK
						0(0,1)CN	1/9	SIDE 0, 0 OR 1 CLOCK (NEG)	0(A,B)MUXWR	1/3	SIDE 0, GROUP A OR B, MUX WRITE
						0(0,1)CP	1/9	SIDE 0, 0 OR 1 CLOCK (POS)	0(A,B)R-48	1/4	SIDE 0, GROUP A OR B, RECEIVE -48 VOLT POWER
						0(0,1)IDN	1/9	SIDE 0, 0 OR 1 IN DATA (NEG)	0(A,B)RECV	1/4	SIDE 0, GROUP A OR B, RECEIVE FROM SWITCHING MODULE
						0(0,1)IDP	1/9	SIDE 0, 0 OR 1 IN DATA (POS)			

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FACILITIES INTERFACE UNIT MODEL 3		DWG SIZE C2
AT&T		ISSUE 5B
SD-5D401-02		SHEET A2

DESIGNATION MNEMONICS

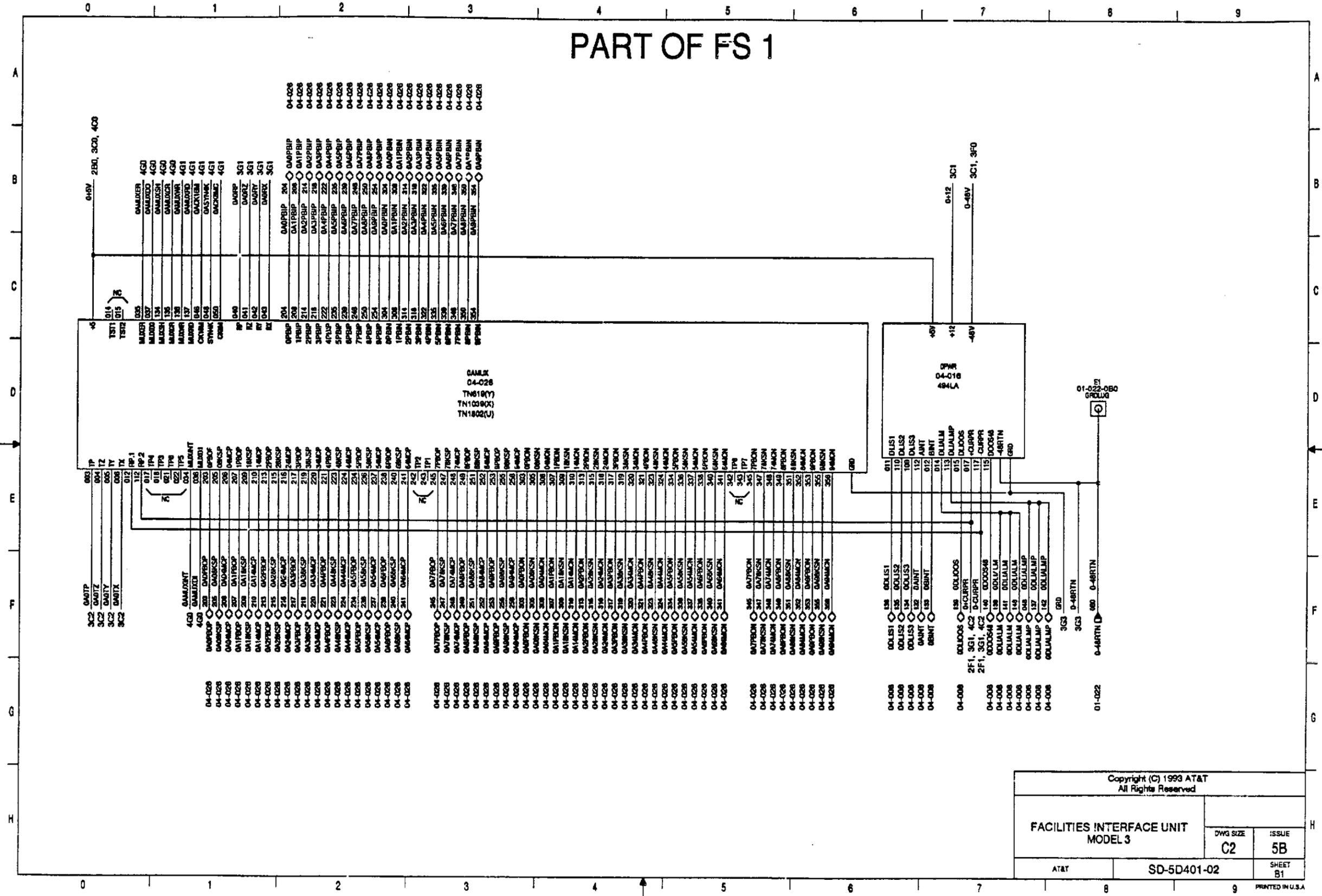
Mnemonic	FS/STM	DEFINITION	Mnemonic	FS/STM	DEFINITION
1(A,B)R-48	2/4	SIDE 1, GROUP A OR B RECEIVER -48 VOLT POWER	1(A,B)(0-9)BESP	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (POS)
1(A,B)RECV	2/4	SIDE 1, GROUP A OR B RECEIVE FROM SWITCHING MODULE.	1(A,B)CONDS	2/4	SIDE 1, CONDITIONED +5 VOLTS
1(A,B)RPWR5	2/4	SIDE 1, GROUP A OR B RECEIVER +5 VOLT POWER	1(A,B)XMIT	2/4	SIDE 1, GROUP A OR B, TRANSMIT TO INTERFACE MODULE
1BSYN2M0	2/4	SIDE 1, SYNC 2 MHZ, ACTIVE LOW	1(A,B)XPWR5	2/4	SIDE 1, GROUP A OR B TRANSMIT +5 VOLT POWER
1(A,B)SYN4K	2/3	SIDE 1, GROUP A OR B, SYNC 4 KHZ	1(0,1)CN	2/9	SIDE 1, 0 OR 1 CLOCK (NEG)
1(A,B)(0-9)PBIN	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (NEG)	1(0,1)CP	2/9	SIDE 1, 0 OR 1 CLOCK (POS)
1(A,B)(0-9)PBIP	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA IN (POS)	1(0,1)IDN	2/9	SIDE 1, 0 OR 1 IN DATA (NEG)
1(A,B)(0-9)PBOM	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (NEG)	1(0,1>IDP	2/9	SIDE 1, 0 OR 1 IN DATA (POS)
1(A,B)(0-9)PBOP	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, DATA OUT (POS)	1(0,1)NINTIN	2/9	SIDE 1, 0 OR 1 NEGATIVE INTERRUPT (NEG)
1(A,B)ORP	2/3	SIDE 1, A OR B GROUP, RECEIVE PARITY	1(0,1)NINTIP	2/9	SIDE 1, 0 OR 1 NEGATIVE INTERRUPT (POS)
1(A,B)ORX	2/3	SIDE 1, A OR B GROUP, RECEIVE DATA X	1(0,1)ODN	2/9	SIDE 1, 0 OR 1 OUT DATA (NEG)
1(A,B)ORY	2/3	SIDE 1, A OR B GROUP, RECEIVE DATA Y	1(0,1)ODP	2/9	SIDE 1, 0 OR 1 OUT DATA (POS)
1(A,B)ORZ	2/3	SIDE 1, A OR B GROUP, RECEIVE DATA Z	1(0,1)SR	2/9	SIDE 1, 0 OR 1 SYNC (NEG)
1(A,B)OTP	2/3	SIDE 1, A OR B GROUP, TRANSMIT PARITY	1(0,1)SP	2/9	SIDE 1, 0 OR 1 SYNC (POS)
1(A,B)OTX	2/3	SIDE 1, A OR B GROUP, TRANSMIT DATA X	14KOUT	1/9	SIDE 1, 4K OUTPUT
1(A,B)OTY	2/3	SIDE 1, A OR B GROUP, TRANSMIT DATA Y	18KINO	2/9	SIDE 1, 8K INPUT FOR CIRCUIT 0
1(A,B)OTZ	2/3	SIDE 1, A OR B GROUP, TRANSMIT DATA Z	18KINI	2/9	SIDE 1, 8K INPUT FOR CIRCUIT 0
1(A,B)(0-9)TICLE	2/6	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 CLOCK	18KREF	2/9	SIDE 1, 8K REFERENCE
1(A,B)(0-9)TISTA	2/5	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, T1 STATUS	18KRTN0	2/9	SIDE 1, 8K RETURN FOR CIRCUIT 0
1(A,B)(0-9)4MCH	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (NEG)	18KRTN1	2/9	SIDE 1, 8K RETURN FOR CIRCUIT 1
1(A,B)(0-9)4MCP	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 4 MHZ CLOCK (POS)			
1(A,B)(0-9)8KSN	2/3	SIDE 1, GROUP A OR B, PERIPHERAL INTERFACE DATA BUS 0 THROUGH 9, 2 KHZ CLOCK (NEG)			

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FACILITIES INTERFACE UNIT MODEL 3		DWG SIZE C2
		ISSUE 5B
AT&T	SD-5D401-02	SHEET A3

APPARATUS INDEX					LEAD INDEX
CODE	EQUIP LOC	SHEET LOC	APP FIG.	OPTION	SEE CAD 1
TN618D	04-056	B4E3	2		
TN618D	04-146	B6E3	2		
TN618	04-026	B1D3	2		
TN618	04-076	B2D3	2		33
TN618	04-116	B6D3	2		33
TN618	04-166	B7D3	2		33
TN1039	04-026	B1D3	2		33
TN1039	04-076	B2D3	2		33
TN1039	04-116	B6D3	2		33
TN1039	04-166	B7D3	2		33
TN1510	04-036	B3E2	2		
TN1510	04-126	B6E2	2		
494LA	04-016	B1D7	2		
494LA	04-106	B8D7	2		
982CF	03-036R	B366	3		33
982CF	05-036R	B366	3		33
982CF	03-126R	B666	3		33
982CF	05-126R	B666	3		33
982CG	01-036R	B365	3		33
982CG	07-036R	B365	3		33
982CG	01-126R	B665	3		33
982CG	07-126R	B665	3		33
982TR	06-036R	B367	3		33
982TR	06-126R	B667	3		33
982TS	02-036R	B367	3		33
982TS	02-126R	B667	3		33
TN1802	04-026	B1D3	2		33
TN1802	04-076	B2D3	2		33
TN1802	04-116	B6D3	2		33
TN1802	04-166	B7D3	2		33
982TRC	06-036R	B337	3		33
982TRC	06-126R	B667	3		33
982TSC	02-036R	B367	3		33
982TSC	02-126R	B667	3		33

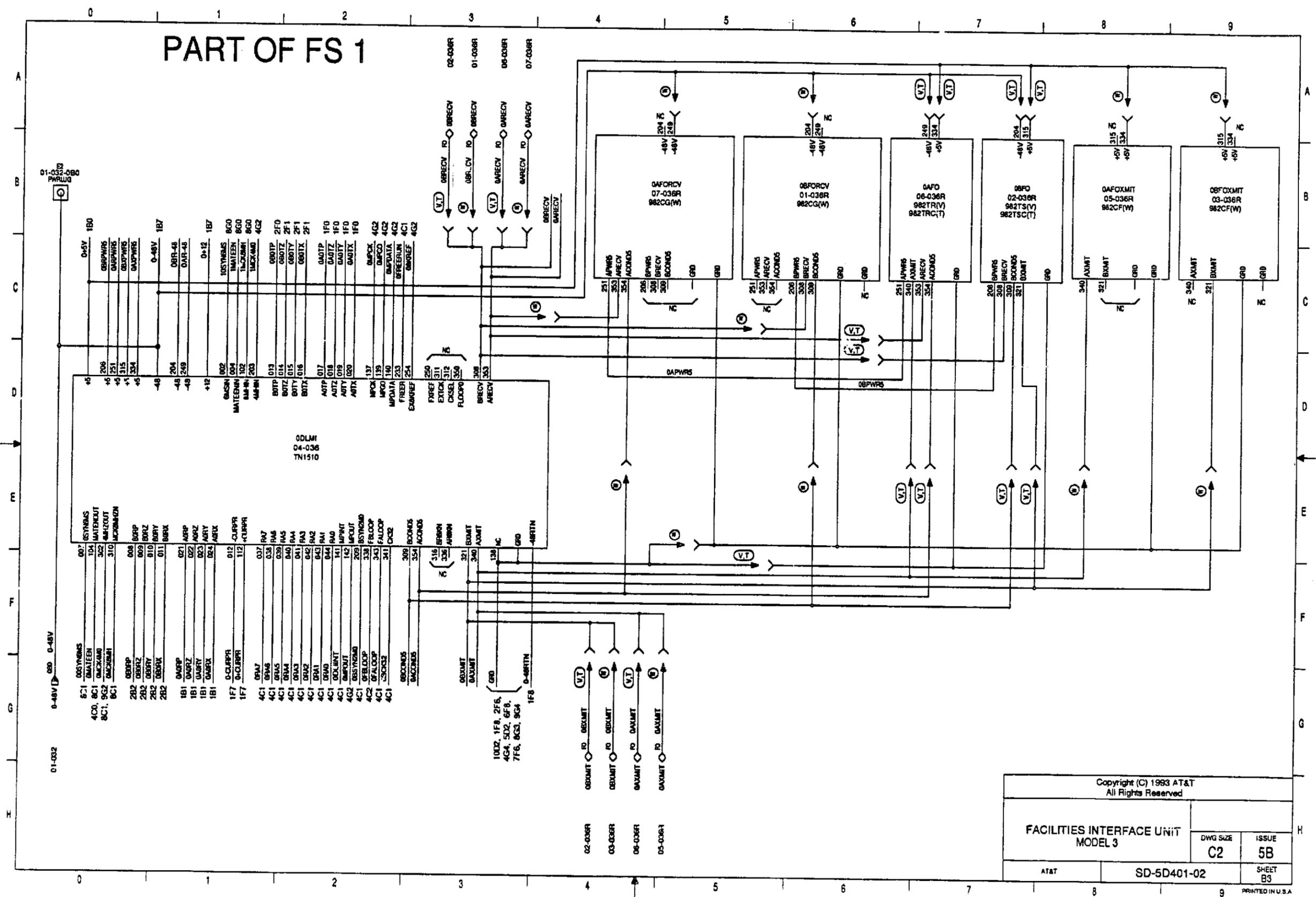
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FACILITIES INTERFACE UNIT MODEL 3		ISSUE 5B
AT&T	SD-5D401-02	SHEET A4

PART OF FS 1



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FACILITIES INTERFACE UNIT MODEL 3		DWG SIZE
		ISSUE
AT&T	SD-5D401-02	SHEET B1

PART OF FS 1



01-032-080
PWRWUB

01-032
0-48V

01-032
0-48V

01-032
0-48V

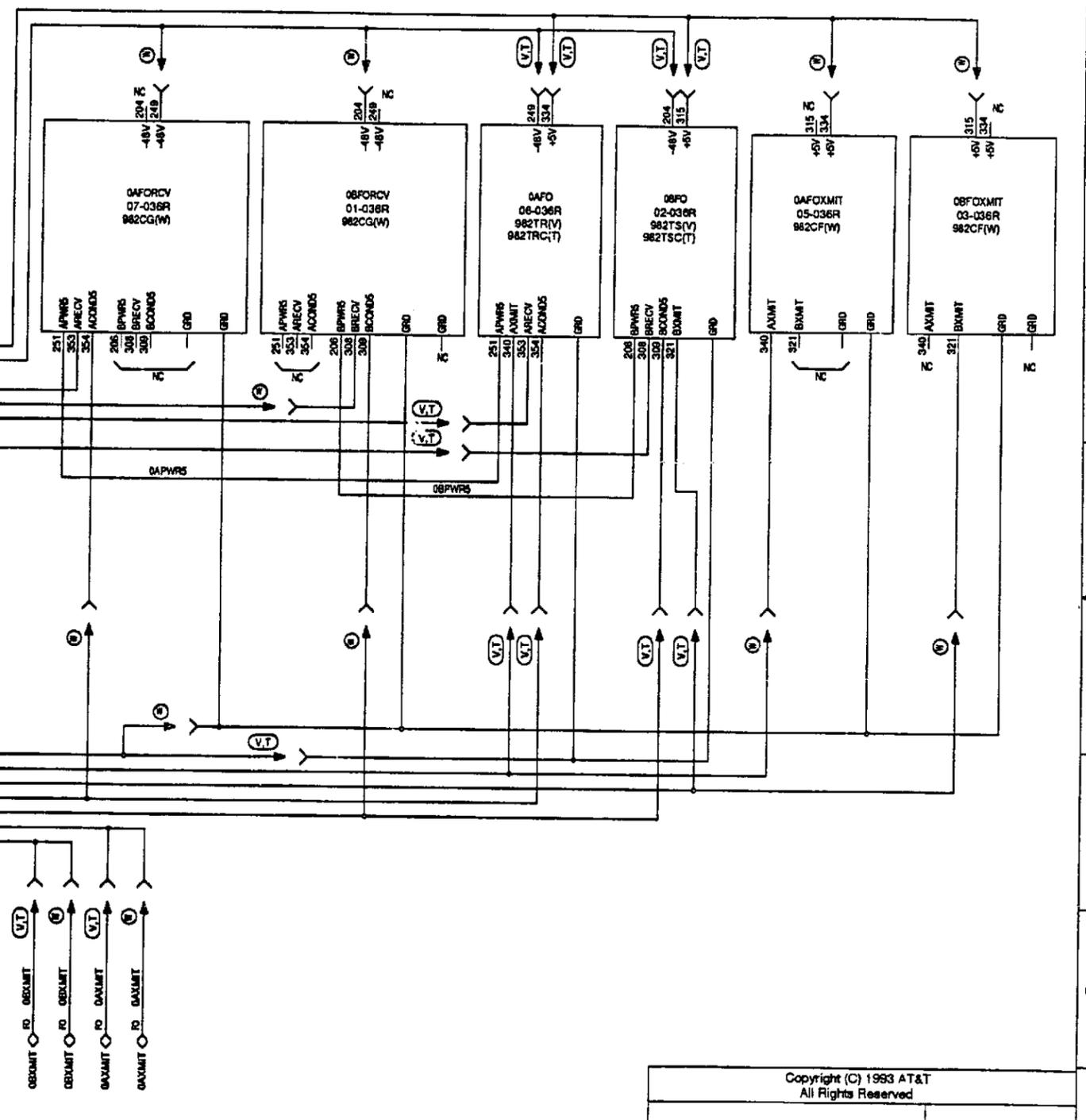
01-032
0-48V

- 045V 180
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- 08PWRS
- 08PWRS
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- 0-48V 187
- 08R-48
- 08R-48
- 0-12 187
- 10SYNMS 8G0
- 1MATEEN 8G0
- 1MATEEN 8G0
- 1MCKAM 8G0
- 1MCKAM 4G2
- 013
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- 007 10SYNMS
- 104 MATEEN
- 322 MCKAM
- 310 MCKAM
- 008 80RP
- 009 80RZ
- 010 80RY
- 011 80RX
- 021 80RP
- 022 80RZ
- 023 80RY
- 024 80RX
- 012 80RPP
- 112 80RPP
- 037 80Z
- 038 80B
- 039 80S
- 040 80A
- 041 80A3
- 042 80A2
- 043 80A1
- 044 80A0
- 141 80PHT
- 142 80PHT
- 209 80SYNMS
- 338 80FLOOP
- 343 80FLOOP
- 341 80CK3
- 309 80CONUS
- 354 80CONUS
- 316 80BRN
- 322 80BRN
- 321 80AMT
- 340 80AMT
- 138 80C
- GRD
- 80RTN

- 007 10SYNMS
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- 322 MCKAM
- 310 MCKAM
- 008 80RP
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- 037 80Z
- 038 80B
- 039 80S
- 040 80A
- 041 80A3
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- 341 80CK3
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- GRD
- 80RTN



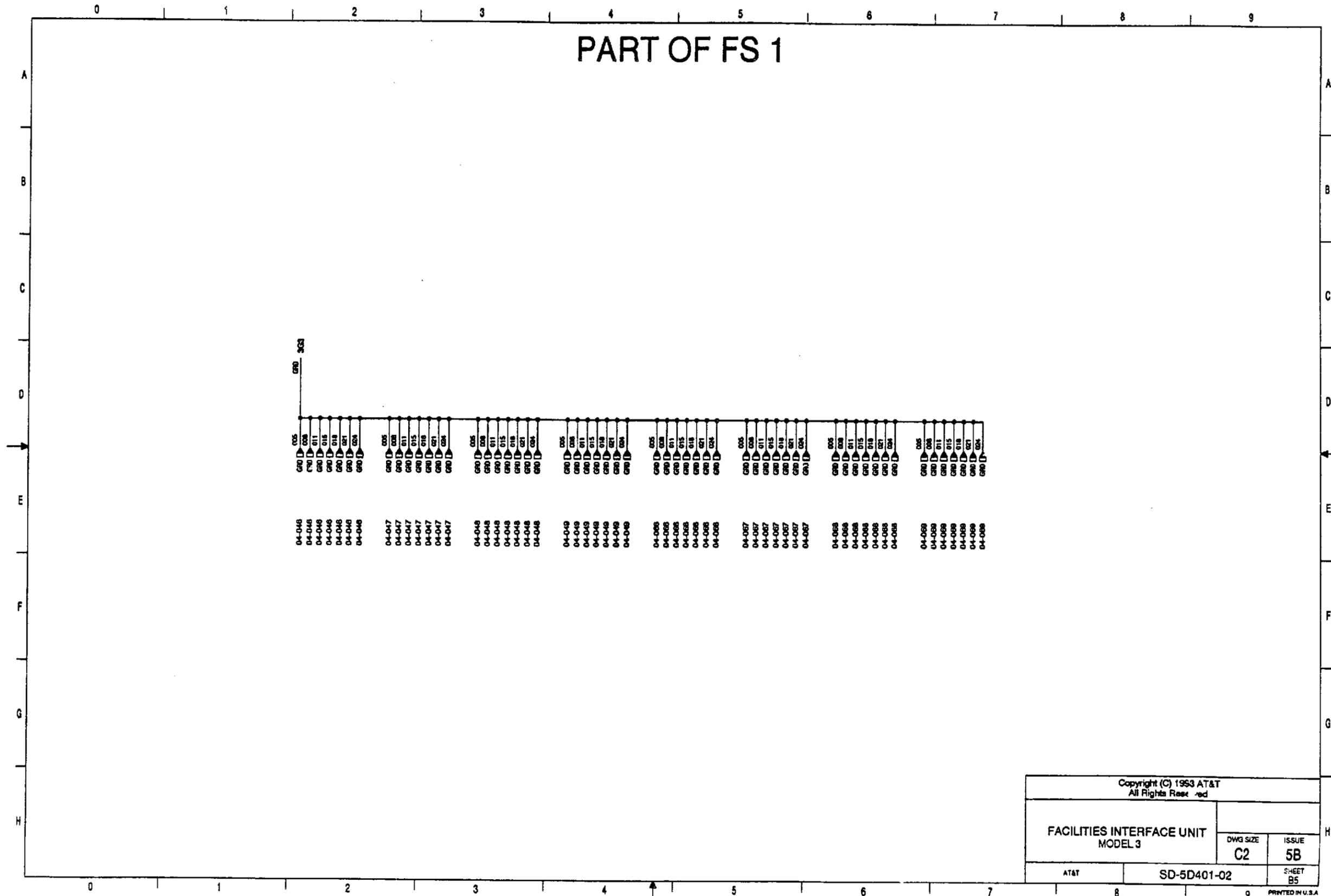
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FACILITIES INTERFACE UNIT
MODEL 3

DWG SIZE C2	ISSUE 5B
SHEET B3	

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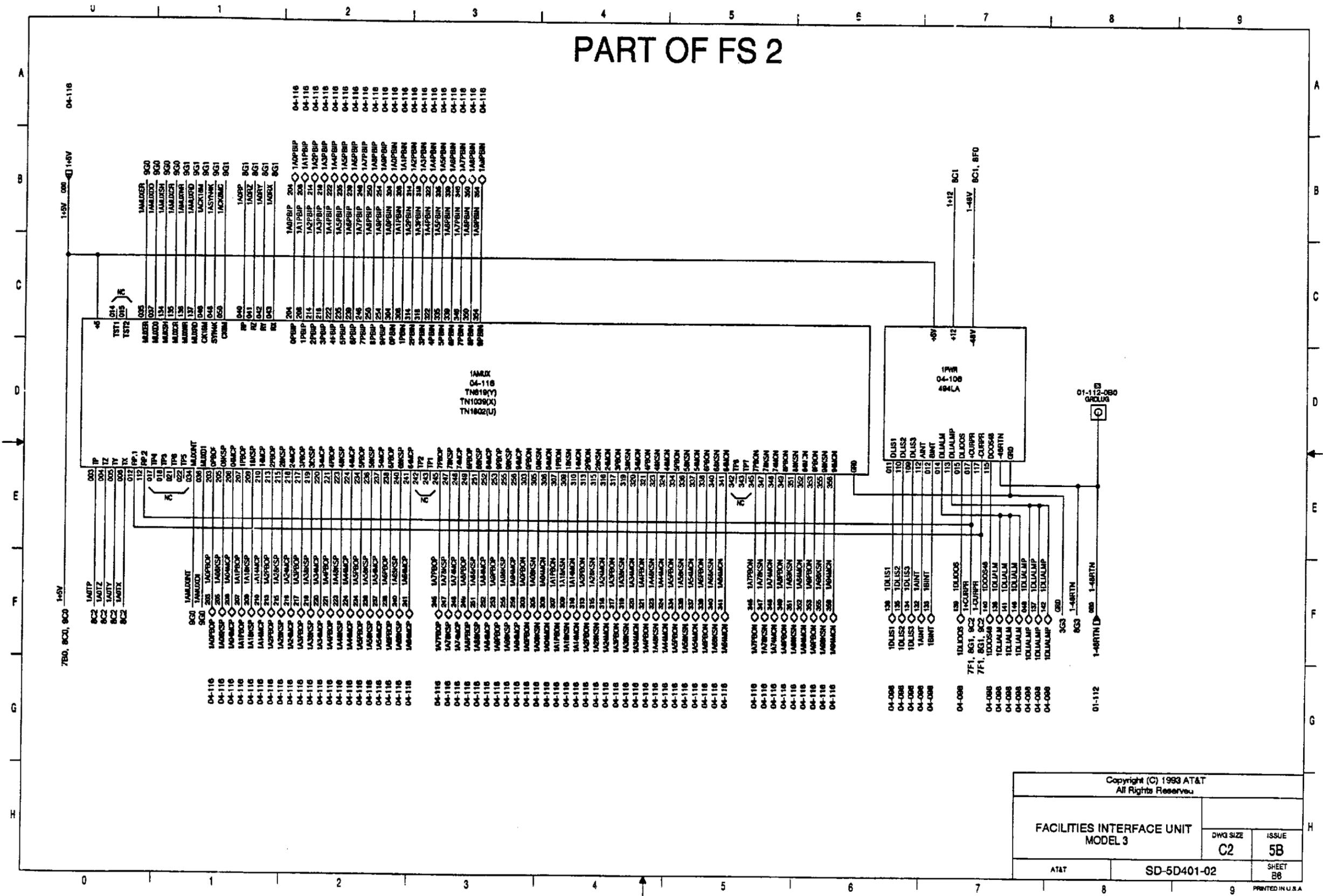
PART OF FS 1



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FACILITIES INTERFACE UNIT MODEL 3		DWG SIZE C2
AT&T		ISSUE 5B
SD-5D401-02		SHEET B5

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PART OF FS 2

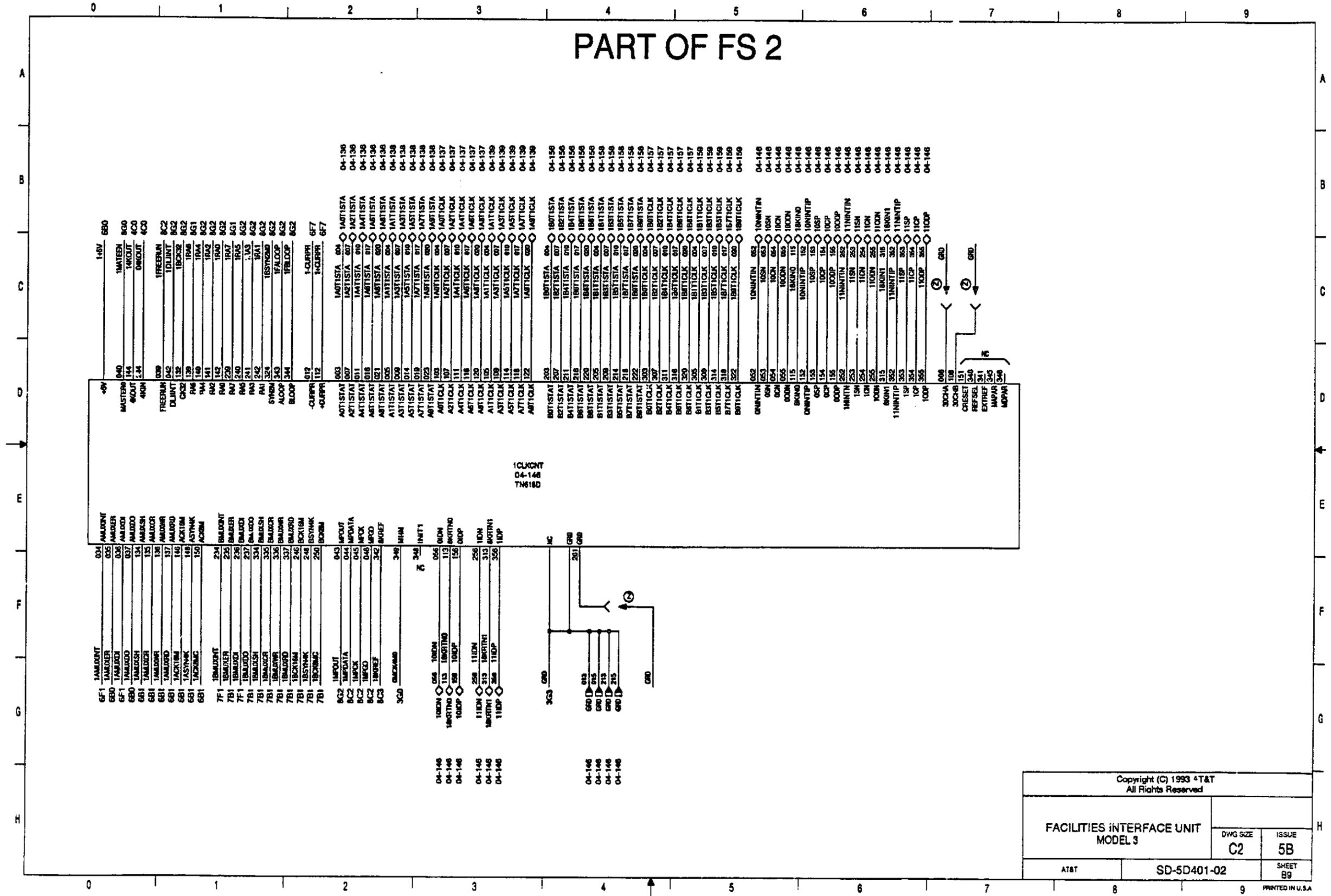


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FACILITIES INTERFACE UNIT MODEL 3		DWG SIZE C2	ISSUE 5B
AT&T	SD-5D401-02		SHEET 88

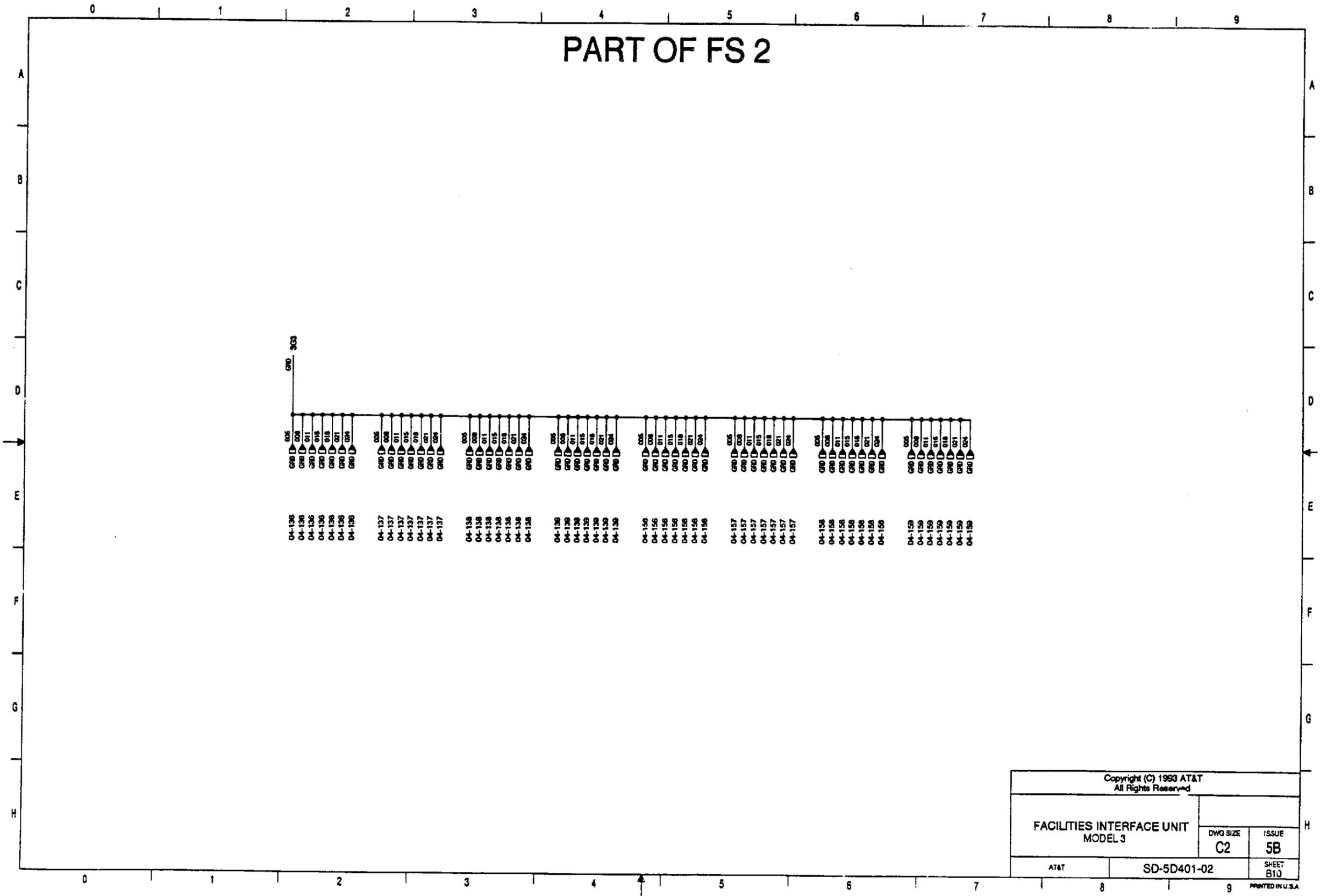
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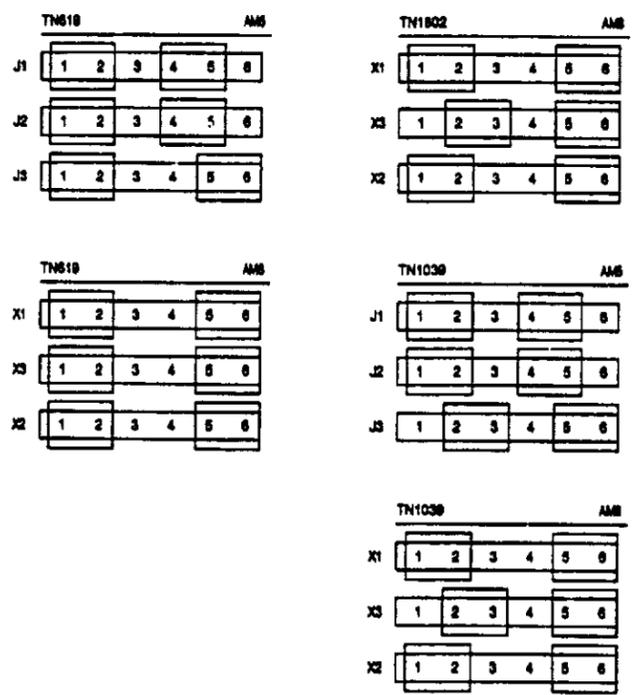
A
B
C
D
E
F
G
H

CIRCUIT NOTES:

101.

DESK	FUSE AMP	POTENTIAL	ONE PER
BATTERY SYMBOL		VOLTAGE RANGE	

102. THE FOLLOWING DIAGRAM PROVIDES PROGRAMMING PLUG POSITION INFORMATION:



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0 1 2 3 4 5 6 7 8 9

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EQUIPMENT NOTES:

201. UNLESS OTHERWISE SPECIFIED, ALL BACKPLANE WIRING WILL BE AUTOMATIC MACHINE WIRING (A-D4) 30 GAUGE, WHICH HAS BEEN PROCESSED BY THE WESWRAP PROGRAMS.

202. ALL PRINTED WIRING CONNECTIONS ARE SPECIFIED BY ED-SD823-30.

203.

APPARATUS CODE	CIRCUIT PACK REMOVAL PROCEDURES		
	PULL HOT	REMOVE UNIT POWER	SEQUENCED

204. CONNECT FRAME GROUND TO BACKPLANE BOARD.

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5B

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INFORMATION NOTES:

301. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS,
CAPACITANCE VALUES ARE IN MICROFARADS,
VALUES PRECEDED BY THE SYMBOL + (PLUS)
OR - (MINUS) ARE IN VOLTS.

FEATURE OR OPTION	PROVIDE		QUANTITY
	APP FIG	QTY	
BACKPLANE & WIRING	24 CHANNEL	1	
	30 CHANNEL	Z	
MINIMUM EQUIPAGE FOR FACILITIES INTERFACE			
LINK INTERFACE			
CLOCK CONTROLLER WITH OR WITHOUT RCU			
POWER			
MULTIPLEXER (SEE NOTE 305 & 306)		2	
24 CHANNEL (TN1802)		U	
24 CHANNEL (TN619)		Y	
30 CHANNEL (TN1038)		X	
NOT LINK FIBER OPTIC CONNECTORS	ODL40 TYPE (4) 982CF (4) 982CG	W	2 PER SIDE
	ODL50 TYPE (2) 982TR (2) 982TS	3	Y 1 PER SIDE
	LDT TYPE (2) 982TRC (2) 982TSC (SEE NOTE 307)	T	1 PER SIDE

INFORMATION NOTES: (CONT)

RECORD OF FIGURES, WIRING AND APPARATUS CHANGES					
CHANGED ON ISS	IF JOB RECORDS DO NOT SPECIFY	THIS OPTION WAS FURN	SEE NOTE	USE IN CIRCUIT	
				AVAIL	DR
24	S,W,V	S,W		S,W,V	
4A	U,X,Y	X,Y		U,X,Y	
5B	T			T	

CIRCUIT PACK CODE OR MICROCODE	COMMON LANGUAGE EQUIPMENT IDENTIFICATION CODE (CLE)
TN6180	ESQ17XAXX
TN619	ESQ21CAXX
TN1038	ESQAAKAXX
TN1510	ESQ7NAAXX
484A	PWQ84EAXX
TN1802	ESQ8B7AAX

305. OPTION Y (TN619) IS FOR FEATURES IN 5E2(2) OR LATER OFFICES. OPTION X (TN1038) IS FOR FEATURES IN 5E3(2) OR LATER OFFICES.

306. OPTIONS Y AND X TO BE USED WHEN FIU INTERFACES WITH A DLTU. OPTION U TO BE USED WHEN FIU 2 OR 3 INTERFACES WITH A DLTU 2.

307. THE 982TRC AND 982TSC LDT PRODUCT MEET THE INTERNATIONAL CIS PER 22 EMC REQUIREMENTS.

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FACILITY INTERFACE UNIT
MODEL 3

DWG SIZE
C2

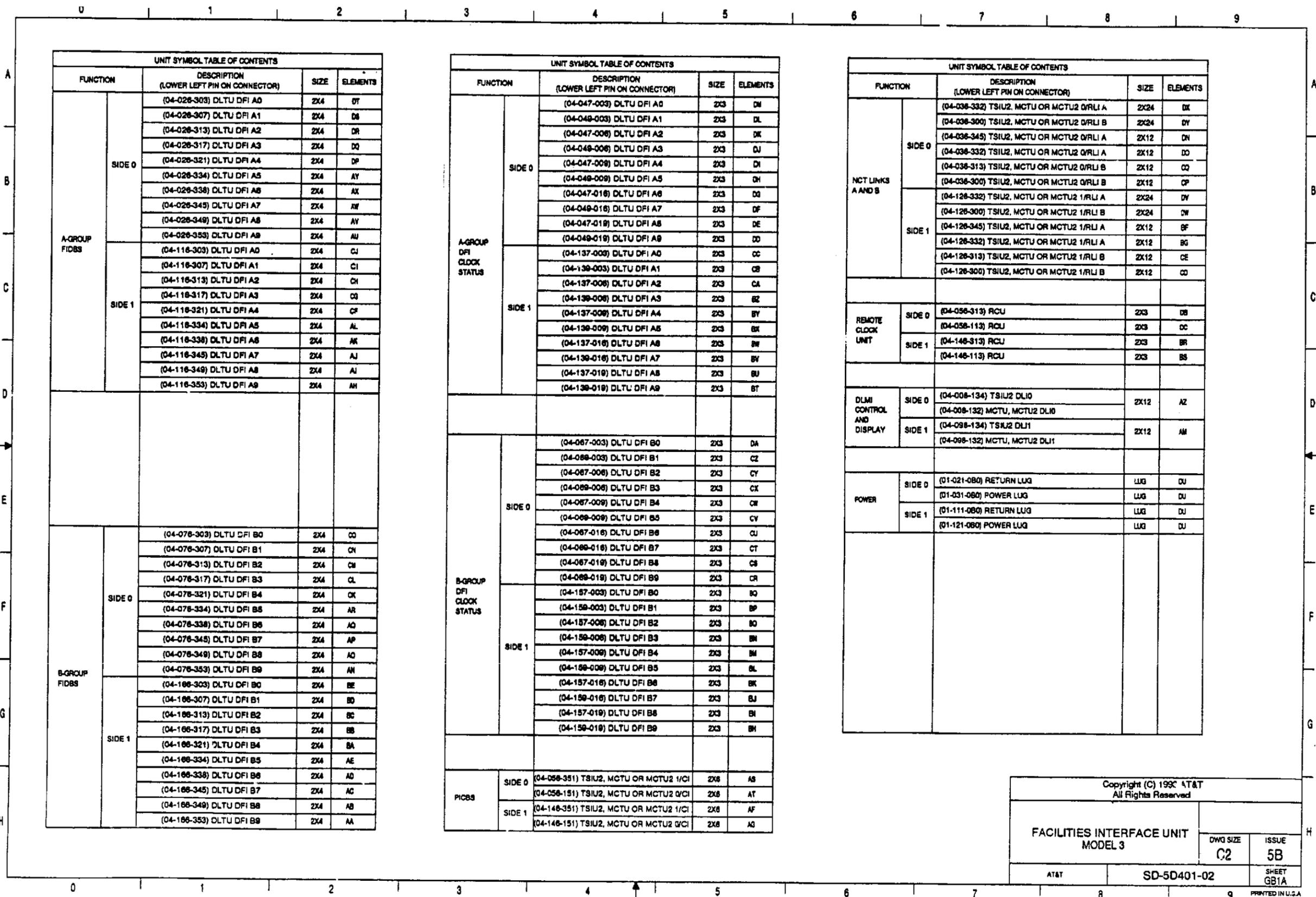
ISSUE
5B

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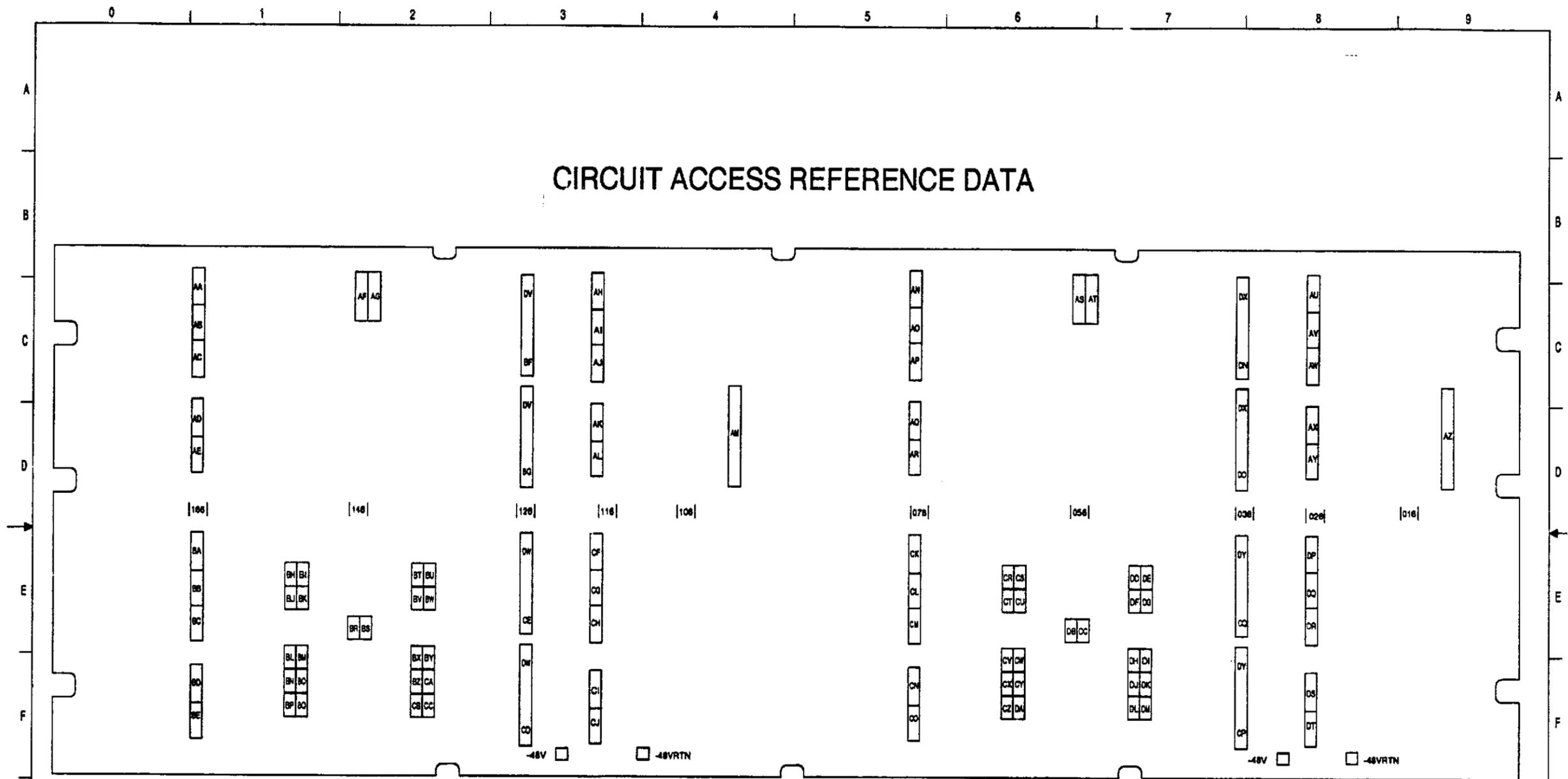
UNIT SYMBOL TABLE OF CONTENTS				
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS	
A-GROUP FIDBS	SIDE 0	(04-026-303) DLTU DFI A0	2X4	DT
		(04-026-307) DLTU DFI A1	2X4	DS
		(04-026-313) DLTU DFI A2	2X4	DR
		(04-026-317) DLTU DFI A3	2X4	DQ
		(04-026-321) DLTU DFI A4	2X4	DP
		(04-026-334) DLTU DFI A5	2X4	AY
		(04-026-338) DLTU DFI A6	2X4	AX
		(04-026-345) DLTU DFI A7	2X4	AW
		(04-026-349) DLTU DFI A8	2X4	AV
		(04-026-353) DLTU DFI A9	2X4	AU
	SIDE 1	(04-116-303) DLTU DFI A0	2X4	CJ
		(04-116-307) DLTU DFI A1	2X4	CI
		(04-116-313) DLTU DFI A2	2X4	CH
		(04-116-317) DLTU DFI A3	2X4	CG
		(04-116-321) DLTU DFI A4	2X4	CF
		(04-116-334) DLTU DFI A5	2X4	AL
		(04-116-338) DLTU DFI A6	2X4	AK
		(04-116-345) DLTU DFI A7	2X4	AJ
		(04-116-349) DLTU DFI A8	2X4	AI
		(04-116-353) DLTU DFI A9	2X4	AH
B-GROUP FIDBS	SIDE 0	(04-076-303) DLTU DFI B0	2X4	CO
		(04-076-307) DLTU DFI B1	2X4	CH
		(04-076-313) DLTU DFI B2	2X4	CM
		(04-076-317) DLTU DFI B3	2X4	CL
		(04-076-321) DLTU DFI B4	2X4	CK
		(04-076-334) DLTU DFI B5	2X4	AR
		(04-076-338) DLTU DFI B6	2X4	AQ
		(04-076-345) DLTU DFI B7	2X4	AP
		(04-076-349) DLTU DFI B8	2X4	AO
		(04-076-353) DLTU DFI B9	2X4	AM
	SIDE 1	(04-166-303) DLTU DFI B0	2X4	BE
		(04-166-307) DLTU DFI B1	2X4	BO
		(04-166-313) DLTU DFI B2	2X4	BC
		(04-166-317) DLTU DFI B3	2X4	BB
		(04-166-321) DLTU DFI B4	2X4	BA
		(04-166-334) DLTU DFI B5	2X4	AE
		(04-166-338) DLTU DFI B6	2X4	AD
		(04-166-345) DLTU DFI B7	2X4	AC
		(04-166-349) DLTU DFI B8	2X4	AB
		(04-166-353) DLTU DFI B9	2X4	AA

UNIT SYMBOL TABLE OF CONTENTS				
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS	
A-GROUP DFI CLOCK STATUS	SIDE 0	(04-047-003) DLTU DFI A0	2X3	DM
		(04-048-003) DLTU DFI A1	2X3	DL
		(04-047-008) DLTU DFI A2	2X3	DK
		(04-048-008) DLTU DFI A3	2X3	DJ
		(04-047-008) DLTU DFI A4	2X3	DI
		(04-048-009) DLTU DFI A5	2X3	DH
		(04-047-018) DLTU DFI A6	2X3	DG
		(04-048-018) DLTU DFI A7	2X3	DF
		(04-047-018) DLTU DFI A8	2X3	DE
		(04-048-019) DLTU DFI A9	2X3	DD
	SIDE 1	(04-137-003) DLTU DFI A0	2X3	CC
		(04-138-003) DLTU DFI A1	2X3	CB
		(04-137-008) DLTU DFI A2	2X3	CA
		(04-138-008) DLTU DFI A3	2X3	BA
		(04-137-008) DLTU DFI A4	2X3	BY
		(04-138-009) DLTU DFI A5	2X3	BX
		(04-137-018) DLTU DFI A6	2X3	BW
		(04-138-018) DLTU DFI A7	2X3	BV
		(04-137-018) DLTU DFI A8	2X3	BU
		(04-138-019) DLTU DFI A9	2X3	BT
B-GROUP DFI CLOCK STATUS	SIDE 0	(04-067-003) DLTU DFI B0	2X3	DA
		(04-068-003) DLTU DFI B1	2X3	CZ
		(04-067-008) DLTU DFI B2	2X3	CY
		(04-068-008) DLTU DFI B3	2X3	CX
		(04-067-009) DLTU DFI B4	2X3	CE
		(04-068-009) DLTU DFI B5	2X3	CV
		(04-067-018) DLTU DFI B6	2X3	CU
		(04-068-018) DLTU DFI B7	2X3	CT
		(04-067-018) DLTU DFI B8	2X3	CS
		(04-068-019) DLTU DFI B9	2X3	CR
	SIDE 1	(04-157-003) DLTU DFI B0	2X3	BO
		(04-158-003) DLTU DFI B1	2X3	BP
		(04-157-008) DLTU DFI B2	2X3	BO
		(04-158-008) DLTU DFI B3	2X3	BN
		(04-157-008) DLTU DFI B4	2X3	BM
		(04-158-009) DLTU DFI B5	2X3	BL
		(04-157-018) DLTU DFI B6	2X3	BK
		(04-158-018) DLTU DFI B7	2X3	BJ
		(04-157-018) DLTU DFI B8	2X3	BN
		(04-158-019) DLTU DFI B9	2X3	BH
PICBS	SIDE 0	(04-058-351) TSIU2, MCTU OR MCTU2 1/CI	2X8	AS
		(04-058-151) TSIU2, MCTU OR MCTU2 0/CI	2X8	AT
	SIDE 1	(04-148-351) TSIU2, MCTU OR MCTU2 1/CI	2X8	AF
		(04-148-151) TSIU2, MCTU OR MCTU2 0/CI	2X8	AG

UNIT SYMBOL TABLE OF CONTENTS				
FUNCTION	DESCRIPTION (LOWER LEFT PIN ON CONNECTOR)	SIZE	ELEMENTS	
NCT LINKS A AND B	SIDE 0	(04-036-332) TSIU2, MCTU OR MCTU2 0/RLI A	2X24	DK
		(04-036-300) TSIU2, MCTU OR MCTU2 0/RLI B	2X24	DY
		(04-036-345) TSIU2, MCTU OR MCTU2 0/RLI A	2X12	DN
		(04-036-332) TSIU2, MCTU OR MCTU2 0/RLI A	2X12	DO
		(04-036-313) TSIU2, MCTU OR MCTU2 0/RLI B	2X12	CQ
	SIDE 1	(04-036-300) TSIU2, MCTU OR MCTU2 0/RLI B	2X12	CP
		(04-126-332) TSIU2, MCTU OR MCTU2 1/RLI A	2X24	DV
		(04-126-300) TSIU2, MCTU OR MCTU2 1/RLI B	2X24	DW
		(04-126-345) TSIU2, MCTU OR MCTU2 1/RLI A	2X12	BF
		(04-126-332) TSIU2, MCTU OR MCTU2 1/RLI A	2X12	BG
REMOTE CLOCK UNIT	SIDE 0	(04-058-313) RCU	2X3	DB
		(04-058-113) RCU	2X3	DC
	SIDE 1	(04-148-313) RCU	2X3	BR
		(04-148-113) RCU	2X3	BS
DLMI CONTROL AND DISPLAY	SIDE 0	(04-008-134) TSIU2 DLI0	2X12	AZ
		(04-008-132) MCTU, MCTU2 DLI0		
	SIDE 1	(04-008-134) TSIU2 DLI1	2X12	AM
	(04-008-132) MCTU, MCTU2 DLI1			
POWER	SIDE 0	(01-021-080) RETURN LUG	LUG	DU
		(01-031-080) POWER LUG	LUG	DU
	SIDE 1	(01-111-080) RETURN LUG	LUG	DJ
		(01-121-080) POWER LUG	LUG	DU

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CIRCUIT ACCESS REFERENCE DATA

FIG. 1

BACKPLANE PICTORIAL WIRING SIDE

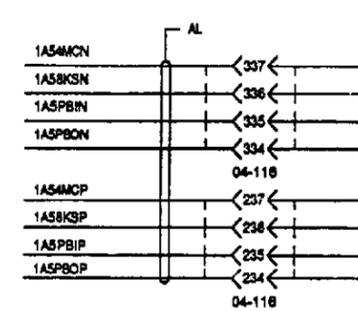
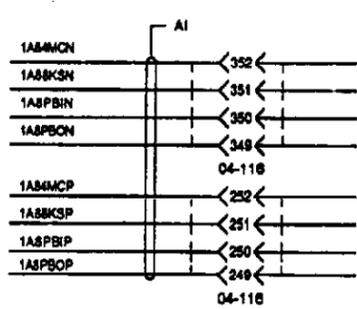
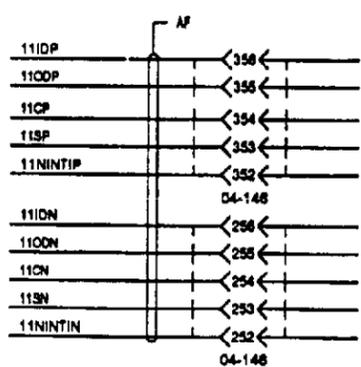
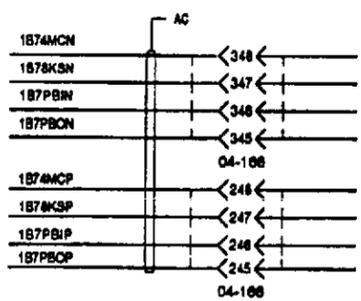
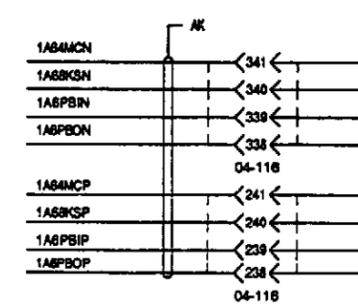
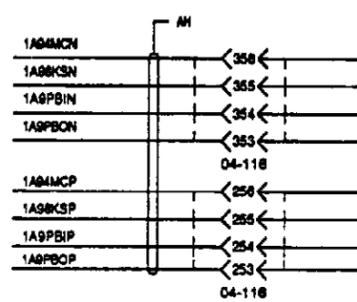
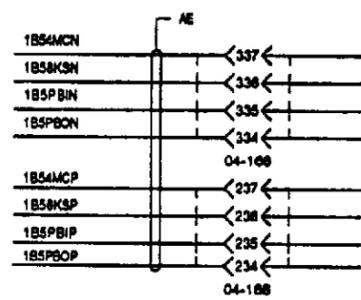
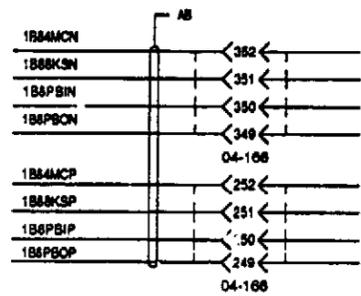
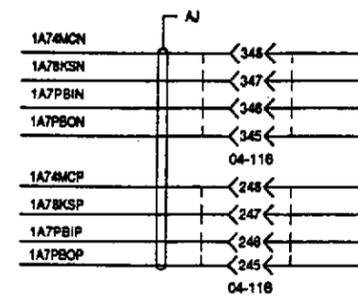
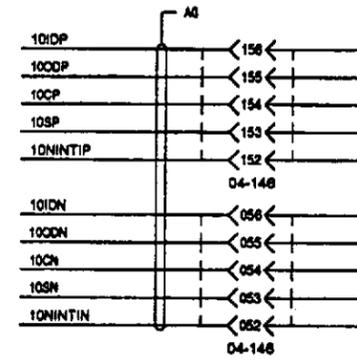
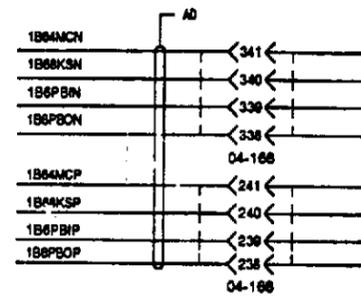
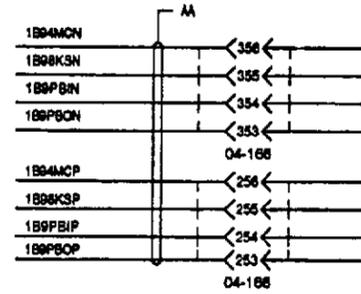
NOTES:
1. POWER AND GROUND LUGS ARE ELEMENT DU.

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UNIT SYMBOL

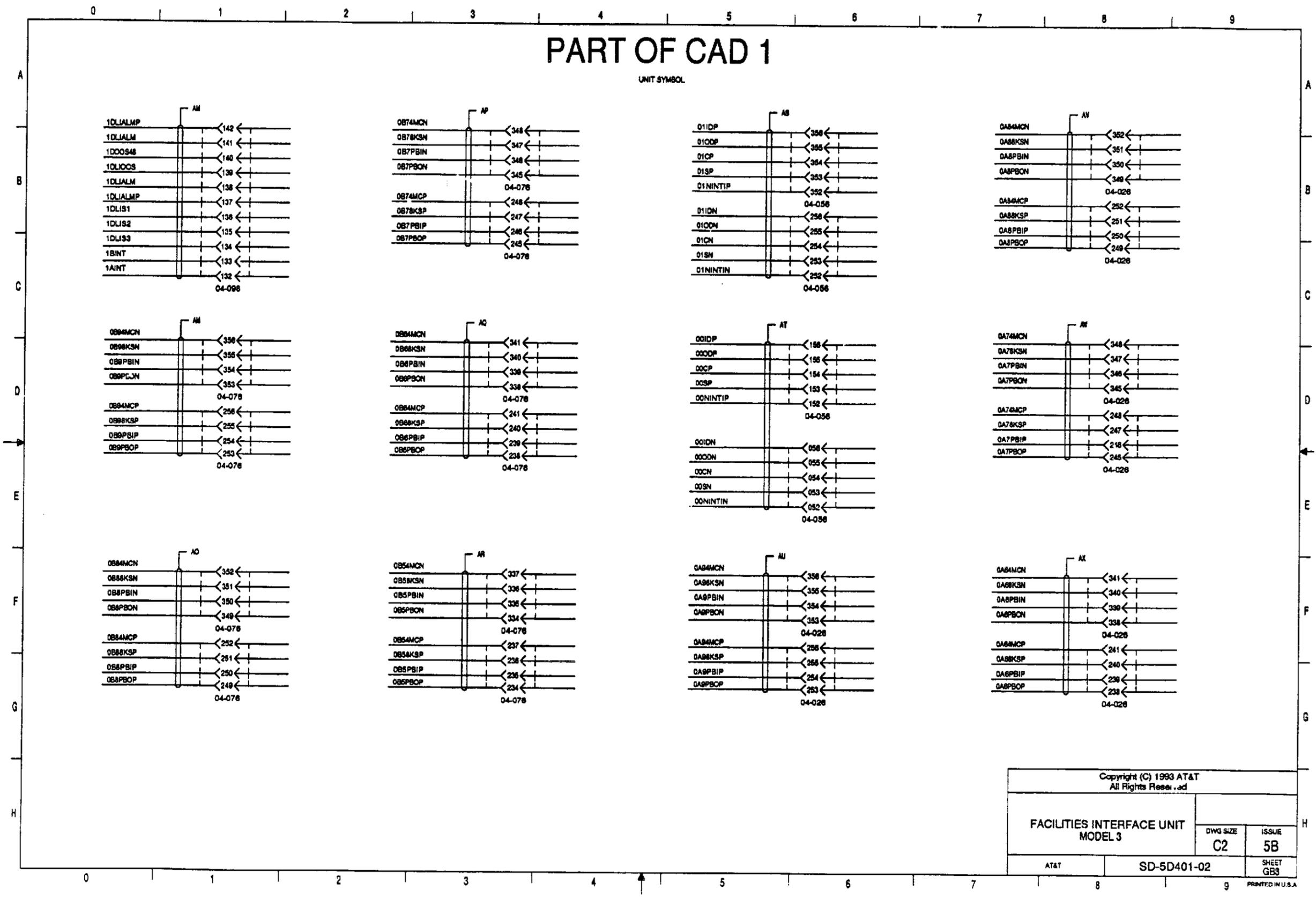


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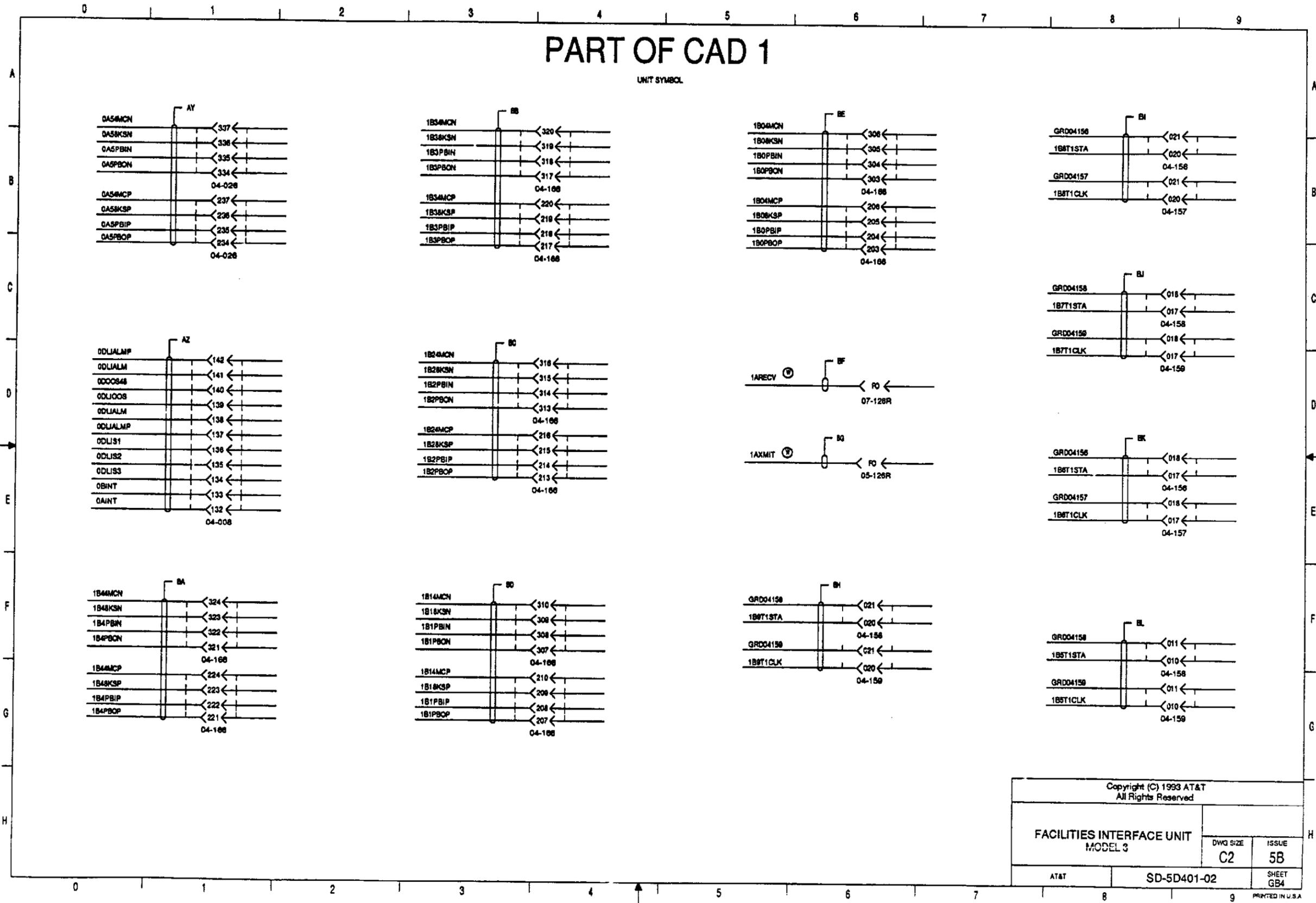


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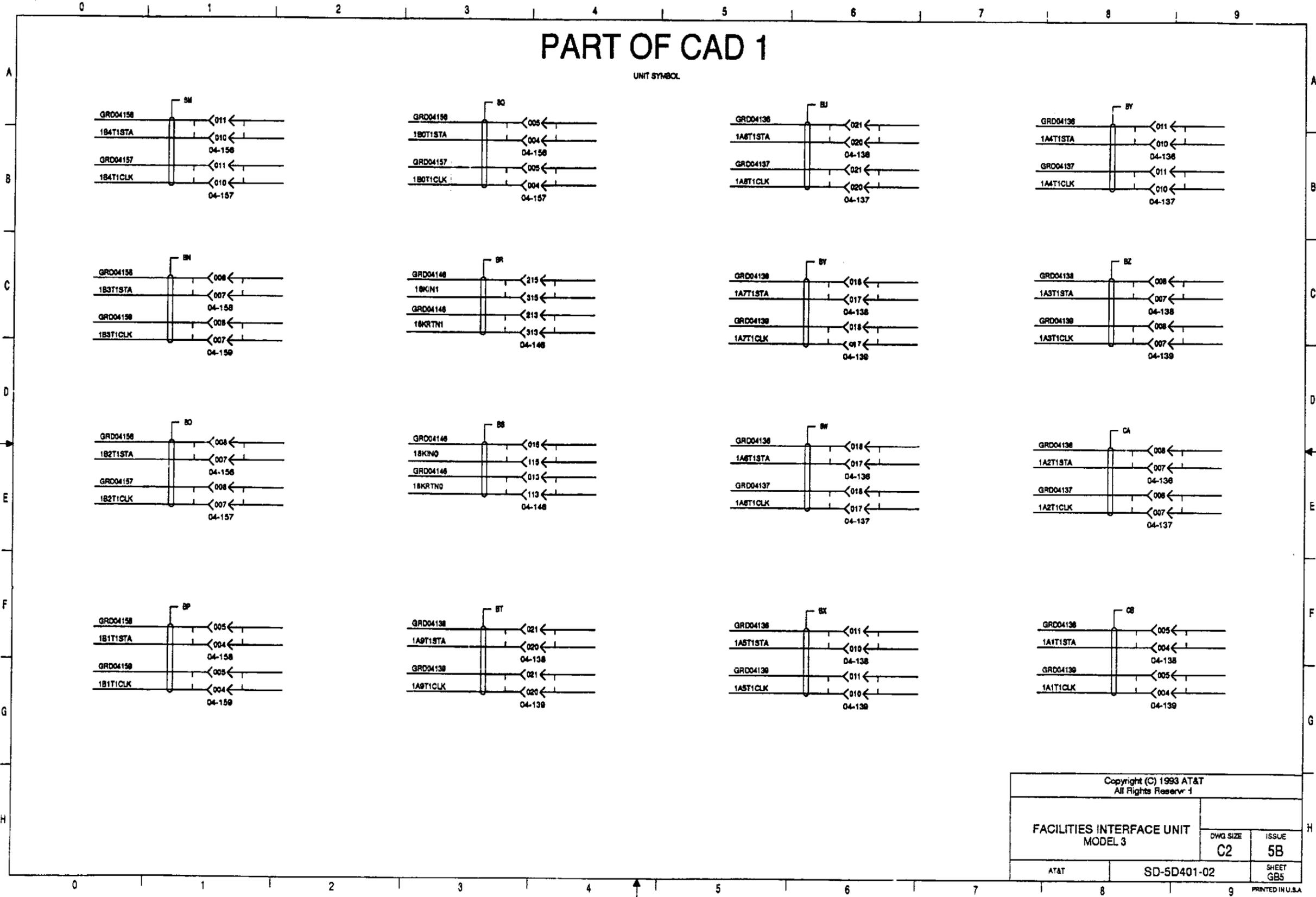
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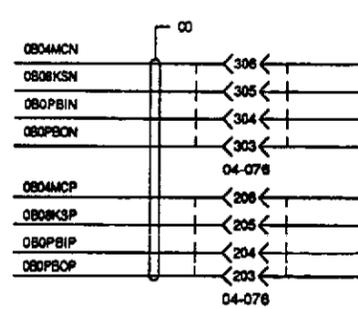
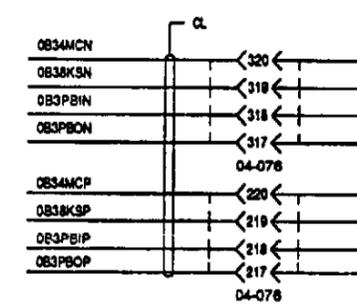
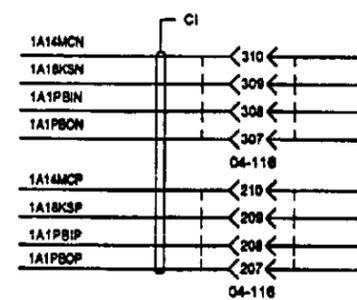
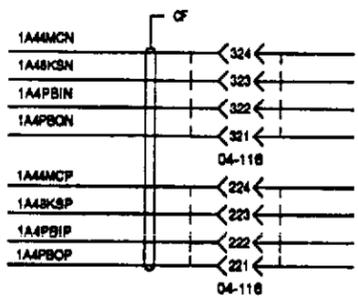
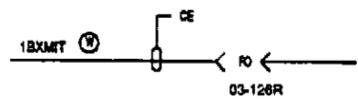
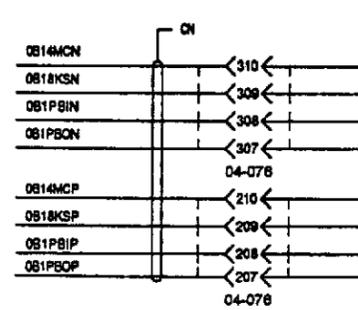
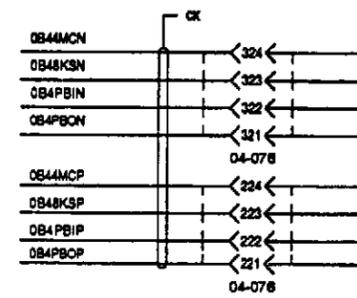
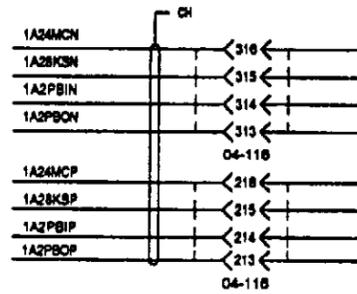
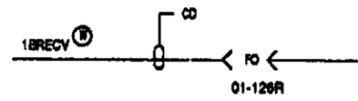
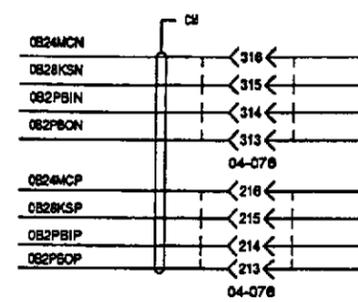
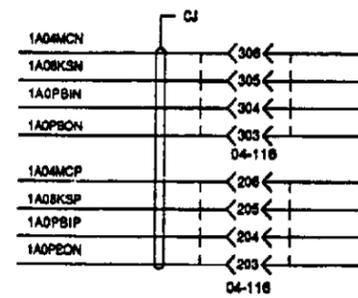
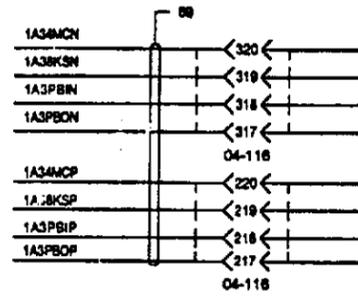
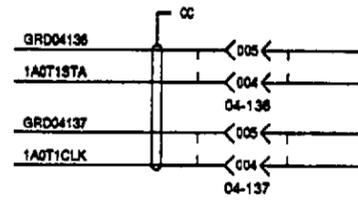
UNIT SYMBOL



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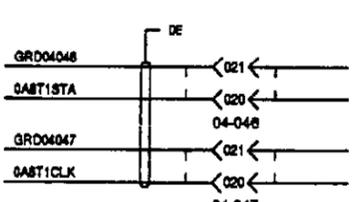
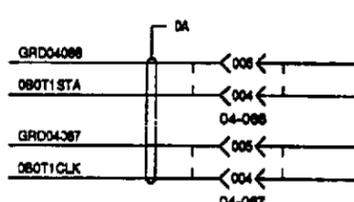
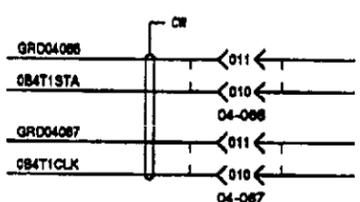
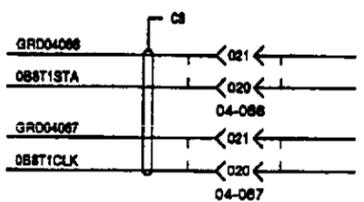
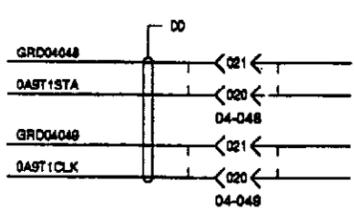
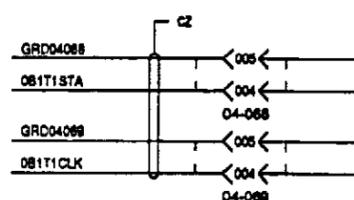
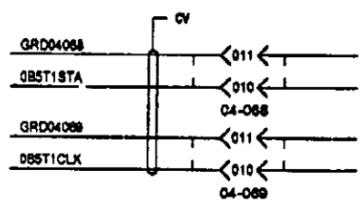
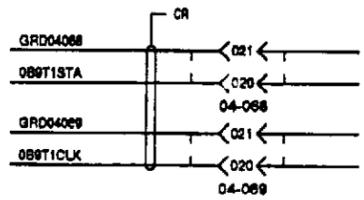
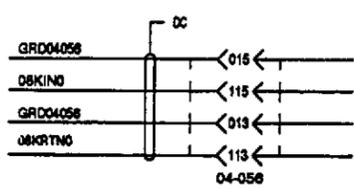
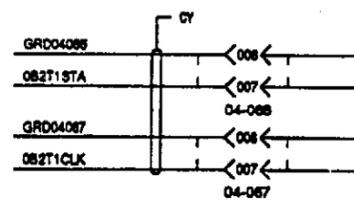
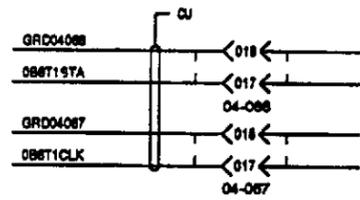
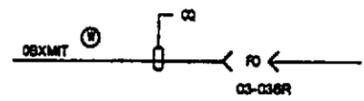
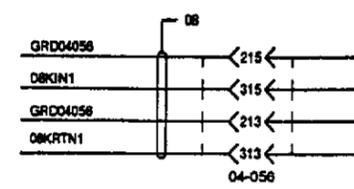
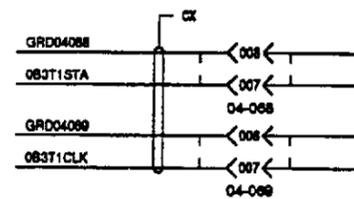
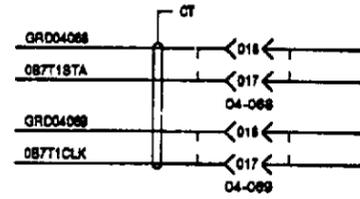
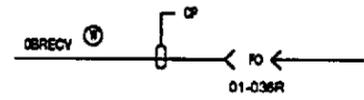
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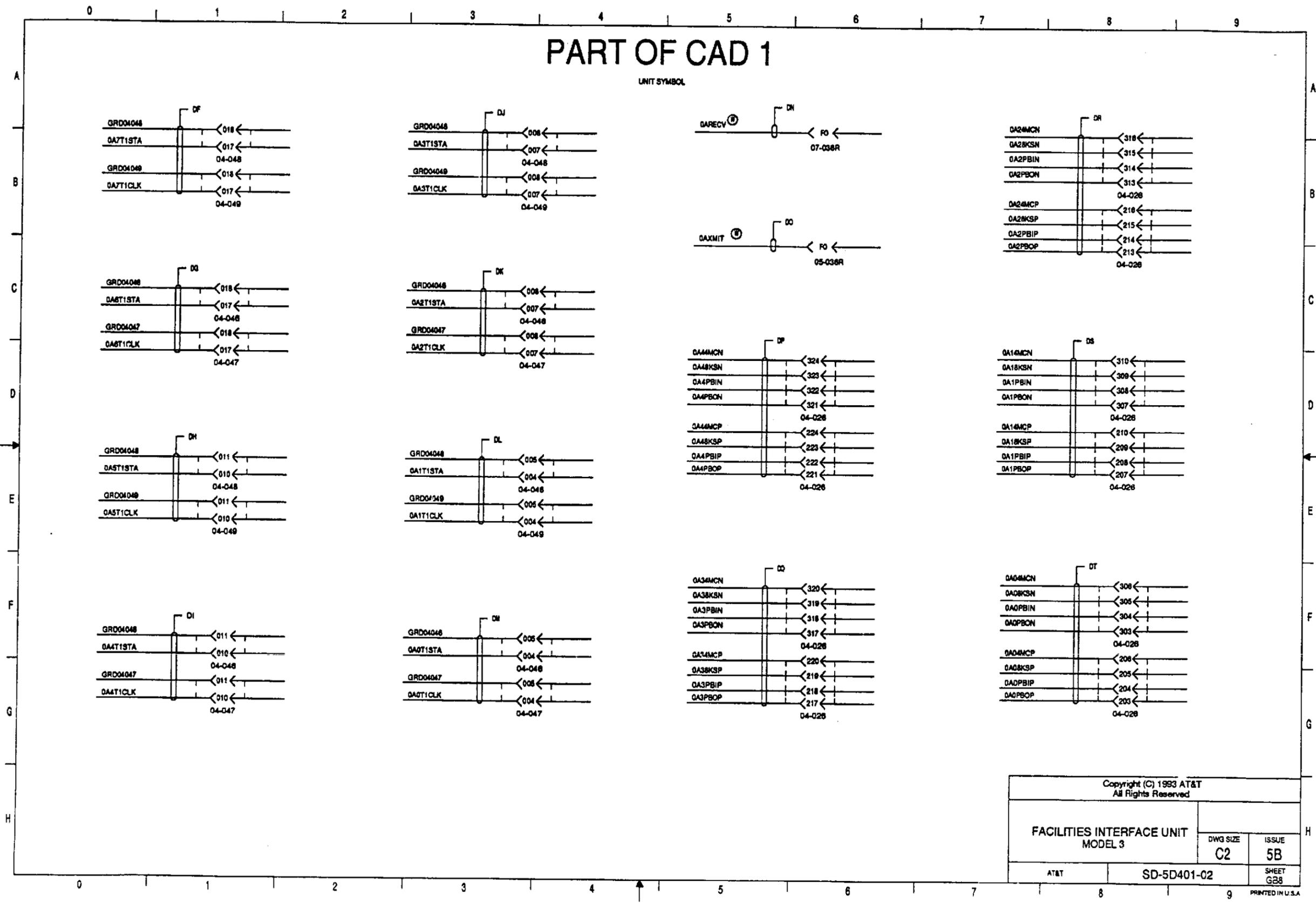


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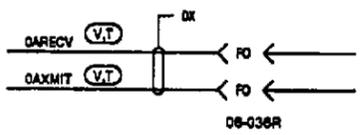
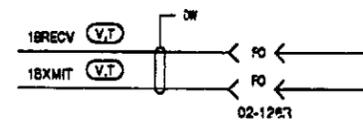
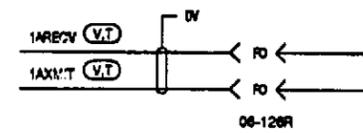
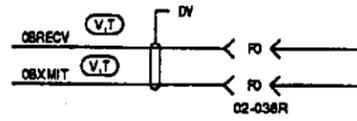
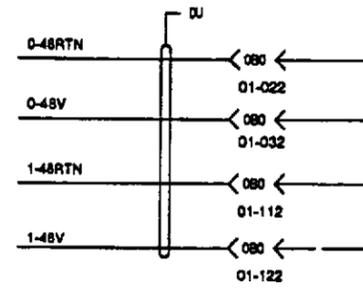
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