

SHEET INDEX

[illegible]

APPARATUS INDEX

DESIG	LOCATION		
	FS	APP FIG.	EQUIP.
CIRCUIT PACKAGES			
CPS 1	1C1	1	
CPS 2	1C3	1	
CPS 3A	1A4	1	
CPS 3B	1C4	1	
CPS 3C	1F4	1	
CPS 3D	1G4	1	
CPS 4	1G4	1	
CPS 5	1D6	1	
CPS 6	1D7	1	

DESIG	LOCATION		
	FS	APP FIG	EQUIP.
FILTERS			
BEF	1C2	1	

CONNECTORS			
F	SEE LPP FIG.	1	
F		2	

DIODES			
CR1	1E6	1	

SUPPORTING INFORMATION

CATEGORY	NO.
EQUIP. DESIGN SPEC	J99289

OPTION INDEX

APP OR REG	LOCATION
Z	APP FIG. 1
Y	APP FIG. 1
X	APP FIG. 1
W	APP FIG. 1

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING, ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE SHEET INDEX.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

REPLACES BUT NOT INTERCHANGABLE WITH SD-95287-01

SD-98148-01

IN99

AT&TCO
STANDARD

COMMON SYSTEMS
"TOUCH-TONE" CALLING
RECEIVING CIRCUIT
TYPE A3

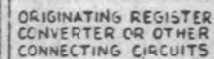
SD-98148-01-A1
11 SHEETS

BELL TELEPHONE LABORATORIES
INCORPORATED

69

FS I

"TOUCH-TONE" CALLING RECEIVING CIRCUIT



12

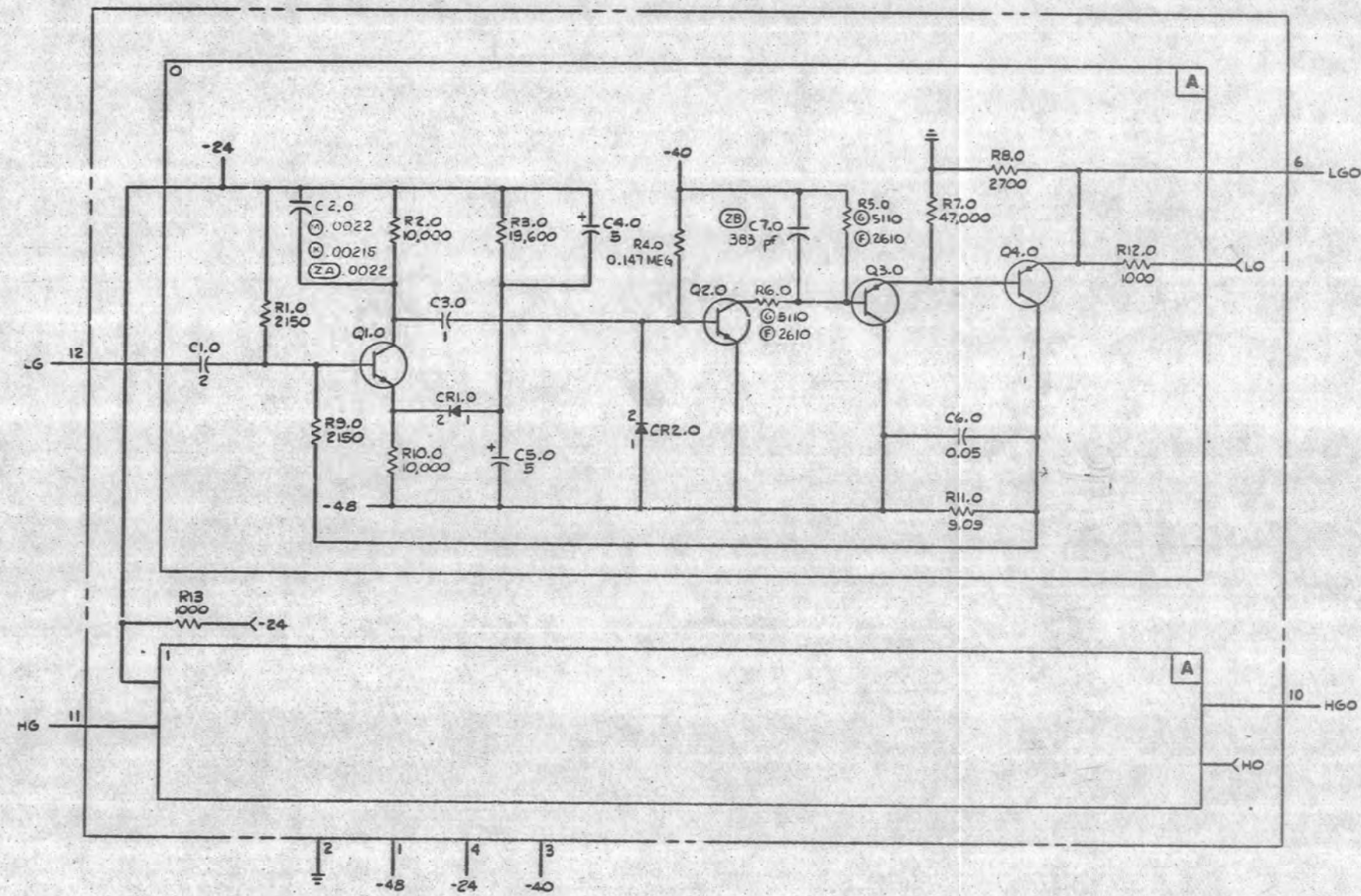
SD-98148-01-B1

②
own size
66

1000

67

CPS 2 GROUP LIMITER B2

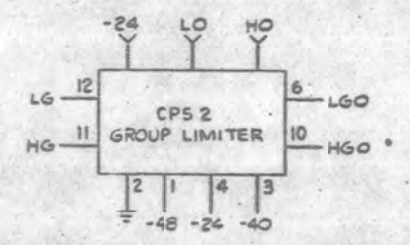


CAPACITOR		RESISTOR		TRANSISTOR	
DESIG	CODE	DESIG	CODE	DESIG	CODE
C1	542F	R1	221A, 2150	Q1	2N16F 66F
C2	KS-14138 L1, .0022	R2	221A, 10,000	Q2	2N16F 66F
	5946 .00215	R3	221A, 19,600	Q3	12D
	KS-20300 LS, .0022 OR	R4	221A, .147 MEG	Q4	12D
	5946 .00215	R5	221A 5110 2610		
C3	542N	R6	221A 5110 2610		
C4	601A	R7	KS-13490, L1, 47,000		
C5	601A	R8	KS-13492, L1, 2700		
C6	KS-13814 L1, .05	R9	221A, 2150		
CB	5700K, 383pf	R10	221A, 10,000		
CR1	4206 458C	R11	221A, 9.09		
CR2	4206 458C	R12	KS-13490, L1, 1000		
		R13	KS-13490, L1, 1000		

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	B2
ASSEMBLY DRAWING	4154778
CONNECTOR ON FRAME	909A

SYMBOL



DESCRIPTION:

THIS PACKAGE CONTAINS TWO LIMITER CIRCUITS, ONE FOR EACH OF THE TWO GROUPS OF "TOUCH-TONE" SIGNALING FREQUENCIES TO PROVIDE AN ESSENTIALLY SQUARE WAVE OUTPUT WHOSE TRANSITIONS OCCUR AT THE ZERO VOLTAGE AXIS CROSSINGS OF THE INPUT SIGNAL. EACH LIMITER CIRCUIT CONSISTS OF TWO LIMITER STAGES FOLLOWED BY TWO CASCADED EMITTER FOLLOWERS TO PROVIDE A LOW OUTPUT IMPEDANCE FOR DRIVING THE CPS 3, 4 CHANNEL CIRCUITS. POWER IS SUPPLIED AT TERMINAL 4 (-24 VOLTS FROM CPS 1), TERMINAL 3 (-40 VOLTS FROM CPS 5) TERMINAL 2 (GROUND) AND TERMINAL 1 (-48 VOLTS). THE LIMITER CIRCUIT WITH COMPONENT POSTSCRIPTS .0 IS INTENDED FOR THE LOW GROUP FREQUENCIES AND THE ONE WITH POSTSCRIPTS .1 FOR THE HIGH GROUP. (R1) AND (R9) BIAS THE BASE OF (Q1) HALFWAY BETWEEN -48 AND -24 VOLTS AND PROVIDE A 1000 OHM INPUT TERMINATION. (R11) PROVIDES NEGATIVE FEEDBACK FROM THE COLLECTOR OF (Q4). THE VOLTAGE DROP ACROSS (R3) AND (R10) IS EQUAL DUE TO THE BASE BIAS AND SINCE (R3) = 2(R10), (Q1) MUST SUPPLY TO (R10) THE OTHER HALF OF THE CURRENT IT NEEDS TO PRODUCE THE REQUIRED VOLTAGE DROP. CURRENT FROM (Q1) FLOWS THROUGH (R2) TO FIX THE COLLECTOR VOLTAGE OF (Q1) HALF WAY BETWEEN ITS EMITTER AND -24 VOLTS. WHEN AN AC SIGNAL IS APPLIED AT THE INPUT, THE POSITIVE HALF CYCLE CAUSES (CR1) TO BE BACK BIASED AND (Q1) SATURATES, AS ITS COLLECTOR CURRENT DOUBLES. THE NEGATIVE HALF CYCLE CUTS (Q1) OFF. HENCE THE COLLECTOR CURRENT OF (Q1) IS A SYMMETRICAL SQUARE WAVE. (Q2) ACTS AS A TRANSISTOR SWITCH. WITH (CR2) THE SWITCH INPUT IMPEDANCE IS ESSENTIALLY EQUAL FOR BOTH POSITIVE AND NEGATIVE INPUT SWINGS. THIS RESULTS IN POSITIVE HALF CYCLE SWINGS ON THE COLLECTOR OF (Q1) DRIVING BASE CURRENT INTO (Q2) EQUAL AND OPPOSITE TO THE CURRENT IN (CR2) ON NEGATIVE HALF CYCLES. HENCE THE BASE CURRENT IN (Q2) IS ESSENTIALLY EQUAL TO THE NEGATIVE HALF CYCLE COLLECTOR CURRENT SWING ON (Q1) AND A SQUARE WAVE OF VOLTAGE IS DEVELOPED AT THE COLLECTOR OF (Q2). THE AMPLITUDE OF THIS SWING IS ESSENTIALLY EQUAL TO THE DIFFERENCE BETWEEN THE -40 VOLT SUPPLY AND THE -48 VOLT SUPPLY. THE -40 VOLT SUPPLY IS ALSO USED TO SET THE THRESHOLD OF THE CPS3, 4 CHANNEL CIRCUIT DETECTORS; HENCE CHANGES IN SUPPLY ARE SELF COMPENSATING. (R5) AND (R6) ACT AS A VOLTAGE DIVIDER TO SUPPLY HALF OF THE COLLECTOR SQUARE WAVE VOLTAGE OF (Q2) TO (Q3) AND BIAS ITS BASE ABOUT A VOLTS ABOVE THE 48 VOLT SUPPLY. (Q3) AND (Q4) ACT AS CASCADED EMITTER FOLLOWERS TO PRODUCE A 4 VOLT P/P SQUARE WAVE OUTPUT WITH A LOW (ABOUT 10 OHMS) OUTPUT IMPEDANCE. RESISTOR (R11) WHICH PROVIDES NEGATIVE FEEDBACK SETS AND STABILIZES LIMITER SENSITIVITY AND, IN CONJUNCTION WITH THE CPS3, 4 CHANNEL CIRCUITS WHOSE INPUT IMPEDANCES ARE MINIMUM AT TOUCH-TONE SIGNALING FREQUENCIES, PROVIDES EQUALIZATION OF LIMITER SENSITIVITY. THIS RESULTS IN LOWER SENSITIVITY AT THE SIGNALING FREQUENCIES AND HENCE PROVIDES PROTECTION AGAINST SPEECH INPUTS SIMULATING SIGNALING FREQUENCY OUTPUTS BY EMPHASIZING OUT OF BAND FREQUENCIES. CAPACITORS (C2) AND (C6) INSURE HIGH FREQUENCY STABILITY. TEST POSTS ARE PROVIDED AT EACH LIMITER OUTPUT AND ON THE -24 VOLT SUPPLY.

COMMON SYSTEMS
"TOUCH-TONE" CALLING
RECEIVING CIRCUIT
TYPE A3

SD-98148-01-B12

BELL TELEPHONE LABORATORIES
INCORPORATED

6S

SD-98148-01-B12

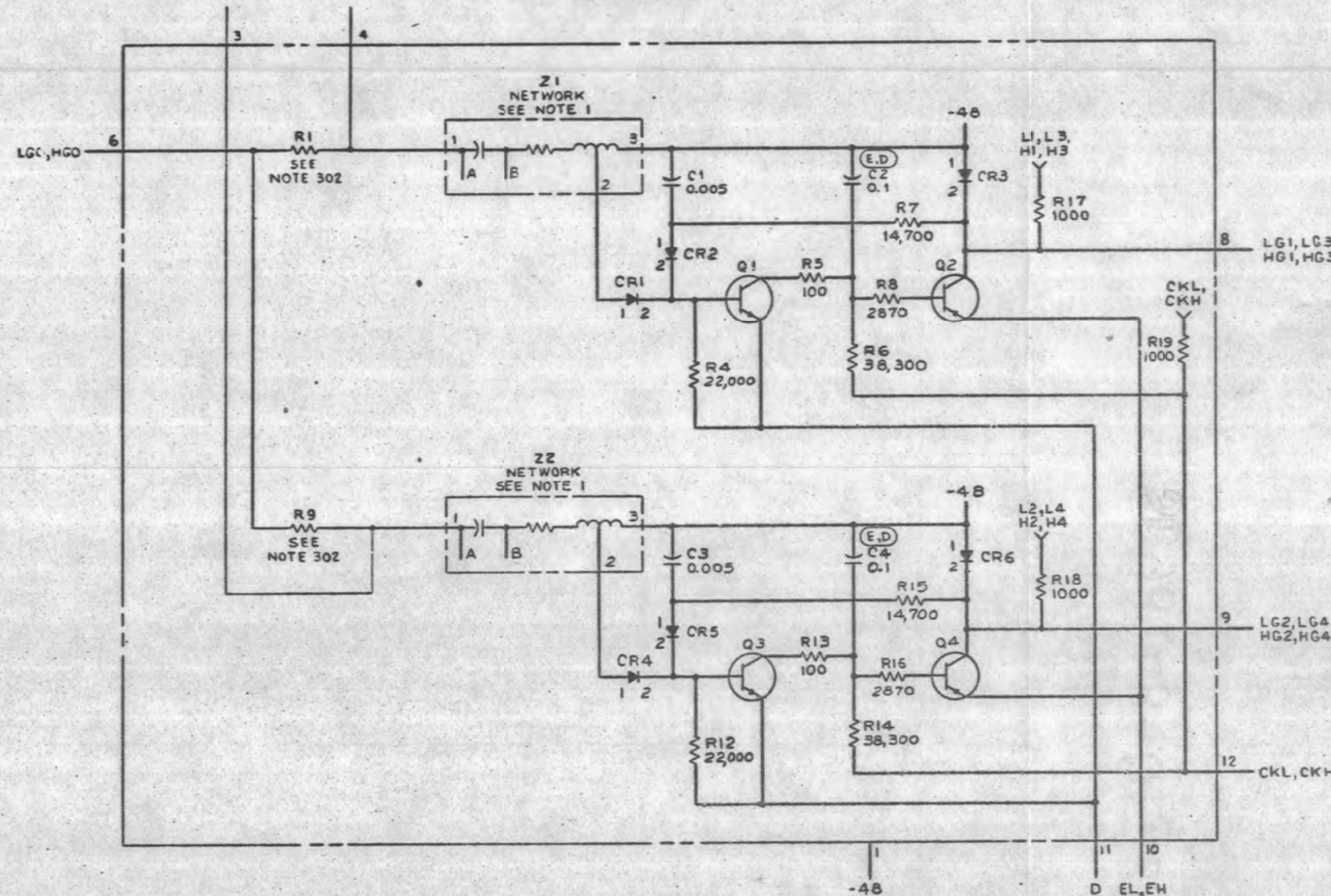
CPS 3A,3B,3C & 3D CHANNEL CIRCUIT B3,B4,B5 & B6

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	B3,B4,B5 & B6
ASSEMBLY DRAWING	A154779
CONNECTOR ON FRAME	909A

DESCRIPTION:

EACH CHANNEL CIRCUIT CONSISTS OF TWO CIRCUITS FOR THE RECOGNITION AND DETECTION OF A SPECIFIC "TOUCH-TONE" SIGNALING FREQUENCY AND FOR LOCKING IN A DETECTED SIGNAL WHILE AN OUTPUT IS BEING DELIVERED TO THE ASSOCIATED CONNECTING CIRCUIT. THE CIRCUIT IS MEANT TO BE DRIVEN BY THE CPS 2 LIMITER WITH THE LOW LIMITER DRIVING THE TWO LOW GROUP CHANNEL CIRCUITS AND THE HIGH LIMITER DRIVING THE TWO HIGH GROUP CHANNEL CIRCUITS AT TERMINAL 6. CONTROL VOLTAGES ARE SUPPLIED BY CPS 6 AT TERMINALS 10 AND 11. OUTPUT LEADS, TERMINALS 8 AND 9 SHOULD RETURN TO -48 VOLTS THROUGH THE ASSOCIATED CONNECTING CIRCUITS DIGIT RELAYS. OUTPUT TERMINAL 12 IS RETURNED TO ABOUT -7 VOLTS THROUGH 1300 OHMS IN CPS 105. ONLY THE TOP HALF OF THE CHANNEL CIRCUIT WILL BE DESCRIBED AS THE OTHER HALF OPERATES IN AN IDENTICAL MANNER EXCEPT AT A DIFFERENT INPUT FREQUENCY. RESISTOR (R1) IS PROVIDED IN SERIES WITH THE TUNED CIRCUIT (Z1). THE LIMITER DRIVES THE TUNED CIRCUIT WITH A SQUARE WAVE OF ABOUT 4 VOLTS P/P. AT RESONANCE THE FUNDAMENTAL FREQUENCY COMPONENT DEVELOPED ACROSS THE SERIES INDUCTANCE IS QUITE LARGE AND PROPORTIONAL TO J. WITH J ADJUSTED TO ABOUT 14, A SINUSOIDAL TAP VOLTAGE OF ABOUT 12 VOLTS PEAK IS DEVELOPED. THE EMITTER OF (Q1) IS NORMALLY BIASED ABOUT 8 VOLTS ABOVE THE -48 VOLT TUNED CIRCUIT RETURN, HENCE POSITIVE HALF CYCLES OF THE TAP VOLTAGE IN EXCESS OF 8 VOLTS PLUS THE BASE - EMITTER DROP OF (Q1) PLUS THE DROP ACROSS (CR1) DRIVE (Q1) ON. HENCE A DETECTOR THRESHOLD OF ABOUT 9.5 VOLTS OR ABOUT 2db BELOW THE +12 VOLT PEAK POSITIVE OUTPUT OF THE TUNED CIRCUITS. IS SET. THIS THRESHOLD INSURES THAT ONLY ONE CHANNEL CIRCUIT DETECTOR WILL BE ENERGIZED BY A GIVEN LIMITER AT A TIME, AND SETS DETECTOR BANDWIDTH TO ABOUT 5% OF THE RESONANT FREQUENCY, DEPENDING ON THE EXACT VALUE OF Q. WHEN A SIGNALING FREQUENCY CAUSES THE TUNED CIRCUIT VOLTAGE TO DRIVE (Q1) ON, (Q1) RAPIDLY DISCHARGES (C2) AND CAUSES A DROP IN VOLTAGE AT TERMINAL 12. THIS INDICATES A SIGNAL CHECK TO CPS 5. AT THE COMPLETION OF THE POSITIVE HALF CYCLE (Q1) TURNS OFF AND (C2) CHARGES WITH A TIME CONSTANT DETERMINED BY (R6), (C2) AND CPS 5. SHOULD THE INPUT SIGNAL STOP AT THIS POINT THE VOLTAGE AT TERMINAL 12 WILL RISE SUFFICIENTLY TO NO LONGER INDICATE A SIGNAL CHECK TO CPS 5, IN ABOUT 4 MILLISECONDS. HOWEVER, AS LONG AS THE INPUT PERSISTS THE COLLECTOR VOLTAGE OF (Q1) WILL BE LESS THAN 16 VOLTS ABOVE THE -48 VOLT SUPPLY. THE OUTPUT TRANSISTOR (Q2) IS NOT ACTIVATED BY CPS 6 VIA TERMINAL 10, UNTIL A VALID SIGNAL HAS PERSISTED LONG ENOUGH FOR THE CPS 5 SIGNAL TIMER TO RUN OUT. AT THIS TIME CPS 6 IS TRIGGERED AND -22 VOLTS IS APPLIED TO TERMINAL 10 AND A 750 OHM RESISTOR IS INSERTED IN SERIES WITH THE -40 VOLT SUPPLY TO TERMINAL 11. IF (Q1) IS OPERATED AT THIS TIME ITS COLLECTOR VOLTAGE IS SUFFICIENTLY NEGATIVE AS TO TURN ON (Q2) THROUGH (R6) CAUSING COLLECTOR CURRENT TO FLOW THROUGH (R7), (CR2) TO THE BASE OF (Q1) LOCKING (Q1) AND (Q2) ON. THE COLLECTOR VOLTAGE OF (Q2) DROPS TO -22 VOLTS CAUSING CURRENT TO FLOW IN THE ASSOCIATED CONNECTING CIRCUIT RELAY VIA TERMINAL 8 AND OPERATING THE RELAY. EMITTER CURRENT FROM (Q1) FLOWS THROUGH THE 750 OHM RESISTOR INSERTED IN SERIES BY CPS 6 CAUSING THE EMITTER VOLTAGE OF (Q1) TO RISE TO A POINT WHERE IT IS IMPOSSIBLE TO OPERATE A DETECTOR FROM A TUNED CIRCUIT OUTPUT. THIS PRECLUDES THE POSSIBILITY OF FALSE DETECTOR OPERATION DURING THE READ OUT INTERVAL. (Q1) AND (Q2) REMAIN LOCKED UNTIL CPS 6 RETURNS TO NORMAL AND REMOVES THE -22 VOLT BIAS FROM TERMINAL 10. IF THE INPUT SIGNAL IS STILL PRESENT AT THIS TIME (Q1) REMAINS OPERATED AS IT WAS INITIALLY AND (Q2) TURNS OFF, RELEASING THE CONNECTING CIRCUIT DIGIT RELAY. (R5) LIMITS THE COLLECTOR CURRENT IN (Q1) WHEN (C2) IS DISCHARGED. CAPACITOR (C1) REDUCES SWITCHING TRANSIENTS. (CR3) PREVENTS NEGATIVE INDUCTIVE SURGES FROM THE DIGIT RELAY WHEN (Q2) TURNS OFF. TEST POINTS ARE PROVIDED AT THE DIGIT RELAY OUTPUTS AND THE CHECK OUTPUT TO CPS 5. TERMINALS 3 AND 4 ARE PROVIDED FOR MANUFACTURING TESTING ONLY.

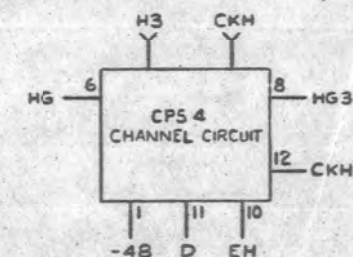


ISSUE
1
2D
3A
4B
5B
8D
10B
12D
A
B
C
D
E
F
G
H

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	B7
ASSEMBLY DRAWING	A154780
CONNECTOR ON FRAME	909A

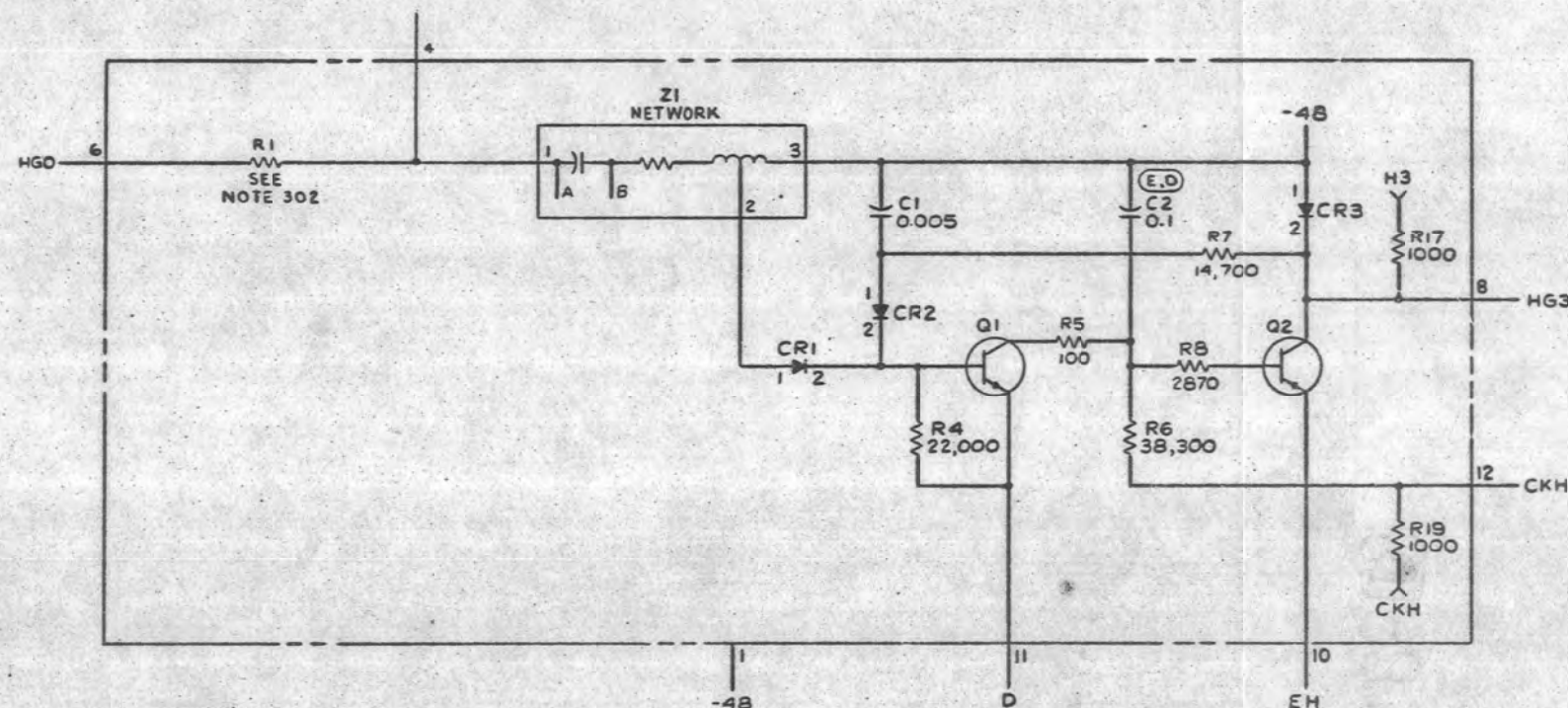
SYMBOL



DESCRIPTION:

THE CPS 4 CHANNEL CIRCUIT OPERATES IN A MANNER IDENTICAL WITH THE CPS 3 CHANNEL CIRCUITS EXCEPT ONLY ONE FREQUENCY CHANNEL (1477 CPS) IS PROVIDED.

CPS 4 CHANNEL CIRCUIT B7



COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	KS-13814, L8, .005
C2	542L, 722C

DIODE

DESIG	CODE
CR1	420G, 458C
CR2	420G, 458C
CR3	441J

NETWORK

DESIG	CODE
Z1	4053G

RESISTOR

DESIG	CODE
R1	221A, SEE NOTE 302
R4	KS-13490, L1, 22,000
R5	KS-13490, L1, 100
R6	221A, 38,300
R7	221A, 14,700
R8	221A, 2870
R17	KS-13490, L1, 1000
R19	KS-13490, L1, 1000

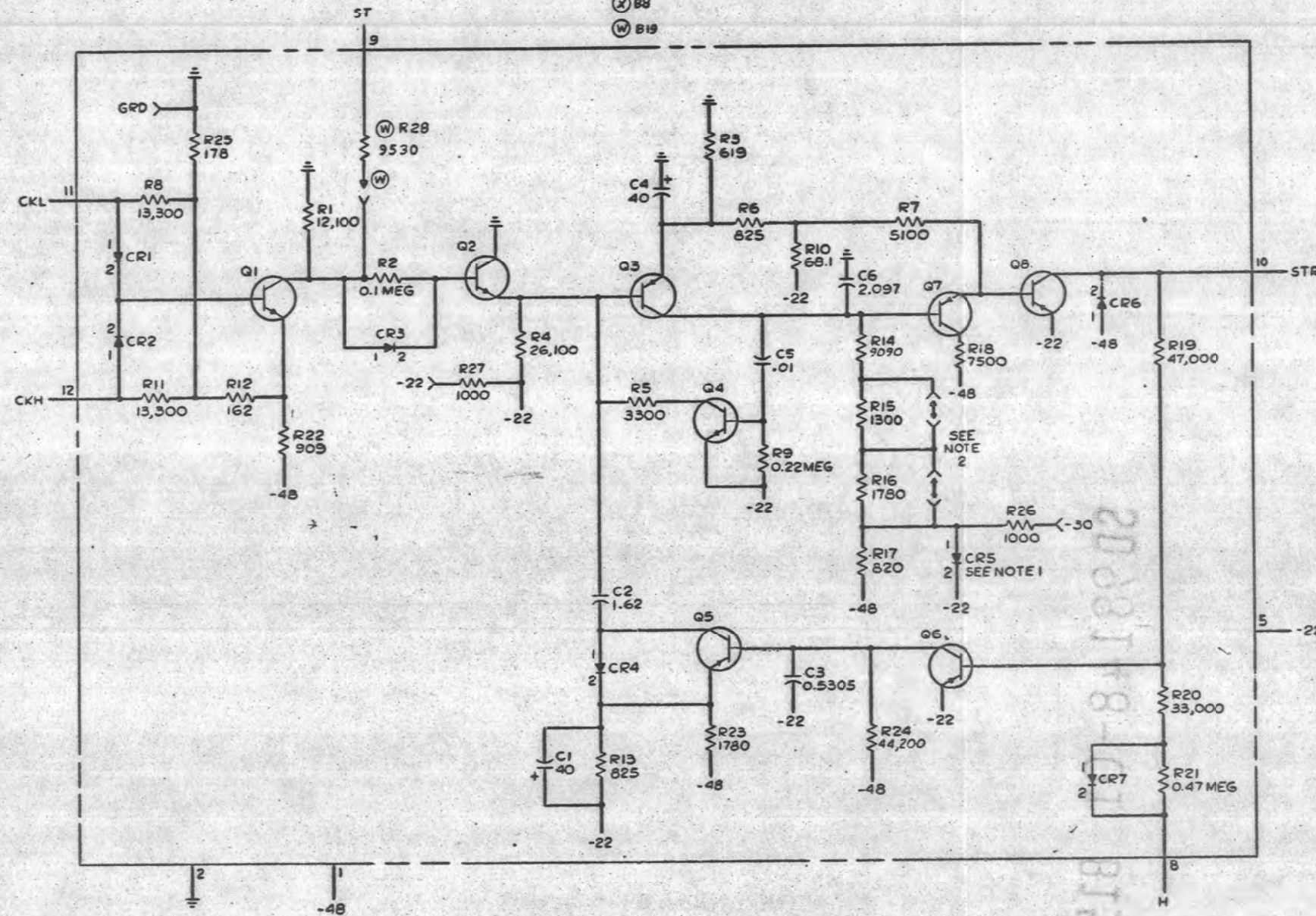
TRANSISTOR

DESIG	CODE
Q1	2C 16F, 2D 66F
Q2	12N

SD-98148-01-B14

1/3 378

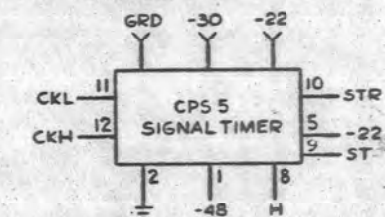
CPS 5 SIGNAL TIMER (X) B8 (W) B19



SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	(X) B8, (W) B19
ASSEMBLY DRAWING	A154781
CONNECTOR ON FRAME	909A

SYMBOL



DESCRIPTION:

THE SIGNAL TIMER IS MEANT TO CHECK AND TIME THE CPS 3, 4 CHANNEL CIRCUIT CHECK SIGNALS AND ENERGIZE A STEERING RELAY AS LONG AS A VALID SIGNAL PERSISTS. A TRIGGER VOLTAGE IS ALSO SUPPLIED TO CPS 6 VIA TERMINAL 10. CONTROL VOLTAGE IS FEEDBACK TO CPS 5 FROM CPS 6 VIA TERMINAL 8. IT HAS TWO INPUTS TERMINALS 11 AND 12, ONE FOR THE LOW GROUP CHANNEL CIRCUITS AND ONE FOR THE HIGH GROUP. (CR1), (CR2) AND (Q1) COMPRISE AN "AND" GATE. THIS GATE OPENS WHEN ONE DETECTION IN BOTH THE HIGH AND LOW GROUP CHANNEL CIRCUITS (CPS 3, 4) OPERATES CAUSING A DROP IN VOLTAGE AT TERMINALS 11 AND 12. (R12), (R22) AND (R25) HOLD THE EMITTER OF (Q1) AT ABOUT -13 VOLTS. WHEN A VALID SIGNAL IS PRESENT AT THE INPUTS AND (Q1) TURNS OFF, ITS COLLECTOR VOLTAGE RISES AND CURRENT FLOWS THROUGH (R1) AND (CR3) TURNING (Q2) ON. WHEN THE ST LEAD (OPTION W) IS PROVIDED, AN OUTPUT, UNDER THE CONTROL OF (Q1) IS AVAILABLE AT THIS TIME. (R2) ABSORBS LEAKAGE CURRENT FROM (Q2) WHEN IT IS OFF. WHEN (Q2) TURNS ON ITS EMITTER VOLTAGE RISES TO ALMOST GROUND POTENTIAL AND (C2) IS CHARGED THROUGH (CR4), AND (Q3) TURNS OFF. THIS PERMITS (C6) TO CHARGE EXPONENTIALLY THROUGH (R14), (R15), (R16) FROM THE REGULATED -30 VOLT SUPPLY CONTROLLED BY (CR5). TERMINAL 5 SHOULD BE CONNECTED TO THE ANODE OF A 22 VOLT ZENER DIODE WITH ITS CATHODE RETURNED TO GROUND. THIS PROVIDES A REGULATED -22 VOLTS AT TERMINAL 5 AND -30 VOLTS AT THE ANODE OF (CR5). (C6) CHARGES SUFFICIENTLY TO TURN (Q7) ON IN ABOUT 21.5 MILLISECONDS. WHEN (Q7) TURNS ON CURRENT FLOWS THROUGH (R18) AND (Q7) TURNING (Q8) ON. TERMINAL 10 SHOULD BE RETURNED TO -48 VOLTS THROUGH THE STEERING RELAY IN THE ASSOCIATED CONNECTING CIRCUIT. TURN ON OF (Q8) RESULTS IN OPERATION OF THIS RELAY AND A POSITIVE VOLTAGE EXCURSION AT TERMINAL 10 WHICH IS USED TO TRIGGER CPS 6. THE -48 VOLTS NORMALLY ON TERMINAL 10 HOLDS (Q6) ON THROUGH (R19). THE TURN ON OF (Q8) PERMITS (Q6) TO TURN OFF, HOWEVER TERMINAL 8 IS NORMALLY HELD AT ABOUT -13 VOLTS BY CPS 6 BUT WHEN (Q8) TURNS ON AND CPS 6 IS TRIGGERED THE VOLTAGE AS TERMINAL 8 CHANGES TO ABOUT -30 VOLTS HOLDING (Q6) ON THROUGH (R20) AND (CR7). WHEN CPS 6 RETURNS TO NORMAL (Q6) IS TURNED OFF WITH (R21) HOLDING ITS BASE VOLTAGE SLIGHTLY ABOVE THE -22 VOLT SUPPLY. WHEN (Q6) TURNS OFF ITS COLLECTOR VOLTAGE RISES WITH A TIME CONSTANT DETERMINED BY (C3) AND (R24), AND REACHES THE TURN ON VOLTAGE OF (Q5) IN ABOUT 10 MILLISECONDS. WHEN (Q5) TURNS ON THE BOTTOM OF (C2) IS CLAMPED TO THE EMITTER VOLTAGE OF (Q5), DETERMINED BY VOLTAGE DIVIDER (R13), (R23) (ABOUT -30 VOLTS). SHOULD THE INPUT SIGNAL CHECK STOP AT THIS TIME (Q1) WOULD TURN ON AND (Q2) TURN OFF, HOWEVER ITS EMITTER VOLTAGE WOULD DROP WITH A TIME CONSTANT DETERMINED BY (C2) AND (R4). THE EMITTER VOLTAGE OF (Q2) WILL REACH THE TURN ON VOLTAGE OF (Q3) IN ABOUT 20 MILLISECONDS. TURN ON OF (Q3) WILL DISCHARGE (C6) AND TURN OFF (Q7) AND (Q8). HENCE, TURNING ON (Q6) AND TURNING OFF (Q5), THUS RESTORING THE CIRCUIT TO NORMAL. IF HOWEVER THE INPUT SIGNAL CHECK STOPS BEFORE (Q6) TURNS OFF AND (Q5) ON, (C2) WILL NOT BE CLAMPED AND THE EMITTER VOLTAGE OF (Q2) WILL DROP INSTANTLY, CAUSING THE CIRCUIT TO RESET ALMOST INSTANTLY.

DESCRIPTION: (CONTINUED)

WHEN (Q3) TURNS ON AND ITS COLLECTOR VOLTAGE STARTS TO RISE, CURRENT FLOWS THROUGH (C5) INTO THE BASE OF (Q4) TURNING IT ON AND INCREASING THE BASE CURRENT TO (Q3) THROUGH (R5) AND THE COLLECTOR OF (Q4). THIS SPEEDS UP THE RESET OF THE SIGNAL TIMER. CAPACITOR (C1) ABSORBS THE CURRENT SURGE WHEN (C2) IS CHARGED AND (C4) ABSORBS THE CURRENT SURGE WHEN (C6) IS CHARGED. (CR6) PROTECTS (Q4) FROM INDUCTIVE SURGES WHEN (Q4) TURNS OFF AND THE STEERING RELAY IS RELEASED. TEST POSTS ARE PROVIDED AT GROUND AND THE -22 AND -30 VOLT SUPPLY POINTS.

SHEET NOTES:

1. ZENER DIODE NOMINAL BREAKDOWN VOLTAGE (CR5) -2.2 VDC
2. RESISTOR (R16) SHALL NORMALLY BE STRAPPED OUT. IF SIGNAL TIMER INTERVAL IS SHORTER THAN REQUIRED, REMOVE STRAP FROM (R16). IF SIGNAL TIMER INTERVAL IS LONGER THAN REQUIRED, STRAP OUT (R16) AND (R15).

COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	602A
C2	535DL
C3	535N
C4	602A
C5	KS-16048, L4, .01
C6	535J

DIODE

DESIG	CODE
CR1	(S) 4206 (R) 458C
CR2	(S) 4206 (R) 458C
CR3	441J
CR4	441J
CR5	(S) 420M (R) 446T
CR6	441J
CR7	441J

RESISTOR

DESIG	CODE
R1	221A, 12,100
R2	KS-13490, L1, .1 MEG
R3	221A, 619
R4	221A, 26,100
R5	KS-13490, L1, 3300
R6	221A, 825
R7	KS-13490, L1, 5100
R8	221A, 13,300
R9	KS-13490, L1, .22 MEG
R10	221A, 68.1
R11	221A, 13,300
R12	221A, 162
R13	221A, 825
R14	221A, 9090
R15	221A, 1300
R16	221A, 1780

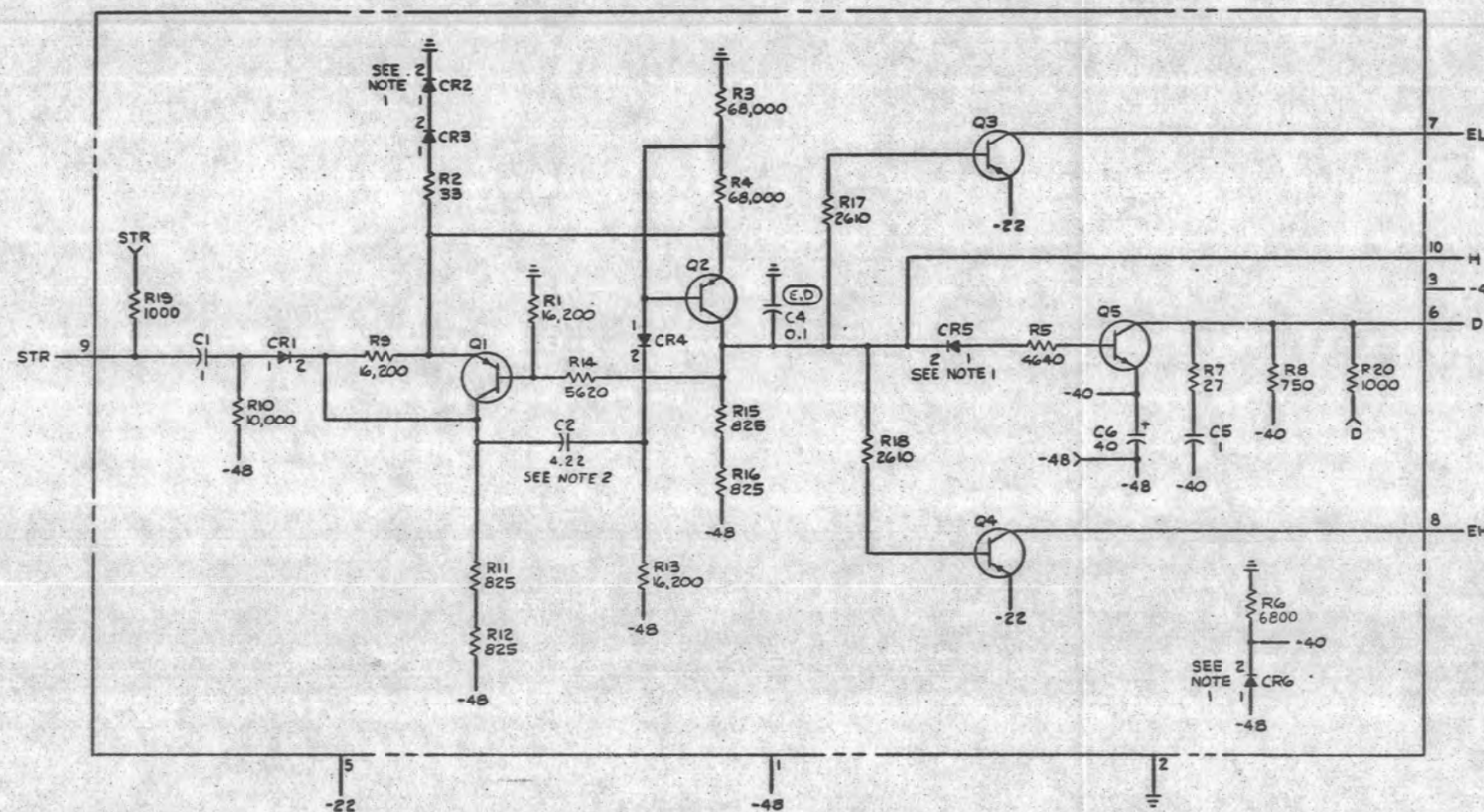
RESISTOR (CONT)

DESIG	CODE
R17	KS-13492, L1, 820
R18	221A, 7500
R19	KS-13490, L1, 47,000
R20	KS-13490, L1, 33,000
R21	KS-13490, L1, .47 MEG
R22	(ZG) KS-14603, L3C, 909
R23	(ZH) KS-20289, L3C, 909
R24	221A, 1780
R25	221A, 178
R26	KS-13490, L1, 1000
R27	KS-13490, L1, 1000
R28	238A, 9530

TRANSISTOR

DESIG	CODE
Q1	(ZC) 16F (ZD) 66F
Q2	(ZC) 16F (ZD) 66F
Q3	12D
Q4	(ZC) 16F (ZD) 66F
Q5	12D
Q6	12D
Q7	12D
Q8	12D

CPS 6 OUTPUT TIMER B9



COMPONENT LIST

CAPACITOR

DESIG	CODE
C1	542N
C2	SEE NOTE 2
C4	542L, 722C
C5	542N
C6	602A

DIODE

DESIG	CODE
CR1	441J
CR2	5420A, 446B
CR3	5420A, 446B
CR4	5420G, 450A
CR5	5420N, 446M
CR6	5420S, 446T

RESISTOR

DESIG	CODE
R1	221A, 16,200
R2	KS-13490, L1, 33
R3	KS-13490, L1, 68,000
R4	KS-13490, L1, 68,000
R5	221A, 4640
R6	KS-13490, L1, 6800
R7	KS-13490, L1, 27
R8	221A, 750
R9	221A, 16,200
R10	KS-13490, L1, 10,000

RESISTOR (CONTINUED)

DESIG	CODE
R11	221A, 825
R12	221A, 825
R13	221A, 16,200
R14	221A, 5620
R15	221A, 825
R16	221A, 825
R17	221A, 2610
R18	221A, 2610
R19	KS-13489, L1, 1000
R20	KS-13490, L1, 1000

TRANSISTOR

DESIG	CODE
Q1	12D
Q2	12D
Q3	12D
Q4	12D
Q5	2C-16F, 2D-66F

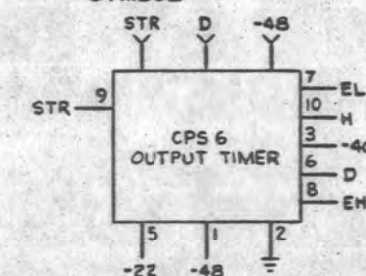
NOTES:

- ZENER DIODE NOMINAL BREAKDOWN VOLTAGE
(CR2) - 6 VDC
(CR3) - 6 VDC
(CR5) - 15 VDC
(CR6) - 8.2 VDC
- THE REQUIRED CAPACITANCE OF 4.22 UF MAY BE OBTAINED BY ONE 535GA CAPACITOR DESIGNATED (C2) OR TWO 535J CAPACITORS WIRED IN PARALLEL AND DESIGNATED (C2A) AND (C2B) RESPECTIVELY.

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	B9
ASSEMBLY DRAWING	A154782
CONNECTOR ON FRAME	909A

SYMBOL



DESCRIPTION:

THE OUTPUT TIMER CONSISTS OF A MONOPULSER FOR TIMING THE DURATION OF CONTROL SIGNALS FEED BACK TO OTHER CPS UNITS. NORMALLY THE FOLLOWING VOLTAGES ARE FEED BACK: TERMINAL 3, ABOUT -40 VOLTS; TERMINAL 10, ABOUT -13 VOLTS, TERMINALS 7 AND 8 OPEN CIRCUIT. WHEN THE TIMER IS TRIGGERED TERMINAL 3 IS RETURNED TO -40 VOLTS THROUGH (R3), TERMINAL 10 GOES TO -30 VOLTS AND TERMINALS 7 AND 8 ARE CONNECTED TO -22 VOLTS. TERMINALS 6, 7 AND 8 FEED THE CPS3, 4 CHANNEL CIRCUITS. TERMINAL 10 SUPPLIES THE CPS 5 SIGNAL TIMER AND TERMINAL 3 SUPPLIES A CONSTANT -40 VOLTS TO CPS 2. NEGATIVE 22 VOLTS IS SUPPLIED TO CPS 5 BY CPS 5. THE MONOPULSER CIRCUIT CONSISTS OF (Q1) AND (Q2) AND THEIR ASSOCIATED CIRCUITRY. ZENER DIODES (CR2) AND (CR3) AND (R2) PROVIDE AN EMITTER BIAS OF ABOUT -14 VOLTS. (Q2) IS NORMALLY HELD ON THROUGH (CR4) AND (R13) AND (Q1) OFF THROUGH (R14) AND (R1). A POSITIVE GOING VOLTAGE ON TERMINAL 9 FROM CPS 5 IS DIFFERENTIATED BY (C1) AND (R10) AND A PULSE OF CURRENT IS APPLIED TO THE COLLECTOR OF (Q1) THROUGH (CR1). THIS PULSE IS COUPLED THROUGH (C2) TO THE BASE OF (Q2) TURNING IT OFF. THE ACCOMPANYING RISE IN THE COLLECTOR VOLTAGE OF (Q2) DRIVES (Q1) ON THROUGH (R14) AND THE COLLECTOR VOLTAGE OF (Q1) RISES, SIMILARLY THE BASE VOLTAGE OF (Q2) THUS HOLDING (Q2) OFF AND (Q1) ON. AT THIS POINT THE VOLTAGE AT THE INTERSECTION OF (C2) AND (R13) IS DRIVEN ABOUT 30 VOLTS ABOVE THE EMITTER VOLTAGE OF (Q2) AND ITS STARTS TO DROP EXPONENTIALLY WITH A TIME CONSTANT DETERMINED BY (R13) AND (C2). IN ABOUT 45 MILLISECOND THIS VOLTAGE HAS DROPPED SUFFICIENTLY TO CAUSE (CR4) TO CONDUCT AND (Q2) TURNS ON TURNING (Q1) OFF AND THE CIRCUIT RESTORES TO NORMAL, WITH THE COLLECTOR VOLTAGE OF (Q1) DROPPING TO -45 VOLTS WITH A TIME CONSTANT DETERMINED BY (R9), (R11), (R12) AND (C2). CAPACITOR (C4) PREVENTS FALSE TRIGGERING BY POWER SUPPLY TRANSIENTS. ZENER DIODE (CR6) IN COMBINATION WITH (R6) ACTS A VOLTAGE REGULATOR TO HOLD TERMINAL 3 ABOUT 3 VOLTS ABOVE THE -48 VOLT SUPPLY. IN THE NORMAL STATE WITH (Q2) ON, ZENER DIODE (CR5) CONDUCTS IN THE REVERSE DIRECTION AND HOLDS (Q5) ON THROUGH (R5). THIS CLAMPS TERMINAL 6 TO THE -40 VOLT SUPPLY. (Q3) AND (Q4) ARE BOTH HELD OFF AT THIS TIME. WHEN THE CIRCUIT IS TRIGGERED AND (Q2) TURNS OFF ITS COLLECTOR VOLTAGE DROPS TO ABOUT -30 VOLTS CAUSING CONDUCTION TO STOP IN (CR5) AND (Q5) TURNS OFF, THUS INSERTING (750 OHMS) (R8) IN SERIES WITH THE -40 VOLT SUPPLY TO TERMINAL 6. (R7) AND (C5) REDUCE SWITCHING TRANSIENTS ON TERMINAL 6. AT THIS TIME (Q3) AND (Q4) ARE TURNED ON THROUGH (R17) AND (R18) AND TERMINALS 7 AND 8 ARE CLAMPED TO -22 VOLTS. AT THE END OF THE MONOPULSER TIMING PERIOD (Q3), (Q4) AND (Q5) RETURN TO THEIR NORMAL STATE AS THE COLLECTOR POTENTIAL OF (Q2) RISES TO -14 VOLTS. (R3) AND (R4) ABSORB LEAKAGE CURRENT FROM (Q2) WHEN IT IS OFF. TEST POINTS ARE PROVIDED AT THE TRIGGERING INPUT (STR), TERMINAL 3 CONTROL OUTPUT AND -43 VOLTS.

SD-98148-01-B16

EXTRA 71

H

G

F

E

D

C

B

A

12

G

F

E

D

C

B

A

ISSUE	NO.
1	1
2D	1
3A	1
4B	1
5B	1
6D	1
10B	1
12D	1

COMMON SYSTEMS "TOUCH-TONE" CALLING RECEIVING CIRCUIT TYPE A3	SD-98148-01-B16
BELL TELEPHONE LABORATORIES INCORPORATED	65

-APP FIG. 1

CIRCUIT PACKAGES			
	DESIG	LOC	CODE
	CPS 1	1C1	B1
	CPS 2	1C3	B2
	CPS 3A	1A4	B3
	CPS 3B	1C4	B4
	CPS 3C	1F4	B5
(Z)	CPS 3D	1G4	B6
(Y)	CPS 4	1G4	B7
(X)	CPS 5	1D6	B8
(W)	CPS 5	1D6	B19
	CPS 6	1D7	B9

CONNECTOR

01 02 03
 04 05 06
 07 08 09
 10 11 12
 13 14 15
 16 17 18
 19 20 21

DESIG	F
CODE	Ⓟ KS-14671 L1 Ⓢ KS-14671 L3 RALE
OPTION	LOC
1	1G0
2	1F0
3	1F0
4	1G0
5	1A0
6	1A0
7	1C0
8	1C0
9	1C0
10	1C0
11	1E0
12	1C0
13	1C0
14	
15	1D0
16	
17	
18	
19	
20	
21	

DIODE

DESIG
CR1

LOC

CODE
J 425H
H 485H

FILTER

DESIG
BEF

LOC

<u>LOC</u>	<u>CODE</u>
1C2	632A

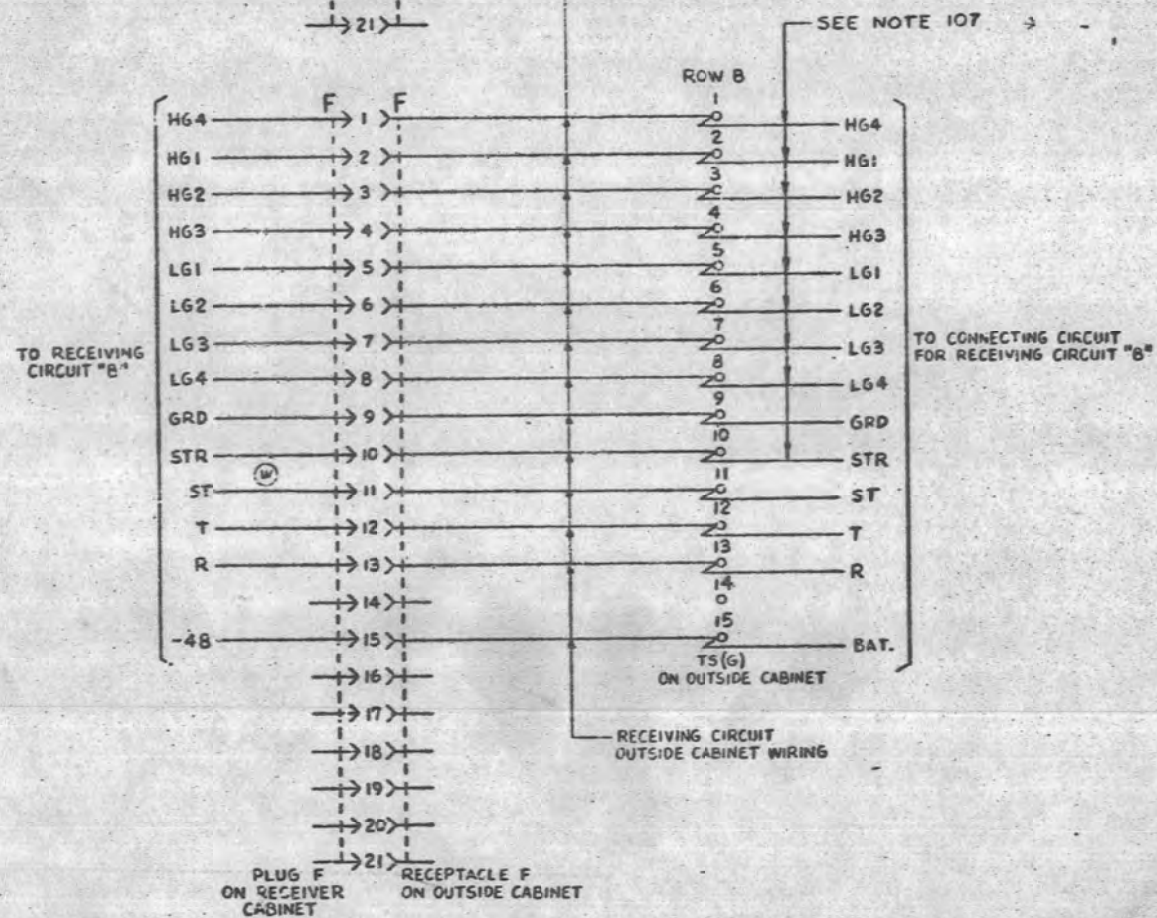
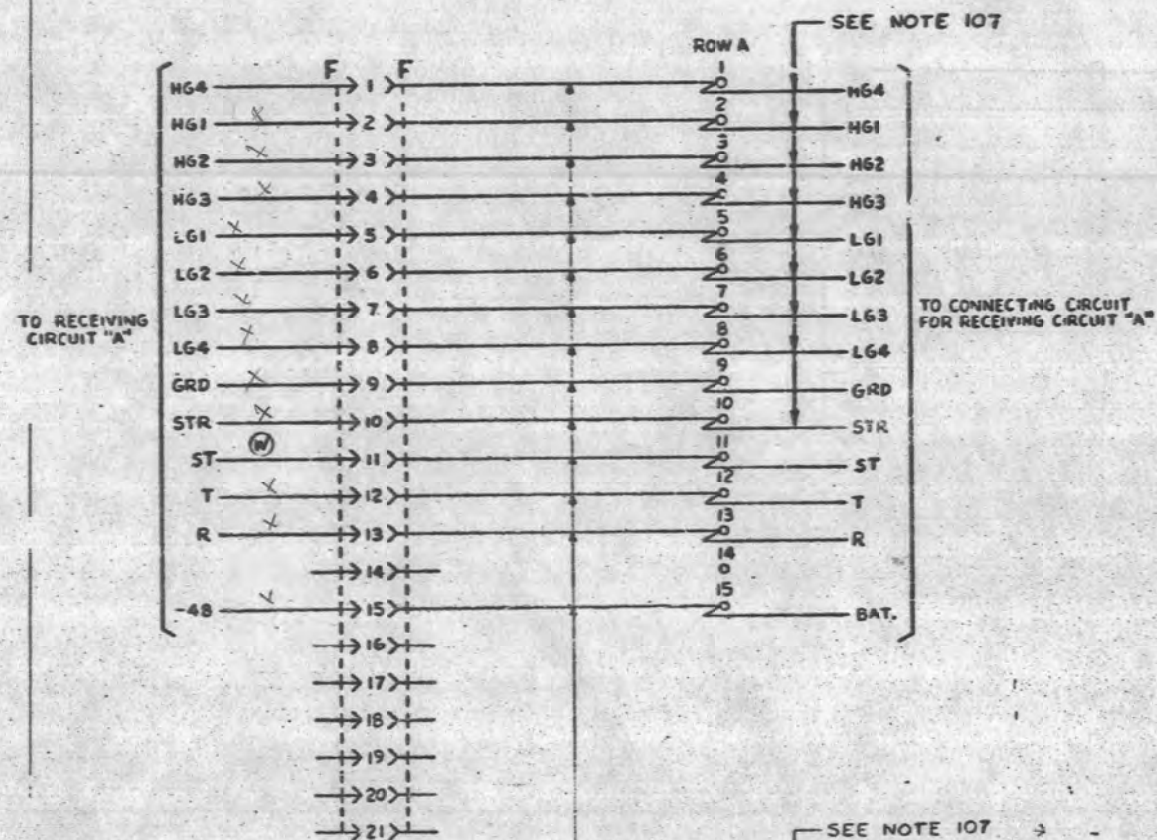
—APP FIG. 2

CONNECTOR

03 02 01
06 05 04
09 08 07
012 011 010
015 014 013
018 017 016
021 020 019

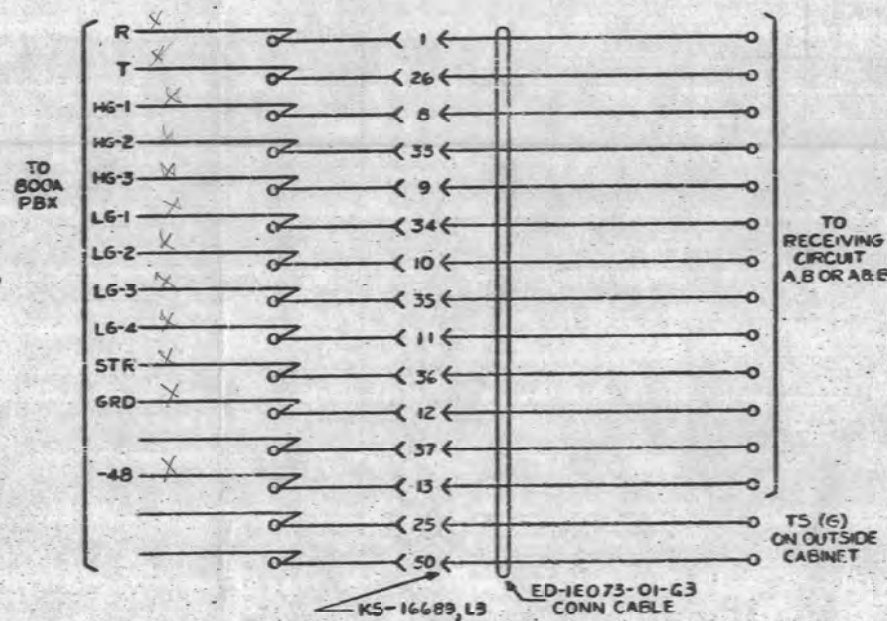
DESIG	F
CODE	KS-14672 L1 KS-14672 L3 FEMALE
OPTION	LOC
1	1F8
2	1F8
3	1F8
4	1G8
5	1A8
6	1A8
7	1C8
8	1C8
9	1C0
10	1C8
11	1E8
12	1C0
13	1C0
14	
15	1D0
16	
17	
18	
19	
20	
21	

CAD. 1



CAD. 2

FOR 800A PBX APPLICATION
ROW A, ROW B OR ROW A&B



1	FC
20	RT
48	MB
58	MB
75	MB