
# Datapath Network Interface Developer Guide

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Datapath Technology
Licensing
Program

Datapath
Network
Interface

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# 1. OBJECTIVES

This document is intended to describe in detail the components of the Datapath Network Interface (DNI) as an aid to the Terminating Equipment (TE) developer. The interworking of these components with each other is described, as well as their functions in the CPE Vendor's TE, for proper interworking with the Data Line Card (DLC) in the DMS switch. The Appendices contain the detailed specification sheets of each component.

## 2. BACKGROUND

Datapath is the name of Northern Telecom's switched data product. It uses a combination of special Customer Premises Equipment (CPE) called Terminating Equipment (TE) and a special Data Line Card (DLC) in the DMS-100 digital switch to provide end to end digital data service up to 64 Kbps.

The Datapath Technology Licensing (DTL) program has been undertaken to assist TE vendors to implement Datapath Terminating Equipment and to shorten the vendor's development cycle.

Overall, the DTL program provides documentation and components for two major functions of the Datapath TE, namely:
a) the T-Link Rate Adaption Protocol, and
b) the Datapath Network Interface.

The Network Interface is unique for the switch to which the TE is attached. In the Datapath products, this interface uses Alternate Mark Inversion (AMI) modulation and Time Compression Multiplexing (TCM) to achieve full duplex operation.

# 3. GENERAL

The DNI Building Blocks consist of

1) the TCM Large Scale Integrated Circuit (Part No. QMV98C)

2) the Loop Hybrid (Part No. QMS91B)

3) the Loop Transformer (Part No. QTK260A6).

The DNI Building Blocks are shown in a black box representation (Fig. 3-1). The Loop Interface (I/F) is at the right, the Serial Data Interface at the left and the Call Control Interface at the bottom.

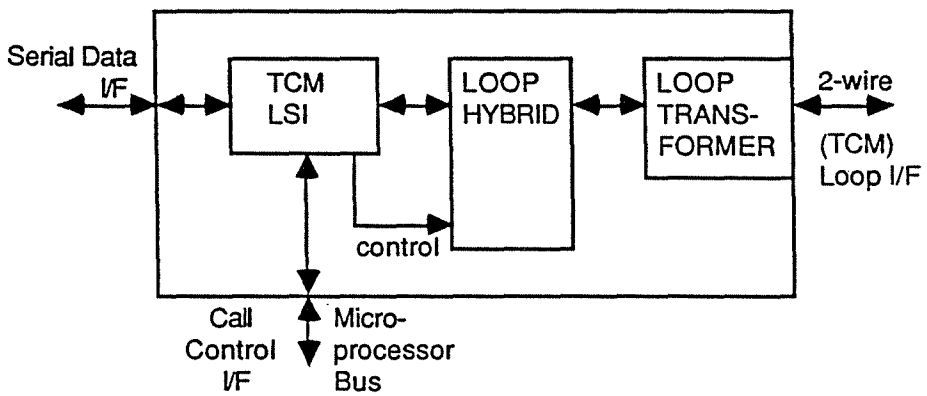



Figure 3-1. DNI Building Blocks

Full duplex data transmission is achieved using Time Compression Multiplexing (TCM) with the Loop Interface circuit in either transmit mode or receive mode at any time. TCM utilizes a frame rate of 1 millisecond. During each frame, 64 bits of subscriber data, 8 bits of supervision and control signals and 2 framing bits are exchanged in each direction. The line transmission rate is 160 Kbps (Ref. 1).

The 2-wire loop is connected to the Loop Transformer which provides the functions of line isolation and impedance matching. This is connected to the Loop Hybrid which does loop equalization and changes Alternate Mark Inversion (AMI) signals from/to the loop transformer to unipolar signals to/from the TCM LSI. The latter (QMV98C) provides some control of the Loop Hybrid for purposes of loop equalization, i.e. to indicate to the Loop Hybrid in which way to compensate for the loop characteristics.

The QMV98C also handles the TCM protocol. To interface to the T-Link Building Block portion of the TE, the QMV98C provides a serial 64Kbps Data channel and a parallel Microprocessor Bus Interface for the Call Control channel.

The following sections describe these components in greater detail, specify the interfaces and provide operational information to the developer.The Appendices provide detailed data (specification) sheets and schematics for the interconnection of the devices.This will allow the developer to integrate the building blocks into a TE design.

## 3.1 Progress Tones Converter

Although not considered part of the DNI building blocks, for purposes of completion, a brief note on the progress tones converter follows.
TEs designed for manual calling require a PCM Decoder to convert PCM encoded progress tones, sent from the switch to the TE, into audio tones. The µLaw PCM encoded tones (e.g. dial tone, busy, reorder, etc) are sent from the switch via the 64 Kbps channel on TCM. In the TE the audio tones are used to drive an acoustic device (e.g. a speaker) to make them audible to the user. The design of the DAC, as well as the acoustic device and keypad, are left for the developer to decide.

## 4. QMV98C TCM LSI

The QMV98C (Fig. 4-1) provides the following functions:

1) Scrambles/descrambles the bits in the Time Compression Multiplex (TCM) frame.

2) Handles the TCM protocol and the framing/deframing of the data and signaling information.

3) Maintains phase-locked loop synchronization with the network.

4) Controls the bridge tap equalizer circuit in the Loop Hybrid.

5) Provides a 64 Kbps serial data channel and the interrupts and clocking for that channel.

6) Provides a parallel Microprocessor bus interface (with interrupt) used to control the QMV98C and to pass the call control channel information.

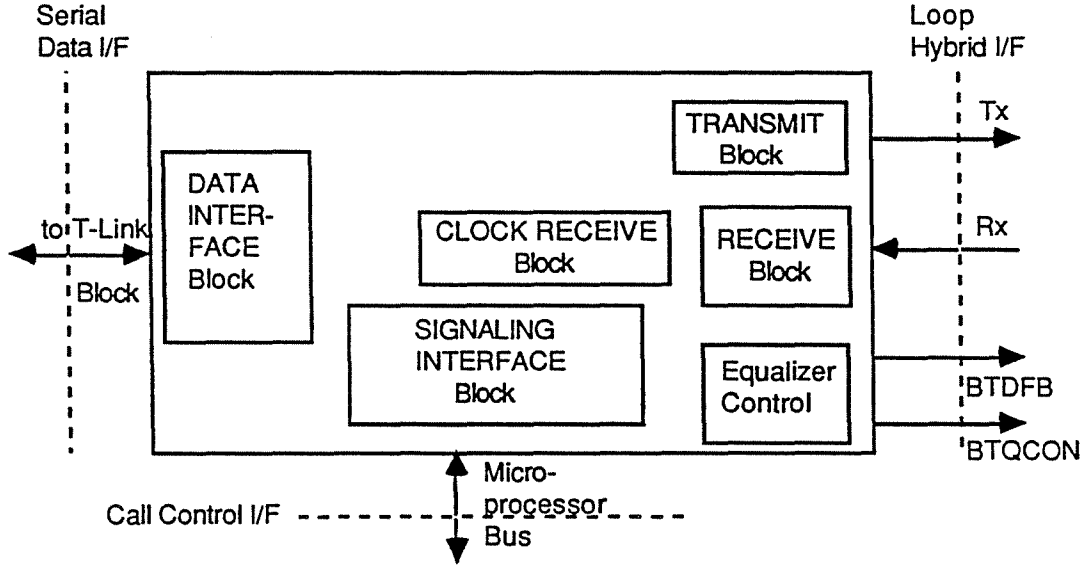



Figure 4-1. QMV98C Block Diagram

Appendix A fully describes the QMV98C specification aspects, i.e.
- Pin Assignments and Functions
- Package Dimensions
- Connection Diagram
- DC Characteristics And Absolute Ratings
- Pin Characteristics
- Waveforms for the Network, Loop, Clock and µProcessor interfaces
- Bit Timing Diagrams for the 64 Kbps Network Interface.

## 4.1 Loop Hybrid Interface

At the Loop Hybrid interface, unipolar signals are transmitted and received by the QMV98C to/from the Loop Hybrid circuit. The QMV98C also provides control for the automatic equalizer circuits in the Loop Hybrid.
The Bridged-Tap equalizer control output current source BTQCON charges or discharges a capacitor, whose voltage controls the equalizer circuit. The Bridged-Tap equalizer sense input signal BTZD (Appx A, Fig.3) acts as the feedback control for this circuit.
The Echo Compensation (decision feedback) output signal BTDFB provides current drive for a second-order decision feedback circuit in the Loop Hybrid (QMS91B; Appx B).

## 4.2 64Kbps Serial Data Interface

Referring to Appx A, Fig 3, this interface passes data at a rate determined by the "64 Kbps interface" input clock. The actual clock rate is 2.56 Mbps.
The data transfer is indicated and bounded by the ENin signal from the QMV98C. When ENin is attached to ENout, it allows 8 bits of data to be transfered in both directions simultaneously using the Lbus (transmitted) and Rbus (received) signals.

## 4.3 Call Control Interface

The Call Control interface is a Microprocessor bus interface and is used for the following functions:

1) Control/status of the QMV98C

2) Passing of call control channel data

3) Maintenance control/status

4) Testing control/indications.

## 5. LOOP HYBRID

The Loop Hybrid (NT part No. QMS91B; Appx B) is currently a thick film hybrid circuit used in the TE and DLC Loop Interface to provide high speed data over a non-loaded 2-wire loop.
The hybrid, together with the QMV98C, compensates for the following limitations of the loop:
1) frequency dependent amplitude distortion
2) effects of bridged tap reflections
3) crosstalk
4) impulse and random noise.

The Loop Hybrid allows data transmission over any mix of 22, 24, and 26 gauge 2-wire metallic loop up to 5.4 Km and a maximum loss of 45 db at 80 KHz.
The Loop Hybrid Block Diagram is shown in Fig. 5-1; a functional description follows.

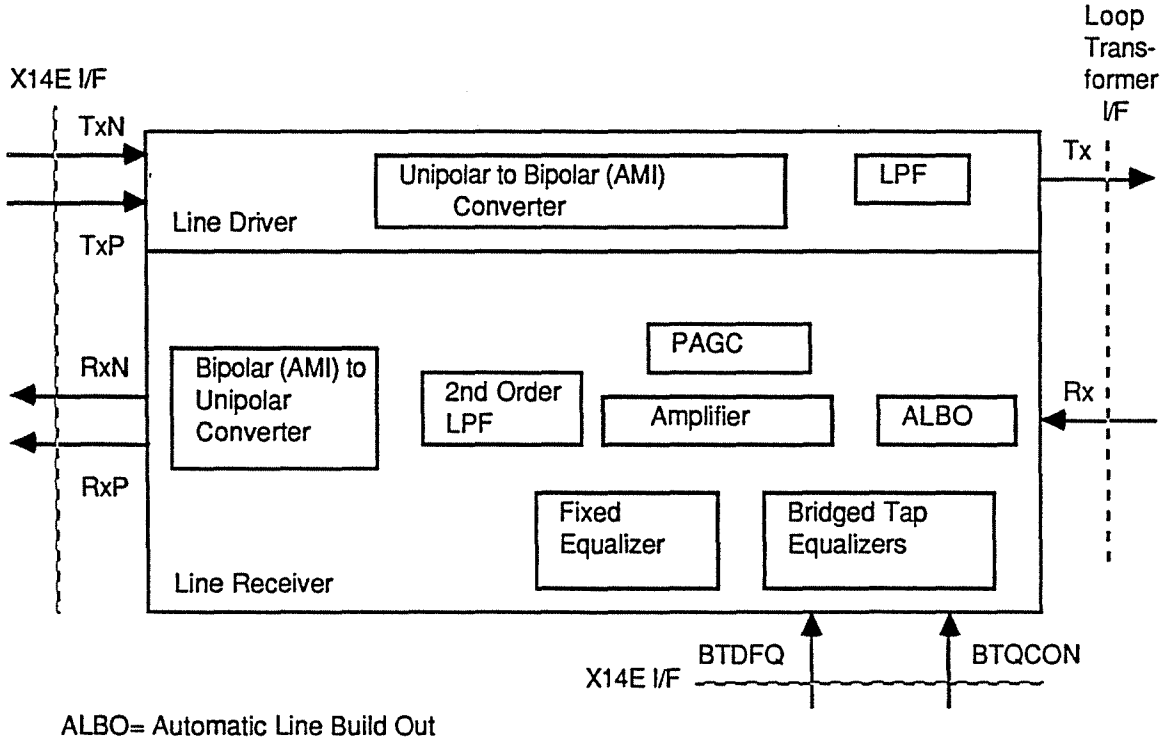



Figure 5-1 Loop Hybrid Block Diagram

## 5.1 Functional Description

LINE DRIVER

The purpose of the line driver is to convert the unipolar, TTL level drive signals (TxN & TxP) into an AMI (bipolar return to zero) 50% modulation signal for transmission.
To reduce crosstalk, the bipolar signal is modified by a Low Pass Filter (LPF) with a corner frequency of approximately 260 KHz.
The input of the operational amplifier is differentially fed and the output is from a push-pull stage. A dual series silicon diode pair ensures the correct biasing levels for the amplifiers.

LINE RECEIVER

The receiver section comprises several sub-circuit blocks (Fig. 5-1).

a) A.L.B.O., Amplifier and P.A.G.C.

The Automatic Line Build Out circuit simulates cable loss so that all loops (irrespective of loop length) appear as a 45 dB loop to the amplifier.

The amplifier is essentially a non-inverting circuit whose gain is controlled by the P.A.G.C. The DC operating point is set by the Vct input voltage generated from a voltage division chain in the bipolar to unipolar circuit.

The gain of the Partial Automatic Gain Control varies as a function of the current generated by the current source in the bipolar to unipolar converter circuit.

b) Fixed Equalizer

The fixed equalizer circuit counteracts the effects of the frequency dependent losses of a metallic loop by introducing a peak gain of approximately 45 dB at 80 KHz. The op amp operating point is set by

the Vct voltage and the output swing is limited by a series diode pair.

A Second-order Low Pass Filter with a 40 dB/decade sharp roll off is used to improve noise immunity.

c) Bridged Tap Equalizers

Data transmission over a two-wire metallic loop at a line rate of 160 Kbps may be severely degraded due to the presence of bridged taps. Bridged taps can result in the reduction in the signal to noise ratio. To compensate for this, a 2-bit bridged tap equalizer has been implemented within the line receiver. The control logic for this circuit is in the QMV96C. Within this equalizer, a correction signal is summed with the recovery data stream. The amplitude and shape of the signal is equal to the amplitude and shape of the signal produced by a bridged tap reflection.

d) Bipolar To Unipolar Converter

In the Bipolar to Unipolar Converter, the bipolar signals from the bridged tap equalizer are converted into unipolar pulses which are sent to the QMV98C.
The ALBO and PAGC control current is also generated here.

# 6. OPERATION

Although Reference 1 contains the Datapath protocol information for normal operation of the Terminating Equipment (TE), it does not include all protocol/timing details for start-up conditions. The following section on the Datapath TE - DLC start-up signalling protocol will complete the specification information.

## 6.1 TE- DLC Start-up Signalling

TCM synchronization needs to be established under the following conditions:

a) when TE power is turned on,

b) when the TE is reset,

c) after the loop has been disconnected and reconnected.

TCM synchronization is established by the QMV98C chips, the "master" being on the Data Line Card (DLC) in the DMS switch and the "slave" being in the TE. The length of time required to gain loop synchronization depends on the quality of the loop. During power-up (TE or DLC), or after the loop has been disconnected, it takes typically between 1 to 3 seconds. For some loop conditions, it might take longer to find synchronization.

### 6.1.1 Software Determining Sync

The TE and the DLC must first find TCM synchronization. This is done by the QMV98C finding the start/stop bits in the receive window. The synchronization occurs in stages:

1) First, the DLC looks for a "sync flag" for 128 milliseconds. If the sync flag changes during the 128 ms timer, the timer re-starts.

2) Next, the DLC begins the FDHP Sync Message Handshake (80 24) expressed in HEXidecimal, i.e. Address 8, Info 0, Command 24 (see Fig. 6-1 and 6-2); note that this command is not shown in the FDHP command list Tables in Ref.1.
The DLC will keep sending (80 24) continuously until thirty-two "FDHP PACKs" are received from the TE (Fig. 6-3).

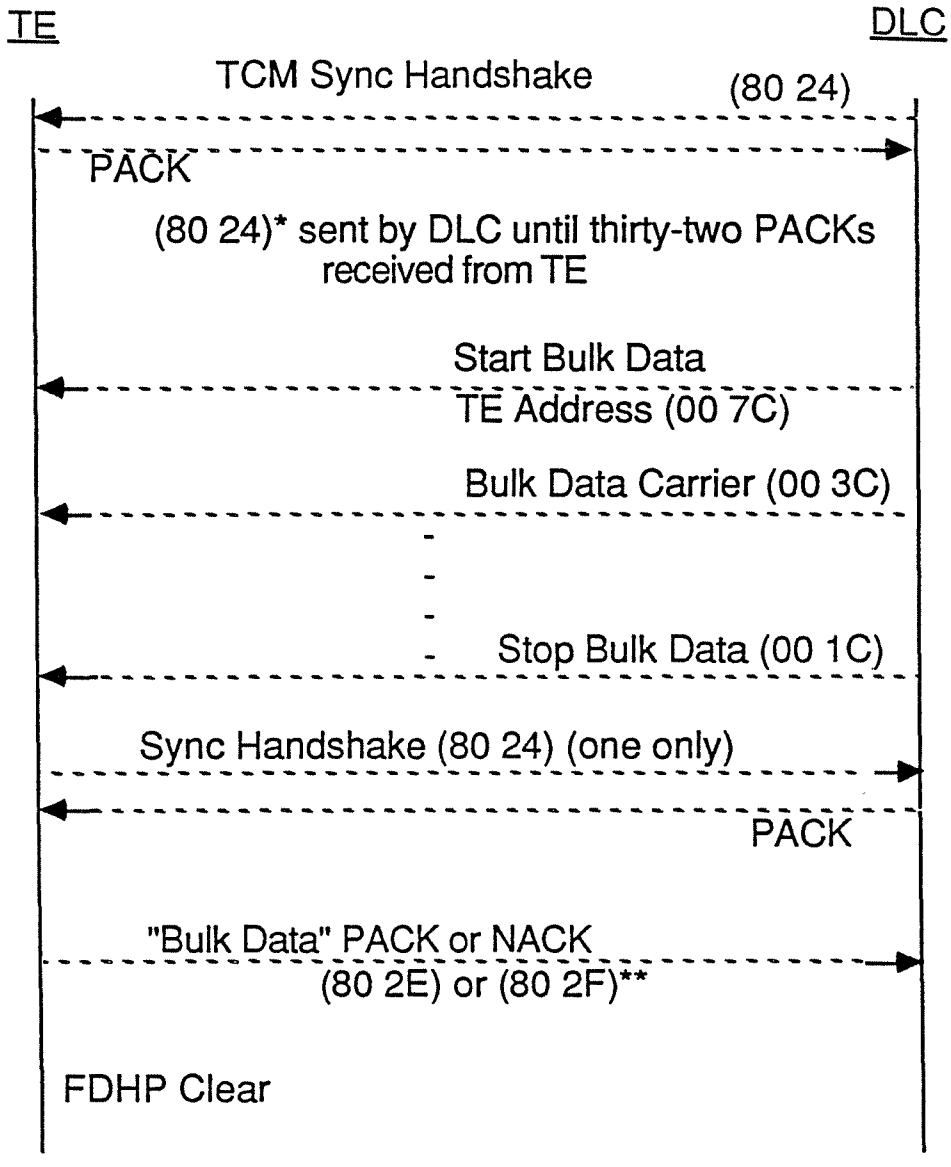
| Description | FDHP Message Format | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Transmitter | | | | | | | | | | | Receiver | | | | | | | |
| | FDHP BYTE | | | | | | | | | | FDHP BYTE | | | | | | | | |
| Transmit State | Tx S1 | Tx S0 | Rx S1 | Rx S0 | D3 | D2 | D1 | D0 | | | Tx S1 | Tx S0 | Rx S1 | Rx S0 | D3 | D2 | D1 | D0 | Receive State |
| | | | | | --NIBBLE-- | | | | | | | | | | | | | | |
| IDLE | 0 | 0 | | | | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 1 | | | | | CTS |
| CHO | 0 | 1 | | | ADDRESS | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 1 | | | | | CTS |
| CHO | 0 | 1 | | | INFO | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 1 | | | | | CTS |
| CHO | 0 | 1 | | | COM- | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 1 | | | | | CTS |
| CHO | 0 | 1 | | | MAND | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 1 | | | | | CTS |
| RACK | 1 | 0 | | | CHECKSUM | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 0 | | | | | PACK* |
| RACK | 1 | 0 | | | CHECKSUM | | | | → | | | | | | | | | | |
| | | | | | | | | | ← | | | | 1 | 0 | | | | | PACK |
| IDLE | 0 | 0 | | | | | | | → | | | | | | | | | | |
| | | | | | | | | | | | *or | 0 | 0 | | | | | | NACK |

Figure 6-1. FDHP Message Format

| Description | DLC → TE ; Sync Message Handshake (80 24) |
|---|---|

| Transmitter (DLC) | | | | | | | | | | | Receiver (TE) | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FDHP BYTE | | | | | | | | | | FDHP BYTE | | | | | | | | | |
| Transmit State | Tx S1 | Tx S0 | Rx S1 | Rx S0 | D3 | D2 | D1 | D0 | | | Tx S1 | Tx S0 | Rx S1 | Rx S0 | D3 | D2 | D1 | D0 | Receive State |
| IDLE | 0 | 0 | X | X | X | X | X | X | → | | | | | | | | | | | |
| | | | | | | | | | ← | | X | X | 1 | 1 | X | X | X | X | CTS |
| CHO | 0 | 1 | X | X | 1 | 0 | 0 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | CTS | |
| CHO | 0 | 1 | X | X | 0 | 0 | 0 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | CTS | |
| CHO | 0 | 1 | X | X | 0 | 0 | 1 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | CTS | |
| CHO | 0 | 1 | X | X | 0 | 1 | 0 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | CTS | |
| RACK | 1 | 0 | X | X | 1 | 1 | 1 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | X | X | 1 | 0 | X | X | X | X | PACK* | |
| RACK | 1 | 0 | X | X | 1 | 1 | 1 | 0 | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | PACK | |
| IDLE | 0 | 0 | X | X | X | X | X | X | → | | | | | | | | | | | |
| | | | | | | | | | ← | | | | | | | | | | CTS | |
| | | | | | | | | | | | *or | | | | | | | | | |
| | | | | | | | | | | | X | X | 0 | 0 | X | X | X | X | NACK | |

Figure 6-2. FDHP Sync Message




* (80 24) FDHP message, where ADDRESS=8,INFO=0, COMMAND=24 are expressed in HEXidecimal notation.
** 80=ADDRESS & INFO, 2E=(Bulk Data)PACK, 2F= (Bulk Data)NACK, expressed in HEX.

Figure 6-3. Sync Sequence & "Bulk Data" Transfer

3) Then the DLC sends the "bulk data" (Ref. 1) to the TE. A TE that is not down-loadable should recognize this bulk data for what it is and ignore it. The DLC now enables its FDHP receiver, which was continuously sending NACKs (i.e. ignoring any message from the TE) up to this point.

4) Two messages should be received by the DLC (i.e. sent by the TE) at this point:
a) The DLC receives and acknowledges the sync handshake message being transmitted by the TE (80 24) (Fig. 6-3). This establishes sync for the TE and the sync indicator should turn on.
b) The TE transmits a "Bulk Data" PACK (80 2E) to acknowledge the "bulk data" download. A TE which does not support a "bulk data" download can either NACK (80 2F) or not send any response. The DLC sends the "bulk data" download only once.

5) The TE and DLC now have TCM/Messaging synchronization. The FDHP messaging is operational and the data channel is available.

To recapitulate, start-up messages from the TE to the DLC include:
1) Sync handshake message 80 24
2) "Bulk data" PACK 80 2E
3) "Bulk data" NACK 80 2F.

The 80 address is sent to the TE only when the DLC is sending the TE "bulk data" after finding TCM sync. Ordinarily, the message would come from the DLC to the DU with 00 address, as for CO to TE FDHP commands in Tables of Ref.1.

### 6.1.2 DLC FDHP Receive/Transmit

The FDHP protocol, commands, messages, etc are described in Ref.1. Following are some notes on implementation details.

Notes on DLC FDHP Receive

a) The TE should never send the unused code 11 in the Tx state, because the DLC would return NACKs until an IDLE (00) is received.

b) Once the DLC is in the NACK receive state, only the TE Tx IDLE (00) will get the DLC back to CTS state. Therefore, a message from the TE can only be retransmitted by first going back to IDLE.

Notes on DLC FDHP Transmit

TE PACK/NACK messages to the DLC are only with respect to the FDHP, i.e.

a) PACK should always be sent if the format (checksum) is received correctly, even if the TE does not support the command in the message.

b) NACK must be sent from the TE only if there is an error in the format (checksum) or the TE is not ready to receive.

To reiterate, if the DLC sends a message which the TE does not support, but was received with the correct format, then the TE must PACK this message when the RACK is received.

TE to Switch Messages

a) The DLC sends NACKs if it is not ready to receive messages. This can occur if the DLC buffer to the Central Control (CC) is full.

b) The TE must send messages to the DLC at a rate no faster than one new message every 130 milliseconds.

Switch To TE Messages

a) The maximum Switch to TE message rate is one new message every 27 milliseconds. If the DLC does not receive a PACK, the DLC will keep trying to send the message for 128 milliseconds. After this time, the message is discarded.

b) Messages to the TE, received during a "bulk data" download , will be interleaved with messages comprizing the download sequence. Priority is given to the outgoing messages to the TE.

To reiterate, Figure 6-3 shows the total messaging required between the DLC and the TE during the sync sequence. This assumes that the DLC has valid "bulk data" to send and is downloading it in the process.

## 7. REFERENCES

1. "Datapath Service Interface Specification", Northern Telecom, NIS S204-2, October, 1986.

2. "Datapath Building Blocks - Overview", Northern Telecom Doc. #TL87-0003-01, PRELIMINARY, March, 1987.

# Appendix A

QMV98C TCM - LSI Spec Sheet

# QMV98C TCM-LSI Data Sheets

## General Description

The QMV98C is an LSI device designed to provide access and control of data over a 2-wire loop using Time Compression Multiplexing (TCM) technology. It provides a transparent, full-duplex, 64 kb/s channel for data transmission, together with an 8 kb/s signalling channel over a single 2-wire loop. The QMV98C also provides control of off-chip line equalizer circuits. Minimal loop interfacing requirements consist of a hybrid thickfilm line equalization circuit (QMS91B) and a coupling transformer (QTK260A6).

## Features

- 160 kb/s TCM loop interface
- Control of an off-chip line equalizer circuit
- 64 kb/s interface supporting a digital serial bus
- parallel microprocessor interface for signalling and control
- 16 internal registers for programming and control status (7 are utilized)
- packaged as 44-pin CQUAD or 68-pin PGA
- 8 kb/s signalling channel for call processing in circuit switched data applications

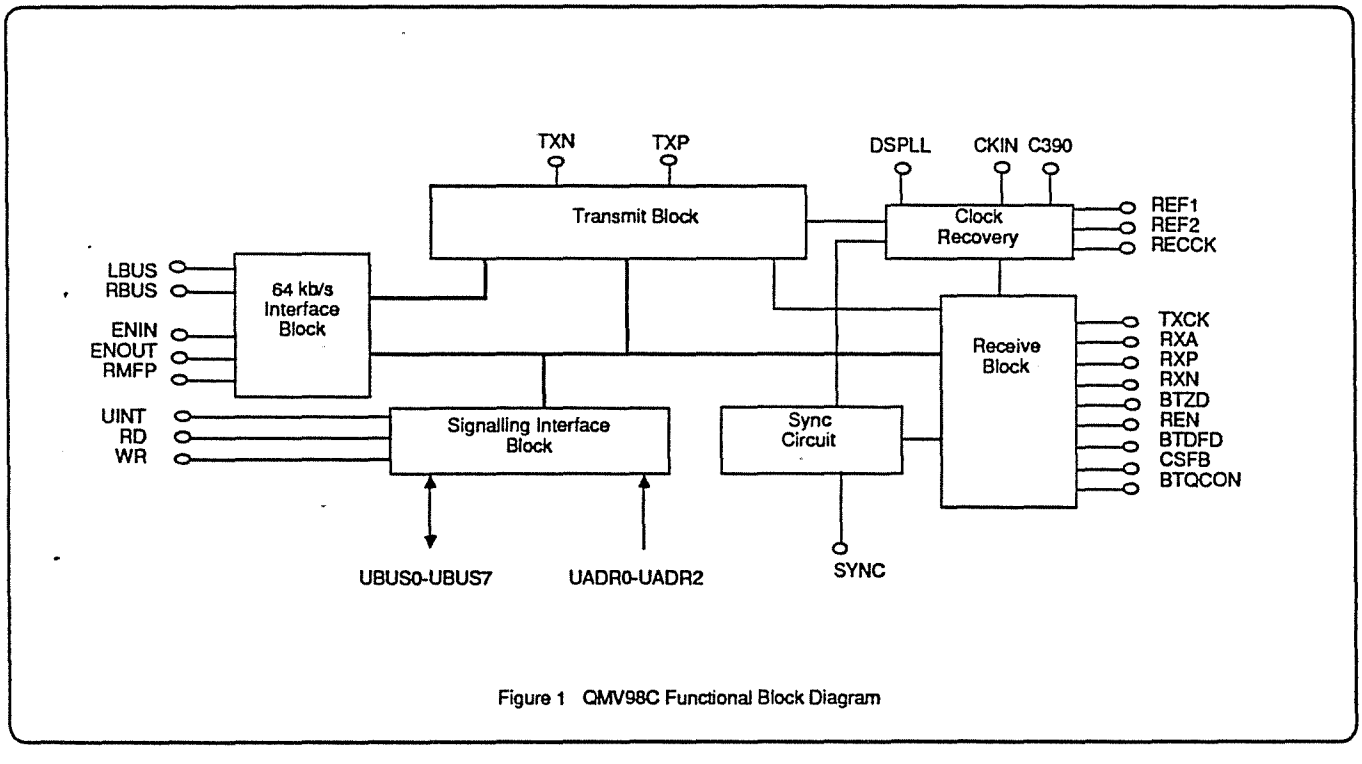



Figure 1 QMV98C Functional Block Diagram

## Table A - Pin Assignments And Functions

| Pin | | | | | Function |
|---|---|---|---|---|---|
| Label | CQUAD No. | PGA No. | Type | Input/ Output | |
| VSS | 24 | 44 | | | General ground connection. Ground return for DC power supply VDD. |
| VDD | 1 | 9 | | | Positive voltage supply. ( +5.0 V ±10% ) |
| REF1 | 30 | 56 | C | I | **CRYSTAL I/O PINS:** REF1 and REF2 provide an external connection for a 10.24 MHz, parallel mode crystal. |
| REF2 | 31 | 57 | C | O | |
| CKIN | 26 | 46 | T | I | **CLOCK IN:** 64 kb/s interface input clock for synchronization of serial data transactions. Connect directly to C390 (pin 27). |
| C390 | 27 | 47 | T | O | 2.56 MHz output clock used to sychronize the 64 kb/s serial data transactions. Connected directly to CKIN (pin 26), this output satisfies the 64 kb/s timing requirements (see Figure 9). |
| TXCK | 43 | 7 | T | O | **TRANSMIT CLOCK:** 160 KHz, TCM loop data transmit clock. Used for internal timing and synchronization of TCM frame. Pin provides external reference only, leave unconnected. |
| RECCK | 39 | 65 | T | O | **RECOVERED CLOCK:** Recovered 160 KHz clock from received TCM loop data. Provided for reference only, leave unconnected. |
| RMFP | 40 | 3 | T | O | **RECOVERED 1 msec FRAME PULSE:** Recovered TCM frame indicator (active low) used for internal synchronization of the 160 kb/s TCM frame transmit data. |
| SYNC | 42 | 6 | T | O | System "sync" indicator (0 = out of sunc; 1 = in sync). This output indicates the status of the TCM loop transactions. |
| RD | 18 | 37 | T | I | **READ:** Parallel data read pulse (active low). A low on this input enables data transfer out of an internal register as selected by address lines (UADR0-2). Data is 8-bit parallel, available on data bus (UBUS). (see Figures 7 & 8 for Read/Write timing diagrams) |
| WR | 19 | 39 | T | I | **WRITE:** Parallel data write pulse (active low). A low on this input enables data transfer into one of the internal registers as selected by address lines (UADR0-2). Data is 8-bit parallel, available on UBUS. |
| LBUS | 6 | 14 | T | O | 64 kb/s, serial output data bus. Synchronization of 64 kb/s data (LBUS & RBUS) is accomplished by gating the data with the ENOUT output. |
| RBUS | 9 | 23 | T | I | 64 kb/s, serial input data bus. |
| BTZD | 28 | 48 | C | I | Bridged-Tap equalizer sense input (from QMS91B). |
| BTQCON | 38 | 64 | S | O | Bridged-Tap equalizer control output " |
| BTDFB | 37 | 63 | S | O | Echo compensation (decision feedback). |
| CSFB | 36 | 62 | S | I | Precision resistor input for BT current sources. |

## Table A - Pin Assignments And Functions (Continued)

| Pin | | | | | Function |
|---|---|---|---|---|---|
| Label | CQUAD No. | PGA No. | Type | Input/ Output | |
| UBUS0<br>UBUS1<br>UBUS2<br>UBUS3<br>UBUS4<br>UBUS5<br>UBUS6<br>UBUS7 | 14<br>15<br>16<br>17<br>20<br>21<br>22<br>23 | 28<br>29<br>30<br>31<br>40<br>41<br>42<br>43 | T<br>T<br>T<br>T<br>T<br>T<br>T<br>T | I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O<br>I/O | UBUS0 - UBUS7 comprise a microprocessor compatible, bidirectional, tristate data bus. Used with address bus (UADR), access to internal registers is gained. Provides access for status read/programming of the QMV98C.<br><br>In input mode when WR=0, RD=1;<br>In output mode when WR=1, RD=0. |
| UADR2<br>UADR1<br>UADR0 | 11<br>12<br>13 | 25<br>26<br>27 | T<br>T<br>T | I<br>I<br>I | Address bus for selecting the internal registers via the microprocessor data bus (UBUS). Refer to Table D for register addressing scheme. |
| UINT | 25 | 45 | T | O | Microprocessor compatible interrupt output. This is an active low output used to interrupt the controlling micro, requesting a signalling channel data transaction. |
| ENIN | 8 | 22 | T | I | **ENABLE INPUT:** An active low enable window used to gate the 8-bit serial data transactions of the LBUS and RBUS. Connect directly to ENOUT. (see to Figures 6 & 9 for 64 kb/s I/F timing) |
| ENOUT | 2 | 10 | T | O | **ENABLE OUTPUT:** Connected directly to ENIN (pin 8), this output satisfies the timing requirements of the 64 kb/s interface. (see Figures 6 & 9) |
| REN | 41 | 5 | T | O | **RECEIVE ENABLE:** Active high output to control the external line equalizer circuit by enabling equalization only during the receive portion of the TCM frame. Connect directly to REN (pin 34) of the QMS91B, external line equalizer circuit. |
| RXP<br><br>RXN | 35<br><br>34 | 61<br><br>60 | C<br><br>C | I<br><br>I | An external bipolar to unipolar converter (contained in QMS91B) converts the analog, bipolar TCM loop data to unipolar signals RXP and RXN. These signals represent the positive and negative pulses of the loop data, respectively. The pulses are active low. (connect pins 34 & 35 of the QMV98C directly to pins 44 & 48 respectively of the QMS91B) |
| TXP<br><br>TXN | 4<br><br>3 | 12<br><br>11 | O<br><br>O | O<br><br>O | These outputs provide active high pulses to an external line driver circuit (QMS91B) which combines the unipolar pulses into a bipolar data stream. TXP & TXN are the positive and negative pulses respectively. Connect directly to TXN & TXP inputs of the QMS91B with 15 KΩ pull-ups to +5V. |
| RXA | 33 | 59 | T | O | Unipolar data output, active high. |
| DSPLL | 44 | 8 | C | I | Test pin; leave open circuit for normal operation. |

- Pin 5 (13 on PGA) should be tied to VDD through a 1.0 KΩ pull-up resistor.
- Pins 7 (20 on PGA), 10 (24 on PGA), 29 (54 on PGA) and 32 (58 on PGA) are no connects.
- All other PGA pins are no connect.

## Table B - DC Characteristics And Absolute Maximum Ratings

| Parameter | Minimum | Maximum | Units |
|---|---|---|---|
| DC Supply Voltage ($V_{dd}$) | +4.50 | +5.50 | Volts |
| DC Supply Current: | | | |
| Operating, no load | | 10.0 | mA |
| Quiescent, no load, no clock | | 2.0 | mA |
| $V_{dd}$-$V_{ss}$ | –0.5 | +7.0 | Volts |
| Voltage at any input pin | $V_{ss}$–0.5 | $V_{dd}$+0.5 | Volts |
| Current at any input pin | –1.0 | +1.0 | mA |
| Current at any output pin | –8.0 | +8.0 | mA |
| Operating temperature range | 0 | +70 | °C |
| Storage temperature range | –60 | +150 | °C |
| Power disssipation | | 400 | mW |

## Table C - Pin Characteristics

• Refer to Table A for pins applicable to each type.

| Pin Type | Parameter | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| **T Inputs** | Input Voltage low level ($V_{il}$) | –0.5 | +0.4 | +0.8 | Volts |
| | Input Voltage high level ($V_{ih}$) | +2.0 | +2.4 | $V_{dd}$+0.5 | Volts |
| | Input Current low level ($I_{il}$) | –14 | –40 | –100 | µA |
| | Input Current high level ($I_{ih}$) | | | ±10 | µA |
| **T Outputs** | Output Voltage low level ($V_{ol}$) | 0 | | +0.5 | Volts |
| | Output Voltage high level ($V_{oh}$) | 2.4 | | $V_{dd}$ | Volts |
| **C Inputs** | Input Voltage low level ($V_{il}$) | –0.5 | | +1.5 | Volts |
| | Input Current low level ($I_{il}$) | | | ±10 | µA |
| | Input Current high level ($I_{ih}$) | | | ±10 | µA |
| **C Outputs** | Output Voltage ($V_o$) | 0.4x$V_{dd}$ | 0.5x$V_{dd}$ | 0.6x$V_{dd}$ | Volts |
| (See Notes) | Output Current low level ($I_{ol}$) | | | | µA |
| | Output Current high level ($I_{oh}$) | | | | µA |
| **S Inputs** | Input Current ($I_i$) | -68 | -50 | -40 | µA |
| **S Outputs** | Output Current reference at BTQCON (Ior) | 40 | 50 | 65 | µA |
| | Output Current low level ($I_{ol}$) | +0.85x$I_{or}$ | +Ior | +1.15x$I_{or}$ | µA |
| | Output Current high level ($I_{oh}$) | –0.85x$I_{or}$ | –$I_{or}$ | –1.15x$I_{or}$ | µA |
| **O Outputs** | Output Voltage low level ($V_{ol}$) | 0 | | +0.5 | Volts |

**Notes:** 1. Measured with a 1MΩ resistor between Ref1 and Ref 2.
2. Use $I_{ol}$ and $I_{oh}$ to calculate the transconductance at Ref1 and Ref 2 (gm = ($I_{oh}$–$I_{ol}$)/($V_{oh}$–$V_{ol}$).
'C' - CMOS 'T' - TTL 'O' - Open Drain 'S' - Special Type (BTQCON & BTDFB only)

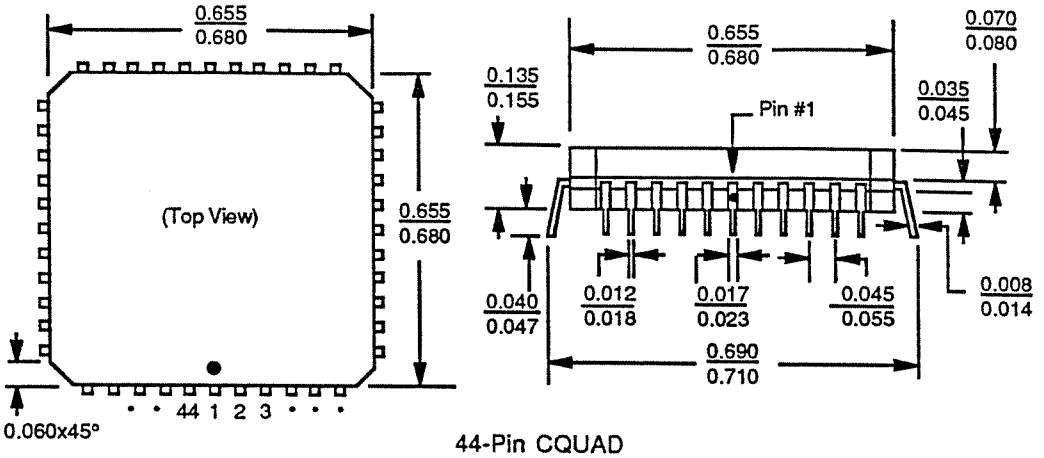
Table D QMV98C Register Addressing

| RD | WR | ADR (UADR2- UADR0) | | | DATA BUS (UBUS7..... UBUS0) | | | | | | | | COMMENTS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A2 | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0 | 1 | 0 | 0 | 0 | X | D6 | X | D4 | X | X | D1 | X | INTERRUPT STATUS REG. |
| 1 | 0 | 0 | 0 | 0 | X | X | X | D4 | X | X | D1 | X | WRITE INTERRUPT REG. |
| 0 | 1 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | RESERVED |
| 1 | 0 | 0 | 0 | 1 | X | X | X | X | X | X | X | X | RESERVED |
| 0 | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | RESERVED |
| 1 | 0 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | RESERVED |
| 0 | 1 | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | READ FDHP |
| 1 | 0 | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | WRITE FDHP |
| 0 | 1 | 1 | 0 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | BIPOLAR VIOLATION COUNTER READ |
| 1 | 0 | 1 | 0 | 0 | X | X | X | X | X | D2 | X | D0 | BIPOLAR VIOLATION COUNTER CONTROL |
| 0 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | RESERVED |
| 1 | 0 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | RESERVED |
| 0 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | RESERVED |
| 1 | 0 | 1 | 1 | 0 | X | X | X | X | X | X | D1 | D0 | LOOPBACK |
| X | X | 1 | 1 | 1 | X | X | X | X | X | X | X | X | RESERVED |

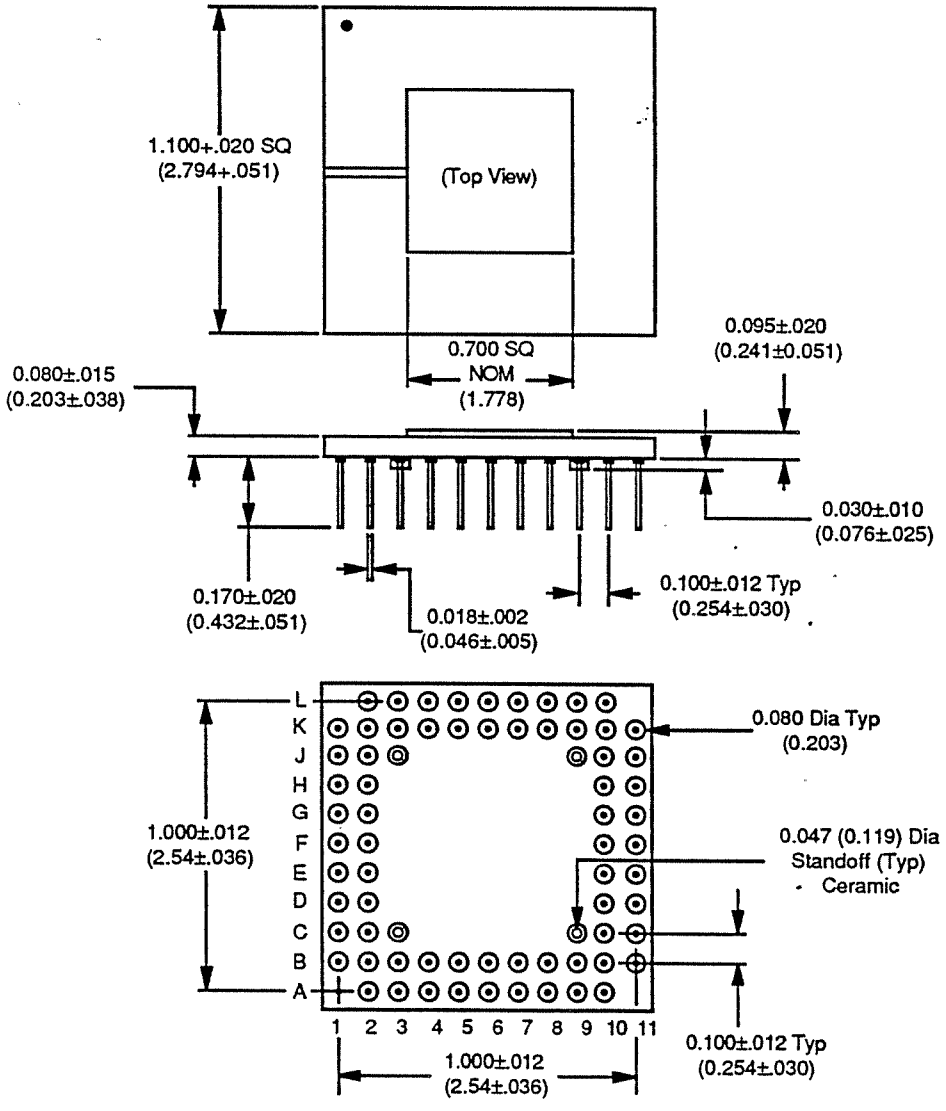
# Table E QMV98C Register Function Summary

| REGISTER NAME | READ/ WRITE | SELECTED BY: RD | WR | ADR2 | ADR1 | ADR0 | BIT DESIGNATION | FUNCTION OF REGISTER BIT(S) |
|---|---|---|---|---|---|---|---|---|
| INTERRUPT STATUS REGISTER | READ | 0 | 1 | 0 | 0 | 0 | D1 | • This bit reflects the status of the FDHP 1msec interrupt. Following reception of an FDHP signalling byte, this bit is set from 0 to 1. The status of this bit is also presented externally to pin UINT as an active low interrupt output signal.<br>D1 = 0, no interrupt pending<br>D1 = 1, FDHP interrupt pending and requires sevicing |
| | READ | 0 | 1 | 0 | 0 | 0 | D4 | • Indicates bipolar violation counter overflow.<br>D4 = 1, overflow occurred<br>D4 = 0, no overflow |
| | READ | 0 | 1 | 0 | 0 | 0 | D6 | • This bit reflects the status of the QMV98C w.r.t. the 160 kb/s TCM data transaction.<br>D6 = 1, TCM system in sync<br>D6 = 0, TCM system out of sync. |
| WRITE INTERRUPT REGISTER | WRITE | 1 | 0 | 0 | 0 | 0 | D1 | • Writing a '1' to this bit resets the interrupt pending state of the FDHP interrupt. Bit D1 of the Interrupt Status Register gets set to '0' and the UINT interrupt line gets set high. This resets the interrupt circuitry to allow signalling of the next FDHP received byte. |
| | WRITE | 1 | 0 | 0 | 0 | 0 | D4 | • Writing a '1' to this register clears the bipolar violation counter overflow pending status to allow accurate BPV counting. Status of BPV counter is reflected in bit D4 of Interrupt Status Register (see above).<br>Note: When resetting the FDHP interrupt pending status, the Write Interrupt Register should be loaded with the binary value "00111111" (D7....D0). Values other than this could cause unknown effects. |
| READ FDHP | READ | 0 | 1 | 0 | 1 | 1 | D0-D7 | • This register is used to access the received FDHP signalling data byte. Upon receiving an FDHP 1 msec interrupt (UINT line goes low), reading this register will return the last received FDHP messaging byte. |
| WRITE FDHP | WRITE | 1 | 0 | 0 | 1 | 1 | D0-D7 | • This register provides storage of the transmit FDHP signalling byte. During the transmit portion of the TCM frame, the data stored in this register will be sent out as the FDHP signalling data. This register should be updated during the FDHP interrupt handler.<br>Note: FDHP READ & FDHP WRITE together provide an 8 kb/s, full-duplex signalling channel. |
| BIPOLAR VIOLATION COUNTER REGISTER | WRITE | 1 | 0 | 1 | 0 | 0 | D2 & D0 | • BPV Counting is performed continuously by the QMV98C. This bit is used to perform prescaling of the BPV count. Initializing the BPV register by writing '00000000' will perform a BPV prescaling (divide by 8), writing '00000100' will turn prescaling off.<br>• Writing '00000001' followed by '00000000' to this register clears the BPV count, (D7...D0). |
| | READ | 0 | 1 | 1 | 0 | 0 | D0-D7 | • Reading the contents of this register returns the contents of the BPV counter. |
| LOOPBACK | WRITE | 1 | 0 | 1 | 1 | 0 | D0-D1 | • This is a write only register used to control the loopback maintenance features of the QMV98C. Bit D0 controls the digital loopback and D1 controls the analog loopback. Writing a '1' to the bit disables the loopback and '0' enables the loopback. Only one loopback can be operated at a given time. |

[Dimensions (min/max) in inches]




44-Pin CQUAD




| Grid Loc. | Pin No. | Grid Loc. | Pin No. |
|---|---|---|---|
| B2 | 1 | K10 | 35 |
| B1 | 2 | K11 | 36 |
| C2 | 3 | J10 | 37 |
| C1 | 4 | J11 | 38 |
| D2 | 5 | H10 | 39 |
| D1 | 6 | H11 | 40 |
| E2 | 7 | G10 | 41 |
| E1 | 8 | G11 | 42 |
| F2 | 9 | F10 | 43 |
| F1 | 10 | F11 | 44 |
| G2 | 11 | E10 | 45 |
| G1 | 12 | E11 | 46 |
| H2 | 13 | D10 | 47 |
| H1 | 14 | D11 | 48 |
| J2 | 15 | C10 | 49 |
| J1 | 16 | C11 | 50 |
| K1 | 17 | B11 | 51 |
| K2 | 18 | B10 | 52 |
| L2 | 19 | A10 | 53 |
| K3 | 20 | B9 | 54 |
| L3 | 21 | A9 | 55 |
| K4 | 22 | B8 | 56 |
| L4 | 23 | A8 | 57 |
| K5 | 24 | B7 | 58 |
| L5 | 25 | A7 | 59 |
| K6 | 26 | B6 | 60 |
| L6 | 27 | A6 | 61 |
| K7 | 28 | B5 | 62 |
| L7 | 29 | A5 | 63 |
| K8 | 30 | B4 | 64 |
| L8 | 31 | A4 | 65 |
| K9 | 32 | B3 | 66 |
| L9 | 33 | A3 | 67 |
| L10 | 34 | A2 | 68 |

68-pin Ceramic Pin-Grid Array (PGA)

Figure 2 Detailed Packaging Information

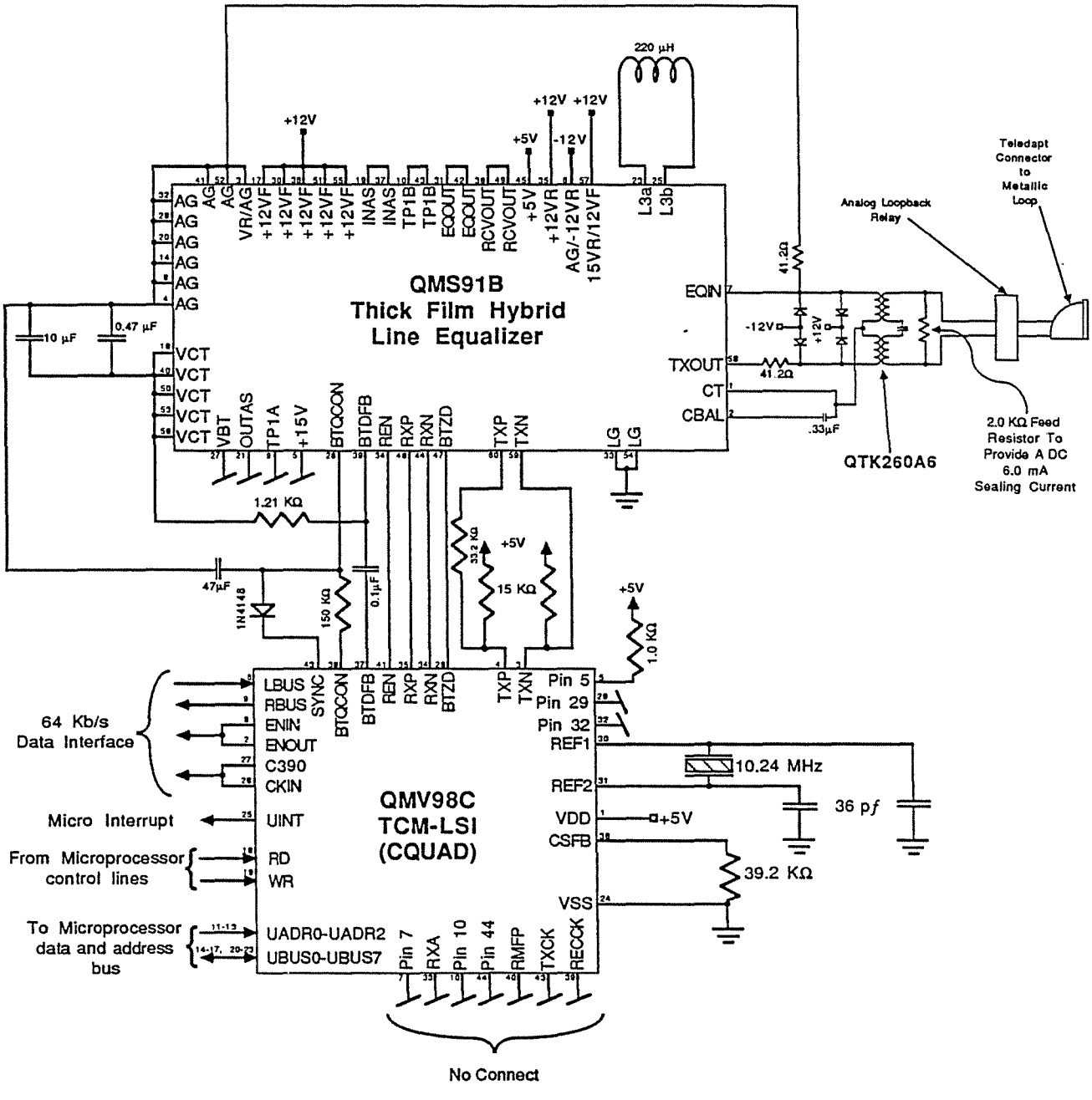
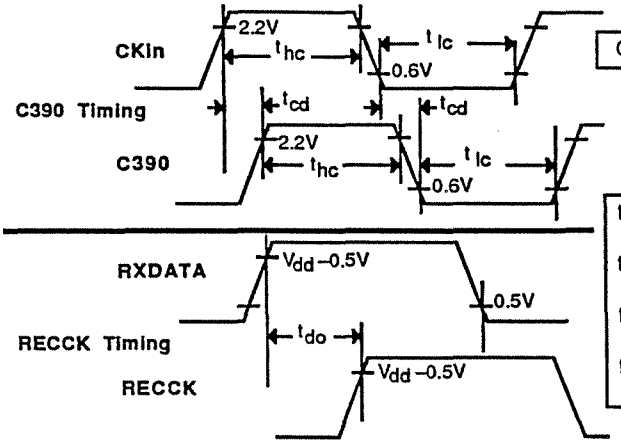



Figure 3 Detailed Interface Information




Clock Freq = 2.56 MHz.

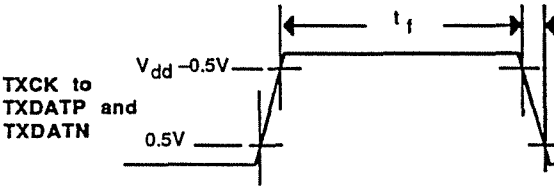
$t_{hc}$ = High time = 130 ns minimum

$t_{lc}$ = Low time = 110 ns minimum

$t_{cd}$ = Delay time= 10 ns minimum; 150 ns maximum.

$t_{do}$ = Delay time= 1.56 µs minimum; 1.78 µs maximum.

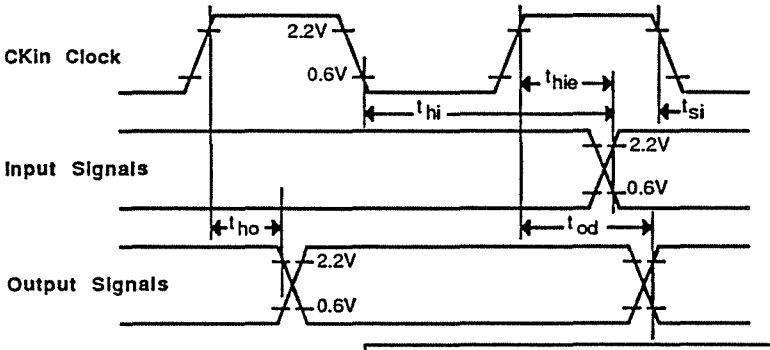
Figure 4 Clock Interface Waveform Timing




$t_p$ = High time = 3.13 µs maximum; 2.75 minimum.

$t_f$ = Fall time = 200 ns maximum.

Figure 5 Loop Interface Waveform Timing




Input Signals: ENIN, RBUS

Output Signals: LBUS, ENOUT

$t_{hi}$ = Hold time = 50 ns minimum

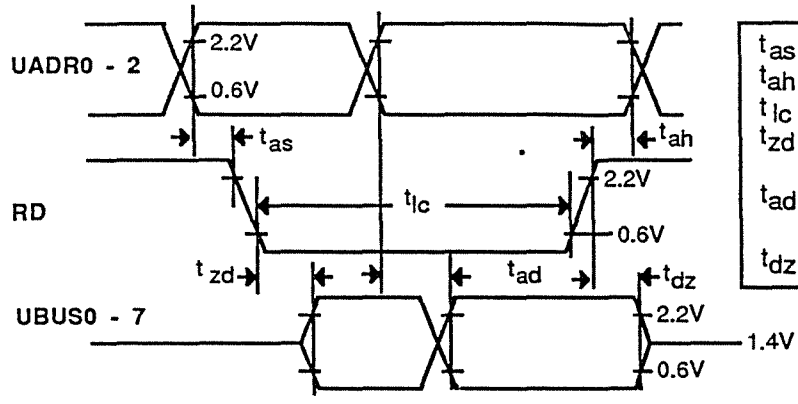
$t_{hie}$ = Hold time = 20 ns minimum (for ENIN only).

$t_{ho}$ = Hold time = 10 ns minimum.

$t_{si}$ = Set-up time = 80 ns minimum (for ENIN).
= 5 ns minimum (for RBUS).

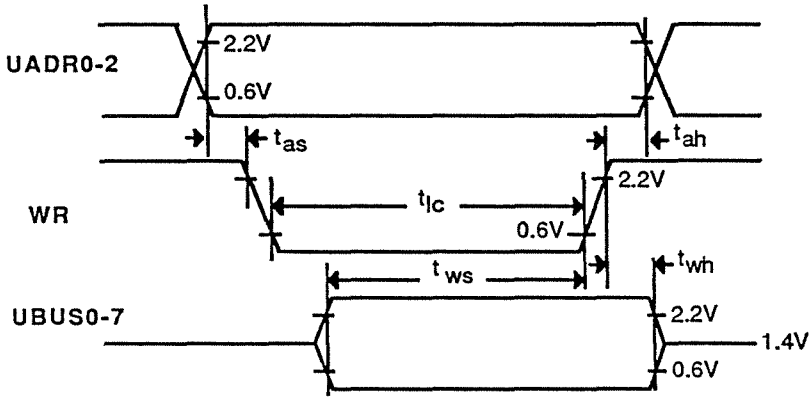
$t_{od}$ = Delay time = 115 ns maximum (for LBUS).
= 0 - 50 ns (for ENOUT).

Figure 6 Network Interface Waveform Timing




| | | |
|---|---|---|
| $t_{as}$ | = Read AddressSet-up | = 100 ns min. |
| $t_{ah}$ | = Read Address Hold | = 50 ns min. |
| $t_{lc}$ | = Read Low time | = 350 ns min. |
| $t_{zd}$ | = Open ckt to Drive delay | = 10 ns min.; 200 ns max. |
| $t_{ad}$ | = Addr to Data delay | = 20 ns min.; 350 ns max. |
| $t_{dz}$ | = Drive to Open ckt | = 100 ns max. |

Figure 7 Micro Interface Read Waveform Timing




| | | |
|---|---|---|
| $t_{as}$ | = Write Address set-up time | = 100 ns min. |
| $t_{ah}$ | = Write Address hold time | = 50 ns min. |
| $t_{lc}$ | = Write Low time | = 350 ns min. |
| $t_{ws}$ | = Write Data set-up time | = 350 ns min. |
| $t_{wh}$ | = Write Data hold time | = 10 ns min. |

Figure 8 Micro Interface Write Waveform Timing

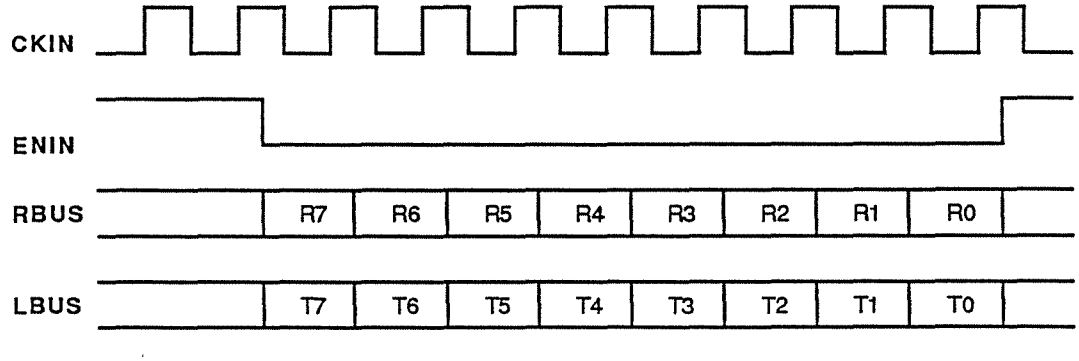



Figure 9 64 Kb/s Interface Functional Timing

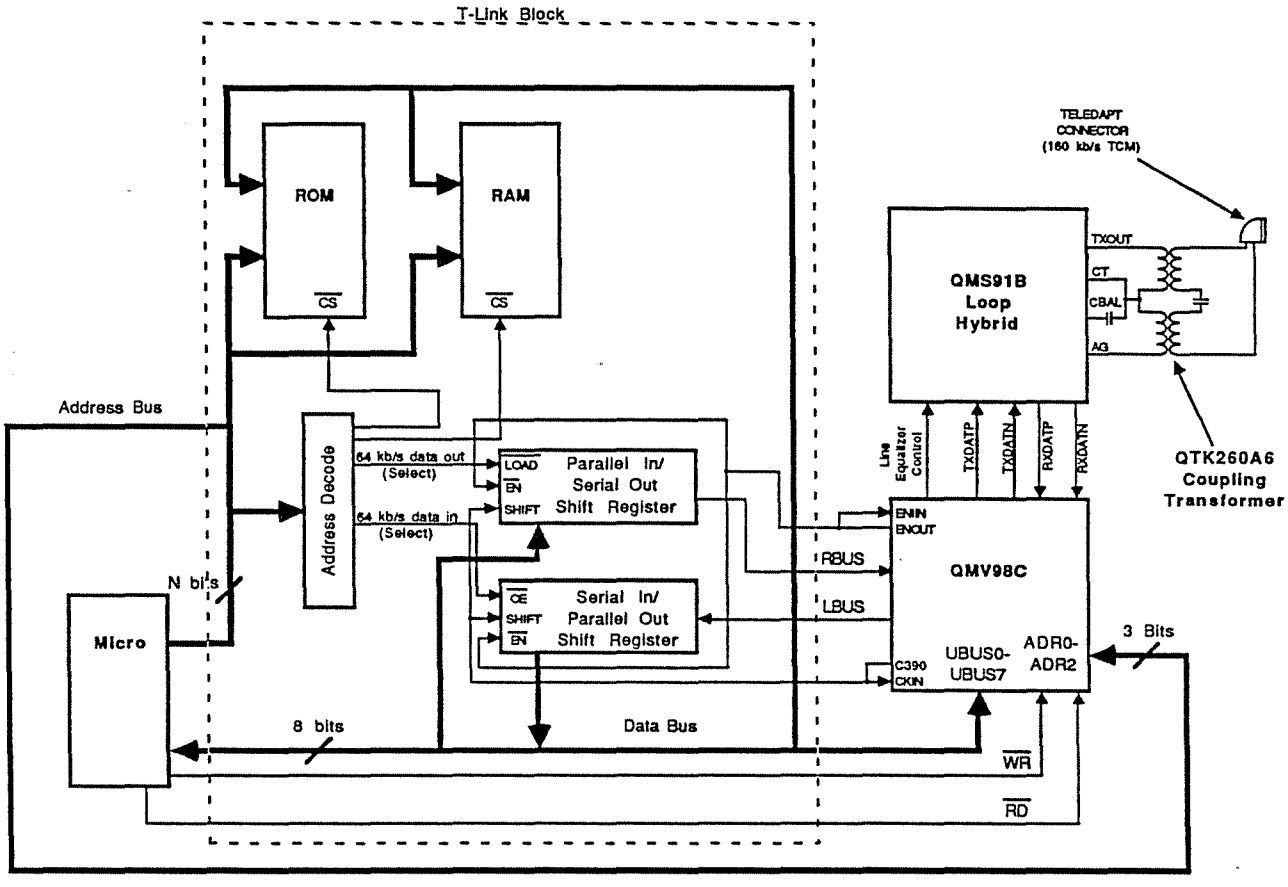



Figure 10 Typical QMV98C Application

## Functional Description

### Introduction

The QMV98C is an LSI device designed to provide access and control of data over 2-wire loops of up to 5.5 Km. It provides a transparent, full-duplex, 64 kb/s channel for data transmission, together with an 8 kb/s signalling channel utilizing Time Compression Multiplexing (TCM) technology on the loop side at a line rate of 160 kb/s and a burst period of 1 msec. The line code is Alternate Mark Inversion (AMI) bipolar modulation. Combined with the QMS91B (external, hybrid, thickfilm, line equalizer) and the QTK260A6 (external coupling transformer), the system provides automatic line equalization for line dispersion and bridged taps.

The QMV98C provides several internal registers for status and signalling information as well as providing control of maintenance loopback features (Tables D and E). It is packaged in both a 44-pin CQUAD device as well a 68-pin, PGA (pin grid array) device and is fabricated with CMOS1BS technology.

The QMV98C integrates most of the digital functions associated with the TCM transmission and is divided into 5 major blocks (refer to Figure 1):

- Transmit Block
- Receive Block
- Signalling Interface
- 64 kb/s Interface
- Clock Recovery Block

The following sections will give a brief description of the major functional blocks within the QMV98C.

### Transmit Block

The transmit block's main function is to take the 64 kb/s data from the 64 kb/s interface and transmit it to the loop interface at 160 kb/s. The transmit logic is made up of an elastic register, a data scrambler and a bipolar modulator circuit and supports the following functions:

- rate conversion (64 kb/s to 160 kb/s) and storage of the transmitted data
- transmit data scrambling with burst synchronization
- bipolar modulation
- loop signalling byte insertion (ie combining of 8 kb/s and 64 kb/s data into a single data stream)
- digital loopback multiplexing

### Receive Block

The receive block adapts the 160 kb/s line data to the 64 kb/s interface. It is responsible for the following functions:

- bipolar to unipolar conversion
- receive loop data sampling
- bridged-tap equalization control
- descrambling of receive data
- provides synchronization for the transmit TCM burst
- signalling byte extraction
- data rate conversion from 160 kb/s to 64 kb/s
- bipolar violation detection

### Signalling Interface Block

The signalling interface block acts as a buffer between the 64 kb/s loop interface and the microprocessor interface. It is connected to an 8-bit bidirectional data bus which is controlled by a 3-bit address bus and read and write lines. The main functions of the signalling interface block are:

- storage of loop signalling data
- bipolar violation counting
- control of loopback maintenance features

### 64 kb/s Interface Block

The 64 kb/s (or Network) interface block interfaces the TCM LSI with the 64 kb/s data channels. It also provides local 1 msec timing for internal use by the chip.

### Clock Recovery Block

The clock recovery circuit uses a digital phase-locked loop (DPLL) to lock onto the incoming loop receive data and generate two recovered clocks (160 KHz and 2.56 MHz) used for TCM timing and synchronization as well as 64 kb/s data transaction timing.

## Operational Description

### QMV98C System Interface

The operation and interfacing requirements of the QMV98C are discussed with reference made to both the "loop" side and the "micro" side. The micro side refers to the 64 kb/s data channel and 8 kb/s signalling channel presented to the user whereas the loop side refers to the 160 kb/s TCM side of the device. To access the 64 kb/s data and 8 kb/s signalling channels the QMV98C provides two interfaces on the micro side:

1) 64 kb/s data.channel interface
2) 8 kb/s signalling channel interface.

### 64 kb/s Data Channel Interface

Interfacing of the 64 kb/s data is accomplished by six lines:

1) LBUS - serial 64 kb/s data bus passing data from the loop to the micro side
2) RBUS - serial 64 kb/s data bus passing data from the micro to the loop side
3) ENIN - tied to ENOUT it validates the 64 kb/s data
4) ENOUT - an output provided by the QMV98C used to synchronize the 64 kb/s data transactions (meets ENIN specification)
5) C390 - a 2.56 MHz clock provided by the QMV98C used to clock the 64 kb/s data into/out of the QMV98C (meets CKIN specification)
6) CKIN - tied to C390 it provides synchronization of the 64kb/s data transfers

Data is transfered into and out of the QMV98C via two 64 kb/s, serial data buses - LBUS and RBUS. The RBUS represents the 64 kb/s data channel from the micro to the loop side and the LBUS represents the 64 kb/s data channel from the loop to the micro side. Hence, combination of the LBUS and RBUS data produces the 64 kb/s full-duplex data channel.

To provide a mechanism for ensuring synchronization of the data transactions, two other signals are required - ENIN and CKIN.The operation of the two buses (LBUS and RBUS) is very similar and hence only the LBUS data transfer will be presented in detail with references made to the RBUS equivalents where necessary. The typical application data presented in Figure 10 will be usefull in the following discussion.

The LBUS passes data in 8-bit bursts from the QMV98C to the microprocessor, ie loop side to micro side transaction. The synchronization of the micro with the QMV98C is accomplished by "gating" the data transaction with an enable window - ENIN. ENIN is an active low enable pulse which remains low for 8 periods of the CKIN clock. During the active portion of the ENIN pulse, data is valid at the LBUS on the falling edge of the CKIN clock. Two other signals are provided by the QMV98C - C390 and ENOUT. In designing with the QMV98C, ENOUT should be tied directly to ENIN and C390 tied directly to CKIN. The C390 output is a 2.56 MHz clock (390 nsec period) recovered from the receive loop data by the QMV98C. The ENOUT output is an active low signal which is synchronized to the C390 clock and presented to pin 27 of the device. Therefore, refering to Figure 10, the suggested method for capturing the LBUS data is to connect the LBUS output to the input of a serial in/parallel out shift register and clocking the data into the shift register on the falling edge of the C390 clock (recall that ENIN=ENOUT and CKIN=C390). The ENOUT enable pulse should be used to allow shifting only during a valid data transaction (ie ENOUT = low). Upon completion of the data transfer, an interrupt signal can be sent to the controlling microprocessor and the data may be read in parallel form.

The operation of the RBUS is handled in much the same way except the direction of the data transfer is now into the device. The RBUS is tied to the output of a parallel in/serial out shift register. Data is loaded (in parallel form) from the microprocessor to the parallel load shift register prior to the active portion of ENOUT. During the active portion of ENOUT, valid data is presented to the RBUS input prior to the falling edge of the C390. The C390 then clocks the valid data into the QMV98C on the falling edge. The C390 also clocks the shift register to ensure that the next bit in the serial data stream is ready for the next transfer. Figures 4, 6 and 9 show the 64 kb/s timing diagrams.

Notes:

1) Following the 8-bit data transfer, both LBUS and RBUS should return to the MARK position (ie logic 1).
2) Data is transfered into and out of the QMV98C MSB first
3) Tie CKIN directly to C390 and ENIN directly to ENOUT.

**8 kb/s Signalling Channel And Micro Interface**

The QMV98C provides an 8 kb/s outband signalling channel on TCM for performing such functions as call set-up and call take-down in circuit switched data applications. The interface to the 8 kb/s channel is handled by a bidirectional, tristate, microprocessor compatible data bus. The interface consists of an 8-bit data bus (UBUS0-UBUS7), a 3-bit address bus (UADR0-UADR2) and read and write control lines (RD, WR). This interface provides access to the 16 internal registers of the QMV98C (only 7 registers have implemented functions) to allow the following functions to be performed:

- status of receive signalling data interrupts
- control of receive signalling data interrupt line (UINT) and status bit
- status of TCM sync (ie TCM side of QMV98C is in sync? - yes/no)
- receive/transmit buffer for FDHP signalling data (ie 8kb/s signalling channel storage)
- control of digital and analog loopback maintenance features of the QMV98C
- maintenance test feature support for bipolar violation counting

The registers are selected according to the values of the RD/WR lines and the address select pins (UADR0-UADR2). Table D shows the register addressing scheme of the QMV98C and Table E gives a brief description of the functions provided by the registers (individual bit function).

The QMV98C is designed to interface directly with a microprocessor. The microprocessor will then play a supervisory roll over the QMV98C and perform such tasks as:

- call set-up prior to data transfer
- call take-down after data transfer session is complete
- call progress monitoring during data call session (ie call may be dropped by the far end)
- power-up system verification by exercising the loopback maintenance features of the device
- monitoring the status of the TCM transaction (ie system is in TCM sync)

The timing diagrams for the READ and WRITE cycles of the signalling channel interface of the QMV98C are presented in Figure 7 and 8.

**Signalling Interface And Internal Registers**

The QMV98C incorperates an 8 kb/s signalling channel. The channel is accessed via two internal registers - "Read FDHP" and "Write FDHP". The data contained in the write FDHP register is combined with 8 bytes of the 64 kb/s data and sent in the TCM frame. The TCM frame has a data rate of 160 kb/s at a burst rate of one msec. Therefore one signalling byte gets sent every 1 msec interval to give a total bandwidth of 8 kb/s. Similary, the read FDHP register receives one byte of information every 1 msec (ie during the receive portion of the TCM transaction). Therefore the combination of the two registers presents a full-duplex, 8 kb/s signalling channel. The channel is supplied for purposes of setting up a circuit switched data connection through a digital telephone network. The channel provides a method for setting up and taking down calls under control of a microprocessor as well as providing a means of monitoring the state of the data connection without loosing any of the 64 kb/s data channel.

To optimize the amount of processing overhead required by the controlling micro, an active low microprocessor compatible interrupt output is provided by the chip - UINT. At the end of reception of a signalling byte from the loop, the UINT line goes low which will generate an interrupt at the micro. To service the interrupt, the micro must read the contents of the read FDHP register and clear the interrupt pending state by storing the binary value of '00111111' (D7-D0) in the WRITE INTERRUPT register. This operation will raise the UINT interrupt line output and reset the QMV98C interrupt circuit for reception of the next receive loop signalling byte. The write FDHP signalling byte should also be updated during this interrupt. This is accomplished by writing the information byte into the write FDHP register.

For polling applications, the status of the UINT interrupt pin is duplicated in bit D1 of the interrupt status register; refer to Tables D and E for register accessing information.

The signalling interface also provides access to several other internal registers. These registers provide status information of TCM sync and control of the maintenance features of the QMV98C.

Bit D6 of the interrupt status register provides an indication of the state of the loop TCM transaction. On power-up reset, the QMV98C automatically starts "hunting" for proper TCM sync. When TCM sync is found, bit D6 gets set from a '0' to a '1'. This condition is also presented on pin 42 (SYNC) of the device. This information can be used by the controlling micro to reflect to the user the status of the data communication channel. This bit is a read only register which follows the SYNC status of the TCM circuitry; therefore writing to this location will have no effect on the operation of the device.

Several maintenance features are supported within the QMV98C. A facility for bipolar violation counting is provided. This function can be set up and controlled by the supervising micro to test/verifiy the QMV98C and the TCM connection.

The BPV counting is continuously performed by the QMV98C. The number of bipolar violations counted is stored in an internal accumulator and may be accessed by reading the contents of the BPV Counter Register. Whenever a bipolar violation is detected, the accumulator gets incremented. Therefore to perform a bipolar violation test, bit D1 must be set low and the accumulator must be reset. This is accomplished by first writing '00000001' (D7...D0) into the BPV Counter register to clear the accumulator followed by '00000000' which enables counting of the bipolar violations. Accessing the BPV Counter register will then indicate the number of bipolar violations encountered.

Notes:
1) clearing the accumulator requires writing a 1 to bit D0 of the BPV Counter register, followed by a 0.
2) overflow of the accumulator is reflected in bit D4 of the Interrupt Status register; therefore this bit must be set to zero when the accumulator is cleared. This is accomplished by writing '1' to bit D4 of the write interrupt register. (1=overflow)
3) Bit D2 of the BPV Counter register can be used to prescale the bipolar violation counter by 8, see Table E.

**Analog And Digital Loopbacks**

The final features of the QMV98C are the analog and digital loopbacks. The analog loop back, when programmed, sets the TCM receive circuitry to receive the data that it transmitted after it has gone through the line equalizer ciruit and reflected off of the coupling transformer. This feature provides a mechanism for local system verification of the QMV98C and associated interface/control support circuitry. For this feature to function properly an additional relay should be added to open circuit the 2-wire loop on the far side of the coupling transformer. This provides a termination for the transmitted data to reflect off in both directions. The analog loopback is controlled by bit D1 of the maintenance register. To turn on the analog loopback the binary value of '00000001' (D7...D0) should be written to the maintenace register. Similary, to turn the analog loopback off the binary value of '00000011' (D7...D0) should be written to the maintenance register.

The digital loopback, when operated, loops back the data at the 64 kb/s interface. Operation of this loopback does not require an external relay, as the loop around is handled internally. Bit D0 of the maintenance register controls the digital loop back. Therefore, writing '00000010' (D7...D0) into the maintenance register activates the digital loopback and similarly, writing '00000011' (D7...D0) turns the digital loopback off.

# Appendix B

Loop Hybrid Spec Sheet

## QMS91B Thickfilm Hybrid Line Equalizer Data Sheets

### General Description

The QMS91B is a thickfilm hybrid line equalizer circuit used with the QMV98C (TCM-LSI) and the QTK260A6 (loop coupling transformer) to provide high speed data transmission over a 2-wire, non-loaded transmission line.

The Hybrid, together with the QMV98C, is designed to allow data transmission over any mix of 22, 24 and 26 gauge 2-wire metallic loop up to 5.4 Km and maximum loss of 45 dB at 80 KHz and compensates for the following loop limitations:

- frequency dependent loss
- effects of bridged-tap reflections
- crosstalk
- impulse and random noise

Full-duplex data transmission is achieved using Time Compression Multiplexing (TCM) with the loop interface circuitry in either transmit mode or receive mode at any given time. The TCM utilizes a frame rate of 1 msec and a line transmission rate of 160 kb/s. During each frame, 74 bits of information are exchanged in each direction:

- 64 bits of subscriber information
  (via a 64 kb/s full-duplex data channel)
- 8 bits of supervision and control information
  (via an 8 kb/s full-duplex signalling channel)
- 2 framing bits (start bit and stop bit)

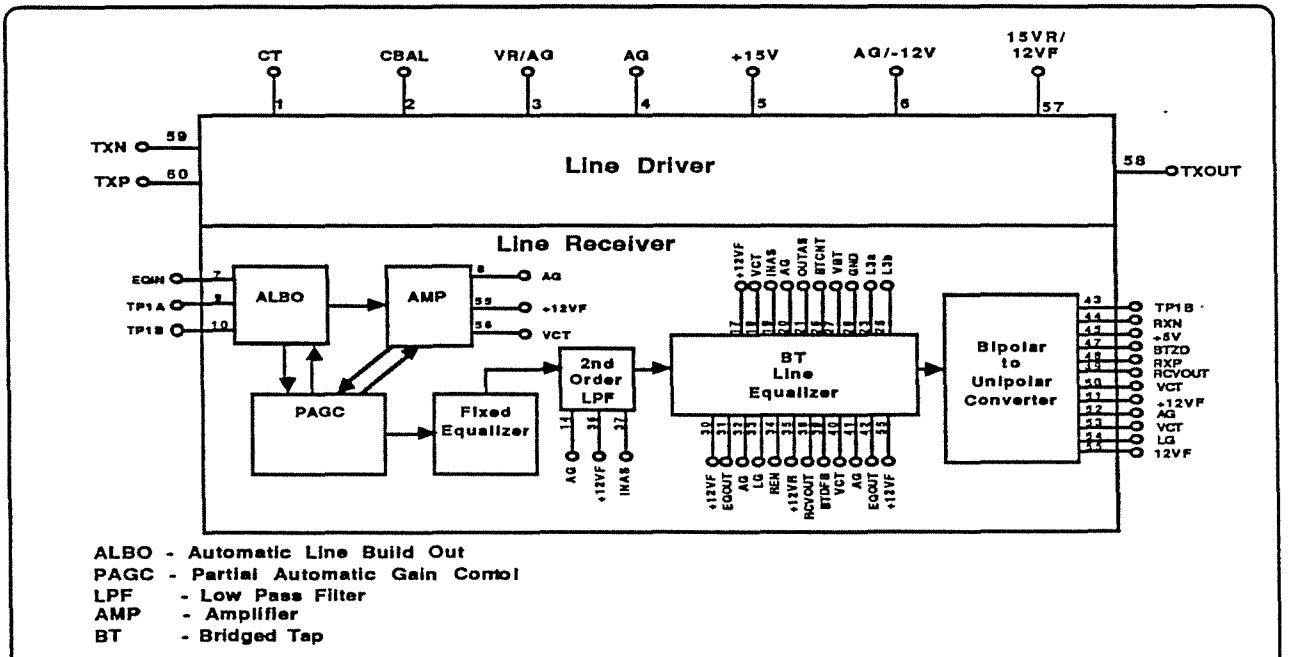



Figure 1 Hybrid Line Equalizer Block Diagram

## Table A - Pin Assignments And Functions

| Pin No. | Symbol | Function |
|---|---|---|
| 4, 8, 14<br>20, 28, 32<br>41, 52, 3 | AG<br>VR/AG (pin 3) | **Analog Ground:** General ground connection. Ground return for DC power supply +12V. |
| 17, 30, 36<br>51, 55 | +12VF | Positive voltage power supply input. Must be +12.0 V DC ±5%. |
| 59<br>60 | TXN<br>TXP * | **Transmit Negative/Transmit Positive:** These inputs are tied directly to pins 3 & 4 (respectively) of the QMV98C (TCM-LSI). The QMV98C provides two unipolar data streams on these inputs which are combined by the QMS91B into a bipolar TCM output to the metallic loop. They should be pulled up externally to the +5V power supply through 15 KΩ resisters. |
| 58 | TXOUT | **Transmit Output:** This output represents the Alternal Mark Inversion (Bipolar), Return to Zero, 50% modulated TCM signal. This output drives one side of a balanced loop coupling transformer which is connected directly to the metallic 2-wire loop (see Figure 3). Peak transmitted power into a 135Ω load is 16 dBm. Peak amplitude is 2.3 Volts across a 135Ω load. |
| 33, 54 | LG | **Logic Ground:** General ground connection. Connect to system logic ground. |
| 18, 40, 50<br>53, 56 | VCT | These pins should be tied together. VCT is an output used to set the DC operating point for the internal Amplifier. It is generated from a voltage division chain in the bipolar to unipolar circuitry. Figure 3 shows a typical connection of VCT to BTDFB (QMS91B & QMV98C) with additional AC coupling to AG. VCT should range from 2.995 to 2.920 V. |
| 5<br>9<br>21<br>27 | +15V<br>TP1A<br>OUTAS<br>VBT | These pins should be left unconnected (n.c.). |
| 45 | +5V | This input should be tied to the +5V logic power supply. Used in the bipolar to unipolar converter as an output reference for the output, unipolar, receive data (RXN, RXP). |

* The connection between TXP (pin 60 QMS91B) and TXP (pin 4 QMV98C) should contain a series 33.2 KΩ resistor (Figure 3).

## Table A - Pin Assignments And Functions (continued)

| Pin No. | Symbol | Function |
|---|---|---|
| 23<br>25 | L3a<br>L3b | These pins are provided for connection of an external 220 µH (±5%) inductor. |
| 1 | CT | **Center Tap:** This pin should be tied directly to the center tap (hybrid side) of the QTK260A6 loop coupling transformer. This pin, along with CBAL, provide a balance network for the coupling transformer. |
| 2 | CBAL | **Center Balance:** (see CT above) This pin should be connected to the center tap of the QTK260A6 coupling transformer through a 0.33 µF capacitor (50 V, ± 5%). |
| 19, 37 | INAS | These two pins should be tied together. |
| 6 | AG/-12VR | -12 Volt supply voltage. Must be -12.0V DC ±5%. |
| 39 | BTDFB | See VCT above (refer to Figure 3). |
| 10, 43 | TP1B | These two pins should be tied together. |
| 38, 49 | RCVOUT | These two pins should be tied together. |
| 44<br>48 | RXN<br>RXP | Unipolar receive data (negative and positive pulses) tied directly to pins 34 and 35 of QMV98C respectively. |
| 57 | 15VR/12VF | Tie to +12.0 V supply voltage. |
| 35 | +12VR | Supply Voltage, +12.0V DC ±5%. |
| 7 | EQIN | **Equalizer Input:** Input to line receiver. This pin should be tied to the receive side of the balance transformer (QTK260A6), see Figure 3. |
| 26 | BTQCON | **Bridged Tap Control:** This input is connected to pin 38 (BTQCON) of the QMV98C through a 150 KΩ resistor (see Figure 3). Used for control of the BT equalizer. |
| 31, 42 | EQOUT | Tie these pins together. |
| 47 | BTZD | This output is a BT feedback control tied directly to pin 28 of the QMV98C. |
| 34 | REN | **Receive Enable:** This input is tied directly to pin 41 of the QMV98C. It is an enable control line for the line receiver. |

## Table B - Absolute Maximum Ratings

| Symbol | Parameter | Value | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| AG/-12V | Supply Voltage | -13.0 | GND | V |
| 12VR | Supply Voltage | GND | +13.0 | V |
| $T_{stg}$ | Storage Temperature | -55 | 125 | °C |

## Table C - Operating Range

| Symbol | Parameter | Value | | | Units |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| 12VF | Supply Voltage | 11.4 | 12.0 | 12.6 | V |
| AG/-12V | Supply Voltage | -12.6 | -12.0 | -11.4 | V |
| $T_A$ | Operating Temperature | 0 | 25 | 70 | °C |

### Bridged Tap Equalizer

Data transmission at a line rate of 160 kb/s over a 2-wire loop may be severely degraded due to bridged tap (BT) reflections. Presence of BT's on the loop results in pulse degradation which reduces the signal to noise ratio. A two-bit, BT Equalizer is implemented in the receiver and consists of:

- A Zero Forcing Equalizer
- A Decision Feedback Equalizer

The BT equalizer is an adjustable filter network which will equalize for BT reflections. A feedback control loop to the QMV98C is supplied via pin 47 (BTZD) and is attached directly to pin 28 of the QMV98C (BTZD).

### Bipolar to Unipolar Converter

The signal at the output of the BT Equalizer is not of suitable shape and level to be used by the data recovery logic within the QMV98C. Therefore, the bipolar signal is fed into a set of comparators where it is converted to a unipolar TTL compatible signal. The outputs (RXP and RXN) are then fed directly into the QMV98C.

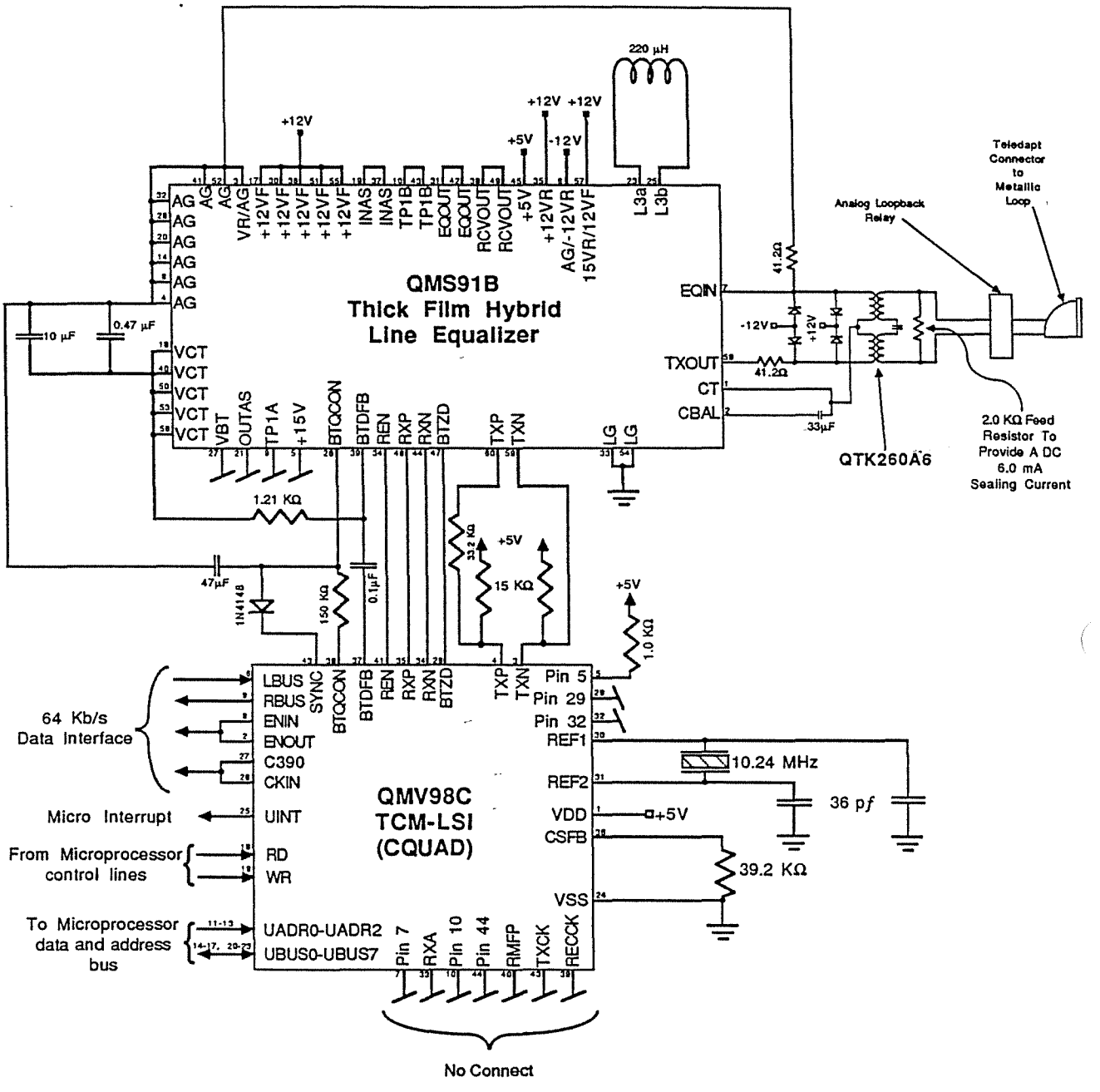
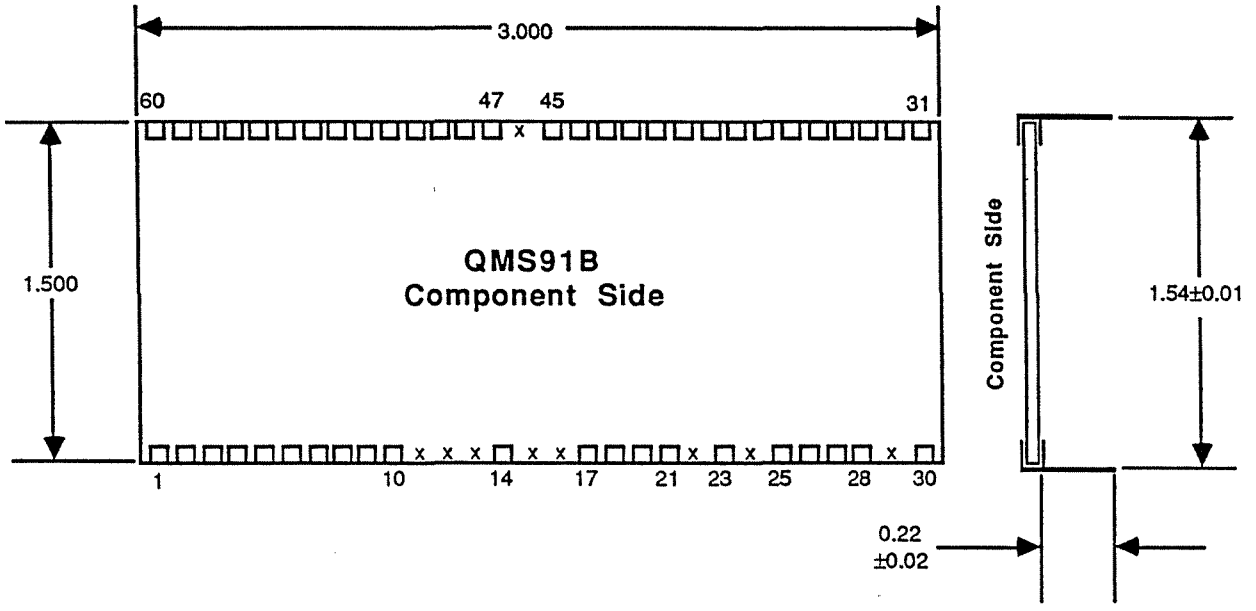



Figure 3 Detailed Interface Information




□ Denotes Pin
x Denotes No Pin In Positions 11, 12, 13, 15, 16, 22, 24, 29 and 46

Note: Dimensions are in inches.
Pin 1 reference mark opposite component side.
Max. Height with components = 0.45

Figure 2 Physical Configuration

## Funtional Description

The QMS91B is comprised of two main functional blocks - line driver and line receiver.

## Line Driver

The line driver circuit is enabled only during the transmit period of the TCM frame. The purpose of the line driver circuit is to convert the unipolar TTL level output signals of the QMV98C (TXN & TXP) into a bipolar Alternate Mark Inversion (AMI), return to zero, 50% modulated signal for transmission. To reduce crosstalk, the bipolar signal is modified by a lowpass filter with a corner frequency of approximately 260 KHz. Peak transmitted power into a 135 Ω load is 16 dBm. Peak amplitude of the transmitted signal is 2.3 volts across a 135 Ω resistive load. The line driver circuit is designed to operate from a +12V supply.

## Line Receiver

The line receiver is enabled only during the receive period of the TCM frame. Its function is to recover data from the bipolar signal received over a 2-wire metallic loop. The receiver automatically equalizes the line for losses ranging from 0 dB to 45 dB at 80 KHz, compensates for bridged taps and provides filtering to reduce the effects of impulse and random noise. The receiver should be transformer coupled from the loop (using the QTK260A6 isolation transformer). As well, additional foreign voltage protection can be added to the circuit side of the transformer via a diode bridge. The analog circuitry of the receiver operates from a single ended, +12 volt supply and together with the line driver is implemented using a thick film technology - QMS91B. Portions of the receiver are digital and are implemented in the QMV98C TCM-LSI (refer to QMV98C data sheets). The receiver can be further broken down into the following sub-blocks:

- Automatic Line Build Out (ALBO) *
- Partial Automatic Gain Control (PAGC)
- Fixed Equalizer *
- Bridged Tap Equalizers *
- 2nd order Low Pass Filter
- Summing Amplifier
- Bipolar to Unipolar Converter *
- Clock Recovery Circuitry (part of QMV98C)

* A brief description of these circuits follows.

## Automatic Line Build Out (ALBO)

The automatic line build out acts as a current controlled filter designed to introduce, in conjunction with the PAGC, a frequency dependent loss equivalent to the difference between actual loop loss and the loss of a 45 dB loop.

## Fixed Equalizer

The output of the PAGC is fed into the fixed equalizer which is designed to compensate for the frequency dependent losses introduced by metallic loop. To further improve the noise performance of the receiver circuit, its output is fed into a a 2nd order low pass filter (Figure 1).

# Appendix C

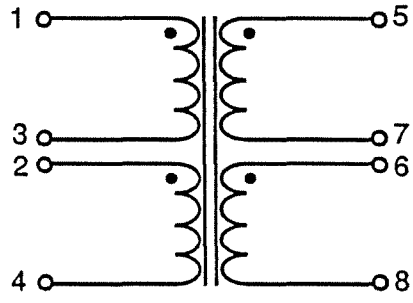
Loop Transformer Spec Sheet

# QTK260A6 Coupling Transformer Data Sheets

## General Description

## Electrical Requirements

### Schematic




### Insulation Resistance

At 200 Volts ±10 percent, the insulation resistance is 500 MΩ minimum when measured as follows (refer to schematic):

(1-4) to (5-8) and core
(5-8) to (1-4) and core.

### Dielectric Withstanding Voltage

Test Voltage: 200 V rms
Nature of potential: AC
Electrification Time: 1 second
Points of application of test voltage:

(1-4) to (5-8) and core
(5-8) to (1-4) and core.

Note: To measure, strap 3 and 2, 7 and 6.

### DC Resistance

$R_{(1-4)}$ = 6.0 Ω maximum; strap 3 and 2, 6 and 7.
$R_{(5-8)}$ = 4.75 Ω maximum; strap 3 and 2, 6 and 7.

### Inductance

$L_{(1-4)}$ = 253 µH minimum, at 0.02 V rms, 1 KHz;
To measure, strap 3 and 2, 6 and 7.

### Leakage Inductance

$L_{(1-4)}$ = 8 µH maximum at 0.01 V rms, 200 KHz;

To measure, strap 3 and 2, 6 and 7.

### Distributed Capacitance

$C_{D(1-4)}$ = 150 pF at 0.01 V rms, 200 KHz;
To measure, strap 3 and 2, 6 and 7.

### Direct Capacitance

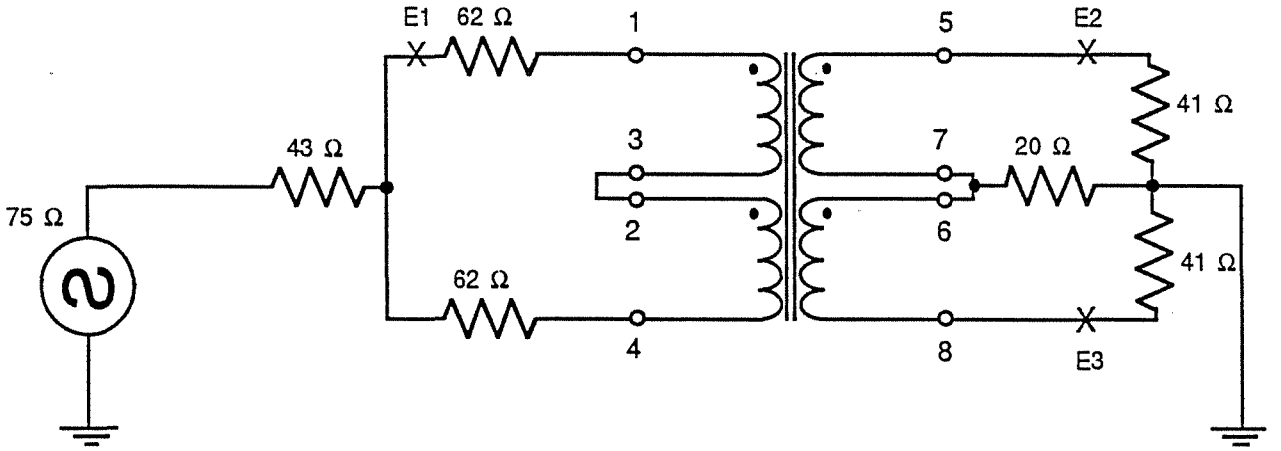
$C_{d(2-7)}$ = 600 pF maximum at 0.01 V rms, 200 KHz;
To measure, strap 3 and 2, 6 and 7.

### Turns Ratio

$$\frac{N_{(1-4)}}{N_{(5-8)}} = 1.249 \text{ minimum, } 1.275 \text{ maximum.}$$

### Balance To Ground

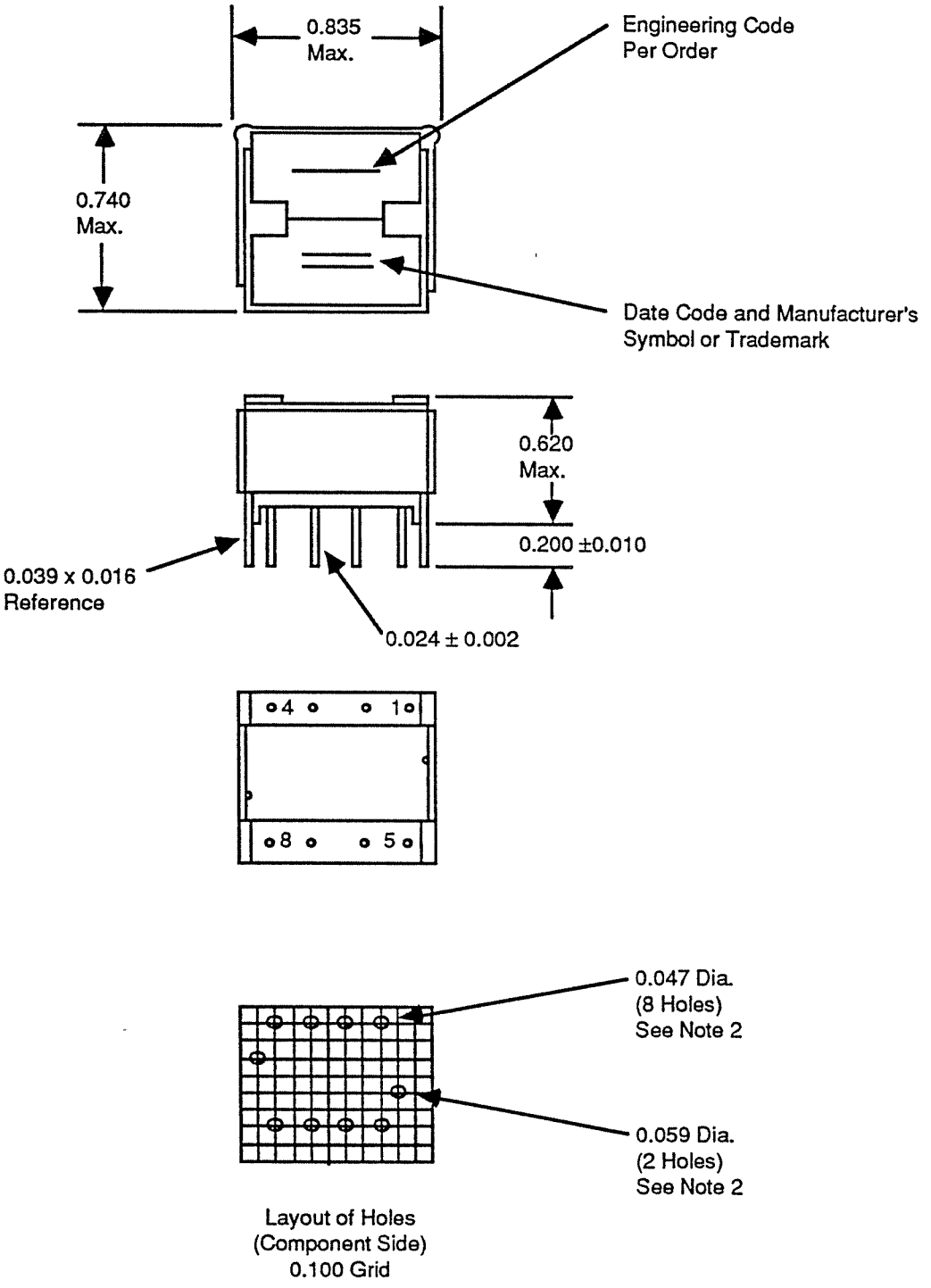
Balance to ground at E2 or E3 at 160 KHz is -44 dB minimum when measured as shown in the following circuit:




Notes: 1) Strap terminals 3 and 2, 6 and 7.

2) Resistors are 1/4 W ±2%.

3) The two 62 Ω resistors are matched to 0.10%.




Notes:
1. Dimensions are in inches.
2. These are finished hole sizes.

Figure 1 Physical Dimensions