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ABSTRACT

This memorandum describes the characteristics of aerospace computers developed in the 1962-1967 period; no attempt is made to extrapolate these characteristics to describe post-1967 computers.

The main functional divisions of memory, central processing unit and input/output are treated separately, as are such overall characteristics as speed, reliability, software availability, and weight, power and volume. Some knowledge of computers is assumed, but in many cases, concepts are explained in detail.

A "typical" 1967 computer cannot be described by a single set of characteristics. Each characteristic has a fairly wide range, reflecting the variety of computers available to meet a variety of applications. The characteristics of the machines surveyed are given in Appendix Table 2 and summarized below along with characteristics of the MIT Block II Apollo Guidance Computer (AGC):

Characteristic	Minimum	Typical	Maximum	AGC
Add Time (μsec)	2	4-12	624	23.4
Multiply Time (μsec)	6	20-60	711	46.8
Divide Time (μsec)	18	22-100	840	81.9
Weight (lbs)	5	30-80	200	58.0
Size (cu.ft.)	0.07	0.4-1.4	2.65	1.0
Power (watts)	4	100-250	567	100
Memory Size (words)	2K	4-16K	131K	38K

One trend in the overall design of aerospace computers is toward computers which look more and more like ground-based machines. Multiple formats for instruction words, instruction sets compatible with ground-based machines, and efforts to provide greater memory capacity through a hierarchy of different types of memories are some examples of this trend.

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TECHNICAL MEMORANDUM

I. INTRODUCTION

This memorandum provides a brief summary of the current state-of-the-art of aerospace digital computers. The information herein is based on the characteristics of aerospace computers which were developed during the period 1962-1967. Data was obtained from manufacturers and from two previous surveys.* No attempt is made to extrapolate the information in the survey to describe the characteristics of post-1967 computers. Although this survey is intended to be comprehensive, it is recognized that some computers of interest may have been omitted. The memorandum is slightly biased toward manned space flight applications, particularly when discussing future research trends.

Section II of the memorandum summarizes characteristics of the major functional subdivisions of a computer--the memory, the input/output, and the central processing unit. Section III summarizes operational and physical characteristics including speed, software, reliability, and weight, power, and volume. Section IV outlines some areas where progress in existing technology is likely to occur or might be needed to handle the requirements of future missions. The Appendix includes an alphabetical list of the computers surveyed, a table of the basic characteristics of these computers and a complete description of several computers of particular interest.

II. FUNCTIONAL SUBDIVISIONS OF AEROSPACE COMPUTERS

A. Memory

Storage devices used in ground-based machines include cores (or other high speed devices), drums, disks, special devices (such as magnetic cards), magnetic tapes, and punched paper cards. This hierarchy, whose division is based on access time and density of information, has seldom been found in

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*"A Fourth Survey of Domestic Electronic Digital Computing Systems", Martin H. Weik, Jr., January 1964, Ballistic Research Laboratories, Aberdeen Proving Ground, Maryland.

"A Survey of Spaceborne Computers", George Liviakis, June 27, 1966, Planning Research Corporation, Los Angeles, California.

spaceborne computers.* Instead, the memory in spaceborne computers to date can be thought of as being divided into one section for the instructions and constants ("program memory"), another section for the variable data and temporary data ("data memory"), and a third section used within the central processing unit (CPU). Sometimes this division is physical as well as conceptual, in which case the program memory is usually read-only, and the data memory read-write; the CPU may have a read-only memory, a read-write memory, or both.

1. Data Memory

Data memories must be built with devices capable of being read from and written into in real time. All of the 40 computers in this survey use core memories for data storage except three** which use destructive readout (DRO) thin film memories and four*** which use other devices. Because of the widespread use of core memories in spaceborne as well as ground-based computers, there is ample information available about them, and they are not further discussed in this report.

2. Program Memory

In machines without a separate program memory, the program and data are both stored in a read-write memory. The program can then be easily modified, either by itself (e.g., to set up the return address when beginning a subroutine) or by external sources (as when entering a new program). It is possible, however, to write a program in a manner that requires no direct modification of instructions. The program can then be stored in a read-only memory, which reduces the probability of inadvertent damage to the program. Of the 40 computers in this survey, 9 have a read-only memory used for program storage, and several others offer a read-only memory as an option.

The read-only memory could be built using conventional DRO cores with an automatic restore cycle after every read cycle, but, more often, it is built with special devices which allow a non-destructive readout (NDRO) technique to be used. The computers in this survey which have separate program memories employ NDRO techniques that are implemented with multiaperature devices, thin-film elements, or wired arrays.

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*The only exception in this survey is the tape unit used as an auxiliary memory unit (AMU) on the Gemini Guidance Computer.

**CDC 449, Univac ADD-1000 and Univac 1824.

***The Honeywell ALERT and Honeywell Subminiature Computer use BIAX elements; the ARMA Micro Computer and IBM Gemini Guidance Computer use transfluxors.

(a) Multiaperature Devices

Transfluxors and BIAX elements (Figure 1) are multiaperature devices used in computers in this survey. Readout from a BIAX element is completely nondestructive, so that no time is needed to restore the information read from the element. A transfluxor has NDRO characteristics, but some degradation of the information occurs and the information is destroyed by repeated read cycles. This is usually compensated for by applying, after each read operation, a "reinforce" pulse to all cores without regard to the address which was read. In one case, the reinforce pulse is applied only after four read operations have been completed.

These elements are electrically alterable, although usually the write operation is longer and requires more power than the write operation for a DRO core. Nonetheless, they can be used in applications where information is read much more often than it is written, such as program storage with only an occasional need to alter the program in real time.

The primary application of these elements, however, is in implementing read-only memories. Their read time (1 μsec or less) is typically 1/10 as long as their write time. This read time compares favorably with the access time of DRO cores used in spaceborne memories.

(b) Thin Films

Thin-film sandwich elements (not to be confused with DRO thin film devices) are another example of NDRO devices used in spaceborne computers. They can be electrically altered, but the write time is typically 1000 times the read time. Therefore, information is usually electrically entered by external equipment and no provision is made for real-time write operations.

(c) Wired Arrays

These memories have information wired into the array and can have the information changed only by disassembly and rewiring. There are two types. The "missing core" memory is implemented by omitting or

removing specific cores, or by shorting specific cores with a single-turn winding. The "core rope" memory, which is the type used for program storage in the Apollo Guidance Computer, is implemented by having the sense or drive winding bypass specific cores. Both types of wired arrays are useful for storing a well debugged program since they reduce the probability of errors caused by power transients or by inadvertent attempts to write over an instruction.

3. Memories Used in CPU

In addition to the implicitly addressed central registers, the central processor sometimes has explicitly addressed storage locations for temporary storage of intermediate results. In addition to being explicitly addressed, this "scratch pad" memory is characterized by being faster than main memory and by providing more storage than is normally available in central registers. The Autonetics D26C uses DRO cores to implement a 256-word memory of this type.

Several computers in this survey use a read-only memory to store control words for their microprograms (a type of hardware-implemented subroutine). For instance, the Burroughs D210 uses a 50-bit by 256-word rope memory for microprogramming of multiply, divide, and interrupt control.

4. Memory Capacity

Memory sizes of the computers in this survey vary widely. Most have a memory with at least 4096 words as a standard size, and there is usually a provision for expanding the capacity to some maximum ranging from 32,000 words to 132,000 words. Most of the computers in this survey have about 1000 words set aside for data (read/write) storage if a read-only memory is used for program storage. The wide variance in memory sizes and memory types can be seen by comparing the size and type of memories in the following four computers:

Name	No. of words in NDRO Memory	No. of words in DRO Memory	Total
CDC 449	3.8K	0.3K	4K
CDC 5360	0	8-32K	8-32K
IBM 4 PI/CP	0	8-32K	8-32K
MIT Block II AGC	36K	2K	38K

Memory capacity plays an important role in comparing the physical characteristics of computers, since the memory accounts for a significant portion (often as much as 50%) of the computer's overall volume and weight. For example, the characteristics of three computers are listed below for two different memory sizes:

Name	Memory Size	Computer Volume (ft^3)	Increase in Volume	Computer Weight (lb)	Increase in Weight
Litton L-304	8K	0.26	-	34	-
	16K	0.39	50%	41	20%
Honeywell ALERT	4K	0.69	-	34	-
	8K	0.95	37%	40	17%
Honeywell SIGN III	2K	0.24	-	12	-
	4K	0.28	17%	13	8%

The three machines listed above are of recent design (1966-67). Although there is not a close correspondence in the percentages given above, it is evident that an increase in memory does significantly increase the volume and weight. Information concerning increased power requirements for additional memory capacity is not available in all cases, but, for example, there is a 7% increase (140 watts to 150 watts) necessary in the case of the ALERT and an 11% increase (45 watts to 50 watts) necessary in the case of the SIGN III.

B. Input/Output (I/O)

I/O characteristics are not discussed in detail in this memorandum because in most applications the I/O unit is designed especially for the task. I/O features are, however, particularly important in space applications since the computer becomes a control element in a real-time system. As a control element, the computer is used to provide real-time control of space vehicle engines and real-time display of information for the astronauts.

The requirement for real-time operation implies a need for one or a combination of the following cases:

(1) a computer which sequentially performs its assigned tasks fast enough so that all tasks are accomplished during a given period;

(2) a computer which periodically scans its tasks (even though it may be in the process of doing one) and does them in an order based on a preassigned priority, or;

(3) a computer which has external interrupts so that, when a task needs to be performed, the program in process can be interrupted and resumed after the task called for by the interrupt has been accomplished.

In terms of speed requirements, or, alternatively, the number of tasks that can be handled with a given speed, (2) above requires less speed than (1), and (3) requires less speed than (2) for a given set of tasks. Both (2) and (3) require a method of retaining the status of the program in process so that it can be resumed.

Typically, tasks may be called for by an astronaut, a clock reaching a predetermined time, data or a command received from the ground, or the updating of data generated on board. This variety of task sources indicates a need, in the case of (2) and (3) above, for a priority system so that a program started by an interrupt can itself be interrupted. The status of the interrupted program is nested with the status of other interrupted programs to be used when the program is resumed according to its level of priority.

With few exceptions,* the computers in this survey have at least one interrupt level (the Litton L-304 has 64 levels) and many provide hardware implementation of program status retention rather than requiring software to handle this function.

Most of the computers in this survey have provisions for input and output of serial and parallel digital data and discrete signals. A separate I/O unit may be needed, though, to handle inputs from shaft-position encoders, real-time clocks, and analog devices or to provide outputs of analog voltages or pulse trains of controlled frequency. A separate I/O unit is

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*For example, the TRW Marco 4418 and the IBM Gemini Guidance Computer have no external interrupts.

particularly desirable if it provides for program continuation during completion of I/O transfers, assignment of priorities to I/O channels and simultaneous operation of two or more I/O channels.

The computers in this survey either incorporate these I/O features or are flexible enough that these features could be added. One computer which has a separate I/O unit is the Saturn LVDC. The Launch Vehicle Data Adapter (LVDA) is a physically separate unit which performs simple logic, simple computations, and signal processing (such as analog to digital conversion) necessary to buffer the LVDC with external equipment. It is desirable for an I/O unit to have the capability of communicating directly with the computer memory (as mentioned above), but where reduction of hardware is more important than increased speed, the I/O data path is through the arithmetic unit. The LVDA represents a compromise between these two possibilities; it can receive data from either the LVDC memory or arithmetic unit but can send data only to the LVDC arithmetic unit.

C. Central Processing Unit (CPU)

Memories are often taken "off-the-shelf", and I/O configurations are usually designed for specific applications, but the central processor is the unique, distinguishing unit of any computer. The features in the CPU which distinguish it from other computers include the type of arithmetic used, the method of addressing, the word length, the instruction repertoire, and the components used to build the CPU.

1. Arithmetic

With a few exceptions, the computers in the survey are parallel, binary, fixed point, general purpose machines with negative numbers represented in complementary notation. Generally, there is good reason for not choosing the alternatives. In most cases, a serial machine would be too slow, and its potential savings in hardware and reduced complexity must be sacrificed. However, the serial Saturn LVDC is an exception which emphasizes the point that "speed" is meaningful only in relation to the tasks at hand.

Fixed-point data representation can provide a wide enough number range for aerospace problems so that the increased hardware necessary for floating point has thus far been too high a price to pay. On the other hand, fixed-point number representation makes the choice of word length more important and also

adds to the programmer's burden. It is likely that as hardware becomes smaller, lighter, and more reliable, floating-point representation will become more common. The IBM 4 PI/EP, introduced in late 1966, and the RCA VIC-36A, under development, both have a floating-point option.

Sign-magnitude number representation, an alternative to complementary notation, complicates the central processor. Its only advantage is ease of interpretation by humans, and, although this is an important factor, it has thus far not been considered important enough to warrant the added complexity.

2. Addressing

Early ground-based digital computers used a four-address instruction word in which the addresses of two operands, the address of the result, and the address of the next instruction were specified. In an attempt to better utilize available memory and to increase the number of addressable words for a given instruction word length, changes were made in the instruction word format. Hardware, in the form of an instruction counter or current address register, and software, in the form of a jump instruction, have replaced the address of the next instruction. Hardware, in the form of an addressable register, and software in the form of a "load register" instruction and a "store register" instruction, have replaced the address of one of the operands and the address of the result.

These changes resulted in single-address machines, both for ground-based and aerospace applications. Thus the machines in this survey are all single address except for the General Precision AN/ASN-24.

Further changes in instruction word formats have resulted in what can be termed modified single address formats. Such formats have become commonplace in current ground-based computers. Aerospace computers which use modified single address formats are the Univac ADD-1000, Univac 1830A, Litton L-304 and L-3050, and the IBM 4 PI machines. These machines provide for one operand to be addressed in memory and another operand or result address to be chosen from registers in the central processing unit. In addition, the 4 PI machines have several different formats, one of which specifies two operand addresses in main memory. This illustrates that advances in addressing techniques have been accomplished by a historical trend to a single address, followed by multiple formats that allow earlier techniques to be used when desirable.

3. Word Length

Choice of computer word length is influenced by instruction word length requirements and data word length requirements, and these requirements are not always compatible. Instruction word length is strongly influenced by the number of commands to be addressed.* Data word length depends heavily on the precision required in the data word; space navigation problems require precision** of the order of one part in $10^{8\pm1}$ (or one part in about 2^{24} to 2^{32}). Most of the computers in this survey are used for guidance and navigation, and have 24-to 32-bit instruction and data words. There are, however, two other choices if the required data word length is longer than is necessary for the instruction word. First, both the instruction and data words can be made shorter and double precision operations used where necessary. For instance, the MIT AGC has 15-bit instruction and data words. Second, the instruction word can be made a different size than the data word. The Hughes HCM-202 uses a 24-bit data word and a 12-bit instruction word with the instructions stored in a separate, read-only, memory; the Saturn LVDC uses a 26-bit data word and a 13-bit instruction word with two instructions stored in each memory location; and the Honeywell Subminiature Computer has a 24-bit data word, a 16-bit instruction word and a 48-bit memory word, with two data words or three instruction words stored in each memory word.

4. Instruction Repertoire

A basic set of instructions for a computer includes provisions to perform arithmetic operations, logic operations, data transfers to and from memory, data transfers to and from external equipment, shift operations, and decision operations. One-third (13) of the computers in this survey use less than 20 instructions to perform these operations. This group of 13 is composed primarily of machines whose date of introduction is late 1963 or earlier. Another group of 13 machines in this survey have more than 50 (and as many as 135) instructions in their repertoire and are composed primarily of machines whose date of introduction is mid-1966 or later. This trend toward a greater number of programmable instructions requires more bits in the

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*Factors such as the number of addressable registers and amount of error detection or correction desired may also affect the choice of word length.

**"Electronic Navigator Charts Man's Path to the Moon", Albert L. Hopkins, Electronics, January 9, 1967.

operation code, but can provide savings in program execution time and in ease of programming. For instance, the Litton L-304 and L-3050 use a MOVE instruction to allow any number of bits in a directly addressed register to be selected by a mask and moved to any desired position in a central register. This MOVE instruction can be used in place of a shift instruction followed by a transfer instruction. These machines also have a GATED COMPARISON instruction, which allows a value in memory to be compared with a value in a central register plus or minus a designated "gated" value. This allows approximate comparisons to be made with a single instruction, instead of comparing with both ends of a range when some tolerance is permissible.

5. Hardware Components

All computers developed after 1963 use IC's in a portion--and usually a major portion--of the CPU. These IC's are generally monolithic bipolar silicon circuits rather than metal oxide-silicon (MOS) circuits. Prior to 1963, the CPU design relied on discrete components or hybrid thin-film circuits.

III. OPERATIONAL AND PHYSICAL CHARACTERISTICS OF AEROSPACE COMPUTERS

A. Speed

Probably one of the most important characteristics of a computer is its "speed", where speed is defined as the time required to accomplish the task for which the computer is programmed. Since computers are programmed for a wide variety of tasks, it is difficult to measure speed defined in this way, so other measures of speed are used. In particular, memory access or cycle times, instruction execution times, and input/output times are used separately or collectively to describe the speed of a machine. These times can be used to describe computer speed, in the manner defined above, only if they are mutually exclusive times. Buffered I/O, memory overlap, and instruction look-ahead allow these times to overlap and increase the effective speed of the machine. Nonetheless, they are good indicators of machine speed because they place an upper limit on the time required to perform a task. In fact, some studies have determined the mix of instructions necessary for performing a specific task and used this information to arrive at a "machine speed" applicable to the task.* Since the functions to be performed by

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*Leviakis, op.cit., p. 2, uses the Eason-Lane mix, which is a variation of the Gibson mix oriented toward automatic checkout problems.

spaceborne computers are not well defined at this time, the approach used here will be to discuss each of the operation times separately.

1. Instruction Execution Time

A good indication of instruction execution times can be obtained by determining the execution time of the add, multiply and divide instruction. Typically, add times will be much smaller than multiply times and multiply times will be slightly smaller than divide times. Other operations such as subtract, transfer, jump, and logic operations will require execution times roughly equivalent to the add time. In the 1962-1967 period, the shortest add time is 2 μsec (HCM-201 and ALERT). The longest add times are 624 μsec, for a serial machine with a drum memory, and 82 μsec, for a serial machine with a magnetic core memory. Most of the recently developed machines have parallel arithmetic units, and have add times less than 10 μsec, with some notable exceptions* which have add times from 20 to 30 μsec. In comparison, the add times of the IBM 360, for the best conditions of overlap, etc., range from 29 μsec for the model 30, through 0.8 μsec for model 75, to 0.18 μsec for the model 92.

It is much more difficult to generalize when discussing multiply and divide times since the variety of ways in which these operations can be done results in a variety of times. For instance, a machine (IBM 4 PI/EP) with 5 μsec add time has multiply and divide times of 9 and 18 μsec respectively, while a machine (Honeywell ALERT) with a 2 μsec add time requires multiply and divide times of 12 and 30 μsec respectively, and a third machine (Hughes HCM-201) with 6 μsec add time, requires 120 μsec for either multiply or divide operations. The best generalization that can be made is that multiply operations take approximately 2 to 60 times as long as an add operation, with an average of about 5 times as long, and divide operations take approximately 3 to 70 times as long as an add operation, with an average of about 8 times as long.

To provide a better perspective of the trends in instruction execution times, add times and multiply times of the computers in this survey have been plotted versus date of introduction in Figures 2 and 3. Add times have memory cycle time as their lower bound, and over the period covered in Figure 2, the shortest add times gradually decrease to 1/6 their pre-1962 minimum. This correlates with the trend toward faster memories. In any given year, there is a wide range of add times, indicating that there are applications where speed is often traded off in favor of power, and sometimes other characteristics, such as simplicity or volume. Note that the add time of the Apollo Guidance Computer (AGC) is an order of magnitude slower than the current state-of-the-art.

*Burroughs D-210, CDC 449, and MIT AGC.

Figure 3 shows that the fastest multiply times have sharply decreased to only 1/40 their pre-1962 minimum. The one point that falls far outside this pattern is item 35, the CDC 449, introduced in early 1967. Again, this shows that speed is not the only characteristic to be considered. Note that the multiply time of the AGC is almost an order of magnitude slower than the state-of-the-art.

2. Memory Cycle Time

Memory cycle time plays an important role in determining instruction execution times since the instruction execution time includes the time to fetch the instruction and, for some instructions, the time to fetch an operand. Of course, as previously mentioned, instruction look-ahead and memory overlap have been used at times to reduce the contribution that memory cycle time makes to the average instruction execution time. For example, the CDC 5400 reads 4 instructions from main memory at one time, and stores them in an instruction look-ahead memory in the CPU; and the 4 μsec add time of the Univac 1830A is decreased to 2 μsec (a 50% decrease!) if advantage is taken of memory overlap.

Computers in this survey have memory cycle times ranging from 27 μsec (ARMA Micro Computer) to 0.6 μsec (RCA VIC-36A), with the range from 2 to 6 μsec being most prevalent.

3. Input/Output (I/O) Time

I/O data rates are not given in the Appendix. The data rate is limited by the memory cycle time. Typical word transfer times (sec./word transferred) are equal to the memory cycle time, with some word transfer times being twice as long as the memory cycle time.

B. Software

The computers in this survey are provided with specially prepared assembly programs that can be run on commercial machines such as the IBM 7090. There are a few (Univac 1830A, IBM 4 PI, and NDC-1051A) which are provided with compilers. Most of them also have diagnostic programs for self-testing, and all of them are provided with software to allow simulation on a commercial machine so that programs can be checked out and debugged.

Some computers in this survey can be grouped into families of aerospace machines, all with the same instruction set but of different sizes and operational capabilities. This concept of a family of machines not only provides more flexibility in sizing a machine to a job, but allows software to be shared. An example of this concept is the Litton L-300 and L-3000 series, comprising 6 machines (only the L-304 and L-3050 have been built).

Another concept is that of a family of ground-based and aerospace machines, which alleviates the need for a simulator and special compilers and assemblers. This concept is typified by the Univac 1830A aerospace computer and 1230* ground-based computer, and the IBM 4 PI/EP aerospace computer and 360 ground-based computers (model 40 and up). In each case, the instruction set of the aerospace machine is a subset of the ground-based machine.

The fact that there are now aerospace computers which are directly compatible with ground-based machines is significant for three reasons. First, they do not require a simulator program, and program debugging becomes a more routine problem. Second, it makes available much of the software experience gained from work on the ground machine, including a greater pool of programming talent. Third, it indicates that technology has reached a point where the physical constraints imposed on aerospace computers have less effect on their computational capability than in the past.

C. Physical Characteristics

Aerospace computers have been characterized by being small (less than 1 cu. ft.), lightweight (less than 100 lbs.), and requiring power of about 100 watts. The increased use of integrated circuits and better interconnection techniques has resulted in a decrease in these volume and weight characteristics, but the trend toward a computer with greater functional capabilities, larger memories and more versatile input/output capabilities has resulted in power requirements which have remained near 100 watts or have increased.

The physical characteristics of aerospace computers of recent design fall into one of two broad categories, depending on the application for which they were designed. Those designed for specific, somewhat limited, applications in space are extremely small (on the order of 0.2-0.4 cu. ft.) and light (on the order of 25-40 lbs.), and have a power requirement of about 100 watts. Those designed either for general use in space applications or for a specific, highly demanding, space application weigh in the 50-75 lbs. range, have a volume less than but close to 1 cu. ft., and a power requirement in the 100 to 300 watt range. Figures 4, 5, and 6 are plots of the weight, size and power, respectively, of the computers in this survey versus the date of introduction.

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*The Univac 1230 is a ground-based machine built for NASA and has not been extensively marketed commercially.

D. Reliability

Reliability estimates, in terms of mean time between failures (MTBF), are given in the Appendix* for those computers for which an MTBF was available from manufacturers' data. The highest reliability claimed is an "equivalent MTBF"** of 25,000 hours for the IBM LVDC. Incorporating triple modular redundant (TMR) logic and duplex memory, there is a large class of single and multiple component failures that the LVDC can experience (even simultaneously) without exhibiting total system failure. However, two failures in the "right" places could cause system failure.

Four machines (D26C, D26J, HCM 205 and TRW 4418) claim MTBF's from 15,000 to 20,000 hours and the majority of the remainder are clustered around 5,000 hours MTBF. MTBF's tend to rise as integrated circuits and various redundancy techniques,*** such as those used in the Saturn LVDC, are used to a greater extent and as better interconnection techniques are perfected.

IV. AREAS FOR FUTURE RESEARCH IN SPACEBORNE COMPUTERS

There are several areas in which progress in aerospace computer technology is likely to occur or might be needed to meet the requirements of future spaceborne missions. The areas considered to be particularly important are system organization, circuit design, memory design, displays, and input techniques.

A. System Organization

Studies of computer system organization have as their goal increased computing capability, increased reliability, and greater ease in programming and maintenance. Present spaceborne systems are primarily centralized machines with a single central processor to receive a multitude of inputs, perform a processing function on a single stream of data with a single instruction

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*Table 2, Characteristics of Aerospace Computers.

**See Appendix, Table 3.

***The IBM OAO Primary Processor and Data Storage used quadruple component redundancy, TMR delay lines and duplex redundant memory. This equipment is not covered in the survey because it performs no arithmetic calculations.

stream, and provide a multitude of outputs. Attention is being given to other system organizations, such as

(1) those based on functional modularity,* where a separate small computer is assigned to a particular task and a simple, reliable "central organizer" integrates the operation of several of these small computers;

(2) multiprocessor systems, where problems are assigned under control of a central executive to one of several identical processors on an as-available basis. Such systems are characterized by the use of multiple streams of instructions, each operating on a single data stream; and

(3) associative parallel processors, which use a single instruction stream to perform simple logic operations on multiple data streams simultaneously.

Studies of these and other organizations, such as the SOLOMON type, which uses a single instruction stream to perform complex operations on multiple data streams simultaneously, are also being investigated for ground-based computers.

B. Circuit Design

Fabrication of integrated circuits has reached a point of high yield, and manufacturers are now attempting to solve the problems associated with putting functions more complex than a few gates on a single chip. This large scale integration (LSI) has the advantage of fewer external interconnections, reduced size, higher speeds, and greater reliability. The present problems include low yield in the manufacturing process, complicated testing procedures, power dissipation, and the absence of accepted logic design techniques using complex circuits. Research toward eliminating these problems includes development of techniques for optimum interconnection of the "good" parts of a single LSI chip (referred to as discretionary wiring), the perfecting of manufacturing and testing processes, and development of new logic design techniques. Of course, counters and shift registers lend themselves well to LSI techniques, but for general use of off-the-shelf LSI circuits, techniques must be developed for designing combinatorial circuits using basic building blocks more complex than individual gates.

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*"Computers and Displays/Controls", Donald J. Pizzicara, Litton Systems, Inc., February 1966, AD 631663.

C. Memory

A most important area for progress in spaceborne computer technology is memories, both from the point of view of need and the point of view of possibility of success. The need is clear--memory contributes a significant share (typically 50% of a "standard" memory size) of the weight, volume and power requirements of present spaceborne computers. For advanced manned missions, vast amounts of bulk storage, as well as increased speed and capacity in prime memory, will be desirable.*

The possibility of success in improving memories appears good. Presently anticipated bulk memory capacity requirements could be satisfied using tape recorders. Furthermore, increased research on plated-wire memories which would greatly reduce power requirements, and research on mass storage media which would greatly reduce volume and weight requirements (including those using optical techniques), is being conducted. LSI techniques in memory circuits and memory elements also appear promising.**

D. Displays and Input Devices

Displays and input devices have not been discussed in this survey because they are generally designed for a specific task. They are mentioned here because of the increased sophistication that will be required of displays and input devices on manned missions of long duration.*** The entire area of man-machine interfaces, including programming

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*10^7 - 10^8 bits is the estimated requirement for program storage on a manned planetary flyby mission in the mid-70's. See "The Flow of Data in Advanced Manned Missions", E. L. Gruman, et al, Bellcomm, Inc., December 28, 1966.

**For a description and evaluation of research being undertaken in these and other techniques, see "Memory Technology for Manned Deep Space Missions - Final Report to NASA Electronics Research Center," MITRE Technical Report MTR-382, February 14, 1967; The MITRE Corporation, Bedford, Massachusetts, (Controlled Distribution).

***For a discussion of these needs, see "Functional Requirements of Spaceborne Computers on Advanced Manned Missions", E. L. Gruman and P. S. Schaenman, Bellcomm, Inc., TM-66-1031-2, October 24, 1966.

languages, color displays, high resolution displays, voice insertion and voice output, is being studied in many places, including the Manned Computer Systems Branch of NASA's Electronic Research Center, Cambridge, Massachusetts.

Donald O. Baechler

1031-DOB-jdc D. O. Baechler

Attachments
Appendix
Tables 1 thru 5
Figures

APPENDIX

TABLE 1: ALPHABETIC LIST OF AEROSPACE COMPUTERS

Table 1, the alphabetic list of the computers surveyed, indicates the year introduced. Each year is divided into three parts--early, mid, and late--and the "date of introduction" indicated for each computer is based on the best information available for the date when the machine was first considered operational; that is, sometime after it was first announced, but earlier than the date of first delivery. The reference number refers to Table 2, Characteristics of Aerospace Computers.

TABLE 2: CHARACTERISTICS OF AEROSPACE COMPUTERS

This table lists the computers in chronological order based on their date of introduction. They are numbered sequentially to provide a cross-reference from the alphabetical list. The conventions used in this table are described below:

1. Name: Manufacturer's name, followed by other identifying names or numbers. Date of introduction is also given.

2. Data Flow: S = serial, or P = parallel, indicates the way data flows in the arithmetic unit; S/P indicates a combination of serial and parallel, and is explained in the "comments" column.

3. Data Type: Fx = Fixed point, Fl = Floating point.

4. No. of Instructions: This is the number of instructions in the instruction set, and does not include variations of basic instructions.

5. Computing Times: No memory overlap is assumed.

6. Memory: "Capacity (MIN)" is the standard memory size for the machine, and "Capacity (MAX)" is the maximum size attainable by adding standard modules.

7. Input/Output: These numbers were obtained from manufacturers' descriptions. Different manufacturers define "channel" in different ways, and interrupts listed in specifications sometimes include internal interrupts as well as external interrupts. Therefore, care should be taken in using the numbers listed.

8. Physical Characteristics: Under "Type of Hardware" the following abbreviations are used:

IC - Integrated Circuits

DCTL - Direct-Coupled Transistor Logic

DTL - Diode-Transistor Logic

TTL - Transistor-Transistor Logic

HL - High Level, as in HLTTL.

The weight, size, and power requirements are given for a machine with a "standard size" memory.

9. MTBF: This is a figure obtained from the manufacturer. The method of calculating the reliability may vary from manufacturer to manufacturer.

10. Comments: Comments describe unique or interesting features, or further explain an entry in the preceding columns.

TABLES 3, 4 and 5: DATA SHEETS

A more complete description than that given in Table 2, Characteristics of Aerospace Computers, is provided for the three machines used in the Apollo program. These are the IBM Launch Vehicle Digital Computer used in the Saturn IB/V (Table 3), the MIT Block II Apollo Guidance Computer used in the Command Module and, in a slightly different configuration, in the Lunar Module (Table 4), and the TRW Marco 4418, used in the Lunar Module as the Abort Electronics Assembly (Table 5).

TABLE 1

ALPHABETIC LIST OF SPACEBORNE COMPUTERS

Name	Reference Number	Year Introduced
AC Spark Plug MAGIC	1	Pre 1962
ARMA Micro Computer	5	Mid 1962
ARMA Micro D	21	Mid 1966
Autonetics D26C	27	Late 1966
Autonetics D26J	16	Late 1965
Burroughs D-210	2	Pre 1962
CDC 449	35	Early 1967
CDC 5360	22	Mid 1966
CDC 5400	28	Late 1966
Computing Devices of Canada AN/UYK-501	23	Mid 1966
General Precision AN/ASN-24	8	Mid 1963
Honeywell ALERT	17	Late 1965
Honeywell Subminiature Computer	3	Pre 1962
Honeywell SIGN III	29	Late 1966
Hughes HCM-201	6	Mid 1962
Hughes HCM-202	9	Mid 1963
Hughes HCM-205	30	Late 1966
Hughes HCM-206	38	Development
IBM 4 PI/CP	31	Late 1966
IBM 4 PI/EP	32	Late 1966

Table 1

Name	Reference Number	Year Introduced
IBM 4 PI/TC	36	Early 1967
IBM Gemini Guidance Computer	7	Early 1963
IBM Saturn IB/V LVDC	10	Mid 1963
Litton L-304	14	Early 1965
Litton L-3050	39	Development
MIT Block I AGC	11	Late 1963
MIT Block II AGC	33	Late 1966
Nortronics NDC-1051	15	Early 1965
Nortronics NDC 1051A	18	Early 1966
RCA VIC-36A	40	Development
SAAB CK37	13	Mid 1964
Sperry Mark XII	19	Early 1966
Sperry Mark XIV	24	Mid 1966
Sperry Mark XVI	34	Late 1966
TI 2501	25	Mid 1966
TRW Marco 4418	20	Early 1966
Univac 1818	37	Early 1967
Univac 1824	12	Late 1963
Univac 1830-A	26	Mid 1966
Univac ADD-1000	4	Pre 1962

TABLE 2 - CHARACTERISTICS OF AEROSPACE COMPUTERS

NAME / DATE INTRODUCED	DATA FLOW	DATA TYPE	NO. OF INSTRUCTIONS	COMPUTING TIME, μ SEC			MEMORY						IN/OUTPUT		PHYSICAL CHARACTERISTICS				MTBF (HRS)	COMMENTS
				ADD	MULT	DIV	TYPE	WORD SIZE (BITS)	CAPACITY (WORDS) MIN	CAPACITY (WORDS) MAX	ACCESS TIME (μ SEC)	CYCLE TIME (μ SEC)	NO. OF CHANNELS	NO. OF INTERRUPTS	TYPE OF HARDWARE	WEIGHT (LBS)	SIZE (CU. FT.)	POWER (WATTS)		
1. AC SPARK PLUG MAGIC PRE 1962	S	Fx	16	70	258	398	DRO CORE	24	4K			4	2	1	DCTL IC	40	0.75	90		MEMORY READOUT IS SERIAL, 2 BITS AT A TIME
2. BURROUGHS D210 PRE 1962	P	Fx	16	30	580	680	DRO CORE CORE ROPE CORE ROPE	24 16 50	256 1K 256	1K 16K 1K	 10 10	15	2	1	MAGNETIC LOGIC	19	0.25	100	7000	USES CORE NULL-DECODER REGISTERS FOR LOGIC. INSTRUCTIONS ARE 16 BITS, DATA IS 24 BITS. 50-BIT ROPE USED FOR MICROPROGRAMMING.
3. HONEYWELL SUB-MINIATURE COMPUTER PRE 1962	S/P	Fx	16	12	242	606	NDRO BIAX	48	3K	8K			80		DISCRETE COMPONENTS	20	0.5	46		SERIAL BYTES OF 6 BITS. MEMORY WORD HAS 3 INSTRUCTION OR 2 DATA WORDS. ONE COMMAND IS A SPARE.
4. UNIVAC ADD-1000 PRE 1962	P	Fx	16	12	711	837	DRO THIN FILM NDRO THIN FILM	24 24	256 7K		 3	3	16	4	DISCRETE COMPONENTS	88	1.1	262		NDRO MEMORY HAS 50 MILLISEC WRITE TIME FROM EXTERNAL EQUIPMENT.
5. ARMA MICRO COMPUTER MID 1962	S	Fx	19	27	135	324	NDRO CORE	22	2K	8K		27	2		DISCRETE COMPONENTS	20	0.4	50		REGISTERS ARE DELAY LINES.
6. HUGHES HCM-201 MID 1962	P	Fx	30	6	120	120	DRO CORE OR NDRO CORE OR DRUM	24 24 24	4K 16K 1500K			6	3	1	DISCRETE COMPONENTS	51		150		CHOICE OF ONE OF THE THREE MEMORIES AVAILABLE.
7. IBM GEMINI GUIDANCE COMPUTER EARLY 1963	S	Fx	16	140	420	840	NDRO CORE	39	4K			4	5	0	DISCRETE COMPONENTS	59	1.65	85		CONCURRENT MULTIPLY/DIVIDE. 13 BITS OF MEMORY WORD ARE READ-ONLY. INSTRUCTION WORD, 13 BITS; DATA WORD, 26 BITS.
8. GENERAL PRECISION AN/ASN-24 MID 1963	S	Fx	12	624	4K	4K	DRUM	25	4K				1	0	DISCRETE COMPONENTS	100	1.2	420		HAS INDEPENDENT, PROGRAMMABLE INTEGRATOR. USES TWO ADDRESSES, OPERAND AND NEXT INSTRUCTION.
9. HUGHES HCM-202 MID 1963	P	Fx	30	6	120	120	DRO CORE NDRO THIN FILM	24 24	512 1024	4K 8K		6 6	3	1	HYBRID THIN FILM	51		150		OTHER MEMORY TYPES ARE AVAILABLE.
10. IBM SATURN IB/V LVDC MID 1963	S	Fx	14	82	328	656	DRO CORE	28	4K	32K	28		1	1	DTL HYBRID	80	2.1	138		REGISTERS ARE GLASS DELAY LINES. CONCURRENT ADD AND MULTIPLY. TWO PARITY BITS IN MEMORY WORD.
11. MIT BLOCK I AGC LATE 1963	P	Fx	11	23.4	117	210	DRO CORE CORE ROPE	16 16	1K 10K			11.4 11.4		8	DCTL IC	87	1	125		SOME I/O HANDLED THROUGH COUNTER INTERRUPTS.
12. UNIVAC 1824 LATE 1963	P	Fx	41	8	92	128	DRO THIN FILM NDRO THIN FILM	24 48	512 4K		 0.7	4	8	1	DTL IC	31.5	0.47	110	10,000	DATA WORD, 24 BITS; INSTRUCTION WORD, 16 BITS.
13. SAAB CK 37 MID 1964	P	Fx	48	5.6	23.8		DRO CORE	26							IC	100		350		MOST COMMOM OPERATIONS USE 13-BIT INSTRUCTION WORD, WITH 13-BIT OPERAND STORED IN OTHER HALF OF THE WORD.
14. LITTON L-304 EARLY 1965	P	Fx	63	5.6	61		DRO CORE	32	4K	131K		1.8	8	1	TTL IC	34	0.26	100	2300	DATA WORD, 16 BITS; INSTRUCTION WORD, 32 BITS
15. NORTRONICS NDC-1051 EARLY 1965	P	Fx	51	8	70	176	DRO CORE	24	2K	8K	2	4	1	4	IC	29	0.5	94	8500	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 2K MEMORY.
16. AUTONETICS D26J LATE 1965	P	Fx	27	8	18	18	DRO CORE	12	4K	8K		4	4	2	DTL IC	20	0.21	62	18,000	16-BIT WORD OPTION IS AVAILABLE.
17. HONEYWELL ALERT LATE 1965	P	Fx	89	2	12	30	NDRO BIAX	24	4K	32K	1	4	3	24	HLTTL IC	73	1.2	150	10,000	AVAILABLE OPTIONS INCLUDE DRO CORE WITH 1 μSEC CYCLE TIME, AND BUFFERED I/O WITH 7 CHANNELS
18. NORTRONICS NDC-1051A EARLY 1966	P	Fx	51	6	26	50	DRO CORE	14	8K	32K		2	2	8	DTL IC	38	0.87	225	3060	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 16K MEMORY.
19. SPERRY MARK XII EARLY 1966	P	Fx	13	18	60		DRO CORE	21	6K				1		IC	64	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
20. TRW MARCO 4418 EARLY 1966	P	Fx	27	10	70	73	DRO CORE	18	4K	8K		5	1	0	DTL IC	34	0.4	75	20,000	MEMORY CAN BE PARTIALLY HARD-WIRED.
21. ARMA MICRO D MID 1966	S	Fx		12	168		DRO CORE NDRO CORE	18 18	128 1920				2		IC	5	0.07	20	50,000	MTBF EXCLUDES POWER SUPPLY.
22. CDC 5360 MID 1966	P	Fx	41	12	90	90	DRO CORE	24	4K	32K	1.5	6	12	1	IC	26	0.6	95	7545	WEIGHT AND SIZE EXCLUDE POWER SUPPLY.
23. COMPUTING DEVICES OF CANADA AN/UYK-501 MID 1966	P	Fx	110	8	110	118	DRO CORE	24	4K	32K	1	2	1	64	IC	82	0.96	240	1180	WEIGHT, SIZE, POWER AND MTBF ARE GIVEN FOR 8K MEMORY. HAS ALTERABLE MICROPROGRAM.
24. SPERRY MARK XIV MID 1966	P	Fx	13	18	60		DRO CORE	21	6K				1		IC	64	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
25. TI 2501 MID 1966	P	Fx	36	4	27	37	DRO CORE	32	4K	16K		2	17	32	IC	65	1.1	350		WEIGHT, SIZE AND POWER ARE GIVEN FOR 4K MEMORY.
26. UNIVAC 1830-A MID 1966	P	Fx	72	4	20	34	DRO CORE	30	4K	131K		2	32	1	IC	200	2.65	567	4500	ALSO HAS DRO THIN FILM CONTROL MEMORY AND 64-WORD CORE ROPE BOOTSTRAP MEMORY. SUCCESSOR TO 1830.
27. AUTONETIC D26C LATE 1966	P	Fx	87	12	45		DRO CORE DRO CORE	30 30	8K 256	32K		6 1	2	8	IC	47	0.65	175	15,600	HIGH-SPEED MEMORY USED FOR SCRATCH PAD.
28. CDC 5400 LATE 1966	P	Fx	73	3.1	25	275	DRO CORE NDRO THIN FILM	24 96	4K 3K			2.5 2.5	5	16	IC	60	1.1	140	2500	4-WORD (96-BIT) READOUT FROM NDRO MEMORY TO AN INSTRUCTION LOOK-AHEAD MEMORY.
29. HONEYWELL SIGN III LATE 1966	P	Fx	53	4	24	24	DRO CORE	20	2K	4K	0.65	2.0	5	1	DTL IC	28	0.49	92		HAS DOUBLE PRECISION ADD INSTRUCTION.
30. HUGHES HCM-205 LATE 1966	P	Fx	42	4	24	25	DRO CORE	18	2K	8K		2.0	1	1	DTL IC	16	0.2	110	4000	WEIGHT, SIZE AND POWER ARE GIVEN FOR 2K MEMORY.
31. IBM 4 PI/CP LATE 1966	P	Fx	34	6.6	29.1		DRO CORE	32	8K	32K	0.9	2.5	3	5	TTL IC	57	.85	250	3000	HAS 1024-2048 WORD MICROPROGRAMMING MEMORY, 70 BITS/WORD, 155 NSEC ACCESS TIME. AVAILABLE WITH 51 OR 77 INSTRUCTIONS. AVAILABLE AS CP-2 WITH HARDWARE DECODE INSTEAD OF MICROPROGRAM.
32. IBM 4 PI/EP LATE 1966	P	FL	135	5.8	9.5	18.3	DRO CORE	36	8K	128K	0.9	2.5	3	5	TTL IC	62	0.9	303	5000	3K x 100 BITS MICROPROGRAMMING MEMORY. FLOATING POINT OPTION. 32-BIT DATA WORD. 1 PARITY BIT PER 8-BIT BYTE.
33. MIT BLOCK II AGC LATE 1966	P	Fx	34	23.4	46.8	81.9	DRO CORE CORE ROPE	16 16	2K 36K			11.4 11.4	15	10	DCTL IC	58	1.0	100		HAS DOUBLE PRECISION ADD.
34. SPERRY MARK XVI LATE 1966	P	Fx	14	12	34		DRO CORE	21	8K	16K		6	4		IC	60	1.5	250		MEMORY CAN BE PARTIALLY HARD-WIRED.
35. CDC 449 EARLY 1967	P	Fx	36	28	604		DRO THIN FILM NDRO μBIAX	24 24	256 3840				1	1	IC	12	.083	4.0		INCLUDES BATTERIES, KEYBOARD AND DIAL READOUT. 12-BIT PARALLEL, 2 BYTE SERIAL.
36. IBM 4 PI/TC EARLY 1967	P	Fx	54	15	51		DRO CORE	8	16K			2.5			TTL IC	27	0.48	75	7500	2 BYTE SERIAL, 8-BIT PARALLEL. MEMORY SIZE GIVEN IN TERMS OF 8-BIT BYTES. DATA WORD IS 2 BYTES AND INSTRUCTION WORD IS 1,2 OR 3 BYTES.
37. UNIVAC 1818 EARLY 1967	P	Fx	28	4	22	22	DRO CORE CORE ROPE	18 18	1K 4K	8K		2 2	12	10	IC	35	0.7	197	1500	WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY.
38. HUGHES HCM-206 DEVELOPMENT	P	Fx	64	2	15		DRO CORE	32	8K	32K		2	2	32	DTL IC	20	0.375	250	6400	INSTRUCTION WORD CAN BE 16 OR 32 BITS.
39. LITTON L-3050 DEVELOPMENT	P	Fx	62	3.3	6		DRO CORE	32	4K	131K		1.6	1	64	IC	44	.33	130	2100	WEIGHT, SIZE AND POWER ARE GIVEN FOR 8K MEMORY.
40. RCA VIC-36A DEVELOPMENT	P	FL					DRO CORE DRO CORE	38 38	8K 512	32K	.650 .326	3.0 0.6	4	4	IC	120	2.6	325		SOME DISCRETE COMPONENTS USED. VARIABLE INSTRUCTIONS CONTROL MICROPROGRAM.

TABLE 3

IBM SATURN IB/V LVDC

TYPE: Serial

DATA WORD LENGTH: 26 bits

NUMBER SYSTEM: Binary, fixed point, 2's complement

INSTRUCTION WORD LENGTH: 13 bits

NUMBER OF INSTRUCTIONS: 18 instructions from 4-bit operation code

INSTRUCTION EXECUTION TIMES:

Add: 82 μsec
Multiply: 328 μsec
Divide: 656 μsec

(Note: Add/subtract can be performed concurrent with multiply/divide.)

ADDRESSING: Single 9-bit address. 8 bits specify one of 256 locations in a memory sector, ninth bit chooses either (1) a base sector called residual memory or (2) a memory sector specified by a 4-bit sector select register.

MEMORY:

Word Length: 26 bits plus 2 parity bits (one for each 13 bits)

Type: Coincident current core, capable of duplex operation

Cycle time: 2 μsec

Capacity: 4K expandable to 32K

INPUT/OUTPUT: One external interrupt. I/O accomplished through the Launch Vehicle Data Adapter (LVDA). Data path is from accumulator or memory to the LVDA, and from the LVDA to the accumulator only.

PHYSICAL CHARACTERISTICS:

Weight: 80 pounds

Volume: 2.1 cubic feet

Power: 138 watts (with 16K memory)

Construction: Hybrid DTL circuits organized in a Triple Modular Redundant (TMR) configuration of three simplex channels, each composed of seven functional modules.

Table 3

SOFTWARE: Assembler available. Simulator for use on IBM 7090/94.

RELIABILITY: Memory duplexing and TMR logic results in calculated reliability ranging from 0.9901 at 100°C to 0.9924 at 60°C for a 250 hour mission. MTBF's required of a nonredundant machine to achieve the same reliability under the same restraints are 25,000 hours and 33,000 hours, respectively.

TABLE 4

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

BLOCK II APOLLO GUIDANCE COMPUTER (AGC)

TYPE: Parallel

DATA WORD LENGTH: 15 bits

NUMBER SYSTEM: Binary, fixed point, modified 1's complement

INSTRUCTION WORD LENGTH: 15 bits

NUMBER OF INSTRUCTIONS: 34 instructions from a 3-bit operation code by programmed setting of an extension register and use of some address bits when certain memory banks are addressed.

INSTRUCTION EXECUTION TIMES:

Add: 23.4 μsec (double precision, 35.1 μsec)

Multiply: 46.8 μsec

Divide: 81.9 μsec

ADDRESSING: Single 12-bit address specifies 38,912 memory locations using memory bank selection registers. (This method is capable of addressing 67,584 locations.)

MEMORY:

	Fixed memory	Erasable memory
Word length:	15 bits plus one parity bit	15 bits plus one parity bit
Type:	Core Rope	Coincident current core
Cycle time:	11.4 μsec	11.4 μsec
Capacity:	36,864 words	2048 words

INPUT/OUTPUT: The I/O data path is between the accumulator and the 15 registers in the I/O control unit. The control unit contains a priority interrupt system.

Table 4

PHYSICAL CHARACTERISTICS:

Weight: 58 pounds

Volume: 1 cubic foot

Power: 100 watts

Construction: Uses 2765 flatpacks, each flatpack contains a dual 3-input DCTL IC NOR gate.

SOFTWARE: Simulator and assembler for use with Honeywell 1800.

TABLE 5

TRW MARCO 4418

LUNAR MODULE ABORT ELECTRONICS ASSEMBLY

TYPE: Parallel

DATA WORD LENGTH: 18 bits

NUMBER SYSTEM: Binary, fixed point, 2's complement

INSTRUCTION WORD LENGTH: 18 bits

NUMBER OF INSTRUCTIONS: 27 instructions from 5-bit operation code

INSTRUCTION EXECUTION TIMES:

Add: 10 μsec

Multiply: 70 μsec

Divide: 73 μsec

ADDRESSING: Single 13-bit address. 3-bit central index register.

MEMORY:

Type: DRO core, some of which can be hard-wired

Cycle time: 5 μsec

Word length: 18 bits

Capacity: 4K words, expandable to 8K

INPUT/OUTPUT: No interrupts. I/O registers attach to main bus. In Lunar Module, D/A, pulse and discrete output circuits are used.

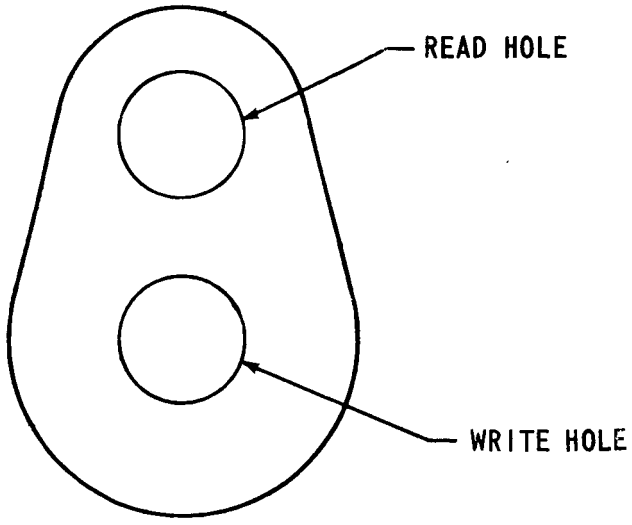
PHYSICAL CHARACTERISTICS:

Weight: 34 pounds

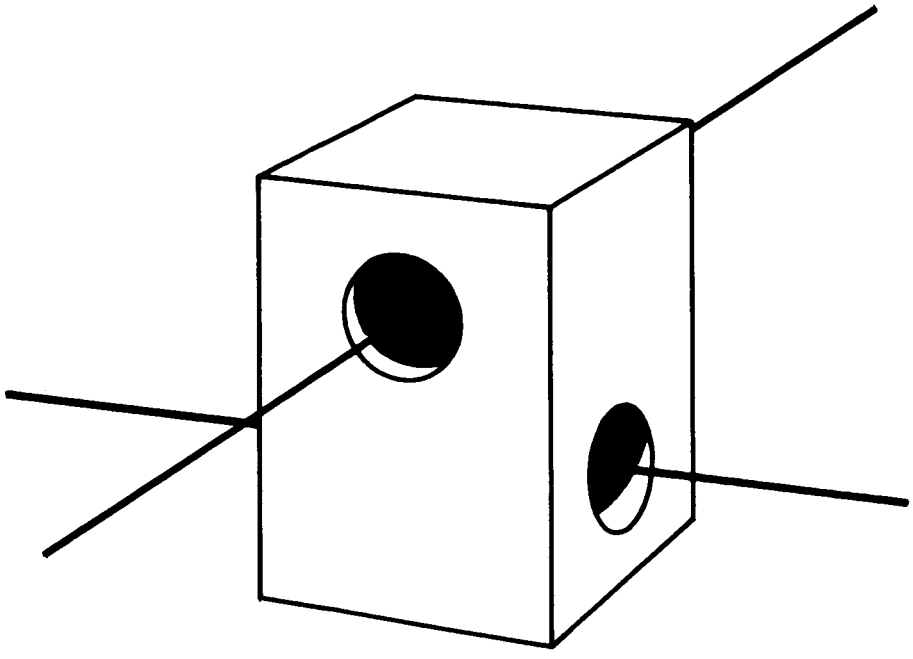
Volume: 0.4 cubic feet

Power: 75 watts

Construction: Uses 1300 flatpacks on 15 ten-layer MLB's. Flatpacks are Signetics SE100 DTL IC.



a) TRANSFLUXOR



b) BIAX

FIGURE I - MULTIAPERATURE DEVICES

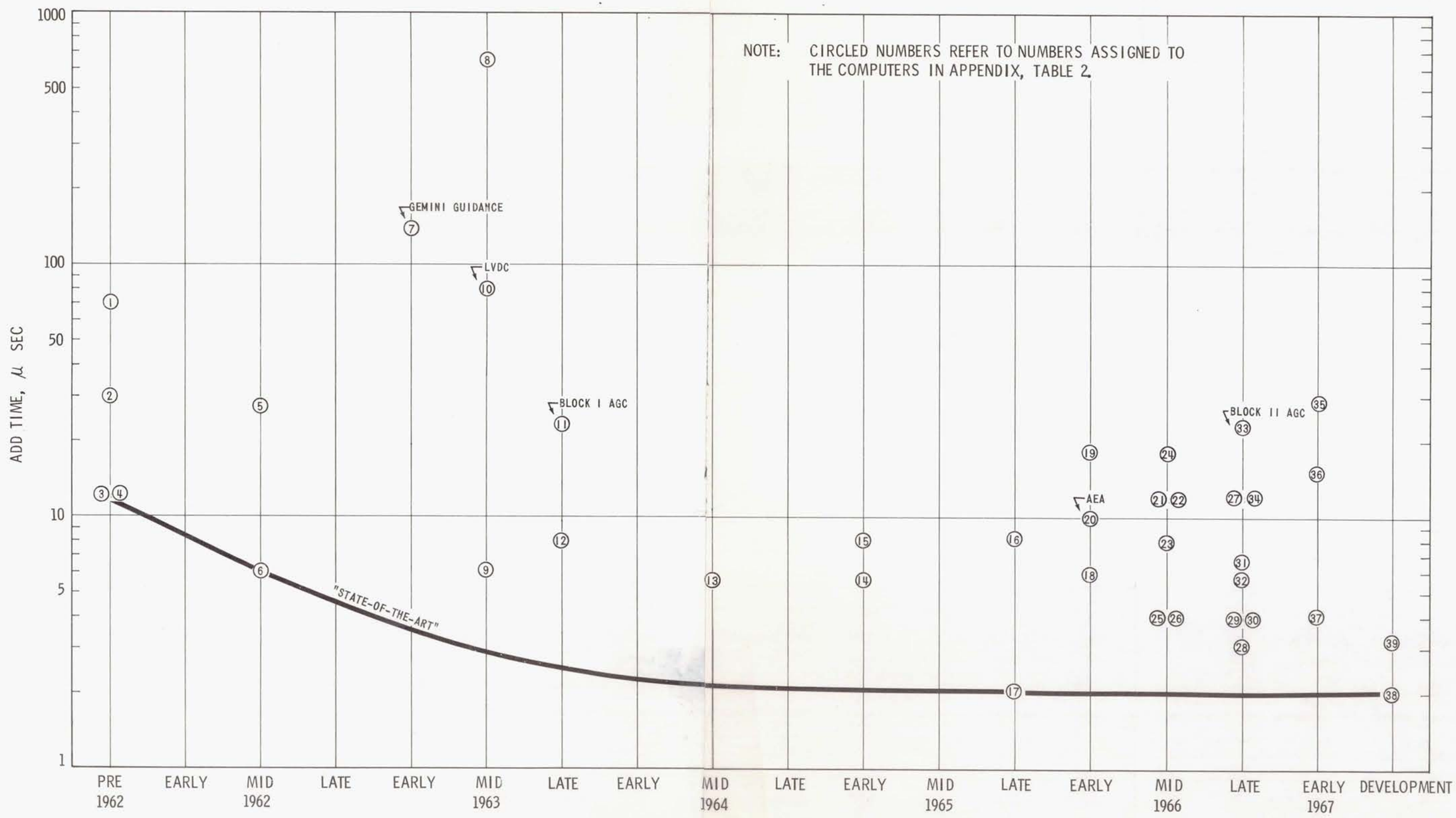


FIGURE 2 - ADD TIMES OF AEROSPACE COMPUTERS

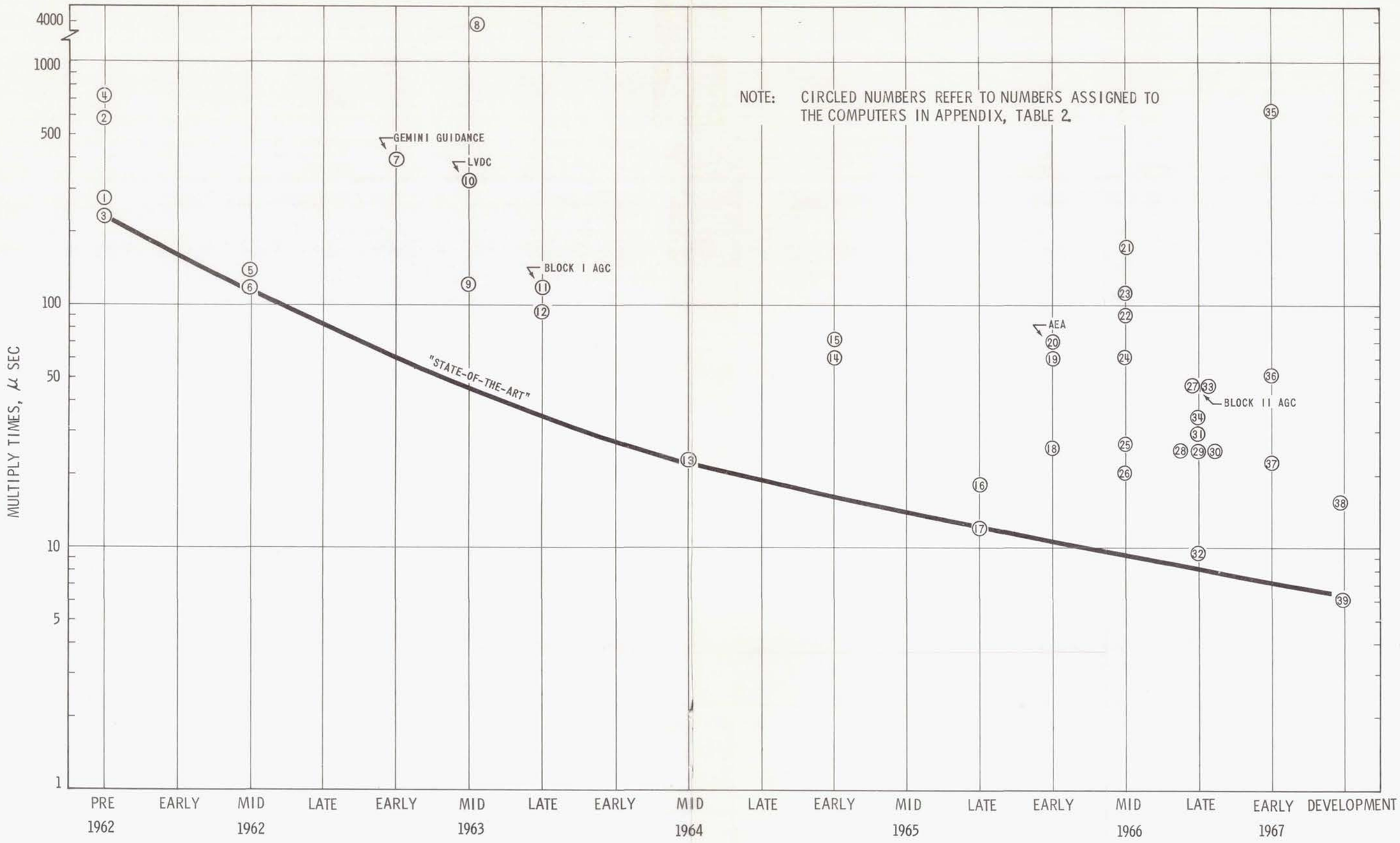


FIGURE 3 - MULTIPLY TIMES OF AEROSPACE COMPUTERS

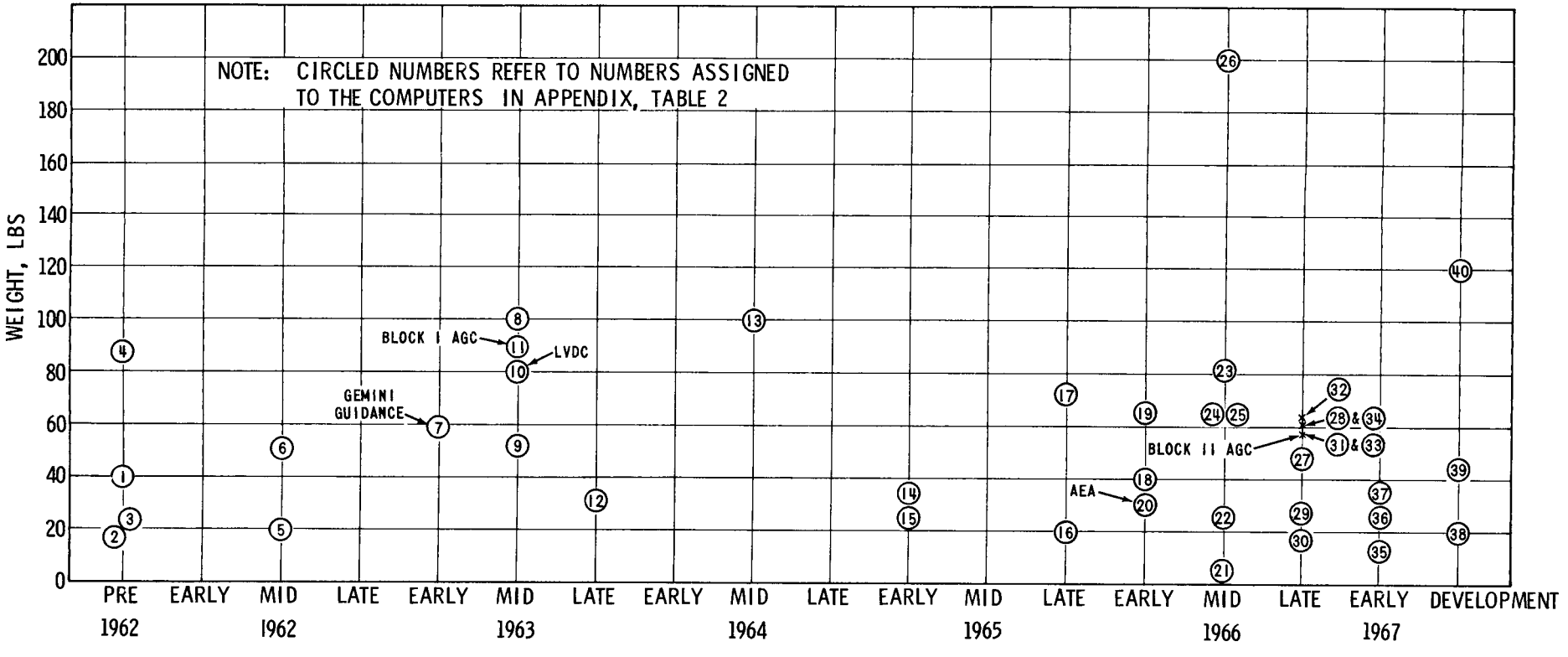


FIGURE 4 - WEIGHTS OF AEROSPACE COMPUTERS

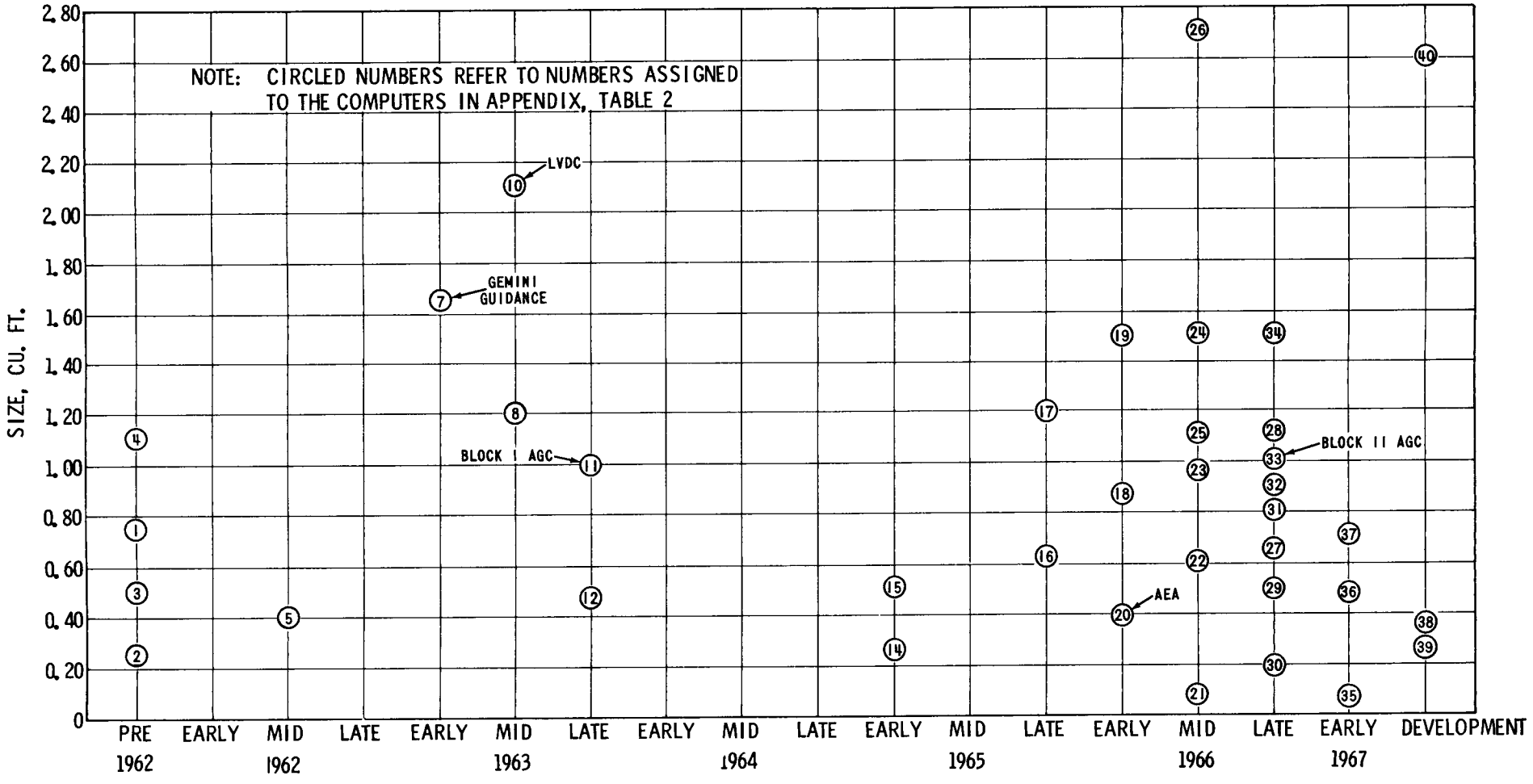


FIGURE 5 - SIZES OF AEROSPACE COMPUTERS

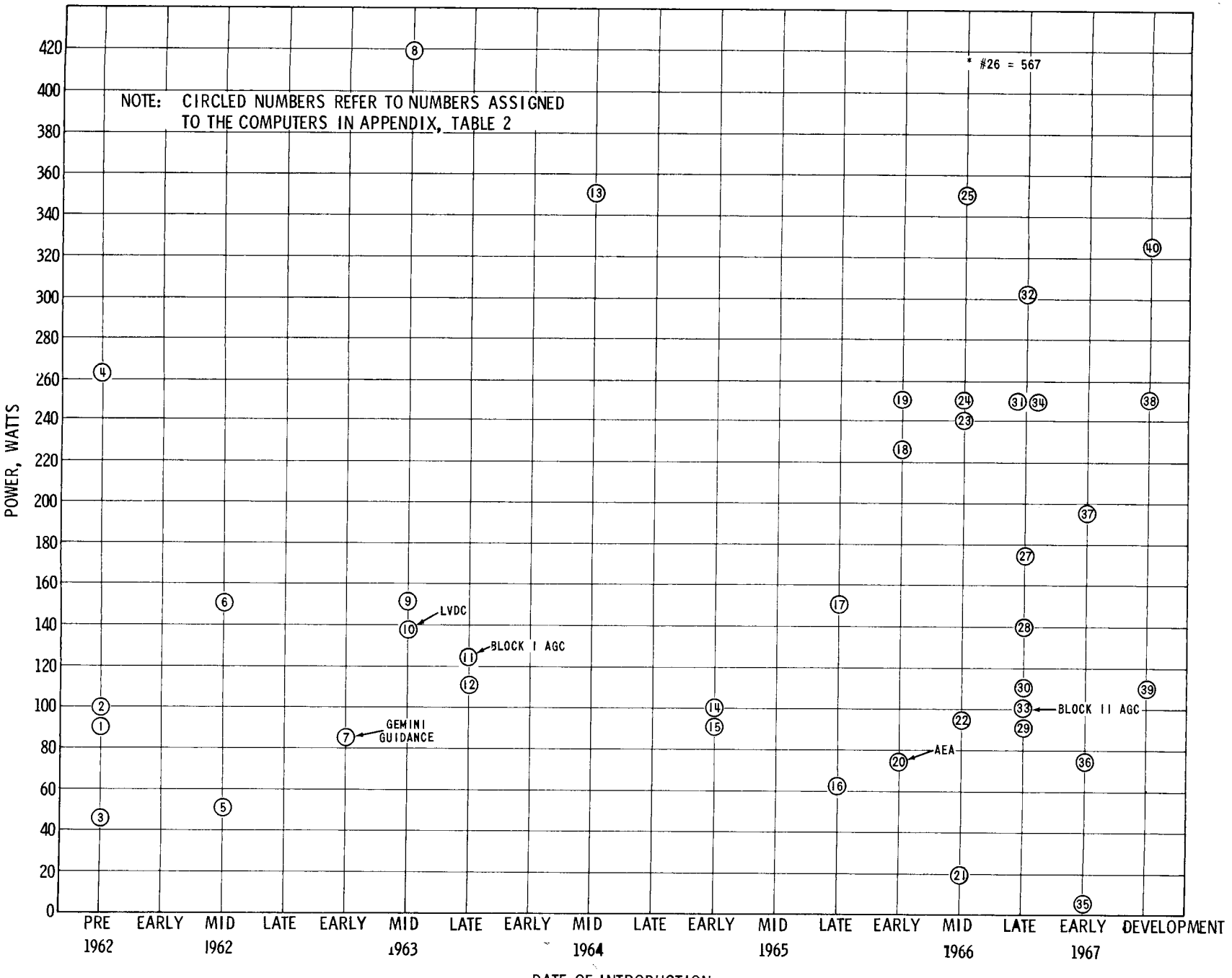


FIGURE 6 - POWER REQUIREMENTS OF AEROSPACE COMPUTERS