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PLACE 2.0—An Interactive Program for PLL Analysis and Design

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Phase Locked Loop Analysis and Circuit Emulation (PLACE) is an interactive program to assist in the design of Phase Locked Loop (PLL) systems. Written in C language, PLACE computes the loop filter components (up to active third-order filters); performs a stability analysis (finding the phase margin and damping ratio); and calculates the lockup time, hold range, and capture range. PLACE computes the PLL output jitter response due to incoming reference signal jitter, output jitter due to reference leakage through the phase detector, and output jitter response due to phase noise of the PLL components. The open and closed loop gain and phase, as well as jitter response, is plotted. Additional features found in PLACE 2.0 are frequency and magnitude of jitter peaking; a sensitivity analysis, which computes changes in loop performance as a function of component variation; and an interactive routine to help the designer optimize PLL performance. Currently residing on Digital Equipment Corporation's *VAX-11/780*, AT&T 3B20, and IBM System/370 processors, PLACE is presently available at most AT&T Bell Laboratories locations. This paper illustrates the capabilities of PLACE, shows several examples, and discusses the required calculations.

I. INTRODUCTION

Phase Locked Loops (PLLs) are used extensively in communication systems. Yet there has been no generally available computer-aided design program specifically targeted to assist the PLL designer in evaluating the performance of his system *before* building it in the

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laboratory. Phase Locked Loop Analysis and Circuit Emulation (PLACE) is an interactive program that allows the designer to optimize his PLL, trading off one parameter (e.g., lockup time) for another (e.g., jitter response). PLACE performs the following functions:

1. Determines if the PLL is stable by computing the phase margin, damping ratio, and undamped natural frequency. PLACE accounts for any parasitic Voltage Controlled Oscillator (VCO) or operational amplifier poles, and phase shift due to the feedback counter.
2. Finds the appropriate loop filter components for a given damping ratio or 3-dB frequency. PLACE notifies the user if desired loop parameters result in unrealistic component values.
3. Computes the PLL system bandwidth, noise bandwidth, and loop filter bandwidth.
4. Approximates the hold range, capture range, and lockup time. (The hold range is normalized for the active loop filter case.)
5. Determines the output jitter response due to the internal phase noise of the PLL components and the output jitter response due to jitter on the incoming reference signal.
6. Determines the sensitivity of PLL performance to component variation.
7. Plots open and closed loop gains, and phase noise response.

Section II of this paper discusses PLACE input/output, Section III shows several examples, and Section IV explains the calculations that PLACE performs.

II. PLACE 2.0 INPUT/OUTPUT

2.1 PLACE 2.0 user input

PLACE consists of a nongraphics module followed by a graphics module. The two modules are independent, and thus a user can invoke PLACE on a nongraphics terminal. PLACE recognizes the PLL shown in Fig. 1, where we have defined the following constants:*

K_p = phase detector gain constant (V/rad)
K_V = VCO gain constant (Hz/V)
N_{FB} = feedback counter divisor
N_{FF} = feed-forward counter divisor.

The program will ask the user for the values of these constants. Typical values for K_p are 1.4 V/rad for an exclusive-or gate, 0.4 V/rad for the RCA 4046 phase comparator II, 0.11 V/rad for the Motorola 4044 phase detector, and 0.16 V/rad for the Motorola 12040.

For best results, the VCO gain constant should be measured because the PLL stability is highly dependent on K_V. The value of K_V will

* Variables used in this paper are defined in Appendix A.

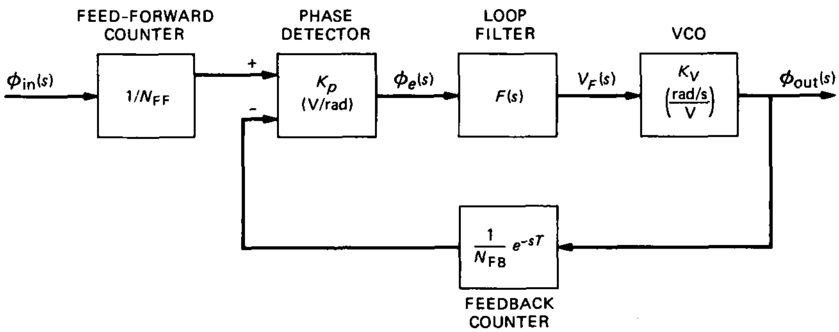

Fig. 1—PLL model depicting the required input parameters for PLACE.

most likely vary over the VCO's frequency range; the sensitivity analysis will compute the effect of this variation. If the results are unacceptable, the user will need to build a linearizer in order to maintain a constant K_V. (See Ref. 1 for an excellent example, or Ref. 2.) If a passive attenuator is used ahead of the VCO, the entered value of K_V must be reduced by the attenuation factor. For frequency synthesizer applications, the feedback divisor N_{FB} is often a variable, and running PLACE twice with the maximum and minimum values will show the change in loop performance.

Next, PLACE asks the user if it is desired to account for any parasitic VCO pole; if a Voltage Controlled Crystal Oscillator (VCXO) is used, it is strongly recommended that this pole be entered since it is often the dominant pole of the PLL. (See Section 4.1.4 on how to measure the VCO pole.) For the active loop filter case, if it is desired to account for the op amp pole, the designer may lump this pole into the VCO pole and enter the value at this time.

Next, PLACE asks for the reference frequency, i.e., the frequency entering the phase detector. The reference frequency is the frequency at which the phase comparison is performed. This information is required for the jitter analysis and implicitly defines the output frequency of the PLL.

PLACE will then ask the user for the type of loop filter desired. Five types of loop filters are recognized (see Fig. 2):

1. No loop filter, where

$$F(s) = 1.$$

2. Resistor Capacitor (RC) loop filter, where

$$F(s) = \frac{1}{1 + \tau s},$$

where $\tau = RC$.

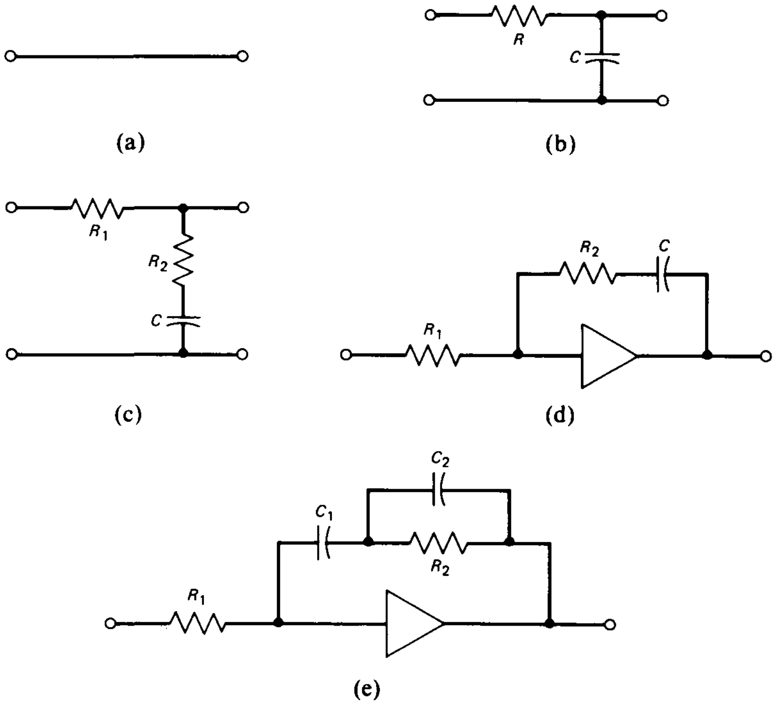

Fig. 2—Loop filter topologies: (a) No loop filter, (b) RC loop filter, (c) lag-lead loop filter, (d) second-order active filter, and (e) third-order active filter.

3. Lag-lead loop filter, where

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},$$

where $\tau_1 = (R_1 + R_2)C$, $\tau_2 = R_2C$.

4. Second-order active filter, where

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s},$$

where $\tau_1 = R_1C$, $\tau_2 = R_2C$.

5. Third-order active filter, where

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s(1 + \tau_3 s)},$$

where $\tau_1 = R_1C_1$, $\tau_2 = R_2(C_1 + C_2)$, $\tau_3 = R_2C_2$.

We now list several guidelines for selecting a loop filter. The choice between an active or passive loop filter must be made first. If the designer chooses a passive loop filter, the lag lead is preferred over the RC loop filter for the following reasons:

1. For the lag-lead loop filter, the designer can specify the loop natural frequency ω_n and damping ζ independently of each other, and thus it is possible to have a narrowband loop with a substantial damping. However, for the RC loop filter, a narrowband PLL (low ω_n) requires a high value of τ (loop filter time constant), but a high τ results in low damping and possible instability (see Section IV).

2. The VCO parasitic pole is less likely to render a lag-lead PLL unstable compared with the RC loop filter PLL. (This is because the open loop phase for the RC loop filter PLL approaches −180 degrees at high frequencies, whereas the phase approaches −90 degrees for the lag-lead case.)

3. The lag-lead PLL exhibits improved transient behavior. For a given PLL damping value, the phase error transient of the lag-lead PLL reaches its steady-state value much sooner than that of the RC loop filter.

4. All of these improvements are obtained for the cost of one resistor.

An active loop filter is required when a higher loop gain is required (to increase the hold range, for example). The advantages of the third-order active filter over the second-order active filter are improved response to phase-step changes, zero steady-state phase error due to frequency ramp inputs, and better reduction of VCO noise.

After selecting a loop filter type, the user has two options: the desired damping and natural frequency may be specified, or the loop filter time constants may be specified. The first option is usually used when designing a new PLL, while the second option is normally used when analyzing an existing PLL.

2.2 PLACE 2.0 output

The user can request a stability analysis, a loop filter analysis, a tracking analysis, a jitter analysis, a sensitivity analysis, and an interactive optimization routine.

The *stability* analysis yields (1) second-order undamped natural frequency ω_n in hertz, (2) phase margin in degrees, (3) phase margin degradation due to the VCO (and/or op amp) pole, (4) phase margin degradation due to any phase delay of the feedback counter, (5) damping, and (6) PLL system bandwidth in hertz.

The *loop filter* analysis yields (1) the loop filter time constants in seconds, (2) values for the loop filter resistors and capacitors, and (3) the loop filter 3-dB frequency.

The *tracking* analysis yields (1) hold range in hertz (for active loop filters, the hold range is normalized, i.e., assuming $F(0) = 1$); (2)

approximate capture range in hertz; (3) approximate pull-in range in hertz; and (4) approximate lockup time in seconds.

The *jitter* analysis yields (1) output jitter due to incoming reference signal jitter: jitter bandwidth in hertz, frequency of jitter peaking in hertz, and noise bandwidth in hertz; (2) output jitter due to reference leakage through the phase detector: frequency of first sideband in hertz, magnitude of first sideband relative to the carrier in decibels, peak phase jitter in degrees, peak frequency deviation in hertz, and loop filter's attenuation of reference frequency in decibels; and (3) output jitter due to VCO phase noise: VCO phase noise reduction 3-dB frequency.

The *sensitivity* analysis computes upper and lower bounds on the hold range, capture range, pull-in range, and lockup time. The user input is the tolerance of the gain constants and loop filter components.

The *optimization* routine asks if the user wants to design for any one of the following: (1) larger hold range, (2) larger capture and pull-in range, (3) faster lockup time, or (4) less output jitter.

PLACE then automatically changes the PLL parameters to achieve the desired goal; then, the user can rerun the loop filter analysis to observe the new component values and use the tracking analysis to observe the new lockup time, etc.

The graphics portion of PLACE plots (on a TEK 4014 or similar device) the open and closed loop gains and phase, and the PLL response to VCO phase noise. For the graphics portion, the S package[3] must be installed on the system.

III. EXAMPLE

This example demonstrates the lag-lead loop filter case; it also demonstrates that the parasitic VCO pole may add sufficient phase shift to cause possible instability.

The user input to PLACE is as follows: The PLL for this example phase locks a 3.088-MHz crystal oscillator to an incoming 1.544 MHz signal. The VCXO has a measured gain constant of 800 Hz/V around the center frequency of 3.088 MHz; it also has a parasitic pole at 10 Hz. The phase detector is a Complementary Metal-Oxide Semiconductor (CMOS) exclusive-or gate measured at 1.4 V/rad; this was derived by measuring the logic high/low levels: $(4.6 - 0.2)/\pi = 1.4$. The phase comparison is done at 4 kHz; thus, the values for the frequency dividers are $N_{FF} = 386 = 1.544$ MHz/4 kHz and $N_{FB} = 772 = 3.088$ MHz/4 kHz. The loop filter resistors and capacitors were measured accurately, yielding time constants of $\tau_1 = 57.4513$ ms and $\tau_2 = 4.00336$ ms.

The results from the stability, loop filter, tracking, and jitter analysis

Table I—Comparing PLACE output with measured results

Parameter	Calculated	Measured
Hold range	+/−568 Hz	+496, −588 Hz
Pull-in range	+/−568 Hz	+493, −585 Hz
Lockup time	324 ms	400 ms
Frequency of jitter peaking	1.6 Hz	1.5 Hz
Magnitude of jitter peaking	1.3 dB	3 dB
Jitter bandwidth	3 Hz	4 Hz
Frequency of first sideband	8 kHz	8 kHz
Magnitude of first sideband	−52 dBc	−50 dBc
Peak base jitter	0.279 degrees	0.343 degrees
Peak frequency deviation	20 Hz	25 Hz
Reference frequency attenuation	23 dB	23 dB

appear in Appendix B. Table I summarizes the calculated results and also shows the measured values. The stability analysis indicates a damping of 0.7 and natural frequency of 2 Hz. The phase margin is 60 degrees: the VCO pole reduced the phase margin by 7.4 degrees, while the feedback counter caused negligible phase margin degradation of 0.02 degree. The PLL bandwidth is 1.2 Hz; this low PLL bandwidth is due to the very low K_V of 800 Hz/V. The previous results can also be found from the PLACE graphic display of open loop gain, shown in Fig. 3. Unity gain occurs at 1.2 Hz, where the phase is −120 degrees.

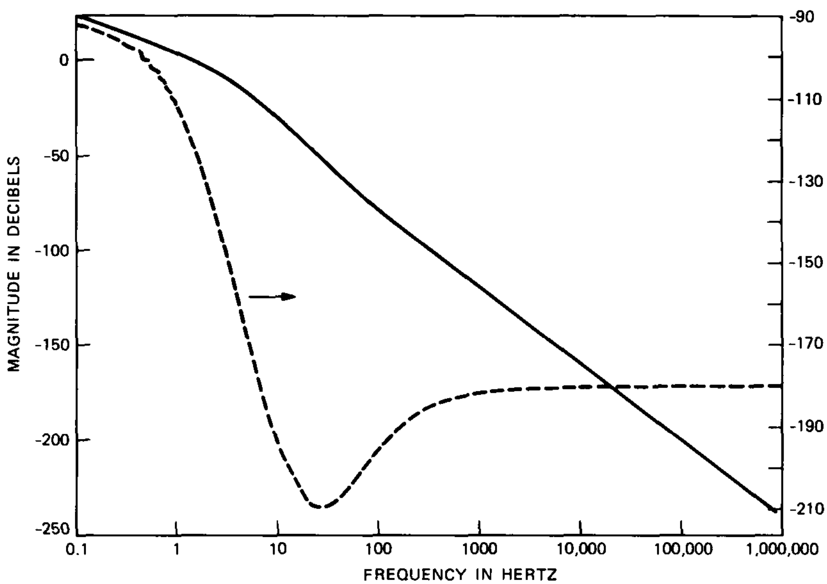

Fig. 3—PLACE graphic display of open loop gain for the lag-lead loop filter example. The magnitude is indicated by the solid line, and the phase is indicated by the dotted line (right scale).

Note that the parasitic VCO pole has brought the total phase shift to −180 degrees (instead of 0 degrees) for high frequencies. The tracking analysis indicates a hold range of +/−568 Hz. The measured value is +496 Hz, −588 Hz. The hold range is asymmetrical due to the larger than 50-percent duty cycle phase detector output during the lock condition. The pull-in range is +493, −582 Hz; it is common for low gain loops to have pull-in ranges close to the hold range.

The calculated lockup time is 324 ms, while the measured time is 400 ms; this may be found from Fig. 4, a display of tuning voltage during the lock-in process.

The jitter analysis indicates 1.3 dB of jitter peaking at 1.6 Hz, and a jitter bandwidth of 3 Hz. The closed loop gain Bode plot is shown in Fig. 5. The peaking is difficult to observe given the scale of the plot. The measured values may be found from Fig. 6, a spectrum analyzer display of closed loop gain versus jitter frequency from an HP 8557A. There is 3 dB of jitter peaking at 1.5 Hz (picture only displays up to 50 Hz). (The measured jitter peaking is higher than calculated due to additional poles in the VCXO.) The gain is down 3 dB (jitter bandwidth) at 4 Hz. The test equipment configuration for measuring the closed loop gain transfer function of Fig. 6 is shown in Fig. 7.

The calculated magnitude of the 8-kHz first sideband off the PLL output carrier is −52 dB; the measured level is −50 dB. This is shown in Fig. 8, a spectrum display from an HP 8557A. The peak phase jitter is 0.279 degree; the measured value from an HP 8901A modulation analyzer is 0.343 degree.

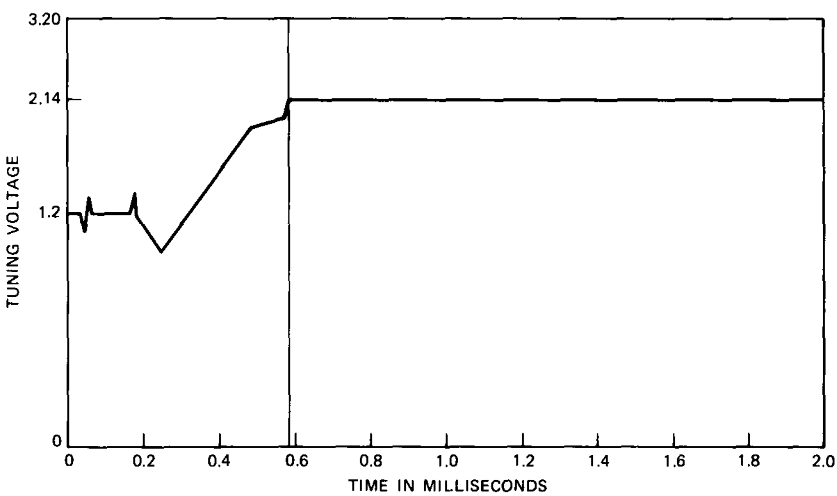

Fig. 4—Tuning voltage versus time during acquisition measured on a Paratronics 5000 logic analyzer.

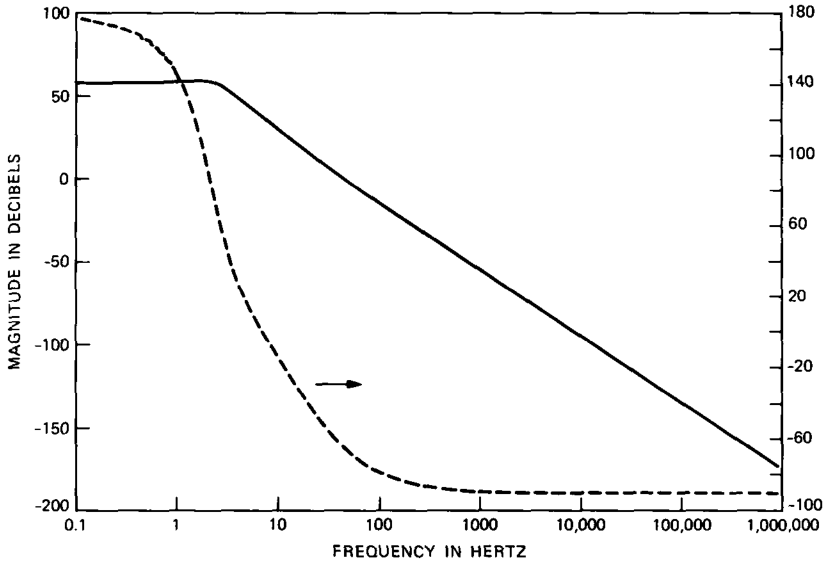

Fig. 5—PLACE graphic display of closed loop gain. The magnitude is indicated by the solid line, and the phase is indicated by the dotted line (right scale).

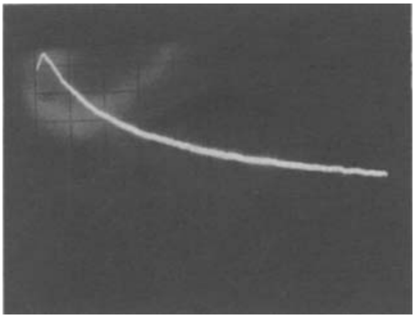

Fig. 6—Measured closed loop gain versus frequency showing 3 dB of jitter peaking. Vertical scale is 10 dB/division, horizontal scale is 5 Hz/division, and resolution bandwidth is 1 Hz.

The sensitivity analysis is also found in Appendix B. The upper and lower bounds found there reflect a 5-percent tolerance on the entered VCO gain constant, and 2-percent tolerance on the loop filter resistors and capacitors.

The remainder of this paper explains the calculations that PLACE performs.

IV. ANALYSIS

4.1 Stability analysis

The stability analysis requires computation of the PLL transfer

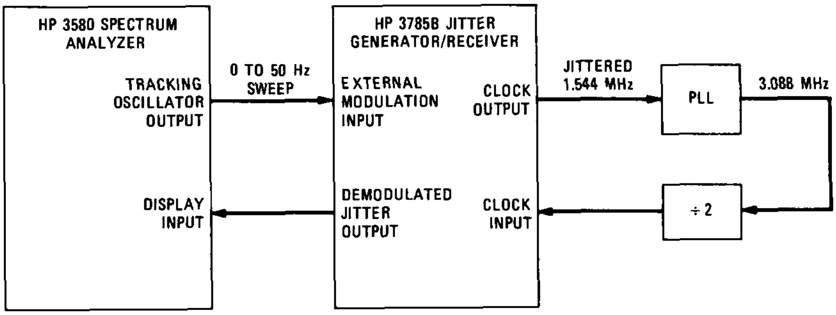

Fig. 7—Test equipment configuration used to obtain the closed loop gain transfer function shown in Fig. 6.

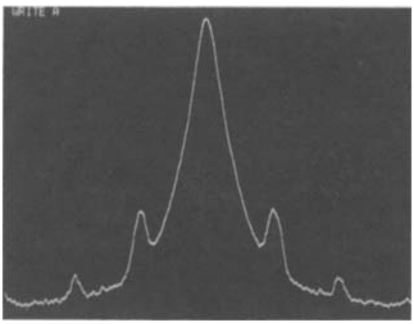

Fig. 8—Spectrum of VCO output carrier showing 8-kHz sidebands down 50 dB. Vertical scale is 10 dB/division, horizontal scale is 5 kHz/division, and resolution bandwidth is 1 kHz.

function. The components of a PLL are shown in Fig. 1; constants are defined in Section 2.1.

For the following calculations, we define $K_{Vr} = 2\pi K_V$ = VCO gain constant in rad/s/V. We also define the lumped gain constant:

$$K = \frac{K_p K_{Vr}}{N_{FB}}.$$

The equivalent frequency domain model of the PLL is also shown in Fig. 1, where $F(s)$ and $V_F(s)$ are the Laplace transforms of the loop filter transfer function and loop filter output voltage, respectively. The VCO model of K_{Vr}/s is derived as follows:

$$f_{out} = \frac{d\phi_{out}}{dt} = K_{Vr} v_F$$

$$L\left(\frac{d\phi_{out}}{dt}\right) = s\phi_{out}(s) = K_{Vr} V_F(s)$$

$$\phi_{out}(s) = \frac{K_{Vr} V_F(s)}{s}.$$

4.1.1 Loop gains

The transfer function for the PLL may be easily derived if we define the feed-forward gain as

$$G(s) = \frac{\phi_{\text{out}}(s)}{\phi_e(s)} = K_p K_{Vr} F(s)/s \tag{1}$$

and the feedback gain as

$$\beta(s) = 1/N_{\text{FB}}. \tag{2}$$

Then, following conventional control theory analysis, the open loop gain is the product of the feed-forward and feedback gains:

$$\beta(s)G(s) = \frac{K_p K_{Vr} F(s)}{sN_{\text{FB}}} = \frac{KF(s)}{s}. \tag{3}$$

The closed loop gain is

$$H(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{G(s)}{1 + \beta(s)G(s)}$$

$$= \frac{K_p K_{Vr} F(s)/s}{1 + K_p K_{Vr} F(s)/sN_{\text{FB}}} = \frac{K_p K_{Vr} F(s)}{s + K_p K_{Vr} F(s)/N_{\text{FB}}} = \frac{N_{\text{FB}} K}{\frac{s}{F(s)} + K}. \tag{4}$$

The error transfer function $E(s) = (\phi_e(s))/(\phi_{\text{in}}(s))$ is easily found as

$$E(s) = \frac{\phi_e(s)}{\phi_{\text{in}}(s)} = \frac{1}{1 + \beta(s)G(s)}. \tag{5}$$

Note that if there is no feedback counter, $\beta(s) = 1$, and then $E(s) = 1 - H(s)$.

The loop type is specified by the number of poles at the origin of $\beta(s)G(s)$. The loop order is specified by the total number of poles in $\beta(s)G(s)$. We have ignored the phase delay through the feedback counter in the above analysis; this phase delay is treated in Section 4.1.5.

4.1.2 Damping, second-order undamped natural frequency ω_n

From the above equations we see that the PLL response is highly dependent on the form of loop filter $F(s)$. By substituting a particular loop filter function $F(s)$ into eq. (4), we can (except for the no loop filter case) get the denominator into the classic second-order control system form of $s^2 + 2\zeta\omega_n s + \omega_n^2$, where ω_n is the undamped natural frequency and ζ is the damping. This is shown in Appendix C.

4.1.3 Phase margin

PLACE calculates the phase of $\beta(s)G(s)$ at unity open loop gain; the difference from −180 degrees is the phase margin. This definition is identical to the stability analysis of feedback amplifiers.

4.1.4 Phase margin degradation due to the VCO (and/or op amp) pole

A parasitic pole causes the open loop gain to fall off more quickly and thus affect the phase margin. The tuning element of a VCO (typically a varactor) cannot respond to rapidly changing tuning voltages. We represent this by assigning a pole to the VCO. It has been the author's experience that this VCO pole may be the dominant pole of the PLL (especially if VCXOs are used). PLACE determines the phase margin degradation due to the parasitic VCO pole by multiplying the open loop gain by $1/(1 + \tau_v s)$, where $\tau_v = 1/(2\pi f_V)$, where f_V is the VCO pole. The VCO pole may be found by impressing an ac modulating signal on the dc voltage to the varactor, and determining the highest modulating frequency for which the VCO output will follow the input. (A typical value for a VCXO is $f_V = 10$ Hz.)

If the user wants to account for the operational amplifier pole for the active loop filter case, he may lump this pole into the VCO parasitic pole. The designer should try to keep the operational amplifier bandwidth much larger than the PLL system bandwidth (defined in Section 4.1.6).

4.1.5 Phase margin degradation due to the feedback counter

The effect of the feedback counter is to add a phase delay of f/f_{ref} to the open loop gain and thus degrade the phase margin by f_u/f_{ref} rad, where f_u is the frequency for unity open loop gain and f_{ref} is the frequency entering the phase detector.[4,5] This is derived as follows.

Since any change in the VCO frequency can be observed by the phase detector only after the feedback counter overflows T seconds later (worst case), the effect of the counter is to produce a maximum delay of up to T seconds, where the delay time T is given by

$$T = N_{FB}(1/f_{VCO}) = N_{FB}\frac{1}{N_{FB}f_{ref}} = 1/f_{ref}.$$

Thus, in the frequency domain we represent the feedback counter by

$$\frac{1}{N_{FB}}e^{-sT} = \frac{1}{N_{FB}}e^{-j2\pi(f/f_{ref})}.$$

PLACE calculates this phase shift and notifies the user of the resulting phase margin degradation.

4.1.6 PLL system bandwidth in hertz

The PLL system bandwidth is the frequency for PLL unity open loop gain; it is found by solving $|\beta(j\omega)G(j\omega)| = 1$ for ω. We have the following:

No loop filter:

$$F(s) = 1,$$

and

$$\mathrm{PLL_{BW}} = \frac{1}{2\pi}\,[K]\ \mathrm{Hz}.$$

RC loop filter:

$$F(s) = \frac{1}{(1 + \tau s)},$$

and

$$\mathrm{PLL_{BW}} = \left[\frac{1}{2\pi}\right]\frac{1}{\sqrt{2}\tau}\,\{\sqrt{1 + 4(\tau K)^2} - 1]^{1/2}$$

$$= \left[\frac{1}{2\pi}\right]\sqrt{2}\zeta\omega_n\{\sqrt{1 + 1/(4\zeta^4)} - 1\}^{1/2}\ \mathrm{Hz}.$$

Lag-lead loop filter:

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},$$

and

$$\mathrm{PLL_{BW}} = \left[\frac{1}{2\pi}\right]\frac{1}{\sqrt{2}\tau_1}\,\{\sqrt{a^2 + 4(\tau_1 K)^2} + a\}^{1/2}\ \mathrm{Hz},$$

where $a = \tau_2^2 - 1$.

Second-order active loop filter:

$$F(s) = (1 + \tau_2 s)/(\tau_1 s),$$

and

$$\mathrm{PLL_{BW}} = \left[\frac{1}{2\pi}\right]\omega_n\{2\zeta^2 + \sqrt{4\zeta^4 + 1}\}^{1/2}\ \mathrm{Hz}.$$

For the third-order active loop filter, the user may specify the desired PLL bandwidth, or, alternatively, the value defaults to $f_{ref}/50$. PLACE uses this value to optimize the loop for best phase noise performance (see Appendix C).

4.2 Loop filter analysis

4.2.1 Loop filter time constants

The loop filter time constants are calculated from the undamped natural frequency and the damping by using the equations derived in Appendix C. Alternatively, the user may directly specify the loop filter time constants.

4.2.2 Loop filter resistors and capacitors

PLACE assumes 0.1-μf capacitors and calculates the resistors from the definition of the time constants. Note that the user can linearly scale the resistors and capacitors to any desired value (e.g., if the user desires 0.01-μf capacitors, multiply the calculated resistor values by 10).

4.2.3 Constraints on lag-lead loop filter

To maintain real values of resistors and capacitors, certain constraints must be met for the lag-lead loop filter case. PLACE first asks for the desired value of ω_n. Then, when it asks for the desired value of damping, the entered value for damping must satisfy two conditions:

1. Since $\tau_2 = 2\zeta/\omega_n - 1/K$, to ensure a positive τ_2 we must ensure

$$\zeta > \frac{\omega_n}{2K}.$$

2. Since $R_1 = (\tau_1 - \tau_2)/C$, to ensure a positive R_1 we must ensure

$$\tau_1 > \tau_2$$

$$\frac{K}{\omega_n^2} > \frac{2\zeta}{\omega_n} - \frac{1}{K}$$

$$\zeta < \frac{K^2 + \omega_n^2}{2\omega_n K}.$$

Hence, after the user specifies the desired value for ω_n, PLACE asks the user to enter a value for damping that satisfies

$$\frac{\omega_n}{2K} < \zeta < \frac{K^2 + \omega_n^2}{2\omega_n K}.$$

4.2.4 Loop filter 3-dB frequency or zero frequency

The frequency at which $F(s)$ is down 3 dB is found by solving $|F(j\omega)| = 0.707$ for ω. We have the following (iff $\tau_1 > \sqrt{2}\tau_2$, else $F(s)$ is never down 3 dB):

RC loop filter:

$$F(s) = \frac{1}{1 + \tau s},$$

and

$$F_{BW} = \frac{1}{2\pi}\left[\frac{1}{\tau}\right] \text{ Hz.}$$

Lag-lead loop filter:

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},$$

and

$$F_{BW} = \frac{1}{2\pi}\left[\frac{1}{\tau_1^2 - 2\tau_2^2}\right]^{1/2} \text{ Hz.}$$

For the second and third active loop filter cases, F_{BW} is undefined because $F(s)$ has a pole at the origin. For these cases PLACE calculates the zero frequency.

4.3 Tracking analysis

4.3.1 Hold range

The hold range is defined as the maximum input frequency range that the PLL will track once it is in lock. It may be found experimentally by slowly varying the input frequency to a PLL that is in lock and noting when lock is lost. (The word "slowly" is emphasized because if the input frequency has a step change, the transient behavior of the loop may cause the PLL to loose lock, even though the step is within the hold range.)

The hold range is independent of the type of loop filter $F(s)$ and is given by numerous authors (e.g., see Ref. 6) as $K_p K_{Vr} F(0)/N_{FB}$, where $F(0)$ is the dc gain of the loop filter. (Note that the error voltage is a constant dc value when the loop is in lock.) For passive loop filters $F(0) = 1$, and accounting for the feed-forward counter, PLACE computes the *hold range* as

$$\pm\frac{1}{2\pi} N_{FF} \frac{K_p K_{Vr}}{N_{FB}} \text{ Hz.} \qquad (6)$$

For active loop filters $F(0)$, and hence the hold range, can be made arbitrarily large (until the VCO or operational amplitude saturates); thus PLACE computes the normalized hold range (it assumes $F(0) = 1$).

When recovering timing from Pulse Code Modulated (PCM) data lines, the hold (and capture) range may be asymmetrical due to the density of ones.[7]

Nonsinusoidal phase detectors theoretically extend the hold and capture ranges. For example, triangular phase detectors have a so-called "extension factor" of $\pi/2$, while sawtooth phase detectors have a factor of π (see Ref. 6). PLACE leaves it to the user to modify the phase detector gain constant K_p (if the designer is so inclined) when PLACE requests the value.

4.3.2 Capture and pull-in range

The *capture* range is defined as the maximum input frequency range for which a PLL will acquire phase lock without skipping cycles (i.e., the phase detector voltage monotonically drives the VCO toward lock, without any beating). (Some authors call this the lock-in range.) The *pull-in* range is defined as the maximum input frequency range for which a PLL will acquire lock (typically with skipping cycles), even if it takes minutes or hours to lock up. (In this case the phase detector output voltage may be a beat note swinging the VCO above and below f_{in}.)

Whereas eq. (6) gives an accurate value for the hold range, the determination of the capture and pull-in range is extremely difficult because the loop starts (by definition) out of lock, and thus a nonlinear analysis is required. The solution cannot be expressed in closed form (except for the $F(s) = 1$ case), and only a graphical phase-plane trajectory procedure[6,8] will yield true results. PLACE approximates the capture and pull-in ranges by using the approximating equations found in the literature and modifying them to account for the feedback and feed-forward counters:

No loop filter:

$$f_{\text{capture}} = f_{\text{hold}} = f_{\text{pull}} = \pm\frac{1}{2\pi} N_{\text{FF}} \frac{K_p K_{V_r}}{N_{\text{FB}}} \text{ Hz}$$

(see Refs. 8 and 9).

RC loop filter: If $K\tau_1 < 0.25$,

$$f_{\text{capture}} = f_{\text{hold}} = f_{\text{pull}} = \pm\frac{1}{2\pi} N_{\text{FF}} \frac{K_p K_{V_r}}{N_{\text{FB}}} \text{ Hz}$$

(see Ref. 10).

Else,

$$f_{\text{capture}} = \pm\frac{1}{2\pi} N_{\text{FF}} 2\zeta\omega_n \text{Hz},$$

and

$$f_{\text{pull}} = \pm\frac{1}{2\pi} N_{\text{FF}} 1.25\omega_n \text{ Hz}$$

(see Ref. 8).

Lag-lead loop filter:

$$f_{\text{capture}} = \pm\frac{1}{2\pi} N_{\text{FF}} K \frac{\tau_2}{\tau_1} = \frac{1}{2\pi} N_{\text{FF}} \tau_2 \omega_n^2 \text{ Hz},$$

(see Refs. 8 and 10), and

$$f_{\text{pull}} = \frac{1}{2\pi} N_{\text{FF}} 2 \left\{ K\zeta\omega_n + \frac{K}{2\tau_1} \right\}^{1/2} \text{ Hz}$$

(see Refs. 10 and 11).

Second-order active filter:

$$f_{\text{capture}} = \pm\frac{1}{2\pi} N_{\text{FF}} 2\zeta\omega_n = \frac{1}{2\pi} N_{\text{FF}} \tau_2 \omega_n^2 \text{ Hz}$$

(see Ref. 8).

For the second- and third-order active loop filter cases, the hold and pull-in ranges will be as large as the maximum frequency range of the VCO, assuming the operational amplifier output does not saturate at the supply rail, and assuming negligible loop delay.

4.3.3 Lockup time

The lockup time is defined for PLACE as the time it takes the PLL to acquire phase and frequency lock from an initial frequency offset equal to the pull-in range. For the no loop filter case and low gain ($K\tau_1 < 0.25$) passive loop filter case, PLACE calculates the lockup time as $T_{\text{lock}} = 1/K$ seconds.[8]

For second-order active loop filters and high-gain ($K\tau_1 > 0.25$) passive loop filters, the lockup time is approximately given by $T_{\text{lock}} = \Delta\omega^2/2\zeta\omega_n^3$ (see Refs. 6 and 8). PLACE lets $\Delta\omega = ([f_{\text{capture}} + f_{\text{pull}}]/2N_{\text{FF}})2\pi$, which is where the approximation is most accurate; for the second-order loop filter, PLACE lets $\Delta\omega = 2\pi(2f_{\text{capture}})$. PLACE does not calculate the lockup time for the third-order loop filter.

4.4 Jitter analysis

In the discussion that follows, the term "reference signal" is the signal entering the phase detector; thus, if $N_{\text{FF}} = 1$, the reference signal is the incoming signal itself. Also, the terms jitter and phase noise are equivalent.

The output jitter of a PLL may be conveniently separated into two main components: jitter generation and jitter propagation. Jitter propagation refers to the output jitter due to jitter on the incoming signal (or the reference signal for frequency synthesizer applications). Jitter generation may be subdivided into five components: output jitter due to leakage of the reference signal through the phase detector; output jitter due to VCO phase noise; and output jitter due to phase noise of the phase detector, frequency divider, and loop filter (if an active loop filter is employed). PLACE analyzes each component of jitter separately.

The most important result of this section may be summarized (without mathematics) as follows: A PLL acts as a high-pass filter to VCO phase noise, and acts as a low-pass filter to incoming reference signal jitter.

4.4.1 Output jitter due to jitter on the incoming reference signal

4.4.1.1 Jitter bandwidth. It may easily be shown that the PLL's response to jitter on the incoming reference signal is given by the closed loop gain transfer function $H(s)$, eq. (4). Merely repeat the analysis of Section 4.1.1 with ϕ_i now representing an instantaneous phase deviation of the incoming reference frequency. Equation (4) is repeated here for convenience:

$$H(s) = \frac{\phi_{\text{out}}(s)}{\phi_{\text{in}}(s)} = \frac{G(s)}{1 + \beta(s)G(s)} = \frac{K_p K_{Vr} F(s)/s}{1 + K_p K_{Vr} F(s)/sN_{\text{FB}}}$$
$$= \frac{K_p K_{Vr} F(s)}{s + K_p K_{Vr} F(s)/N_{\text{FB}}} = \frac{N_{\text{FB}} K}{(s/F(s)) + K}.$$

Thus, above the frequency for unity closed loop gain $H(s)$, the input signal jitter will be attenuated. Thus a PLL acts as a low-pass filter to jitter on the incoming reference signal. Also, notice from eq. (4) that within the PLL system bandwidth, a PLL multiplies the reference noise by the feedback counter divisor N_{FB}. That is, the feedback counter effectively adds 20 log N_{FB} dB/Hz phase noise to the reference signal.

The jitter bandwidth is the frequency at which $H(s)$ is down 3 dB from its dc value. If we neglect any parasitic VCO or operational amplifier poles, we have the following:

No loop filter:

$$F(s) = 1,$$

and

$$\text{jitter}_{\text{BW}} = \frac{1}{2\pi} [K] \text{ Hz}.$$

RC loop filter:

$$F(s) = \frac{1}{1 + \tau s},$$

and

$$\text{jitter}_{\text{BW}} = \left[\frac{1}{2\pi}\right]\omega_n\{(2\zeta^2 + 1) + \sqrt{(2\zeta^2 - 1)^2 + 1}\}^{1/2} \text{ Hz.}$$

Lag-lead loop filter:

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},$$

and

$$\text{jitter}_{\text{BW}} = \left[\frac{1}{2\pi}\right]\omega_n\{a + \sqrt{a^2 + 1}\}^{1/2} \text{ Hz,}$$

where

$$a = 2\zeta^2 + 1 - \frac{4\zeta\omega_n}{K} + \frac{\omega_n^2}{K}.$$

Second-order active loop filter:

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s},$$

and

$$\text{jitter}_{\text{BW}} = \left[\frac{1}{2\pi}\right]\omega_n\{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}\}^{1/2} \text{ Hz.}$$

When there are parasitic poles (which often reduce the bandwidth values calculated above), PLACE uses an iterative search to find the jitter bandwidth.

4.4.1.2 Frequency and magnitude of jitter peaking. The peak jitter gain $|H(j\omega_{\text{peak}})|$ is equivalent to the peak magnitude of $H(s)$. *Jitter peaking* is the difference (in decibels) between the closed loop gain peak magnitude $|H(j\omega_{\text{peak}})|$ and the dc value of $H(s)$. To find it we first find the frequency of peak jitter gain ω_{peak} by setting the derivative of $|H(j\omega)|^2$ to zero and solving for ω_{peak}. Then we substitute ω_{peak} back into $H(j\omega)$. Neglecting any parasitic VCO or operational amplifier poles, we get the following results:

No loop filter:

$$F(s) = 1,$$

and

$$\omega_{\text{peak}} = 0$$

and

$$|H(j\omega_{\text{peak}})| = 0.$$

RC loop filter:

$$F(s) = \frac{1}{1 + \tau s},$$

$$\omega_{\text{peak}} = \omega_n\sqrt{1 - 2\zeta^2},$$

and

$$|H(j\omega_{\text{peak}})| = \frac{1}{2\zeta\sqrt{1 - \zeta^2}}.$$

Second-order active loop filter:

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s},$$

$$\omega_{\text{peak}} = \frac{\omega_n}{2\zeta}\{\sqrt{1 + 8\zeta^2} - 1\}^{1/2},$$

and

$$|H(j\omega_{\text{peak}})| = (4\zeta^2)\left\{\frac{1}{[4\zeta^2 - 1]^2 - 3 + 2\sqrt{(1 + 8\zeta^2)}}\right\}^{1/2}.$$

For the lag-lead and third-order active loop filters, PLACE uses an iterative search to find the jitter peaking. The above equations do not reveal the jitter peaking due to parasitic poles. PLACE uses an iterative search to find the jitter peaking in such cases.

4.4.1.3 Noise bandwidth. The noise bandwidth of a PLL is the bandwidth of an equivalent rectangular filter that would yield the same output noise power (variance) as the PLL, if they both have white noise inputs of equal density. PLACE calculates the one-sided noise bandwidth, where $N_{BW} = \int_0^\infty |H(j\omega)|^2 d\omega$. Various authors have evaluated the integrals, and we have the following:

No loop filter:

$$F(s) = 1,$$

and

$$N_{BW} = \frac{K}{4}\text{ Hz}.$$

RC loop filter:

$$F(s) = \frac{1}{1 + \tau s},$$

and

$$N_{\mathrm{BW}} = \frac{K}{4} = \frac{\omega_n}{8\zeta}\ \mathrm{Hz}.$$

Lag-lead loop filter:

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},$$

and

$$N_{\mathrm{BW}} = \frac{K}{4}\left[\frac{K + 1/\tau_2}{K + 1/\tau_1}\right]\ \mathrm{Hz}.$$

Second-order active loop filter:

$$F(s) = \frac{1 + \tau_2 s}{\tau_1 s},$$

and

$$N_{\mathrm{BW}} = \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right)\ \mathrm{Hz}.$$

For the third-order active loop filter, the noise bandwidth is approximately given by the PLL system bandwidth defined earlier.

The output noise of the PLL, given a white noise input with power P_{in} is given by $P_{\mathrm{out}} = P_{\mathrm{in}} N_{\mathrm{BW}}$. Similarly, the output signal-to-noise ratio of the PLL is inversely proportional to the noise bandwidth.

4.4.2 Output jitter due to leakage of the reference through the phase detector

4.4.2.1 Frequency and magnitude of first sideband. Any feedthrough of the reference frequency through the loop filter phase modulates the VCO, producing sidebands at the VCO output. The frequency of the first sideband is the frequency leaving the phase detector: twice the reference frequency for exclusive-or gate phase detectors, the reference frequency for other phase detectors. The magnitude of the first sideband is found as follows: the modulating frequency is $f_m = f_{\mathrm{ref}}$, and the Modulation Index (MI) is $\mathrm{MI} = \Delta f / f_m = \Delta f / f_{\mathrm{ref}}$. Using conventional frequency modulation/phase modulation analysis, we can express the resulting VCO output voltage $v(t)$ by using Bessel functions as

$$V_0\{J_0(\mathrm{MI})\cos(\omega_0 t) \pm J_1(\mathrm{MI})\cos(\omega_0 \pm \omega_m)t\},$$

where we have neglected the higher-order sidebands. Now, if the modulation index is small (MI < 0.3), we have $(J_1(\mathrm{MI}))/(J_0(\mathrm{MI})) = \mathrm{MI}/2$. For example, $(J_1(0.2))/(J_0(0.2)) = 0.0995/0.9900 = 0.1 = \mathrm{MI}/2$. Hence,

$$\frac{\text{First sideband amplitude}}{\text{VCO carrier amplitude}} = \frac{J_1(\mathrm{MI})}{J_0(\mathrm{MI})} = \frac{\mathrm{MI}}{2} = \frac{\Delta f}{2f_m} = \frac{\Delta f}{2f_{\mathrm{ref}}}. \quad (7)$$

When we realize that most of the signal power is in the carrier for small modulation indices, we see that the above equation is the definition of the $\mathscr{L}(f)$ (see Refs. 12 and 13) used in specifying oscillator phase noise.

Now, Δf is the frequency deviation of the VCO:

$$\Delta f = \Delta V_F K_V = V_{\mathrm{pk}} | F(j\omega) | K_V,$$

where V_{pk} is the peak amplitude of f_{ref} at the phase detector output. (For exclusive-or gate phase detectors, the phase detector output frequency is twice f_{ref}.)

Thus, the magnitude of the first sideband (relative to the carrier) at the PLL output is given by

$$20 \log V_{\mathrm{pk}}\left[\frac{K_V | F(j\omega) |}{2f_{\mathrm{ref}}}\right], \quad (8)$$

where $F(j\omega)$ is evaluated at ω_{ref}. (This result agrees with Ref. 14.) PLACE asks the user for the value of V_{pk}, the peak voltage output from the phase detector.

4.4.2.2 Peak frequency deviation and phase jitter. It can be shown that the peak phase deviation is related to $\mathscr{L}(f)$ by the following relation:[15]

$$\mathscr{L}(f) = \frac{\Delta\phi_{\mathrm{peak}}}{2}.$$

The magnitude of $\mathscr{L}(f)$ is given by eq. (7); PLACE 2.0 solves the above equation for the peak phase deviation in radians. Then, the peak phase jitter in degrees is 57.3 times as large. The peak frequency deviation is found by using $\Delta f_{\mathrm{peak}} = f_m \Delta\phi_{\mathrm{peak}}$.

As long as the peak phase jitter is less than approximately 28 degrees, the PLL will generally stay in lock (see Ref. 16).

4.4.2.3 Loop filter's attenuation of reference frequency. PLACE calculates the magnitude of $F(s)$ at the reference frequency and informs the user of the result.

4.4.3 Output jitter due to PLL components

4.4.3.1 Output jitter due to VCO phase noise. PLACE calculates the

PLL's relative response to VCO phase noise (i.e., it calculates the PLL's attenuation of VCO phase noise); PLACE does not calculate the absolute value of the VCO-generated phase noise itself. (References 9, 12, and 17 explain how to measure the absolute VCO phase noise.)

A VCO may be modeled as a pure signal source corrupted by an instantaneous phase fluctuation $\phi_{VCO}(t)$. We modify the PLL model by adding this noise source to the VCO of Fig. 1. The total PLL output phase is now $\phi_{out}(t) = \phi_{loop}(t) + \phi_{VCO}(t)$, where $\phi_{loop}(t)$ is the output phase for a PLL with an ideal VCO. We now have the following:

$$\phi_e(s) = \phi_{in}(s) - \phi_{out} \frac{(s)}{N_{FB}},$$

but

$$\phi_{out}(s) = \phi_e(s)F(s)K_pK_V/s + \phi_{VCO}(s),$$

so that

$$\phi_e = \frac{\phi_{out} - \phi_{VCO}}{F(s)K_pK_V/s}.$$

Algebraic manipulations yield

$$\phi_{out} = \phi_{in} \frac{N_{FB}KF(s)/s}{1 + KF(s)/s} + \phi_{VCO} \frac{1}{1 + KF(s)/s}$$

$$\phi_{out} = \phi_{in} \frac{G(s)}{1 + \beta(s)G(s)} + \phi_{VCO} \frac{1}{1 + \beta(s)G(s)}. \tag{9}$$

Thus, the PLL response to VCO phase noise is given by

$$\frac{1}{1 + \beta(s)G(s)}. \tag{10}$$

(This result is confirmed in Refs. 5, 8, and 13.) The above equation tells us that the −3 dB point of the PLL response to VCO phase noise occurs when $|\beta(s)G(s)| = 1$; but this occurs at the PLL system bandwidth (defined in Section 4.1.6). Hence, the PLL will pass through the VCO phase noise unattenuated above the PLL system bandwidth. Below the PLL system bandwidth, the output jitter due to VCO phase noise is reduced by the loop gain $\beta(s)G(s)$.

In short, a PLL acts as a high-pass filter to VCO phase noise.

4.4.3.2 Output jitter due to frequency divider phase noise. In Section 4.4.1.1 it was shown that the feedback counter effectively adds 20 log N_{FB} dB/Hz phase noise to the reference signal; this section discusses the jitter generated in the frequency divider itself.

Phase noise generated in digital frequency dividers is due to the internal active devices. Typical noise floors for Transistor-Transistor Logic (TTL), Emitter-Coupled Logic (ECL), and Metal Oxide Semiconductor (MOS) dividers are −120 to −140 dB. TTL dividers have the lowest noise, followed by ECL, and then MOS. (Typical values may be found in Ref. 9.)

As in the case for VCO phase noise, PLACE does not need to know the absolute value of the divider noise. The PLL response to this noise is the same as for jitter on the incoming signal, because the PLL cannot tell whether the noise comes from the divider or signal inputs to the phase detector. Thus, the PLL response to divider noise is identical to the low-pass filter shape computed for incoming line jitter. [The PLL response to noise from an active loop filter is also given by eq. (4).]

In timing recovery circuits, the divider noise is negligible compared with the input signal jitter. In frequency synthesizers, however, the two may be equal, and then the resultant noise equals their rms sum.

4.4.3.3 Output jitter due to phase detector phase noise. Typical noise floors for phase detectors are −150 to −160 dB/Hz (see Ref. 15). The PLL response to this phase noise is again given by eq. (4). The phase detector noise floor improves 3 dB per octave of reference frequency reduction.

4.5 Sensitivity analysis

PLACE asks the user for the tolerance of the VCO and phase detector gain constants, and the tolerance on the loop filter resistors and capacitors. It then performs a Taylor series expansion and retains the first-order terms. Then it calculates upper and lower bounds for the hold range, capture and pull-in ranges, and lockup time. This allows the designer to observe the effect of component variation on the PLL.

4.6 Optimization routine

PLACE 2.0 features an interactive routine that allows the designer to optimize PLL performance. The user specifies either a larger hold range, larger capture and pull-in range, faster lockup time, or less output jitter. After the user specifies a desired item to optimize, PLACE automatically adjusts the PLL damping and natural frequency to achieve the desired goal.

V. CONCLUSION

An interactive program to aid in the development of PLLs has been written. PLACE has been successfully used in the design of PLLs for digital channel banks, muldems, and radio transmission systems. In addition, routine use of PLACE on several existing PLL designs revealed problems that were subsequently corrected before the product was placed in the field. The program has saved many PLL designers from tedious calculations, allowing a better understanding of PLL performance.

VI. ACKNOWLEDGMENT

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APPENDIX A

List of Symbols

$E(s)$	Error transfer function
$F(s)$	Loop filter transfer function
F_{BW}	Loop filter 3-dB frequency
f_m	Frequency of modulation
f_{ref}	Reference frequency
f_u	Frequency for unity open loop gain
f_V	Frequency of VCO pole
f_{VCO}	Frequency of VCO
$f_{capture}$	Capture range
f_{hold}	Hold range

f_{pull}	Pull-in range
$G(s)$	Feed-forward gain
$H(s)$	Closed loop gain
$\vert H(j\omega_{peak})\vert$	Magnitude of jitter peaking
K	Lumped gain constant, $K = (K_p K_{Vr})/N_{FB}$
K_p	Phase detector gain constant in V/rad
K_V	VCO gain constant in Hz/V
K_{Vr}	VCO gain constant in rad/s/V
N_{BW}	Noise bandwidth in hertz
N_{FB}	Feedback counter divisor
N_{FF}	Feed-forward counter divisor
PLL_{BW}	PLL bandwidth
T_{lock}	Lockup time
v_F	Loop filter output voltage
$V_F(s)$	Loop filter output voltage
$\beta(s)$	Feedback gain
Δf	Frequency deviation
Δf_{peak}	Peak frequency deviation
$\Delta\phi_{peak}$	Peak phase deviation
ζ	Damping
$\phi_{in}(s)$	Input phase
$\phi_{out}(s)$	Output phase
$\phi_e(s)$	Phase error
ω_n	Natural frequency
ω_{peak}	Frequency of jitter peaking

APPENDIX B

PLACE 2.0 Output for Lag-Lead Loop Filter Example

Stability Analysis:

2nd-Order Undamped Natural Frequency (Hz)	Phase Margin (degrees)	PLL Bandwidth (Open Loop Gain = 1) (Hz)	Damping
2.0	59.3	1.2	0.7

Your VCO pole at 10.0 Hz reduced the phase margin by 7.41 degrees, and reduced the PLL bandwidth by 0.1 Hz.

Your feedback counter reduces the phase margin by 0.02 degree.

Loop Filter Analysis:

Assuming 0.1 uf capacitor, our loop filter components are:

T1=(R1+R2)C	T2=R2 (C)	R1(ohms)	R2(ohms)	C(uf)	Loop Filters 3-dB Freq. (Hz)
0.05745130	0.00400336	534479	40034	0.100000	2.8

Tracking Analysis:

Hold Range (+/− Hz)	Capture Range (+/− Hz)	Pull-In Range (+/− Hz)	Lockup Time (sec)
568.0	39.6	568.0	0.32447433

Jitter Analysis:

1. Output Jitter Due to Incoming Reference Signal Jitter:

Frequency of Jitter Peaking (Hz)	Magnitude of Jitter Peaking (dB)	Noise Bandwidth (Hz)	Jitter Bandwidth (Hz)
1.6	1.272	22.5	3

2. Output Jitter Due to Reference Leakage Through the Phase Detector:

Frequency of 1st Sideband (Hz)	Magnitude of 1st Sideband (dBc)	Peak Phase Jitter (degrees)	Peak Frequency Deviation (Hz)	Ref. Freq. Attenuation (dB)
8000	−52	0.278	19.4	23

3. Output Jitter Due to VCO Phase Noise:
Your PLL attenuates VCO phase noise BELOW 1.2 Hz.

Sensitivity Analysis:

	Hold Range (+/− Hz)	Capture Range (+/− Hz)	Pull-In Range (+/− Hz)	Lockup Time (sec)
Lower Bound:	539.0	36.1	539.0	0.30792615
Nominal:	568.0	39.6	568.0	0.32447433
Upper Bound:	597.0	43.1	597.0	0.34102252

APPENDIX C

Loop Gain Derivation

C.1 Case 1. No loop filter: F(s) = 1

From eq. (4), the closed loop gain is

$$H(s) = \frac{N_{FB}K}{s/F(s) + K} = \frac{N_{FB}}{1 + s/K},$$

the closed loop gain magnitude is

$$|H(j\omega)| = N_{FB}\left[\frac{1}{1 + \left(\frac{\omega}{K}\right)^2}\right]^{1/2},$$

and the closed loop gain phase is

$$\phi(j\omega) = -\arctan(\omega/K).$$

From eq. (3), the open loop gain is

$$\beta(s)G(s) = K/s,$$

the open loop gain magnitude is

$$|\beta(j\omega)G(j\omega)| = K/\omega,$$

and the open loop gain phase is

$$\theta(j\omega) = -90 \text{ degrees (due to the VCO).}$$

Note that the phase margin is 90 degrees and the loop is theoretically unconditionally stable; but, if we account for any parasitic VCO pole (or any other parasitic poles lumped into the VCO pole), PLACE shows that the PLL can be unstable for very high loop gain K. No loop filter results in a first-order type-1 PLL.

C.2 Case 2. RC loop filter: $F(s) = 1/(1 + \tau s)$

From eq. (4), the closed loop gain is

$$H(s) = \frac{N_{FB}K}{s/F(s) + K} = \frac{N_{FB}K}{s^2\tau + s + K} = \frac{N_{FB}K/\tau}{s^2 + s/\tau + K/\tau}.$$

We can get the denominator into the classical second-order control system form of $s^2 + 2\zeta\omega_n s + \omega_n^2$ if we let $\omega_n^2 = K/\tau$ and $2\zeta\omega_n = 1/\tau$. Then,

$$H(s) = \frac{N_{FB}\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{N_{FB}}{\left(\frac{s}{\omega_n}\right)^2 + 2\zeta\frac{s}{\omega_n} + 1},$$

where the *undamped natural frequency* is

$$\omega_n = \sqrt{K/\tau},$$

and the *damping* is

$$\zeta = \frac{1}{2\omega_n\tau} = \frac{1}{2\sqrt{K\tau}}.$$

Thus, the closed loop gain magnitude is

$$|H(j\omega)| = N_{FB}\left[\frac{1}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2}\right]^{1/2},$$

and the closed loop gain phase is

$$\phi(j\omega) = -\arctan\frac{2\zeta\frac{\omega}{\omega_n}}{1 - \left(\frac{\omega}{\omega_n}\right)^2}.$$

From eq. (3), the open loop gain is

$$\beta(s)G(s) = \frac{K}{s(1 + \tau s)},$$

the open loop gain magnitude is

$$|\beta(j\omega)G(j\omega)| = \frac{K}{\omega}\frac{1}{\sqrt{1+(\omega\tau)^2}},$$

and the open loop gain phase is $\theta(j\omega) = -90 - \arctan \omega\tau$.

Note that the phase starts off at −90 degrees and approaches −180 degrees at high frequencies. The larger the value of τ, the lower the damping and the smaller the phase margin. The RC loop filter results in a second-order type-1 PLL.

C.3 Case 3. Lag-lead loop filter: $F(s) = (1 + \tau_2 s)/(1 + \tau_1 s)$

From eq. (4), the closed loop gain is

$$H(s) = \frac{N_{FB}K}{s/F(s) + K} = \frac{N_{FB}K(1+\tau_2 s)}{s(1+\tau_1 s) + K(1+\tau_2 s)}$$

$$= \frac{N_{FB}K(1+\tau_2 s)/\tau_1}{s^2 + s\,\dfrac{1+K\tau_2}{\tau_1} + \dfrac{K}{\tau_1}}.$$

We can get the denominator into the classical second-order control system form of $s^2 + 2\zeta\omega_n s + \omega_n^2$ if we let $\omega_n^2 = K/\tau_1$ and $2\zeta\omega_n = (1 + K\tau_2)/\tau_1$. Then,

$$H(s) = N_{FB}\omega_n^2\,\frac{1 + s(2\zeta/\omega_n - 1/K)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = N_{FB}\,\frac{1 + s(2\zeta/\omega_n - 1/K)}{\left(\dfrac{s}{\omega_n}\right)^2 + 2\zeta\dfrac{s}{\omega_n} + 1},$$

where the undamped natural frequency is

$$\omega_n = \sqrt{K/\tau_1},$$

and the damping is

$$\zeta = \frac{1}{2\omega_n}\left(\frac{1}{\tau_1} + \frac{\tau_2 K}{\tau_1}\right) = \frac{\omega_n}{2}(\tau_2 + 1/K).$$

Thus, the closed loop gain magnitude is

$$|H(j\omega)| = N_{FB}\left\{\frac{1 + (2\zeta\omega/\omega_n - \omega/K)^2}{\left[1 - \left(\dfrac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\dfrac{\omega}{\omega_n}\right)^2}\right\}^{1/2},$$

and the closed loop gain phase is

$$\phi(j\omega) = \arctan\left(2\zeta\frac{\omega}{\omega_n} - \frac{\omega}{K}\right) - \arctan\frac{2\zeta\dfrac{\omega}{\omega_n}}{1 - \left(\dfrac{\omega}{\omega_n}\right)^2}.$$

From eq. (3), the open loop gain is

$$\beta(s)G(s) = \frac{K(1 + \tau_2 s)}{s(1 + \tau_1 s)},$$

the open loop gain magnitude is

$$|\beta(j\omega)G(j\omega)| = \frac{K}{\omega}\left\{\frac{1 + (\omega\tau_2)^2}{1 + (\omega\tau_1)^2}\right\}^{1/2},$$

and the open loop gain phase is

$$\theta(j\omega) = -90 + \arctan(\omega\tau_2) - \arctan(\omega\tau_1).$$

Note that the phase starts off at −90 degrees, approaches −135 degrees midway between $1/\tau_1$ and $1/\tau_2$, and then approaches −90 degrees again for high frequencies.

The lag-head loop filter results in a second-order type-1 PLL. (For large gain K, eq. (7) reduces to eq. (8), i.e., the lag-lead loop filter is an approximation of the second-order active loop filter.)

C.4 Case 4. Second-order active loop filter: $F(s) = (1 + \tau_2 s)/(\tau_1 s)$.

If it is desired to account for the operational amplitude pole, the designer may lump this pole into the VCO parasitic pole. Try to keep the operational amplitude bandwidth much larger than the PLL bandwidth (defined in Section 4.2).

From eq. (4), the closed loop gain is

$$H(s) = \frac{N_{FB}K}{s/F(s) + K} = \frac{N_{FB}K(1 + \tau_2 s)}{s^2\tau_1 + K(1 + \tau_2 s)} = \frac{N_{FB}K(1 + \tau_2 s)/\tau_1}{s^2 + sK\tau_2/\tau_1 + K/\tau_1}.$$

We can get the denominator into the classical second-order control system form of $s^2 + 2\zeta\omega_n s + \omega_n^2$ if we let $\omega_n^2 = K/\tau_1$ and $2\zeta\omega_n = K\tau_2/\tau_1$. Then,

$$H(s) = \frac{N_{FB}\omega_n^2\left(1 + \dfrac{2\zeta}{\omega_n}s\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = N_{FB}\frac{1 + s(2\zeta/\omega_n)}{\left(\dfrac{s}{\omega_n}\right)^2 + 2\zeta\dfrac{s}{\omega_n} + 1},$$

where the undamped natural frequency is

$$\omega_n = \sqrt{K/\tau_1},$$

and the damping is

$$\zeta = \frac{1}{2\omega_n}\frac{K\tau_2}{\tau_1} = \frac{\omega_n\tau_2}{2}.$$

Thus, the closed loop gain magnitude is

$$|H(j\omega)| = N_{FB}\left\{\frac{1 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2}{\left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2 + 4\zeta^2\left(\frac{\omega}{\omega_n}\right)^2}\right\}^{1/2},$$

and the closed loop gain phase is

$$\phi(j\omega) = \arctan[2\zeta(\omega/\omega_n)] - \arctan\frac{2\zeta\frac{\omega}{\omega_n}}{1 - \left(\frac{\omega}{\omega_n}\right)^2}.$$

From eq. (3), the open loop gain is

$$\beta(s)G(s) = \frac{K(1 + \tau_2 s)}{\tau_1 s^2},$$

the open loop gain magnitude is

$$|\beta(j\omega)G(j\omega)| = \frac{K}{\tau_1\omega^2}\sqrt{1 + (\omega\tau_2)^2},$$

and the open loop gain phase is

$$\theta(j\omega) = -180 + \arctan(\omega\tau_2).$$

Note that the phase starts off at −180 degrees and approaches −90 degrees at high frequencies. Thus, the second-order PLL exhibits a large phase margin, even with parasitic (VCO) poles. Ensure $\tau_1 < \tau_2$ for good stability.

This loop filter results in a second-order type-2 PLL.

C.5 Case 5. Third-order active loop filter: $F(s) = (1 + \tau_2 s)/[\tau_1 s(1 + \tau_3 s)]$

From eq. (4), the closed loop gain is

$$H(s) = \frac{N_{FB}K}{s/F(s) + K} = \frac{N_{FB}K(1 + \tau_2 s)}{s^2\tau_1(1 + \tau_3 s) + K(1 + \tau_2 s)}$$

$$= \frac{N_{FB}K(1 + \tau_2 s)}{s^3\tau_1\tau_3 + s^2\tau_1 + sK\tau_2 + K}.$$

Thus, the closed loop gain magnitude is

$$|H(j\omega)| = N_{FB}K\left\{\frac{1 + (\omega\tau_2)^2}{[K - \omega^2\tau_1]^2 + [\omega K\tau_2 - \omega^3\tau_1\tau_3]^2}\right\}^{1/2},$$

and the closed loop gain phase is

$$\phi(j\omega) = \arctan(\omega\tau_2) - \arctan\frac{(\omega K\tau_2 - \omega^3\tau_1\tau_3)}{(K - \omega^2\tau_1)}.$$

From eq. (3), the open loop gain is

$$\beta(s)G(s) = \frac{K(1 + \tau_2 s)}{\tau_1 s^2(1 + \tau_3 s)},$$

the open loop gain magnitude is

$$|\beta(j\omega)G(j\omega)| = \frac{K}{\tau_1\omega^2}\left\{\frac{1 + (\omega\tau_2)^2}{1 + (\omega\tau_3)^2}\right\}^{1/2},$$

and the open loop gain phase is

$$\theta(j\omega) = -180 + \arctan(\omega\tau_2) - \arctan(\omega\tau_3).$$

Note that the phase starts off at −180 degrees, approaches −135 degrees midway between τ_2 and τ_3, and then approaches −180 degrees again for high frequencies.

For the third-order active filter case, it is possible to define an equivalent damping and natural frequency if we let $1/\tau_3$ be much higher than $1/\tau_2$. Rather than making this approximation, PLACE solves directly for the phase margin using an algorithm (see Ref. 18) that optimizes phase noise performance. The point of minimum phase shift (i.e., the inflection point of the open loop gain phase) is placed at exactly the frequency ω_u for unity open loop gain. (The user can specify ω_u, or else PLACE defaults the value to $f_u = f_{ref}/50$.) This will occur when the loop filter time constants obey the following relations:

$$\tau_3 = \frac{\sec(\text{pm}) - \tan(\text{pm})}{\omega_u}$$

$$\tau_2 = \frac{\tau_3}{\omega_u^2}$$

$$\tau_1 = \frac{\text{K}}{\omega_u^2}\left\{\frac{1 + (\omega_u\tau_2)^2}{1 + (\omega_u\tau_3)^2}\right\}^{1/2}.$$

PLACE asks the user for the desired phase margin and computes the above values for τ_1, τ_2, and τ_3. Later the user has the opportunity to enter his own values for these variables.

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