The 5ESS Switching System:

Hardware Design

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This paper gives a general description of the *5ESS*™ switch hardware design. A significant amount of new hardware, including numerous very-large-scale integration circuits, microprocessors, signal processors, and memory devices, is used in the *5ESS* switch design to accomplish its operational and maintenance design objectives. By adhering to the distributed and modular architecture in all the hardware designs, the incorporation of advancing technologies and new functionality is accomplished with ease.

I. INTRODUCTION

The *5ESS* switch hardware architecture is composed of the Administrative Module (AM),‡ one or more Switching Modules (SMs), and a Communications Module (CM) as major system elements. Control of the office is distributed between the AM, which consists of a single AT&T 3B20D computer complex, and one or more SM processors. Communication among all these processors is performed by the Message Switch (MSGS) contained in the CM. Switching in the office is performed with a time-space-time Pulse Code Modulation (PCM) digital switching network. This network consists of a Time-Slot Interchanger (TSI) in each SM and a single Time-Multiplexed Switch (TMS) within the CM. The TMS, MSGS, and SMs are interconnected with high-speed optical-fiber links that carry network data, control

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messages, and timing information. Interfaces to lines, trunks, and pair-gain systems are provided by a variety of digital and analog interface units. Numerous other circuits, such as the Signal Processor (SP), Digital Service Unit (DSU), and Metallic Service Unit (MSU) provide the resources and functionality necessary for call processing and maintenance of the office. SMs can be located up to 125 miles from the office, and connected by T-carrier facilities.

The hardware design, which used sophisticated machine aids extensively, has taken advantage of many technological advances. A new high-voltage Gated-Diode-Crosspoint (GDX) technology is employed in a solid-state, low-cost, and efficient line concentrator. Very large scales of integration are used in 64K-bit memory chips, custom logic, digital signal processing, and time-slot interchanging. A single-chip codec/filter is employed. Optical-fiber links pioneer an interframe interconnection media. Extensive use is made of microprocessors to realize the design of the 5ESS switch's distributed processing architecture.

The major hardware design objectives included a highly reliable system, functionality for numerous switching applications, the ability to accept gracefully the introduction of new technology and low cost. In addition, minimizing power consumption and floor space and providing for short installation intervals are included as design objectives.

The physical design of the 5ESS switch is covered in a companion paper.[1]

II. CONTROL STRUCTURE

The switching network of the 5ESS switch is controlled, as shown in Fig. 1, by the AM and the SM. The AM performs the switching network path-selection function, whereas the SM performs most of the call-processing functions. Control information among the processors within these modules is communicated via messages that are transferred from the sending processor to the receiving processor by the MSGS. Messages that originate or terminate at the SM processor are transmitted by the MSGS over optical-fiber links.

2.1 Message switch

All interprocessor message transfers are performed by the MSGS. For a message to be transferred from one SM processor to another, the originating processor, illustrated in Fig. 2, transmits the message on a dedicated control time slot over its Network Control and Timing (NCT) link to the TMS. The message is switched from the TMS onto another NCT link that connects to the MSGS. Within the MSGS, an MSGS peripheral controller known as the module message processor
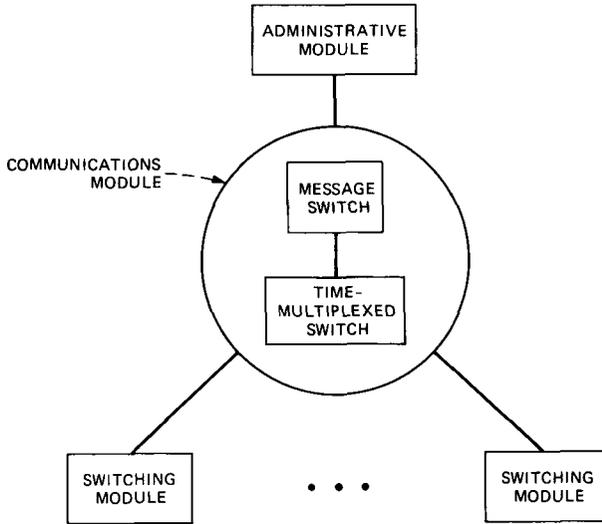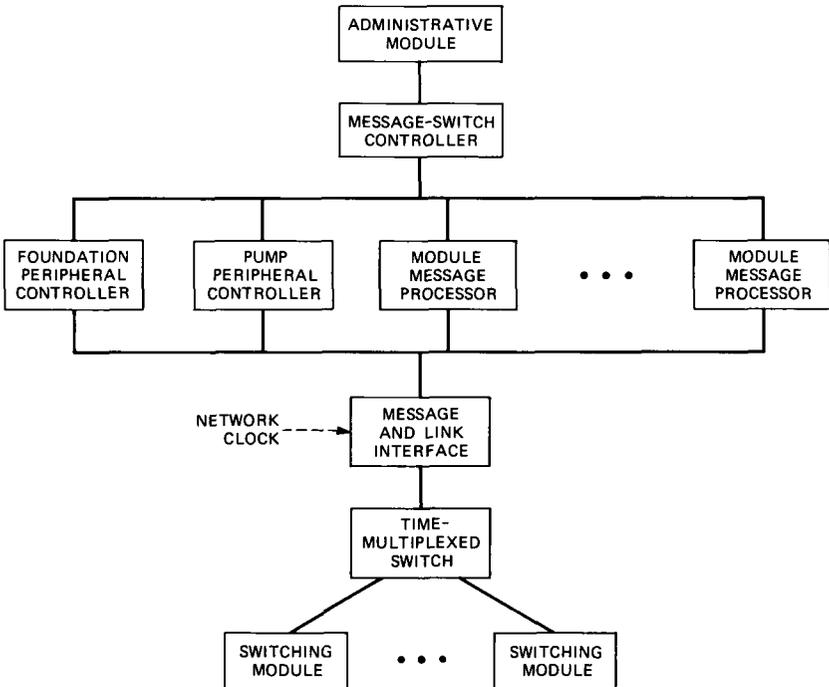
Fig. 1—*5ESS* hardware architecture.

Fig. 2—Message-switch interprocessor communication.

receives the message and, with the help of the MSGS controller, transfers the message to the dedicated control time slot of the destination SM processor. If the message is destined for the AM, the MSGS controller transfers the message from the module message processor to the AM over a high-speed serial bus.

In addition to the messages associated with normal operation of the switch, the MSGS is designed to transfer large quantities of bulk data and program text from the AM to an SM processor. A pump peripheral controller is used for this operation. The effective data rate of this type of transfer is 192K bytes per second. At this data rate an SM processor can be loaded with 4M bytes of program text and data in about 40 seconds (including protocol overhead time).

The MSGS is also capable of transferring special maintenance messages from the AM to an SM processor. These messages, known as processor-intervention messages, travel through the MSGS in parallel with normal messages and are sent by the AM to force the SM processor into a particular state.

Messages from the AM that control the operations of the MSGS can be transferred over the high-speed serial bus to the MSGS controller. Depending on the type of message, either the MSGS controller will be the destination of the message, or an MSGS peripheral controller will be the destination. Control messages from the MSGS controller or an MSGS peripheral controller to the AM can also be transferred.

One specific MSGS peripheral controller, known as the foundation peripheral controller, processes AM control messages that are destined for, or originate from, the network clock, the TMS, and the MSGS's message and link interface circuitry. The foundation peripheral controller communicates with the network clock, the TMS, and the message and link interfaces over a standard dedicated bus known as the control and diagnostic access link.

2.1.1 Message-switch controller

The MSGS controller is designed around four bit-sliced microprocessor chips. The design includes circuitry to interface with the AM's dual serial channel that allows direct memory access transfers of data between the AM's processor and the MSGS controller.

Also included in the design is a microprocessor I/O bus. This bus allows the MSGS controller to communicate via direct memory access with up to 14 MSGS peripheral controllers that may be handling message traffic for up to 48 SM processors.

Up to 5 million, 30-byte messages can be handled per hour by this design. Microcoded algorithms are used to achieve this message throughput. The design includes nearly nine thousand 40-bit in-

structions of microcode. About one-half of these instructions are for maintenance functions and the rest are for message-processing functions.

2.1.2 Message-switch peripheral controllers

There can be a total of 14 MSGS peripheral controllers equipped in the MSGS. One of these is the foundation peripheral controller and another is the pump peripheral controller. The remaining 12 controllers are module message processors that are available for communication with SM processors. Each of these 12 module message processors handles eight BX.25 links. To provide interprocessor communication with high reliability, the entire complex of 14 MSGS peripheral controllers is duplicated and four BX.25 links (two from each duplicated side) are interconnected for communication with each SM processor.

Each MSGS peripheral controller is designed around a microprocessor chip that is operated at an 8-MHz clock rate. The design's memory system supports 128K bytes of dynamic RAM for software text and data. An additional 16K bytes of ROM is provided for initialization programs. In addition, 8K bytes of RAM is specifically designed for message queues. This special "mailbox" memory includes arbitration circuitry to control access in a prioritized way by the processor itself and the MSGS controller.

2.2 Switching module processor

The SM processor performs most of the call-processing functions that control the *5ESS* switching network. The design supports up to 16M of RAM for program text and data and up to 128K bytes of ROM for initialization programs. To achieve high reliability the processor and memory system are fully duplicated. Special circuitry is included to provide the required maintainability and real-time performance.

2.2.1 Processor core functions

The SM processor is designed around a single microprocessor chip that is operated at a 9-MHz clock rate. Circuitry to provide interrupt handling, address mapping, bus control, power-up sequencing, alarming, and several other special functions is included as part of the processor's core design, as diagrammed in Fig. 3.

Three interrupt levels are used in the SM processor: one for operational and routine maintenance, the second for reconfiguration messages, and the third for reset errors. There are several different sources of interrupts at each of these levels. They may all be masked under software control with the exception that critical maintenance
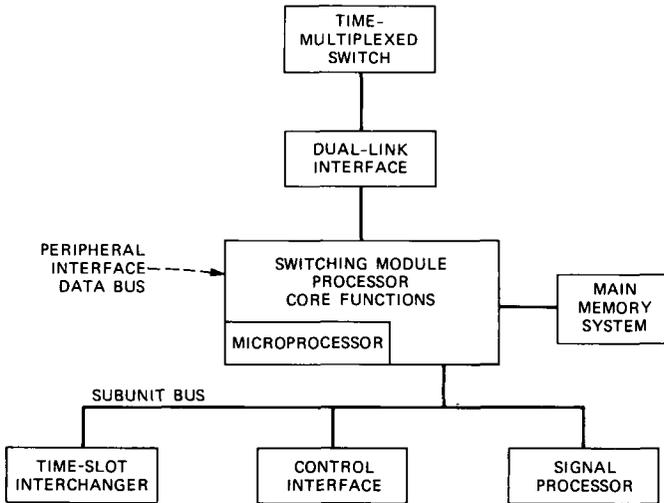
Fig. 3—Switching module processor connectivity.

messages, such as reset, sanity-timer time-out, and test system inter-
rupts, may not be masked.

2.2.2 Processor I/O

I/O operations for the SM processor consist of either interprocessor
message transmissions or communication with the other circuitry in
the SM, such as the TSI.

Interprocessor messages are formatted and queued for transmission
by software routines. The SM processor transfers these messages by
direct memory access circuitry to a synchronous data link control chip
that applies BX.25 protocol to the messages. The messages are then
transmitted in the appropriate control time slot by the dual-link
interface circuit.

Large quantities of data and program text may be loaded into the
SM processor's memory system. This operation, known as "pump,"
requires special circuitry in the SM processor and a connection to the
Peripheral Interface Data Bus (PIDB).

The SM processor communicates with other units within the SM
on the subunit bus. The subunit bus allows 16 bits of data and 6
device address bits to be transmitted to the subunits. Each unit on
this bus receives its own unit-select signal and is capable of specifying
the number of processor wait states needed to complete its operation.
There are currently three different subunits: the TSI, the SP, and the
control interface.

Of particular importance, the control interface circuitry provides an
interface for control information to all the SM peripheral units. This

interface is over a standardized bus known as the Peripheral Interface Control Bus (PICB). By using this bus peripheral units can evolve independently of the SM processor.

In addition to interprocessor messages and subunit I/O operations, numerous (about 100) special-function and status-register operations are performed. These operations, as with the message and subunit bus functions, are memory-mapped operations. One class of special registers is known as the shadow registers. These registers capture the state of various bus levels and other machine registers when certain maintenance interrupts occur. The captured information allows for higher resolution of the source of the interrupt that may have been caused by either a hardware or software failure.

2.2.3 Processor main memory system

The SM processor's I/O total address spectrum encompasses 16 million locations. Memory-mapped I/O uses 8K addresses, leaving the remaining locations available for program text and data. The main memory system provides up to 128K bytes of ROM for processor initialization programs, and 8K bytes of fast static RAM for operating system stacks and special diagnostic functions. The remainder of the memory spectrum may be populated with dynamic RAM as needed. Currently, about 4 megabytes of RAM are required, 64K bytes of ROM, and 8K bytes of fast static RAM.

The dynamic RAM portion of the memory system uses memory planes that are organized as 40-bit words by 256K locations. The 40 bits per location are addressable by the memory system's controller as 4 bytes. The remaining 8 bits contain the Hamming function code for that location.

The memory system controller includes Hamming function circuitry. This circuitry is capable of detecting double-bit errors and correcting single-bit errors. This circuitry is implemented in custom gate arrays.

The memory system includes both write-protection and stack-protection circuitry. The write-protection circuitry inhibits mutilation of software text and protected data. The stack-protection circuitry inhibits a software function from writing into another function's stack frame and guards against stack overflows.

III. SWITCHING NETWORK

The network of the 5ESS switch, a time-space-time network, is depicted in Fig. 4. The time-division portion consists of distributed, concentrating TSIs that each multiplex up to 1024 time slots from the network's periphery (lines, trunks, and service circuits) to 512 time slots toward the space-division portion. The CM contains a TMS that is a very fast space-division switching fabric that makes and tears
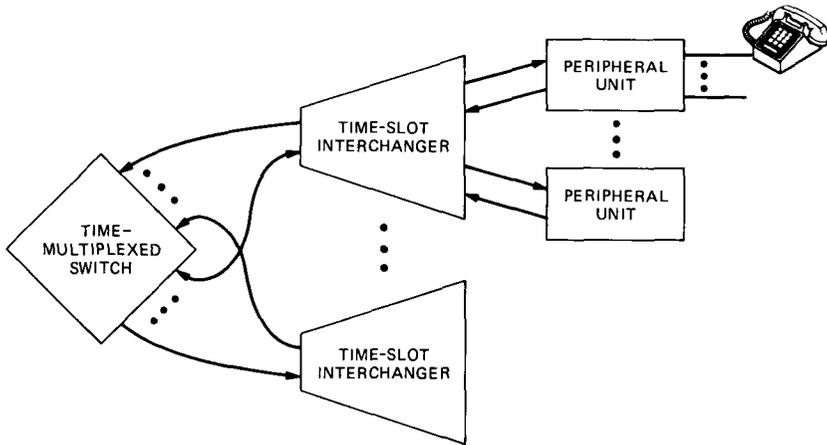
Fig. 4—Time-space-time digital switching network.

down connections between TSIs on an individual time-slot basis. The TSIs and the TMS are interconnected by optical-fiber links. Timing for the *5ESS* switch is provided by the CM's network clock and is distributed by the TMS to the TSIs over the optical-fiber links.

Within the *5ESS* switch the signaling and control information is carried along with data throughout the switch. The TSIs, the TMS, and the optical-fiber links are designed for 16-bit time slots in which 8 bits are data and 8 bits are signaling and control information. The signaling bits are used in a variety of ways. For example, one signaling bit typically carries on-hook/off-hook status and therefore can be used to detect switchhook "flashes." Another signaling bit is used within the *5ESS* switching fabric to mark the status of each time slot as idle or busy. Yet another bit, the parity bit, is important to the detection of hardware faults. Some signaling is contained within the data band, for example, tone-dialing signals and dial tone. The above examples are intended to convey the idea that a considerable amount and variety of signal processing must occur within the switch. Signal processing is performed in either of two units: an SP that is closely associated with each TSI and is used for functions that must be performed on a per-time-slot basis; and a digital service unit that performs more complex signal processing that can be shared over several active time slots.

3.1 Design considerations

Although implementation cost is a design consideration, an even more important consideration for the switching network hardware is reliability. Several of the approaches taken to ensure operational reliability for the switching network are listed below.

1. All the major switching units are duplicated, and selected units are cross coupled.

2. Circuitry that can detect, contain, and report hardware faults is included. In this circuitry, error containment is a major consideration that must be provided so that hardware errors propagate as little as possible and never to the duplicated portion of the network.

3. Although software can completely control the hardware configuration, certain classes of serious faults are handled autonomously by the hardware.

Another major design consideration is to provide for potential design evolution. For the lifetime of the switching network to extend over decades or more, it is essential for the hardware design to be capable of evolving to take advantage of technology evolution and market needs. This consideration led to careful partitioning of functions with attention to interfaces. The following examples are illustrative.

1. The optical-fiber links that connect the TMS to the TSIs carry all interconnection information (data, control, and timing). With technology evolution it is expected that the maximum distance possible for the optical-fiber link connection will be many miles. This will result in a widely distributed switching network.

2. The connection of the TSI to the SM peripheral units that interface to lines and trunks is over a standardized data bus known as the PIDB. This bus carries timing, data, and signaling. Peripheral units can evolve independently of the TSI by using this bus.

3. Evolution was also considered in the design of the interfaces to the software system. For example, the TMS controller was designed so that software can communicate with it via high-level messages that are independent of a particular hardware implementation of the TMS.

3.2 Design descriptions

3.2.1 Optical-fiber links

Multimode optical-fiber links interconnect the TSIs and the TMS. Information is transmitted in nonreturn-to-zero format at 32.768 Mb/s framed into two hundred fifty-six 16-bit time slots at an 8-kHz frame rate. Separate fibers are used for each direction of data flow. Therefore, four links are required in each direction to support each TSI. An LED serves as the optical transmitter and a pin photodiode is used as a light transducer in the receiver. Clock and frame timing is extracted from the data stream by the receiver-associated circuits to accomplish synchronous data transmission. Up to a full frame of buffer storage is provided at the receiving end to remove any constraint on cable-length matching.

3.2.2 Time-multiplexed switch

A simplex TMS is composed of two independent switching fabrics and a common microprocessor controller. Each 32 × 32 switch unit interfaces to one NCT link from as many as 30 SMs, a test input, and

a link from the MSGS. Optical-fiber links carrying even-numbered time slots connect to the "even" switch unit, while odd-numbered time slots connect to the "odd" switch unit. Data from the link interfaces are divided into dual 16-Mb/s data streams for transmission through the switch multiplexers. Error reporting and analysis, path request handling, and initialization are tasks of TMS controller firmware, which provides an intelligent interface between the AM and the switch unit hardware. Link time slots passing through faulty circuitry will have their busy/idle status bits forced to the idle state for interpretation by special maintenance circuits in the TSI.

3.2.3 Time-slot interchanger

Within each SM, dual 512 × 512 TSIs perform the switching function in each direction of the path connection (periphery-to-network or network-to-periphery). Special loopback paths within each TSI establish peripheral-to-peripheral and network-to-network connections. Each slide of the duplicated TSI is able to select automatically network data from either side of the duplicated TMS by examining "valid data" markers on every incoming network time slot.

The digital service unit tone generators and decoders have switched access so that the unit can be the source of or receive data on any peripheral or network time slot. The SM processor also has switched access, which allows it to be the source of and to observe data on any TSI time slot.

A 2:1 concentration function allows up to 32 peripheral data buses of 32 time slots each to access the 512 time slots of the TSI.

Data going from the TSI to the periphery can be optionally attenuated by a digital attenuation function in the TSI. This function is individually controllable on a per-time-slot basis to provide a selectable attenuation level of up to 15 dB.

The TSI also provides dedicated signaling bit access to and from the SP for all signaling and control bits on each of the 512 peripheral time slots in the TSI.

3.2.4 Signal processor

The SP can be the source of signaling and control bits on each of the 512 peripheral time slots in the TSI. In addition, the SP monitors all incoming signaling and control bits from the 512 time slots for state changes and reports all transitions that last longer than 6 ms. The SP is controlled by the SM processor so that reports of signaling changes on any time slot can be inhibited or allowed.

3.2.5 Digital service unit

The DSU provides the 5ESS switch with digital signal processing capabilities. The capacity of a DSU is engineered to meet peak service

demands so that the digital processing resources can be shared across all active channels. The *5ESS* switch requires two applications of the DSU. The first application, known as the local DSU, provides heavily used services by locating a DSU within each SM. A local DSU is responsible for creating and transmitting call-progress tones, multifrequency signals, tone-dialing signals, and common channel interoffice signaling continuity check tones. It also does dial-pulse collection, tone-dialing decoding, and detection of multifrequency signals. The second DSU application, called the global DSU, provides low-runner services such as three-party conferencing and special transmission test functions. A global DSU is shared across all SMs in an office.

To provide reliable operation the DSU is composed of two service groups that share the load so that a single fault can at most reduce DSU capacity by 50 percent. The DSU uses AT&T Technologies digital signal processing chips for almost all its required services.

IV. SUBSCRIBER INTERFACE AND METALLIC TESTING

4.1 Line unit

The *5ESS* switch Line Unit (LU) interfaces to analog subscriber lines. In particular, this includes conventional loop-start, ground-start, and PBX trunks. Since these analog terminations typically constitute most of the terminations in an office, the LUs represent a large fraction of the total equipment and cost of the *5ESS* switch. Thus, an important engineering consideration in the design of the LU is its manufacturing and maintenance cost.

Since the LU interfaces with conventional subscriber loops, it must be capable of withstanding lightning surges and power crosses, and it must interface with a large variety of station equipment. In addition, it is desirable to minimize the amount of engineering required for any given LU within an office, since equipment terminations and traffic patterns tend to change and evolve with changing communication needs in an area.

Finally, the reliability and maintenance of the unit are prime considerations in the design. It is essential that the unit require minimal maintenance, and it is also highly desirable that the equipment be designed such that faults and problems can be isolated without denying service to the connected subscribers.

These design objectives are provided in the *5ESS* switch LU by joining a new high-voltage silicon technology (used to achieve a concentrating network function on ceramic hybrids) with state of the art low-voltage complementary metal-oxide semiconductor silicon technology (used to provide the analog-to-digital conversion function). This combination of technologies gives the advantages of low cost and digital device technology for the *5ESS* switch LU.
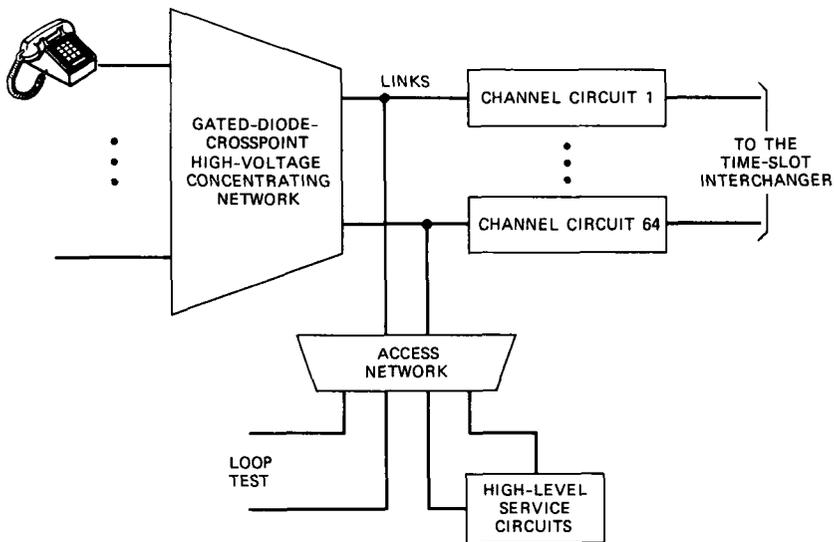
Fig. 5—Subscriber line unit.

4.1.1 Concentration network

Subscriber appearances terminating on the LU are switched to channel circuits that provide battery feed, analog-to-digital conversion, and other functions, as indicated in Fig. 5. The concentration ratio of lines to channel circuits is a function of the expected traffic level in the application. Ratios of 8:1 and 6:1 are achieved by simply removing optional plug-in circuit packs. Ringing and loop-testing functions are provided through an access network that further concentrates the 64 links to six high-level service circuits and two test ports.

The fundamental building block of this space-division concentrator is the GDX device. This 590V silicon technology device was initially developed to meet the needs of the 5ESS LU application. The device itself is configured as a 2 × 2 switch that serves both the tip and ring conductors of a connection.

The GDX device is packaged in a hermetically sealed chip carrier that, in turn, is mounted on a ceramic substrate that interconnects several GDX devices. This hybrid integrated circuit also has control circuitry for the local GDX devices. Since large voltages can be present on the tip and ring conductors (±265V), special hybrid integrated-circuit technology and high-voltage control circuits were also specially developed for this application. Five hybrid integrated-circuit codes were developed for the space-division concentrator network.

These GDX hybrid integrated circuits are placed on conventional double-sided printed wiring boards along with the power supplies,

alarm circuits, overvoltage protection circuits, and the required control logic. Sixty-four customers are served by three circuit packs that constitute a grid. For maintenance and control purposes, the three circuit packs are handled by software as a single unit.

The origination detection circuits do not use the usual "balanced" detector design, but, rather, they use a detector/filter combination on the ring conductor only. This arrangement with separate cutoff cross-point control on the 1400-ohm scan resistors to ground and battery allows the same electrical circuit to work for loop-start or ground-start applications. This option can be selected in system software and requires no special equipment rearrangements.

An LU can be equipped with six to eight grids, depending on the expected traffic level. When equipped with eight grids, the unit serves 512 lines with traffic levels up to 3.2 CCS/line. When equipped with six grids, the unit serves 384 lines with up to 5.2 CCS/line.

4.1.2 Access network

The space-division network as depicted in Fig. 5 provides switched paths between two classes of service circuits. Sixty-four channel circuits provide battery feed, two-wire to four-wire conversion, loop supervision, and analog-to-digital functions for the subscriber terminations. The access network connects high-level service circuits that provide ringing voltages, coin control pulses, and network test functions.

4.1.3 Channel circuits

Since the channel circuits serve the connected subscribers through a GDX network, several new requirements are placed on them. The GDX device exhibits a nonlinear characteristic when the current through the device reverses direction. To prevent this device characteristic from interfering with telephone calls in the talking state, the battery-feed current is supplied differentially to the tip and ring conductors but floating with respect to earth ground. To prevent loop conductors from corroding as a result of positive potentials on the conductors, a special circuit on the channel pack detects cable corrosion conditions and biases the loop conductors negative. The GDX network also has a finite series resistance for which the channel circuit must compensate with added gain. Finally, the channel circuit's hybrid circuits must appropriately terminate both loaded and nonloaded customer loops. The appropriate balance network is selected by system software from information stored in the SM processor's memory resulting from on-hook loop tests done periodically by system maintenance software.

Since the *5ESS* system is intended for international as well as domestic applications, several different versions of channel circuits are

available. Termination impedances, battery-feed-current profiles, and A-law or μ-law codec versions are available. The modularity of partitioning in the system allows this critical function to take advantage of rapidly changing technology in planned product evolution for future applications.

4.1.4 High-level service circuits

The subscriber loop plant requires a variety of signal voltages, including 20 Hz, 88V rms ringing, ±130V coin-control pulses, and others. In addition, the LU itself must check its operations and be capable of further diagnostic tests that detect faulty circuits. Previous systems have met these requirements by terminating a variety of special-purpose circuits on the switching network. These special-purpose circuits in general were engineered for each application.

In the *5ESS* LU, special signaling requirements are met by a universal high-level service circuit that is configured under software control. Because each circuit can handle a variety of tasks and the holding time for a particular task is short, six circuits can meet the needs of 512 lines independent of the particular service mix on that unit.

The high-level service circuit itself is a dc-to-dc converter capable of 15W and 200V. The output of this converter is fed to the switching network through a full-wave bridge-type switching circuit that acts as an amplifier to low-level signals produced by the signal generator on the circuit pack. The low-level signal generator produces 20-Hz signals and other required signal voltages, and the bridge switch amplifier produces at the high-level service circuit output a signal amplified 50 times. This circuit pack also contains an accurate current-sensing circuit that is used to verify proper operation of the LU and to detect the presence of the ring trip condition during ringing on the subscriber loop.

High-level service circuits are time shared among various system processes under software control. The circuit can be reconfigured quickly (100 ms) to provide a burst of ringing, do a power-cross check, collect a coin from a coin phone, or do a network integrity check.

4.2 Metallic service unit

The MSU provides a two-wire metallic switching matrix that interconnects dc and low-frequency test equipment to subscriber lines and metallic trunks. It is a highly concentrated resource that accommodates service circuits that are traffic engineered for each office. The service circuits do basic test, test interconnection, and alarm-reporting functions. The service circuit functions have been packaged into five circuit pack codes that provide metallic access, GDX compensation,

automatic line insulation testing, and general scan and distribute functions. To perform a typical test the system software configures the service circuits into the switching network as appropriate.

For reliability purposes, an MSU contains two service groups, each with its own common control circuit and interface to the SM processor. In large offices several MSUs may be needed to accommodate all the necessary service circuits. These units are interconnected by a metallic test interconnect bus that enables any single test resource to access any line or trunk in the office.

V. TRANSMISSION INTERFACES

There are three different transmission interface units that may be provided in an SM for connection to analog trunk facilities, a T1-carrier, and subscriber line carrier equipment. These units make extensive use of custom Very-Large-Scale Integration (VLSI) devices to achieve cost-effectiveness and dense packaging.

5.1 Trunk unit

The trunk unit provides the interface for all analog trunks on the *5ESS* switch. This includes both metallic and analog carrier trunks. The trunk types provided include E&M (both two-wire and four-wire), loop (both incoming and outgoing), and a test trunk interface.

Although many types of trunks are supported, the trunk circuits differ only in the type of signaling and transmission scheme that they use. These differences are provided by trunk facility interface circuitry. The control and voice interface is common on all *5ESS* switch trunk circuits and provides the analog-to-digital conversion (codec) function and trunk circuit control functions.

5.2 Digital line trunk unit

The Digital Line Trunk Unit (DLTU) is designed to interface digital trunks on the *5ESS* switch. The primary function of the DLTU is to convert the bipolar T1-carrier format into a unipolar format and distribute the T1-carrier frame onto the 32-time-slot PIDB frame of the SM.

The DLTU contains up to ten Digital Facility Interface (DFI) circuits, a power-start circuit, and an equalizer circuit. The power-start circuit controls power to a DLTU, and the equalizer is used to guarantee that the DSX-1 is at an equal-level point in the office.

The key circuit in the DLTU is the DFI circuit that provides all the functions required to terminate a T1 line. Four custom VLSI devices provide the functions of bipolar-to-unipolar conversion, framing, slip control, signaling extraction, and insertion and line formatting. The 24 PCM time slots from the T1 line are evenly distributed over

the 32 time slots available on the PIDB. Idle code is used to fill the eight remaining time slots.

Control information from the SM is interfaced by two custom VLSI devices to a microcomputer. These devices provide the protocol conversion needed and a buffered communication interface to the SM processor. The microcomputer guarantees the integrity of the messages passed between it and the SM processor. The microcomputer also maintains the facility. For example, it estimates error rates, performs facility alarm processing, and measures the quality of the other circuitry in the DLTU by running in-service tests.

A second type of DFI circuit uses an additional VLSI device and additional memory to provide a 4-kb/s BX.25 data link. This type of DFI circuit is used to interface between a Host Switching Module (HSM) and a Remote Switching Module (RSM) (see Section VI). It uses the extended framing format in a mode that provides 23 clear channels for PCM and a 24th channel that carries network signaling information.

Recognizing that the *5ESS* switch plays an important role in the emerging integrated services digital network and taking advantage of firmware control and VLSI technology, two new capabilities not found in the existing network were added to the DFI circuit. They are 64-kb/s clear-channel capability and compatibility with the new extended framing format. Consequently, as the integrated services digital network evolves, the *5ESS* switch can evolve without changing its digital interface hardware.

For international applications a 30-channel DFI circuit is provided by using the same VLSI devices used on the interface for digital message trunks with modified firmware and front-end circuitry.

5.3 Digital carrier line unit

The Digital Carrier Line Unit (DCLU) provides direct interfaces for up to six *SLC*® 96 or *SLC* 5 carrier remote terminals. Except for control and data multiplex functions, it is similar to a DLTU.

Up to 9:1 digital concentration is provided by terminating 576 lines through *SLC* carrier remote terminals spread over two service groups on up to four PIDBs. Each service group under normal operation will interface 288 lines. If a service group fails, the nonfaulted service group can share the load of the faulted service group, thus maintaining customer access to the switch. Consequently, the DCLU operates in an active/active shared mode. Digital concentration is provided by a data multiplex circuit, while distribution of control information from PICBs is done by a control multiplex circuit.

To mitigate the blocking that could occur from digital concentration, a TSI function and on-hook/off-hook supervision are included in the

DCLU. A VLSI device is used for TSI and signaling functions to prevent severe blocking.

VI. REMOTE SWITCHING MODULE

The objective of the *5ESS* switch RSM is to provide the capability within the *5ESS* switch architecture to connect a remotely located SM over T-carrier transmission facilities to a host *5ESS* switch. This capability enables *5ESS* switches to be geographically extended from the host switching machine.

6.1 Design considerations

The applications for RSMs include the replacement of small community dial offices and large clusters of digital loop carrier systems. These applications place certain implementation constraints on both the design and its cost. Some of the principal considerations of the design of the RSM are as follows:

1. The RSM hardware design is constrained to share as much hardware from the SM as possible to maximize commonality and minimize overall hardware cost.

2. Reliability is a major consideration that requires duplication of all major switching units and adherence to all the reliability constraints placed on a nonremoted SM. In particular, the RSM, during a loss of T-carrier facilities, must operate in a stand-alone mode.

3. The RSM is designed to accommodate both domestic and international applications.

6.2 Design descriptions

The remote switching capability consists of an RSM connected over T-carrier facilities to an HSM. As depicted in Fig. 6, the HSM is located in the host office with the CM and AM. Each HSM can support up to a maximum of five RSMs. The RSM can be located as far as 100 miles away from the HSM.

6.2.1 Host switching module

Digital facilities from an RSM are terminated on a DLTU located in the HSM. The termination of these digital facilities is treated by the HSM in the same way as any other nonconcentrated facility. The HSM provides access to the TMS for the data channels on these facilities. Each RSM requires from 4 to 20 T1 lines. An RSM used for community dial office consolidation is expected to require only 6 T1 lines. Since an HSM can support traffic associated with at least 20 T1 lines, the HSM's excess capacity can be shared over several RSMs, T1 trunks, digital loop carrier systems, or analog facilities.
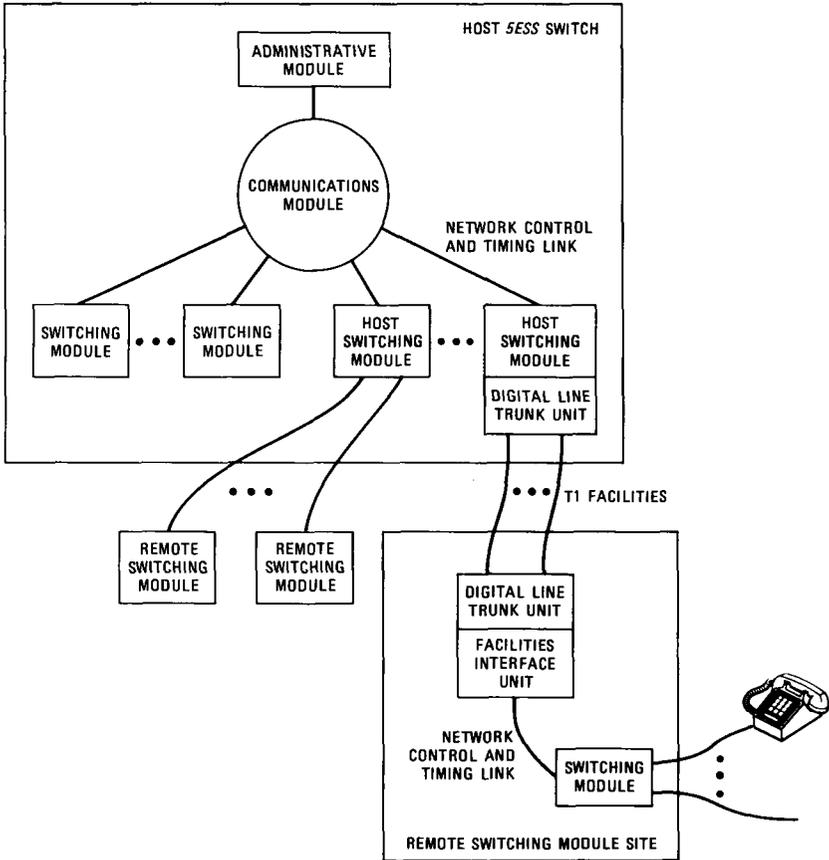
Fig. 6—Host switch with remote switching modules.

Control links for an RSM are routed through the HSM as nailed-up data channels that are assigned cooperatively by the AM and the HSM software. The two required control links are established on the active side of the TMS and duplicated on the standby side. They appear on separate facilities between the HSM and the RSM to minimize the probability of a single failure taking out both control links.

6.2.2 Remote switching module

An RSM is equipped in a way similar to a 5ESS SM except for the addition of a Facilities Interface Unit (FIU). The FIU connects the RSM's SM processor and time-slot interchange unit to the digital trunk facilities provided by the HSM. Data, control, and timing are recovered from the T1 lines, and this information is reformatted into

a pair of NCT link signals, which are routed to the time-slot interchange unit over optical-fiber links. The subunits of the FIU are controlled by peripheral control channels from the active SM processor. Each peripheral control channel is realized through a PICB. A maximum of 22 peripheral control channels are required to support up to 20 DFI circuits and the duplex FIU hardware. Through the peripheral control channels, RSM maintenance software initializes each subunit, receives reports of hardware failures, and does diagnostic testing.

The FIU interface with the trunk facility is through one or two DLTUs that are equipped with DFI circuits. Each T1 line must be terminated on an office repeater that supplies signal equalization, regeneration, and, if needed, line powering. The resultant signals are routed to a DLTU through a standard DSX-1 cross-connect that provides test access to the facility. The DFIs are configured to operate in the RSM mode, whereby they provide 23 clear data channels. In this mode the DFIs also provide T-carrier clock signals to the FIU. These signals are used to lock a local crystal oscillator within the FIU to the network clock provided by the HSM. This oscillator, in turn, determines the data rate on the NCT links, thus assuring synchronization of the RSM to its HSM. This same oscillator provides accurate timing for the RSM during stand-alone operation.

Data through the FIU are multiplexed from up to 20 DFI subunits into two 256 time-slot frames that are formatted into two service groups of two NCT links. Data are similarly demultiplexed in the reverse direction. This multiplex/demultiplex function is performed under a fixed address and time-slot mapping scheme that is driven by time-slot clock and frame synchronization signals produced by the FIU control circuitry.

The hardware of an RSM includes a standard SM with its peripheral circuits, an FIU, and associated DFI(s) for interfacing to the T-carrier facilities. The FIU itself contains only two different circuit pack codes and takes advantage of commonality with other *5ESS* switch equipment by using some of the NCT circuits.

As a result of the flexibility built into the FIU, certain expansion capabilities may be attained through little effort. For example, the RSM hardware can be configured for international applications by simply altering the ROM information stored in the FIU.

VII. SUMMARY

The *5ESS* digital switching system is highly reliable, modular, compact, and low in cost. Its architecture will permit rapid deployment of new services. The modular hardware design allows switching capacity, processing power, and peripheral units to be added incrementally. In addition, this hardware modularity allows the *5ESS* switch hardware

units to evolve independently and take maximum advantage of the advances in semiconductor technology.

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