DESIGN OPTIMIZATION CASE STUDIES

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Designing high quality products at low cost is an economic and technological challenge to the engineer. A systematic and efficient way to meet this challenge is a new method of design optimization for performance, quality, and cost. The method, called "robust design," has been found effective in many areas of engineering design. In this paper, the basic concepts of robust design will be discussed and two applications will be described in detail. The first application illustrates how, with a very small number of experiments, highly valuable information can be obtained about a large number of variables for improving the life of router bits used for cutting printed wiring boards from panels. The second application shows the optimization of a differential operational amplifier circuit to minimize the dc offset voltage by moving the center point of the design, which does not add to the cost of making the circuit.

An Economic and Technological Challenge

A goal of product or process design is to provide good products under normal manufacturing conditions and under all working conditions throughout intended life. Further, the cost of making the product (including development and manufacturing) must be low, and the development must be speedy to meet the market needs. Achieving these goals is an economic and technological challenge to the engineer. A systematic and efficient way to meet this challenge is the method of design optimization for performance, quality, and cost, developed by Genichi Taguchi of Japan. Called "robust design," the method has been found effective in many areas of engineering design in AT&T, Ford, Xerox, ITT, and other American companies. In this paper we will describe the basic concepts of robust design and describe the following two applications in detail:

- A router bit life improvement study
- Optimization of a differential operational amplifier circuit

The first application illustrates how, with a very small number of experiments, highly valuable information can be learned about a large number of variables for improving the life of router bits used for cutting printed wiring boards from panels. The study also illustrates how product life improvement projects should be organized for efficiency. This case study involved conducting hardware experiments, whereas in the second case study a computer simulation model was used. The second application shows the optimization of a differential op-amp circuit to minimize the dc offset voltage. This is accomplished primarily by moving the center point of the design, which does not add to the cost of making the circuit. Reducing the tolerance could have achieved similar improvement, but at a higher manufacturing cost!

Principles of Robust Design

Genichi Taguchi views the quality of a product in terms of the total loss incurred by a society from the time the product is shipped to the customer. The loss may result from undesirable side effects arising from the use of the product and from the deviation of the product's function from the target function. What is novel about this view is that it explicitly includes the cost to the customers and the notion that even products that meet the "specification limits" can impart loss due to nonoptimum performance. For example, the amplification level of a public telephone set may differ from cold winter to hot summer; it may differ from one set to another; also it may deteriorate over a period of time. A consequence of this variation is that a user of the phone may not hear the conversation well and that an expensive compensation circuit may have to be provided. The quadratic loss function can estimate with reasonable accuracy the loss due to functional variation in most cases. For a broad description of the principles of robust design see References 2 to 5.

Sources of Variation. Robust design is aimed at reducing the loss due to variation of performance from the target. In general, a product's performance is influenced by factors that are called noise factors. There are three types of noise factors:

1. *External*—factors outside the product, such as load conditions, temperature, humidity, dust, supply voltage, vibrations from nearby machinery, human errors in operating the product, and so forth.
2. *Manufacturing imperfection*—the variation in the product parameters from unit to unit, inevitable in a manufacturing process. For example, the value of a particular resistor in a unit may be specified as 100 kilohms, but in a particular unit it turns out to be 101 kilohms.
3. *Deterioration*—when the product is sold, all its performance characteristics may be right on target, but as years pass by, the values or characteristics of individual components may change, leading to product performance deterioration.

One approach to reducing a product's functional variation is to control the noise factors. For the telephone set example, it would mean to reduce allowable temperature range, to demand tighter manufacturing tolerance or to specify low-drift parameters. These are costly ways to reduce the public telephone set amplification variation. What then is a less costly way? It is to center the design parameters in such a way as to minimize sensitivity to all noise factors. This involves exploiting the nonlinearity of the relationship between the control factors, the noise factors, and the response variables. Here, control factor means a factor or parameter over which the designer has direct control and whose level or value is specified by the designer.

Note that during product design one can make the product robust against all three types of noise factors described above, whereas during manufacturing process design and actual manufacturing one can reduce variation due to manufacturing imperfection, but can have only minor impact on variation due to the other noise factors. Once a product is in the customer's hand, warranty service is the only way to address quality problems. Thus, a major portion of the responsibility for the quality and cost of a product lies with the product designers and not with the manufacturing organization.

Steps in Product/Process Design. Product and process design are complex activities involving many steps. Three

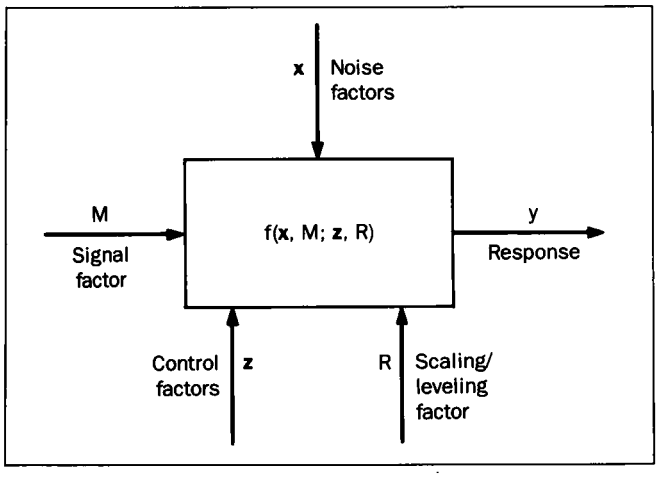


Figure 1. Block diagram of a product or process.

major steps in designing a product or a manufacturing process are system design, parameter design or design optimization, and tolerance design. System design consists of arriving at a workable circuit diagram or manufacturing process layout. The role of parameter design or design optimization is to specify the levels of control factors that minimize sensitivity to all noise factors. During this step, tolerances are assumed to be wide so that manufacturing cost is low. If parameter design fails to produce adequately low functional variation of the product, then during tolerance design, tolerances are selectively reduced on the basis of cost effectiveness.

The Design Optimization Problem. A product or a process can be represented by a block diagram (Figure 1) proposed by Taguchi and Phadke.[3] The diagram can also be used to represent a manufacturing process or even a business system. The response is represented by y. The factors that influence the response can be classified into four groups as follows:

1. Signal factors (M): These are the factors that are set by the user/operator to attain the target performance or to express the intended output. For example, the steering angle is a signal factor for the steering mechanism of an automobile. The speed control setting on a fan and the bits 0 and 1 transmitted in communication systems are also examples of signal factors. The signal factors are selected by the engineer on the basis of engineering knowledge. Sometimes two or more signal factors are used in combination; for example, one signal factor may be used for coarse tuning and one for fine tuning. In some situations, signal factors take on a fixed value, as in the two applications described in this paper.
2. Control factors ($\mathbf{z}$): These are the product design parameters whose values are the responsibility of the designer. Each of the control factors can take more than one value; these multiple values will be referred to as levels or settings. It is the objective of the design activity to determine the best levels of these factors. A number of criteria may be used in defining the best levels; for example, we would want to maximize the stability and robustness of the design while keeping the cost to a minimum. Robustness is the insensitivity to noise factors.
3. Scaling/leveling factors (R): These are special cases of control factors that can be easily adjusted to achieve a desired functional relationship between the signal factor and the response y. For example, the gearing ratio in the steering mechanism can be easily adjusted during the product design phase to achieve the desired sensitivity of the turning radius to a change in the steering angle. The threshold voltage in digital communication can be easily adjusted to alter the relative errors of transmitting 0's and 1's. Scaling/leveling factors are also known as adjustment design parameters.
4. Noise factors ($\mathbf{x}$): Noise factors, described earlier, are the uncontrollable factors and the factors that we do not wish to control. They influence the output y and their levels change from one unit of the product to another, from one environment to another, and from time to time. Only the statistical characteristics of the noise can be known or specified, not their actual values.

Let the dependence of the response y on the signal, control, scaling/leveling, and noise factors be denoted by

$$y = f(\mathbf{x}, M; \mathbf{z}, R)$$

Conceptually, the function f consists of two parts: $g(M; \mathbf{z}, R)$, which is the predictable and desirable functional relationship between y and M, and $e(\mathbf{x}, M; \mathbf{z}, R)$, which is the unpredictable and less desirable part. Thus,

$$y = g(M; \mathbf{z}, R) + e(\mathbf{x}, M; \mathbf{z}, R)$$

In the case where we desire a linear relationship between y and M, g must be a linear function of M. All nonlinear terms will be included in e. Also, the effect of all noise variables is contained in e.

The design optimization can usually be carried out in two steps:

- Find the settings of control factors to maximize the predictable part while simultaneously minimizing the unpredictable part. This can be accomplished through an optimization criterion called signal-to-noise (S/N) ratio. In this step the variability of the functional characteristic is minimized.
- Bring the predictable part, $g(M; \mathbf{z}, R)$, on target by adjusting the scaling/leveling factors.

Design problems come in a large variety. For a classification of design problems and the selection of S/N ratios see Reference 3.

Router Bit Life Improvement

The Routing Process. Typically, AT&T printed wiring boards are made in panels of 18 × 24 inch size. Appropriately sized boards, say 8 × 4 inches, are cut from the panels by stamping or by routing. A benefit of routing is that it gives good dimensional control and smooth edges, thus reducing friction and abrasion during circuit pack insertion. However, when the router bit gets dull, it produces excessive dust, which cakes on the edges and makes them rough. In such cases, a costly cleaning operation is necessary to smooth the edges. But changing the router bits frequently is also expensive.

The routing machine has four spindles, all synchronized in rotational speed, horizontal feed (x-y feed) and vertical feed (in-feed). Each spindle does the routing operation on a separate stack of panels. Two to four panels are usually stacked for cutting by a spindle. The cutting process consists of lowering the spindle to an edge of a board, cutting the board all around using the x-y feed of the spindle, and then lifting the spindle. This is repeated for each board on the panel.

Our objective in this experiment was to increase the life of the router bits, primarily in regard to the onset of excessive dust formation. The dimensions of the board were well in control and were not an issue.

Selection of Control Factors and Their Levels. Selecting appropriate control factors and their alternate settings is an important aspect of optimization. Prior knowledge and experience about the process is used in this selection. The alternate settings are called levels. It is a good practice to choose these levels wide apart so that a broad design space is studied in one set of experiments and there is a potential for major improvement. For the routing process, the eight control factors listed in Table I were chosen.

Suction is used around the router bit to remove the dust as it is generated. Obviously, higher suction could reduce the amount of dust retained on the boards. The starting suction was 2 inches of mercury—the maximum available for the pump. We chose 1 inch of mercury as the alternate level, with the plan that if a significant difference in the dust was noticed, we would invest in a more powerful pump. Related to the suction are suction foot and the depth of backup slot. The suction foot determines how the suction is localized near the cutting point. Two types of suction foot were chosen: solid ring and bristle brush. Underneath the panels being routed is a backup board. Slots are precut in the backup board to provide air passage and a place for dust to temporarily accumulate. The depth of the slots was a control factor in this study.

Stack height and x-y feed are control factors related to the productivity of the process; that is, they determine how many boards are cut per hour. The 3/16-inch stack height means three panels were stacked together, while 1/4-inch stack height means four panels were stacked together. The in-feed determines the impact

Table I. Control Factors and Levels for the Routing Process

Factor	Level			
	1	2	3	4
A. Suction (in of Hg)	1	2*		
B. x-y feed (in/min)	60*	80		
C. In-feed (in/min)	10*	50		
D. Type of bit	1	2	3	4*
E. Spindle position†	1	2	3	4
F. Suction foot	SR	BB*		
G. Stacking height (in)	3/16	1/4*		
H. Depth of slot (mils)	60*	100		
I. Speed (rpm)	30,000	40,000*		

†Spindle position is not a control factor. In the interest of productivity, all four spindle positions must be used.
*Denotes starting condition for the factors.

force during the lowering of the spindle for starting to cut a new board. It could influence the life of the bit by causing breakage or damage to the point. Four different types of router bits made by different manufacturers were used. The router bits varied in cutting geometry in terms of the helix angle, the number of flutes, and the point. Spindle position was not a control factor. All spindle positions must be used in production, otherwise productivity would suffer. It was included in the study so that we could find best settings of the control factors to work well with all four spindles.

In addition to the variation from spindle to spindle, the noise factors for the routing process are the bit-to-bit variation, the variation in material properties within a panel and from panel to panel, the variation in the speed of the drive motor, and similar factors.

The Orthogonal Array Experiment. The full factorial experiment to explore all possible factor-level combinations would require $4^2 \times 2^7 = 2048$ experiments. Considering the cost of material, time, and availability of facilities, the full factorial experiment is prohibitively large. However, it is unnecessary to perform the full factorial experiment because processes can usually be characterized by relatively few parameters. An orthogonal array design with 32 experiments was created from the L_{16} array and the linear graphs given in Reference 1. The array appears in Table II. This design allowed us to obtain uncorrelated estimates of the main effect of each control factor as well as of the spindle position, and the interactions between x-y feed and speed, in-feed and speed, stack height and speed, and x-y feed and stack height. This information about the effect of control factors was used to decide the best setting for each factor. The 32 experiments were arranged in groups of four so that for each group there was a common speed, x-y feed, and in-feed, and the four experiments in each group corresponded to four different spindles. Thus each group constituted a machine run using all four spindles, and the entire experiment could be completed in eight runs of the routing machine.

The study was conducted with one bit per experiment; thus a total of only 32 bits was used. During each machine run, the machine was stopped after every 100 inches of cut (100 inches of router bit movement in the x-y plane) so that the amount of dust could be inspected. If the dust was beyond a predetermined level, the bit was recorded as failed. Also, if a bit broke, it was obviously considered to have failed. Otherwise, it was considered as having survived.

Before the experiment was started, the average bit life was estimated at around 850 inches. Therefore, to save time, each experiment was stopped at 1700 inches of cut, which is twice the estimated original average life, and the survival or failure of each bit was recorded.

Table II gives the experimental data in hundreds of inches. A reading of 3.5 means that the bit failed between 300 and 400 inches. Other readings have similar interpretations, except the reading of 17.5, which means survival beyond 1700 inches, the point where the test was terminated. There are 14 readings of 0.5, indicating extremely unfavorable conditions. There are eight cases of life equal to 17.5, indicating very favorable conditions. During experimentation, it is important to take a broad range for each control factor so that roughly equal numbers

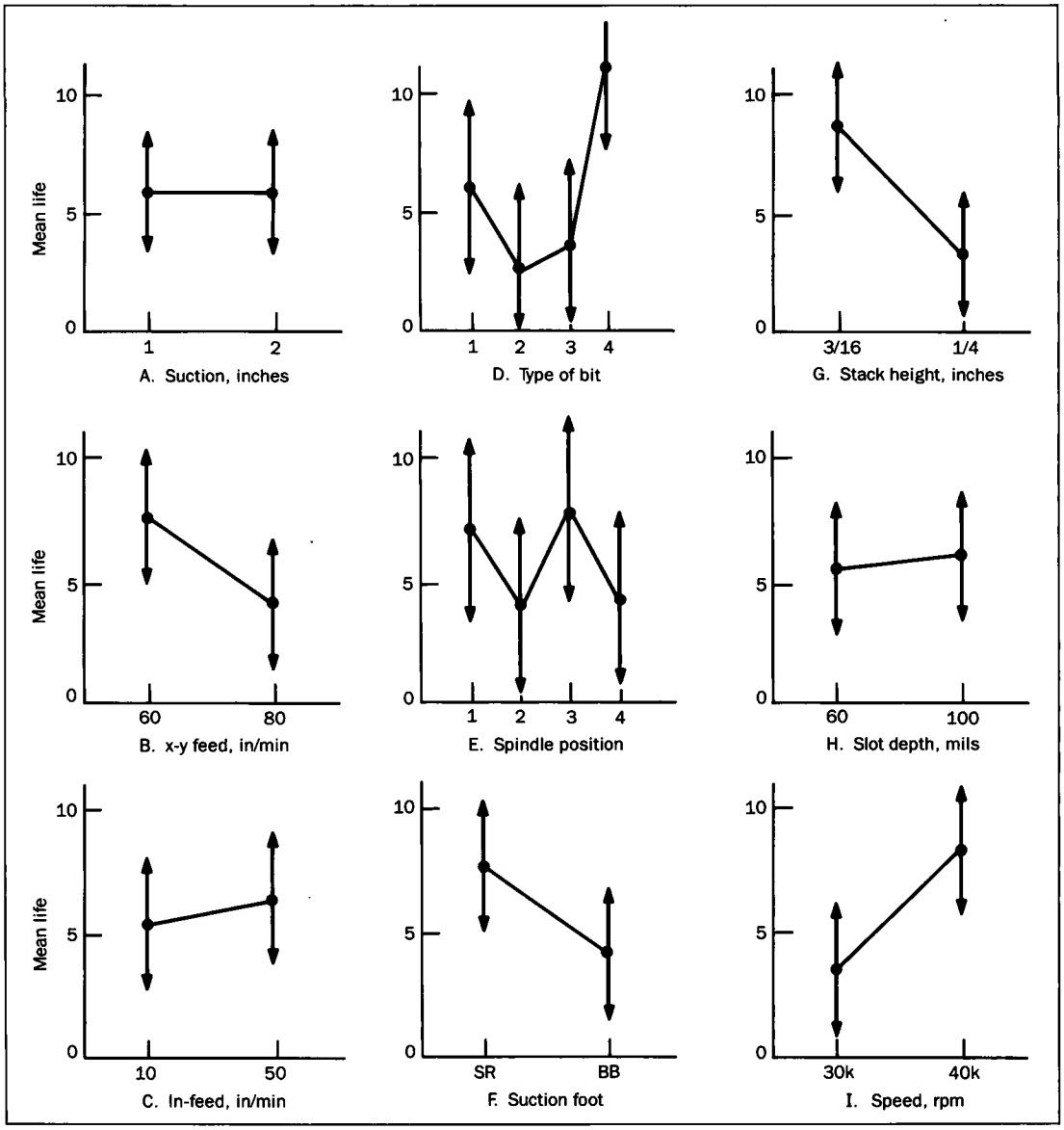


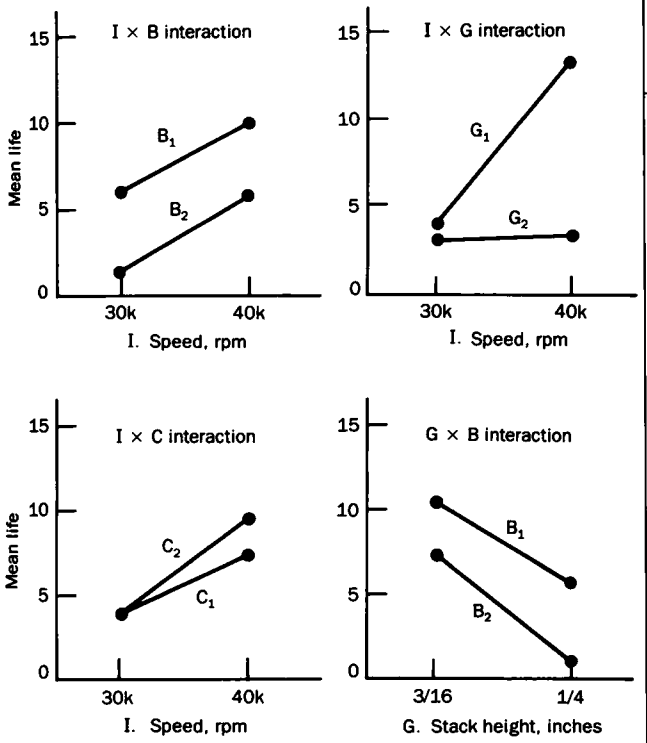
Figure 2. Average factorial effects, left, and selected two-factor interactions, right. Mean life is given in hundreds of inches. The 2σ limits are also shown. The table indicates the starting and optimum control factor levels for the routing process.

of favorable and unfavorable conditions are created. In this way, much can be learned about the optimum settings of control factors.

Analysis of the Life Data and Results. Two simple and separate analyses of the life data were performed to determine the best level for each control factor. The first analysis was to determine the effect of each control factor on the failure time. The second analysis was performed to determine how changing the level of each factor changes the survival probability curve (life curve).

The first analysis was performed by the standard procedure for fractional factorial experiments given in References 6 and 7. In this analysis of variance, the effect of censoring was ignored. The results are plotted in Figure 2. The following conclusions are apparent from the plots:

- 1-inch suction is as good as 2-inch suction.
- Slower x-y feed gives longer life.
- The effect of in-feed is small.
- The starting bit is the best of the four bit types.
- The differences among the spindle positions are small.



Starting and optimum control factor levels for the routing process

	Starting	Optimum	
A. Suction	A_2	A_2	
B. x-y feed	B_1	B_1	
C. In-feed	C_1	C_1	
D. Type of bit	D_4	D_4	
E. Spindle position	$E_1 - E_4$	$E_1 - E_4$	
F. Suction foot	F_2	F_1	←
G. Stack height	G_2	G_1	←
H. Depth of slot	H_1	H_1	
I. Speed	I_2	I_2	

- A solid ring suction foot is better than the bristle brush type.
- Lowering the stack height makes a large improvement. This change, however, raises machine productivity issues.
- The depth of slot in the back-up material has negligible effect.
- Higher rotational speed gives improved life. If the machine stability permits, even higher speeds should be tried in the next cycle of experiments.

The only two-factor interaction that is large is the stack height versus speed interaction. However, the optimum settings of these factors suggested by the main effects are consistent with those suggested by the interaction. The best factor level combination suggested by the above results and the starting factor level combination are tabulated in Figure 2.

Using the linear model of Reference 1 and taking into consideration only the terms for which the variance ratio is large, that is the factors B, D, F, G, I and interaction I × G, we can predict the router bit life under starting, optimum, or any other combination of factor settings. The predicted life under the starting conditions is 860 inches and under optimum conditions is 2200 inches. Because of the censoring at 1700 inches, these predictions are obviously likely to be on the low side. The prediction for optimum conditions especially is likely to be much less than the realized value. From the machine logs, the router bit life under starting conditions was found to be 900 inches, while the confirmatory experiment under optimum conditions yielded an average life in excess of 4150 inches.

In selecting the best operating conditions for the routing process, one must consider the overall cost, which includes not only the cost of router bits but also the cost of machine productivity, the cost of cleaning the boards if needed, and so forth. Under the optimum conditions listed in Figure 2, the stack height is 3/16 inch as opposed to 1/4 inch under the starting conditions. This means three panels are cut simultaneously instead of four panels. The lost machine productivity due to this change can however

Table II. Experiment Design and Observed Life for the Routing Process

Experiment No.	Suction A	x-y feed B	In-feed C	Bit D	Spindle E	Suction foot F	Stack height G	Depth H	Speed I	Observed life*
1	1	1	1	1	1	1	1	1	1	3.5
2	1	1	1	2	2	2	2	1	1	0.5
3	1	1	1	3	4	1	2	2	1	0.5
4	1	1	1	4	3	2	1	2	1	17.5
5	1	2	2	3	1	2	2	1	1	0.5
6	1	2	2	4	2	1	1	1	1	2.5
7	1	2	2	1	4	2	1	2	1	0.5
8	1	2	2	2	3	1	2	2	1	0.5
9	2	1	2	4	1	1	2	2	1	17.5
10	2	1	2	3	2	2	1	2	1	2.5
11	2	1	2	2	4	1	1	1	1	0.5
12	2	1	2	1	3	2	2	1	1	3.5
13	2	2	1	2	1	2	1	2	1	0.5
14	2	2	1	1	2	1	2	2	1	2.5
15	2	2	1	4	4	2	2	1	1	0.5
16	2	2	1	3	3	1	1	1	1	3.5
17	1	1	1	1	1	1	1	1	2	17.5
18	1	1	1	2	2	2	2	1	2	0.5
19	1	1	1	3	4	1	2	2	2	0.5
20	1	1	1	4	3	2	1	2	2	17.5
21	1	2	2	3	1	2	2	1	2	0.5
22	1	2	2	4	2	1	1	1	2	17.5
23	1	2	2	1	4	2	1	2	2	14.5
24	1	2	2	2	3	1	2	2	2	0.5
25	2	1	2	4	1	1	2	2	2	17.5
26	2	1	2	3	2	2	1	2	2	3.5
27	2	1	2	2	4	1	1	1	2	17.5
28	2	1	2	1	3	2	2	1	2	3.5
29	2	2	1	2	1	2	1	2	2	0.5
30	2	2	1	1	2	1	2	2	2	3.5
31	2	2	1	4	4	2	2	1	2	0.5
32	2	2	1	3	3	1	1	1	2	17.5

*Life was measured in hundreds of inches of movement in x-y plane. Tests were terminated at 1700 inches.

be made up by increasing the x-y feed. If the x-y feed is increased to 80 in/min, the productivity of the machine would get back approximately to the starting level. The predicted router bit life under these alternative optimum conditions is 1700 inches, which is twice the predicted life for starting conditions. Thus a 50 percent reduction in router bit cost can be achieved while still maintaining machine productivity. An auxiliary experiment would be needed to precisely estimate the effect of x-y feed under the new settings of all other factors. This would enable us to make

an accurate economic analysis.

Survival Probability Curve. The life data can also be analyzed in a different way, by the minute analysis method described in Reference 1, to construct the survival probability curves for the levels of each factor. To do so, we look at every 100 inches of cut and note which router bits have failed and which have survived. Treating this as 0-1 data, we can determine factorial effects by the standard analysis method. Thus for suction levels A_1 and A_2, the survival probabilities at 100 inches of cut were estimated to be 0.44 and 0.69. Likewise the probabilities are estimated for each factor and also for each time period: 100 inches, 200 inches, etc. These data, plotted in Figure 3, graphically display the effects of factor level changes on the entire life curve. The conclusions from these plots are consistent with the conclusions from the analysis described earlier.

Plots like Figure 3 can be used to determine the entire survival probability curve under a new set of factor level combinations such as the optimum combination. See Reference 1 for the method of calculation.

Notice that in this method of determining life curves, no assumption was made regarding the shape of the curve—whether it follows a Weibull or a lognormal distribution, for example. Also, the total amount of data needed to come up with the life curves is small. In this example it took only 32 samples to determine the effects of eight control factors. For a single good fit of a Weibull distribution one typically needs several tens of observations. So the approach used here can be very beneficial for reliability improvement projects.

There are, of course, some caveats. First, as in any fractional factorial experiment, one needs to guard against the interactions among the various control factors. But this difficulty can be overcome through the confirmatory experiment. Second, the method for determining the statistical significance of the differences between the life curves for different factor levels needs more research.

Circuit Design Optimization

The differential operational amplifier circuit is commonly used in telecommunications. An example is as a preamplifier in coin telephones, where it is expected to function over a wide temperature range. An important characteristic of this circuit is its offset voltage. (If the offset voltage is large, then the circuit cannot be used over long loops between the central office and the telephone). So the optimization objective was to minimize the offset voltage. The balancing property of the circuit makes the offset voltage small under nominal conditions. What needs to be minimized is the effect of tolerances and temperature variation on the offset voltage.

In the circuit diagram (Figure 4), there are two current sources, five transistors, and eight resistors. This differential operational amplifier circuit is made as part of a larger integrated circuit.

Control and Noise Factors. The balancing property of the circuit dictates the following relationship among the nominal values of the various circuit parameters: RFP = RFM, RPEP = RPEM, RNEP = RNEM, AFPP = AFPM, AFNP = AFNM, SIEPP = SIEPM, and SIENP = SIENM. The circuit parameter names beginning with AF refer to the alpha parameter of the transistors and those beginning with SIE refer to the saturation currents of the transistors. Further, the gain requirements of the circuit dictate the following ratios of resistance values RIM = RFM/3.55 and RIP = RFM/3.55. These relationships among the circuit parameters are called tracking relationships.

There are only five control factors for this circuit: RFM, RPEM, RNEM, CPCS, and OCS. The transistor parameters could not be specified for this design because the manufacturing technology was preselected, and it dictated the nominal values of all transistor parameters. Also, the tracking relationships determine the nominal values of the remaining resistors.

The number of noise parameters is 21. They are the tolerances on the eight resistors, 10 transistor parameters corresponding to the five transistors, two current sources and the temperature. The mean values and tolerances for these noise factors are given in Table III. The mean values of only the first five parameters are determined by the circuit design.

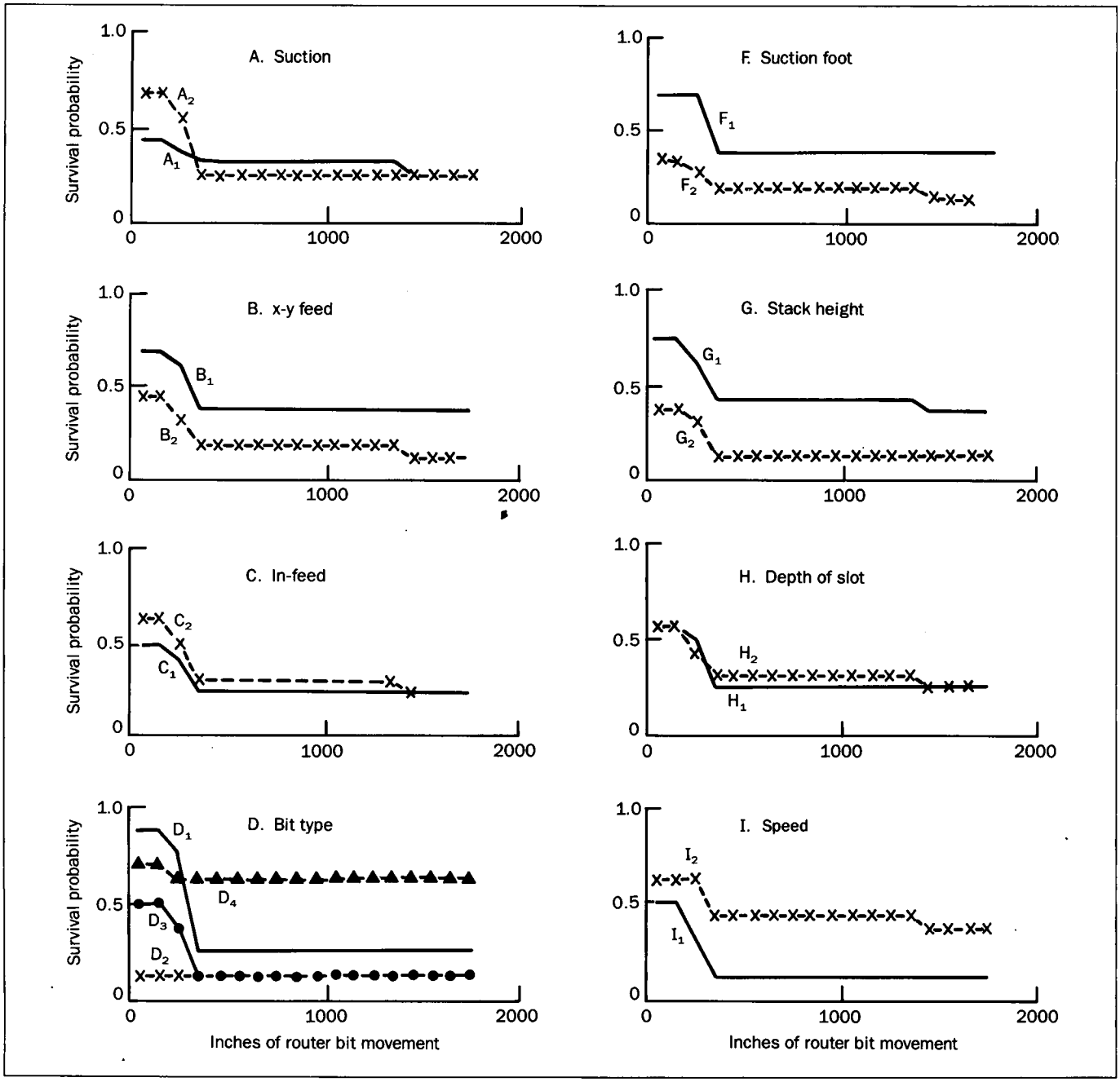


Figure 3. Survival probability curves for router bits.

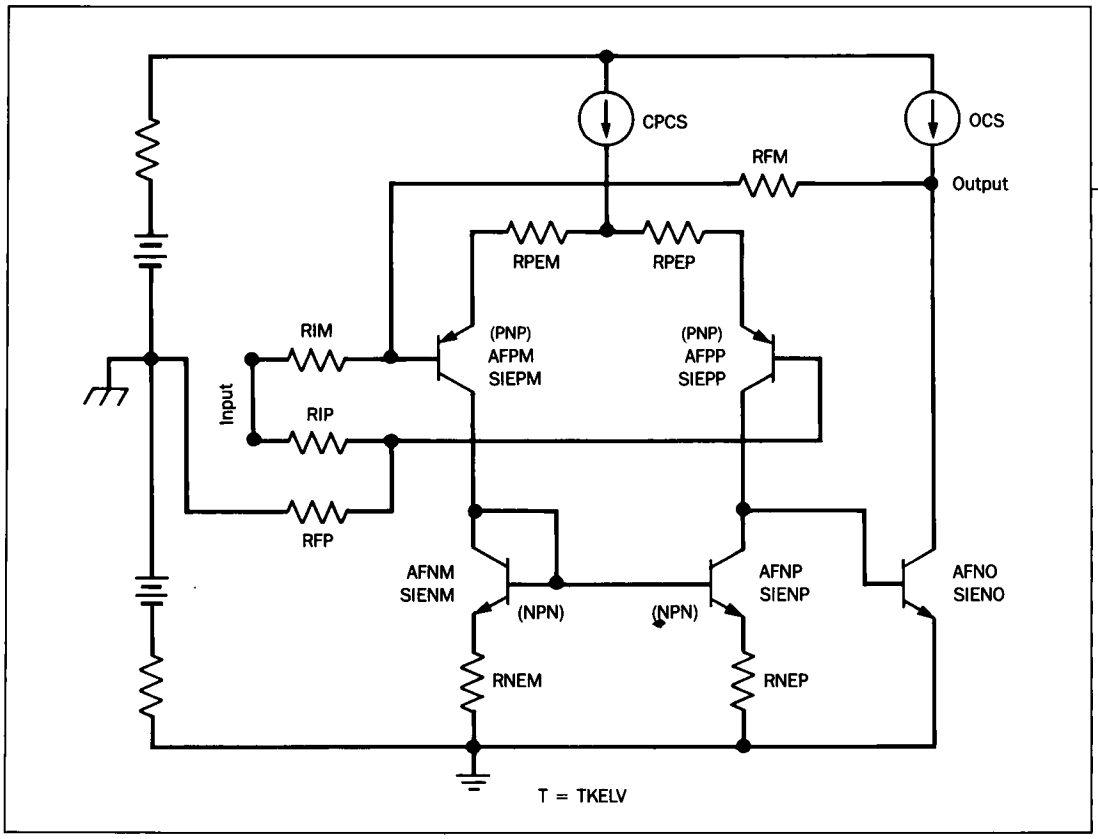


Figure 4. Circuit diagram for a differential operational amplifier.

The tolerances listed are the 3σ limits. Thus for RPEM the σ is 21/3 = 7 percent of its nominal value. Further, the interdependency or the correlation among the noise factors is also expressed through tracking. To see this point, let us look at the relationship between RPEP and RPEM. The 21 percent tolerance for RPEM represents the specimen-to-specimen variation within a lot and the lot-to-lot variation. But on a given specimen, the two resistors RPEM and RPEP are located physically close together. So there is less variation between the two resistances. This is the origin of the correlation between the two resistances. Suppose in a particular specimen RPEM = 15 kilohms. Then for that specimen RPEP will vary around 15 kilohms with 3σ limits equal to 2 percent of 15 kilohms. If for another specimen RPEM is 16.5 kilohms (10 percent more than 15 kilohms), then RPEP will vary around 16.5 kilohms with 3σ limits equal to 2 percent of 16.5 kilohms.

The saturation currents are known to have long-tailed distributions. So the tolerances are expressed as multiplicative instead of additive. In other words, these tolerances are taken to be additive in the log domain.

Evaluation of Mean Squared Offset Voltage. For a particular design, that is, for a particular selection of the control factor values, the mean squared offset voltage can be evaluated in many ways. Two common methods are:

- Monte Carlo simulation. Random number generators are used to determine a large number of combinations of noise factor values. The offset voltage is evaluated for each combination and then the mean squared offset voltage is calculated. For obtaining accurate mean squared values, the Monte Carlo method usually needs a large number of evaluations of the offset voltage, which can be expensive.
- Taylor series expansion. In this method, one finds the first derivative of the offset voltage with respect to each noise factor at the nominal design point. Let $x_1, \ldots, x_k$ be the noise factors, with variances $\sigma_1^2, \ldots, \sigma_k^2$, respectively. Let v be the offset voltage. Then the estimated mean square offset voltage is

$$r = \sum_{i=1}^{k} \left(\frac{\partial v}{\partial x_i}\right) \sigma_i^2$$

Second-order Taylor series expansion is sometimes taken if curvatures and correlations are important. When the tolerances are large so that the nonlinearities of v are important, the Taylor series approach does not give very accurate results.

In this application, however, we used the approach suggested by Taguchi. The orthogonal array, L_{36}, taken from Reference 1, was used to estimate the mean squared offset voltage as a standardized measure to be optimized. Simulation studies reported by Taguchi during his trips to AT&T Bell Laboratories have shown that the orthogonal array method gives more precise estimates of variances and means when compared to the Taylor series expansion method.

For the resistance and current source tolerances two levels were chosen, situated one standard deviation on either side of the mean. These noise factors were assigned to columns 1 through 10 of the L_{36} matrix (Table IV). For the 10 transistor parameters and the temperature, three levels were chosen, situated at the mean and at $\sqrt{3/2}$ times the standard deviation on either side of the mean. These noise factors were assigned to columns 12 through 22 of the matrix L_{36}. The submatrix of L_{36} formed by columns 1 through 10 and 12 through 22 is denoted by $\{J_{jl}\}$ and is referred to as the noise orthogonal array.

Each row of the noise array represents one specimen of differential op-amplifier with different values for the circuit parameters in accordance with the tolerances. Let v_j be the offset voltage corresponding to row j of the noise orthogonal array. Then the mean square offset voltage is estimated by

$$r = \frac{1}{36}\sum_{j=1}^{36} v_j^2$$

Since the most desired value of the offset voltage is zero, the appropriate S/N ratio to be maximized for optimizing this circuit is

$$\eta = -10 \log_{10} r$$

Table III. Noise Factors for the Differential Op-Amp Circuit

	Name	Mean	Tolerance	Levels (multiply by mean) 1	2	3
1.	RFM	71 kilohms	1%	0.9967	1.0033	
2.	RPEM	15 kilohms	21%	0.93	1.07	
3.	RNEM	2.5 kilohms	21%	0.93	1.07	
4.	CPCS	20 μA	6%	0.98	1.02	
5.	OCS	20 μA	6%	0.98	1.02	
6.	RFP	RFM	2%	0.9933	1.0067	
7.	RIM	RFM/3.55	2%	0.9933	1.0067	
8.	RIP	RFM/3.55	2%	0.9933	1.0067	
9.	RPEP	RPEM	2%	0.9933	1.0067	
10.	RNEP	RNEM	2%	0.9933	1.0067	
11.	AFPM	0.9817	2.5%	0.99	1	1.01
12.	AFPP	AFPM	1/2%	0.998	1	1.002
13.	AFNM	0.971	2.5%	0.99	1	1.01
14.	AFNP	AFNM	1/2%	0.998	1	1.002
15.	AFNO	0.975	1%	0.99	1	1.01
16.	SIEPM	3.OE-13 A	Factor of 7	0.45	1	2.21
17.	SIEPP	SIEPM	Factor of 1.214	0.92	1	1.08
18.	SIENM	6.OE-13 A	Factor of 7	0.45	1	2.21
19.	SIENP	SIENM	Factor of 1.214	0.92	1	1.08
20.	SIENO	6.OE-13 A	Factor of 2.64	0.67	1	1.49
21.	TKELV	298 K	15%	0.94	1	1.06

Optimization of the Design. Orthogonal array experimentation is also an efficient way to maximize a nonlinear function—in this case the maximization of η with respect to the control factors. The control factors and their alternate levels are listed in Table V. The L_{36} array was used to simultaneously study the five control factors. (In this case, the array L_{18} would have been sufficient.) The factors RFM, RPEM, RNEM, CPCS, and OCS were assigned to columns 12, 13, 14, 15, and 16, respectively. The submatrix of L_{36} formed by columns 12 through 16 is denoted by $\{I_{ik}\}$ and is referred to as the control orthogonal array.

Table IV. L_{36} Orthogonal Array

No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	2	2
3	1	1	1	1	1	1	1	1	1	1	1	3	3	3	3	3	3	3	3	3	3	3	3
4	1	1	1	1	1	2	2	2	2	2	2	1	1	1	1	2	2	2	2	3	3	3	3
5	1	1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3	3	3	1	1	1	1
6	1	1	1	1	1	2	2	2	2	2	2	3	3	3	3	1	1	1	1	2	2	2	2
7	1	1	2	2	2	1	1	1	2	2	2	1	1	2	3	1	2	3	3	1	2	2	3
8	1	1	2	2	2	1	1	1	2	2	2	2	2	3	1	2	3	1	1	2	3	3	1
9	1	1	2	2	2	1	1	1	2	2	2	3	3	1	2	3	1	2	2	3	1	1	2
10	1	2	1	2	2	1	2	2	1	1	2	1	1	3	2	1	3	2	3	2	1	3	2
11	1	2	1	2	2	1	2	2	1	1	2	2	2	1	3	2	1	3	1	3	2	1	3
12	1	2	1	2	2	1	2	2	1	1	2	3	3	2	1	3	2	1	2	1	3	2	1
13	1	2	2	1	2	2	1	2	1	2	1	1	2	3	1	3	2	1	3	3	2	1	2
14	1	2	2	1	2	2	1	2	1	2	1	2	3	1	2	1	3	2	1	1	3	2	3
15	1	2	2	1	2	2	1	2	1	2	1	3	1	2	3	2	1	3	2	2	1	3	1
16	1	2	2	2	1	2	2	1	2	1	1	1	2	3	2	1	1	3	2	3	3	2	1
17	1	2	2	2	1	2	2	1	2	1	1	2	3	1	3	2	2	1	3	1	1	3	2
18	1	2	2	2	1	2	2	1	2	1	1	3	1	2	1	3	3	2	1	2	2	1	3
19	2	1	2	2	1	1	2	2	1	2	1	1	2	1	3	3	3	1	2	2	1	2	3
20	2	1	2	2	1	1	2	2	1	2	1	2	3	2	1	1	1	2	3	3	2	3	1
21	2	1	2	2	1	1	2	2	1	2	1	3	1	3	2	2	2	3	1	1	3	1	2
22	2	1	2	1	2	2	2	1	1	1	2	1	2	2	3	3	1	2	1	1	3	3	2
23	2	1	2	1	2	2	2	1	1	1	2	2	3	3	1	1	2	3	2	2	1	1	3
24	2	1	2	1	2	2	2	1	1	1	2	3	1	1	2	2	3	1	3	3	2	2	1
25	2	1	1	2	2	2	1	2	2	1	1	1	3	2	1	2	3	3	1	3	1	2	2
26	2	1	1	2	2	2	1	2	2	1	1	2	1	3	2	3	1	1	2	1	2	3	3
27	2	1	1	2	2	2	1	2	2	1	1	3	2	1	3	1	2	2	3	2	3	1	1
28	2	2	2	1	1	1	1	2	2	1	2	1	3	2	2	2	1	1	3	2	3	1	3
29	2	2	2	1	1	1	1	2	2	1	2	2	1	3	3	3	2	2	1	3	1	2	1
30	2	2	2	1	1	1	1	2	2	1	2	3	2	1	1	1	3	3	2	1	2	3	2
31	2	2	1	2	1	2	1	1	1	2	2	1	3	3	3	2	3	2	2	1	2	1	1
32	2	2	1	2	1	2	1	1	1	2	2	2	1	1	1	3	1	3	3	2	3	2	2
33	2	2	1	2	1	2	1	1	1	2	2	3	2	2	2	1	2	1	1	3	1	3	3
34	2	2	1	1	2	1	2	1	2	2	1	1	3	1	2	3	2	3	1	2	2	3	1
35	2	2	1	1	2	1	2	1	2	2	1	2	1	2	3	1	3	1	2	3	3	1	2
36	2	2	1	1	2	1	2	1	2	2	1	3	2	3	1	2	1	2	3	1	1	2	3

Each row of the control orthogonal array represents a different design. For each design the *S/N* ratio was evaluated using the procedure described under "Evaluation of Mean Squared Offset Voltage." The simulation algorithm is graphically displayed in Figure 5. Standard analysis of variance was performed on the η values to generate Table VI. The effect of each factor on η is displayed in Figure 6.

From Table VI it is apparent that only RPEM, CPCS, and OCS have an effect on η that is much bigger than the error variance. The effect of RPEM is the largest, and there is indication that reduction in its value below 7.5 kilohms could give even more improvement in offset voltage. For both current sources, 10 μA to 20 μA seems to be the flat region, indicating that we are very near the best values for these parameters. Also, the potential improvement by changing these current sources from 10 μA to 20 μA seems small. Thus we chose the following two designs as potential optimum points:

- Optimum 1: Only change RPEM from 15 kilohms to 7.5 kilohms. By the procedure in "Evaluation of Mean Squared Offset Voltage," the value of η for this design was found to be 33.70 dB compared to 29.39 dB for the starting design. In terms of the rms offset voltage this represents an improvement from 33.9 mV to 20.7 mV.
- Optimum 2: Change RPEM to 7.5 kilohms. Also change both CPCS and OCS to 10 μA. The η for this design was computed to be 35.82 dB, and rms offset voltage was seen to be 16.2 mV.

In the discussion so far, we have paid attention to only the dc offset voltage. Stability under ac operation is also an important consideration. For a more elaborate study of this characteristic, one must generate more data like those in Table VI and Figure 6. The optimum control factor setting should then be obtained by jointly considering the effects on both the dc and ac characteristics. If conflicts occur, appropriate trade-offs can be made using the quantitative knowledge of the effects. In our study, we simply checked for ac stability at the two optimum conditions. For sufficient safety margin with respect to ac stability, we selected optimum 1 as the best

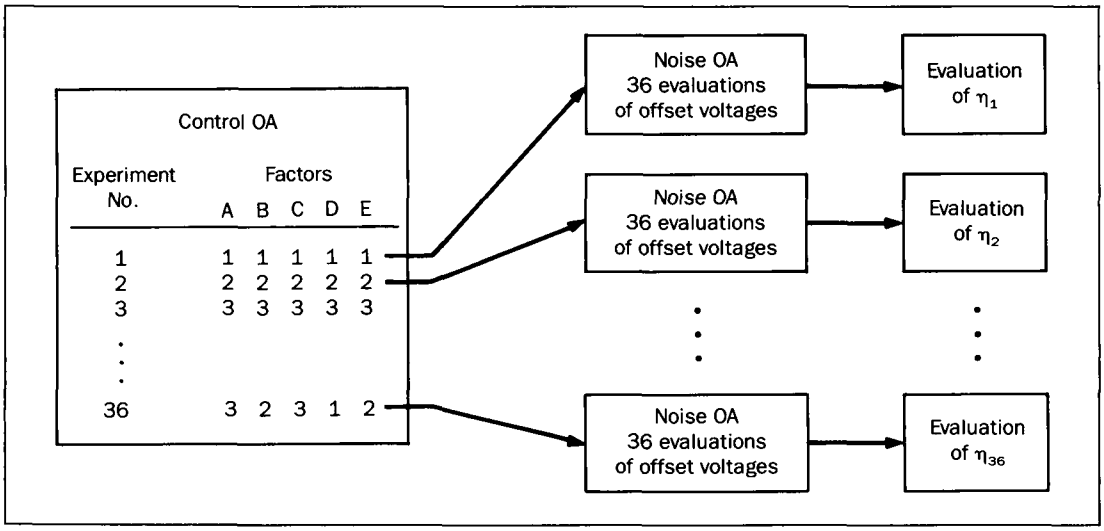


Figure 5. Simulation algorithm.

Table V. Control Factors for the Differential Op-Amp Circuit

Label	Name	Description	Levels 1	2	3
A	RFM	Feedback resistance, minus terminal (kilohms)	35.5	71	142
B	RPEM	Emitter resistance, PNP, minus terminal (kilohms)	7.5	15	30
C	RNEM	Emitter resistance, NPN, minus terminal (kilohms)	1.25	2.5	5
D	CPCS	Complementary pair current source (μA)	10	20	40
E	OCS	Output current source (μA)	10	20	40
				Starting design	

design and called it simply the optimum design.

Tolerance Design. With the sensitivity to noise minimized for the dc offset voltage, the next step is to examine the contribution to the mean squared offset voltage by each noise source. By performing analysis of variance of the 36 offset voltages corresponding to the noise orthogonal array for the optimum control factor settings, we obtained Table VII, which gives the breakdown of the contribution of each tolerance to the total mean squared offset voltage. The table also gives a similar breakdown of the mean squared offset voltage for the starting design. The reduction in the sensitivity of the design to various noise sources is apparent.

The table exhibits the typical Pareto principle. That is, a small number of tolerances account for most of the variation in the response. In particular, SIENP has the largest contribution to the mean squared offset volt-

Table VI. Analysis of Variance for $\eta = -10 \log_{10}$ (mean squared offset voltage)

Control factor	Level means 1	2	3	Sum of squares	Degrees of freedom	Mean square	F
A. RFM	26.5	26.4	25.3	9.9	2	4.95	0.5
B. RPEM	30.3	26.4	21.5	463.7	2	231.85	25.0
C. RNEM	25.1	25.8	27.3	29.9	2	14.95	1.6
D. CPCS	27.5	27.1	23.6	111.1	2	55.55	6.0
E. OCS	27.3	27.0	23.8	87.5	2	43.75	4.7
Error				231.6	25	9.26	

Overall mean = 26.05

age. Hence it is a prime candidate for reducing the tolerance, should we wish to further reduce the mean squared offset voltage. AFNO, AFNM, and SIEPP have moderate contribution to the mean squared offset voltage. The rest of the noise factors contribute negligibly to the mean squared offset voltage. So if it will yield further manufacturing economies, relaxing these tolerances should be considered carefully.

Reducing Computational Effort. The optimization of the differential op-amp discussed earlier needed $36 \times 36 = 1296$ evaluations of the circuit response—namely the offset voltage. Although in this case the computer time needed was not an issue, in some cases making an evaluation of each response can be expensive. In such cases, significant reduction of the computational effort can be accomplished by using qualitative engineering knowledge about the effects of the noise factors. For example, we form a *composite noise factor*. The high level of the composite noise factor corresponds to the combination of the individual noise factor levels that give high response. The *low* and *nominal* levels of the composite noise factor can be defined similarly. Thus the size of the noise orthogonal array can be drastically reduced, leading to much smaller computational effort during design optimization. Further reduction in computational effort can be obtained by taking only two levels for each noise factor; however, generally we recommend three levels. For tolerance design, we need to identify the sensitivity of each noise factor. Therefore a composite noise factor would have to be dissolved into its various components.

Conclusion

The robust design method has now been used in many areas of engineering throughout the United States. For example, robust design has lead to improvement of several processes in *very large scale integration (VLSI) fabrication*: window photolithography, etching of aluminum lines, reactive ion etching processes, furnace operations for deposition of various materials, and so forth. These processes are used for manufacturing 1-megabit and 256-kilobit memory chips, 32-bit processor chips, and other products. The *window photolithography* application docu-

Table VII. Breakdown of Mean Square Offset Voltage by Noise Sources

Noise factor*	Contribution to mean square offset voltage (10^{-4} V^2) Starting Design	Change RPEM to 7.5 kilohms
SIENP	6.7	2.3
AFNO	2.2	0.8
AFNM	1.6	0.4
SIEPP	0.5	0.5
RPEP	0.2	0.1
AFPP	0.1	0.1
Remainder	0.2	0.1
Total	11.5	4.3

*The six largest contributors to the mean squared offset voltage are listed here.

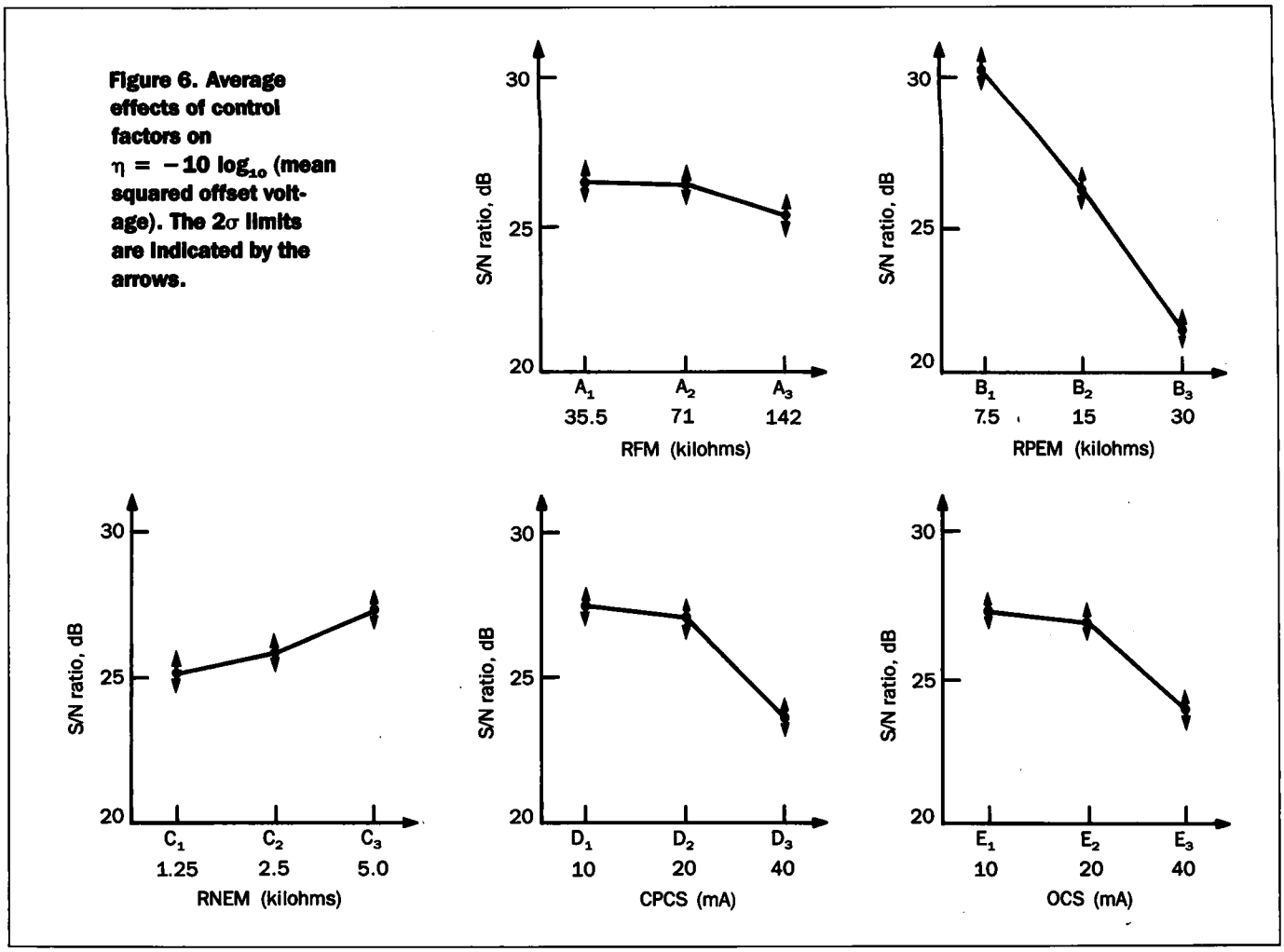


Figure 6. Average effects of control factors on $\eta = -10 \log_{10}$ (mean squared offset voltage). The 2σ limits are indicated by the arrows.

mented in Reference 8 was the first application in the United States that demonstrated the power of Taguchi's approach to quality and cost improvement through robust process design. In particular, the benefits of the application were:

- Fourfold reduction in process variance.
- Threefold reduction in fatal defects.
- Twofold reduction in processing time. This resulted from the fact that the process became stable so that time-consuming inspection could be dropped.
- Easy transition of design from research to manufacturing.
- Easy adaptation of the process for finer line technology, which is usually a very difficult problem.

The *aluminum etching* application was an interesting one in that it originated from a belief that poor photoresist print quality leads to line width loss and to undercutting. By making the process insensitive to photoresist profile variation and other sources of variation, the visual defects were reduced from 80 percent to 15 percent. Moreover, the etching step could then tolerate the variation in photoresist profile.

In *reactive ion etching* of tantalum silicide, the process gave highly nonuniform etch quality, so only 12 out of 18 possible wafer positions could be used for production. After optimization, 17 wafer positions became usable—a hefty 40 percent increase in machine capacity. Also, the efficiency of the orthogonal array experimentation allowed this project to be completed in the 20-day deadline. Thus in this case $1.2 million was saved in equipment replacement costs not counting expense of disruption on the factory floor.[9]

The *router bit life improvement* project described in this article led to a two- to fourfold increase in the life of router bits used in cutting printed wiring boards. The project illustrates how reliability or life improvement projects can be organized to find best settings of control factors with a very small number of samples. The number of samples needed in this approach is very small yet it can give valuable information about how each factor changes the survival probability curve.

In the *differential op-amp circuit optimization* example described in this article, a 40-percent reduction in the rms offset voltage was realized by simply finding a new design center. This was done by reducing sensitivity to all tolerances and temperature, rather than reducing tolerances, which could have increased manufacturing cost.

Here the noise orthogonal array was used in a novel way—to efficiently simulate the effect of many noise factors. This approach can be beneficially used for evaluating designs and for system or software testing. Further, the approach can be automated and made to work with various computer-aided design tools to make design optimization a routine practice.

This approach was also used to find optimum proportions of ingredients for making *water-soluble flux.*[10] By simultaneous study of the parameters for the wave soldering process and the flux composition, the defect rate was reduced by 30 to 40 percent.

Orthogonal array experiments can be used to tune hardware/software systems.[11] By simultaneous study of three hardware and six software parameters, the response time of the UNIX® operating system was reduced 60 percent for a particular set of load conditions experienced by the machine.

Under the leadership of American Supplier Institute and Ford Motor Company, a number of automotive suppliers have achieved quality and cost improvement through robust design. Many of these applications are documented in Reference 12.

These examples show that robust design is a collection of tools and comprehensive procedures for simultaneously improving product quality, performance, and cost, and also engineering productivity. Its widespread use in industry is bound to have a far-reaching economic impact.

Acknowledgments

The two applications described in this paper would not have been possible without the collaboration and diligent efforts of many others. The router bit life improvement study was done in collaboration with Dave Chrisman of AT&T Technologies, Richmond Works. The optimization of the differential op-amp was done jointly with Gary Blaine, a former member of the technical staff at AT&T Bell Laboratories, and Joe Leanza of AT&T Information Systems. The survival probability curves were obtained with the software package for analysis of variance developed by Chris Sherrerd of Bell Laboratories. Rajiv Keny and Paul Sherry of Bell Laboratories provided helpful comments on this paper.

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