SILICON CRYSTAL GROWTH AND EPITAXIAL LAYER DEPOSITION FOR VLSI DEVICES

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Silicon for microelectronic devices is prepared by a complex process that converts polycrystalline material into a single crystal ingot of silicon weighing as much as 40 kilograms. The crystal must conform to precise mechanical, electrical, chemical, and crystallographic standards. The crystal ingot is sliced into wafers which are polished and covered with an epitaxial layer having the same crystal structure as the wafer but different electrical properties. Understanding and controlling the growth processes involved in producing the single-crystal ingot and the epitaxial layer is crucial to manufacturing the high-quality starting material for today's very large scale integrated circuits.

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Introduction

All silicon-based microelectronic devices, from discrete transistors and diodes to the latest very large scale integration (VLSI) chips, are made from the same basic material—a silicon single crystal possessing tightly defined mechanical, electrical, chemical, and crystallographic properties.

The silicon single crystal is grown by a special crystal-growing process which converts semiconductor-grade polycrystalline material into a cylindrically shaped single-crystal ingot whose diameter is typically 125 mm. The growing process also determines several other characteristics required by the finished wafer. These include the distribution of both intentional and unintentional nonsilicon elements such as the carrier-providing (dopant) element, oxygen, and carbon. Thin slices are cut from the crystal ingot, polished, and covered by the chemical deposition of an epitaxial layer. It is in this layer that the active regions of most VLSI devices are fabricated.

The epitaxial layer radically alters the wafer's properties. The critical properties of the layer are its thickness, purity, carrier concentration, and microperfection; in other respects, it is the same single crystal as the polished wafer. Understanding and controlling the charac-

Figure 1. A Czochralski-grown single-crystal ingot of silicon is made from a doped melt of ultrapure silicon. The wafers in the foreground were sliced from such an ingot. They illustrate successive stages of surface finish: from left, as sliced, after lapping, and after polishing.

teristics of the epitaxial wafer are particularly important in the production of VLSI devices.

Crystal Growing Process

Single-crystal silicon for VLSI devices is grown mainly by the Czochralski (CZ) process, in which an appropriately doped single-crystal ingot is formed from ultrapure polycrystalline silicon and a small quantity of a desired intentional impurity (dopant element) in a highly specialized CZ silicon furnace.

The total concentration of electrically active elements in the as-received polycrystalline silicon charge material is generally less than 2 parts per billion. Also of importance for VLSI applications are the concentrations of heavy metals and carbon, which are typically less than 10 parts and 1 part per million, respectively.

Current polysilicon charge masses for 125-mm production applications are in the range of 30 to 40 kg. The dopant species is determined by the design requirements of the particular device code. Boron, phosphorus, antimony, or arsenic is the dopant element generally used. A specific quantity of dopant appropriate for the desired carrier concentration is weighed out and placed in a quartz crucible along with the raw polysilicon. A small silicon seed crystal having the desired crystallographic orientation, either <111> or <100>, is attached to the end of the furnace's crystal support (either solid shaft or cable), which is concentric to the crucible and "hot zone" of the furnace. The furnace is then closed off to atmosphere, evacuated, and backfilled with argon gas to an operating pressure of approximately 20 torr.

Power is then applied to the graphite heating element in the hot zone to a level necessary to melt the silicon charge, which has a melting temperature of approximately 1420°C. This meltdown destroys the silicon's polycrystalline structure and allows a uniform distribution of the dopant in the molten silicon.

After the melt has stabilized thermally, at a temperature just above the melting point of silicon, the seed crystal is lowered and brought into contact with the melt surface, and resolidification of the molten silicon commences on the seed. Upward translation of the seed crystal is then begun. As silicon and dopant atoms leave the liquid to join the solid seed crystal, they replicate the single-crystal atomic arrangement of the seed.

In this portion of the growing cycle, called the "neck" portion, temperature and seed translation rate are controlled to effect a narrowing from the original seed diameter of 6 to 12 mm down to 2 to 4 mm, while attaining a withdrawal rate of 3 to 5 mm per minute. Growing the neck in this manner transforms the crystallographic nature of the neck from one with crystallographic defects, called dislocations, to one that is without defects, called dislocation-free or DF.

Dislocations are linear deviations from perfect atomic arrangement within a single crystal. They are unacceptable in the final crystal and in polished or epitaxial wafers. Once a DF growth state is achieved, the pull rate and the power input to the melt are reduced. These changes cause the crystal to grow outward from the neck diameter to the desired diameter or shoulder of the ingot. Once that is achieved, the pull rate is abruptly increased to stop the radial growth and begin the growth of the cylindrical portion of the crystal, called the "body."

In this portion of the growing cycle, many interacting process parameters must be continuously monitored and adjusted by the process controller to maintain a constant crystal diameter and DF crystal structure. When the crucible is almost completely depleted of its molten contents (about 10 percent of the initial silicon charge remaining), body growth at constant diameter is transformed to a gradual, tapered termination of the crystal (Figure 1).

Figure 2. Modern furnaces for the Czochralski process are complex, highly specialized equipment controlled by microprocessors.

Hardware. A basic CZ silicon furnace (Figure 2) has five features:

- An electrical resistance heating power source and temperature control system that can hold very fine temperature control about the melting point of silicon when coupled with a properly designed hot zone.
- A hot zone, often consisting of graphitic material, to maintain a proper thermal environment for both the molten silicon and the growing crystal ingot.
- A means of supporting, vertically translating, and rotating both the growing crystal and the crucible.
- A means of providing and maintaining a particular pressure and flow of an inert ambient atmosphere (usually argon) within the furnace.
- A microprocessor-based process control system to continuously monitor and adjust all process parameters in all portions of the growth cycle. The control system requires a minimum of operator intervention.

Heat-Transfer Considerations. A major consideration in the CZ process is that of maintaining the DF growth mode. Adverse thermal gradients can create excessive thermal stresses or instabilities at the interface between solid and liquid states. These thermal gradients can be controlled through heat-transfer technology.

A serpentine graphite resistance heater supplies the necessary energy for the CZ process. Approximately 80 percent of this heat flows radially inward by radiation heat transfer. It is then absorbed by hot zone elements and conducted to the silicon melt that is in contact with the quartz crucible (Figure 3).

In the melt, heat is transferred from the crucible walls to the solid-liquid interface principally by the natural convection vortex pattern established by buoyancy forces. Here, a fluid element of molten silicon rises along the walls of the crucible as it become heated, releases heat to the surroundings via the free-melt surface and to the growing crystal, and then upon cooling, falls to the bottom of the crucible near the centerline to begin the cycle again. This convection is characteristically turbulent in large silicon CZ melts, with thermal instabilities of several degrees centigrade in magnitude not uncommon. At the solid-liquid crystal interface, material from the melt is constantly being solidified, resulting in an isothermal moving boundary. Heat conducted within the crystal away from the growing crystal interface principally consists of heat that has been convected to the crystal from the melt and heat of fusion that is liberated as solidification of the molten silicon proceeds.

The design of the components in the hot zone directly influences thermal boundary conditions imposed on the growing crystal. These conditions, in turn, govern the temperature distribution in the growing ingot, which affects in a major way the degree of crystallographic perfection obtained. These boundary conditions also determine the size of the crystal growth operating region for the production of good material.

Because of the important role of heat transfer in the CZ crystal-growing process, engineers at the AT&T

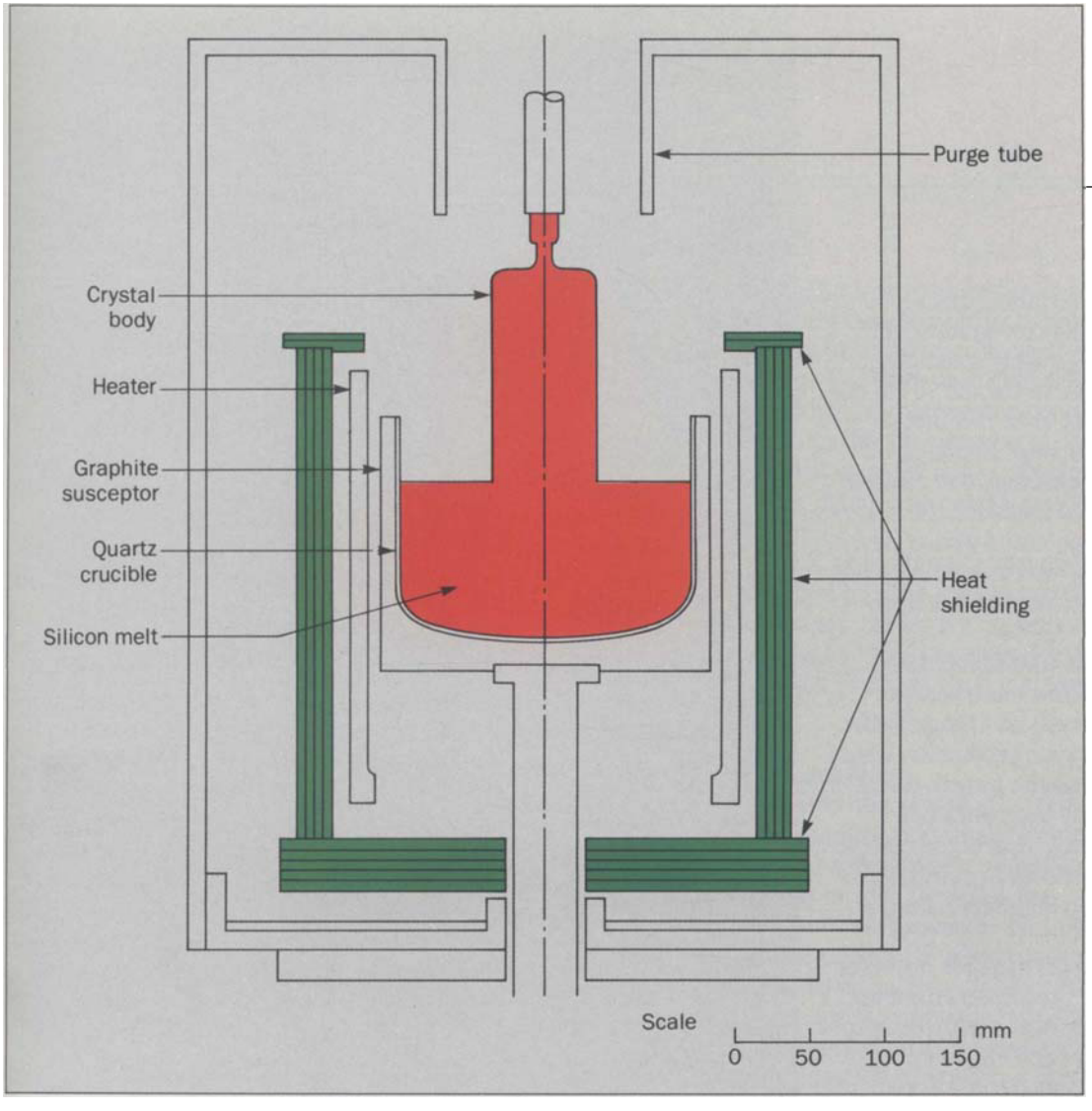

Figure 3. The energy for the Czochralski process is supplied by an electrical resistance graphite heater incorporated in the graphitic hot zone within the furnace. This assembly of hot-zone components is essential for maintaining the proper thermal environment for the melt and growing crystal.

Engineering Research Center have developed a comprehensive heat-transfer analysis model of the process which predicts the temperature distribution everywhere in the growing silicon crystal ingot, and provides thermal information on heat transfer processes in other parts of the grower. Typical model predictions are shown in Figure 4. The model is currently being used as a design tool to provide quantitative thermal information about the process. This information is being used to evaluate the feasibility of proposed process and hardware modifications and to aid in the development of high-performance hot zone designs to economically meet the VLSI material needs of AT&T well into the next decade.

On the basis of this analysis and the resulting enhanced thermal understanding of the growth process, the crystal-growing state of the art has been extended beyond the current production-scale 30- to 40-kg charge levels with AT&T's development of a unique, high-capacity, high-yield hot zone design having a 70- to 80-kg processing capability. To date, the new hot zone design has been run at the 60-kg melt charge level, resulting in the growth, for the first time, of a DF, semiconductor grade crystal ingot (see Figure 5) having a length of 1.7 m (67 in) with a diameter of 125 mm. To the best of our knowledge and

according to the recent literature, this represents the largest semiconductor-grade ingot ever made in the crystal-growing community. Development work to achieve the full 70- to 80-kg potential of the new hot zone continues.

Trends in Crystal Growing. Trends in CZ silicon crystal growing technology will continue to be driven by the need to minimize the silicon material cost per unit of potential device area on a wafer, while meeting increasingly demanding material specifications required for finer-line device designs.

One such trend is toward increased wafer diameters, which allow more and/or larger VLSI chips to be made on a single wafer. At present, the most common production wafer diameter is 125 mm. CZ silicon growth diameter capability has generally been ahead of device processing capability. This is the case at present with the latest generation of furnaces capable of growing 150- to 200-mm-diameter crystals.

Increasing melt size parallels diameter growth. This relation has progressed from the 1-in-diameter, 1-kg charge of the mid-1960s to the 125-mm-diameter, 30- to 40-kg material of today. It is expected that this trend will continue and eventually may surpass the 70- to 80-kg range described above for the efficient and economical growth of 150- to 200-mm-diameter material in the 1990s.

Still another trend in crystal technology is toward customizing the growing process to accommodate particular device designs. This would extend beyond gross characteristics of crystal orientation, dopant species, and resistivity range. For example, silicon crystal producers now offer material in several oxygen content ranges. This type of customization will likely be extended to include other characteristics of the material such as carbon content, oxygen precipitate

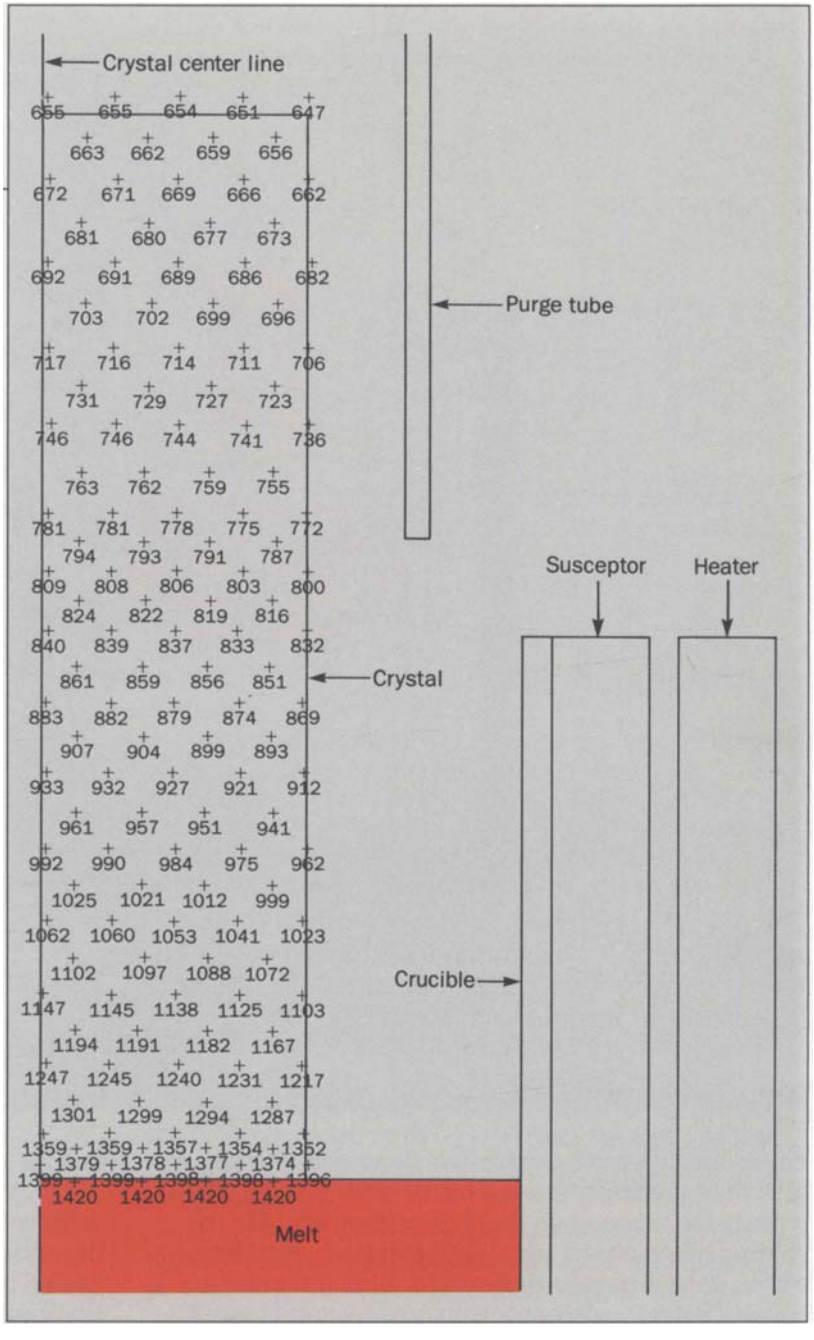

Figure 4. Computed temperature distribution in degrees Celsius in growing crystal. The length is 170 mm and the diameter is 80 mm.

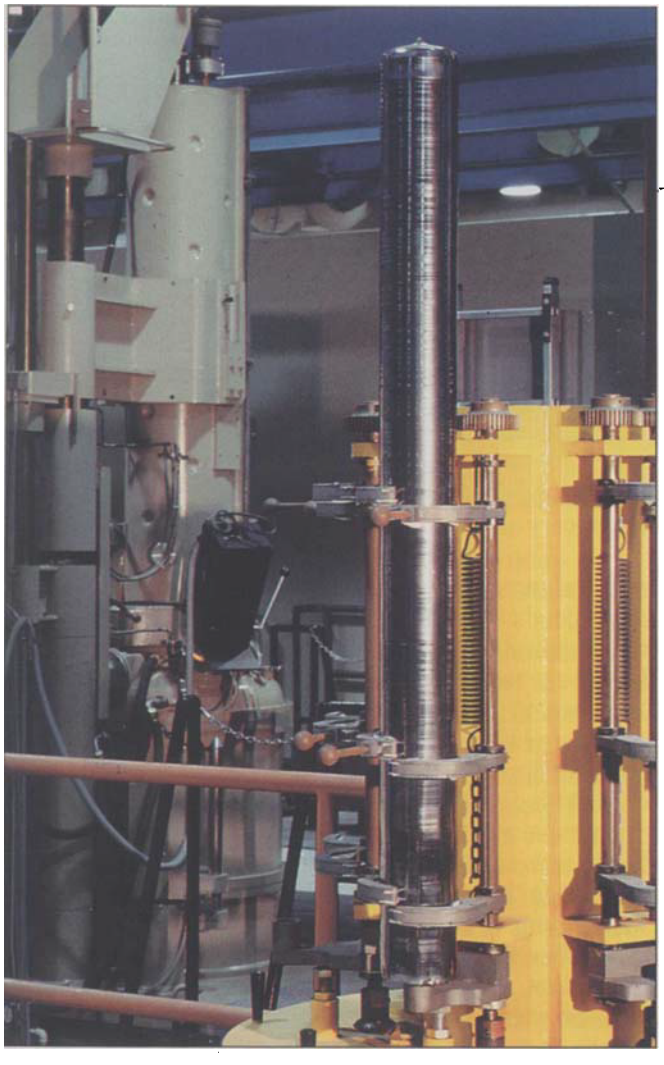

Figure 5. A 60-kilogram state-of-the-art ingot grown at AT&T has a length of 1.7 meters (67 inches) with a diameter of 125 millimeters. This ingot is believed to be the largest semiconductor-grade ingot ever grown.

density, and oxygen and resistivity distribution, as silicon makers and users become more aware of their effects on device performance and yields.

Until the late 1970s, crystal growing technology relied on relatively unsophisticated analog-based furnace control and monitoring systems. CZ process success thus depended heavily on the skill of machine operators. However, the addition of the microprocessor to the crystal growing furnace over the last six years has promoted consistency in both process and product, and provided the technological vehicle needed to program the many process parameters involved in growing crystals with customized properties. The next attainable step in process automation is networking microprocessor-controlled furnaces to a central computer for the purpose of downloading instructions to individual furnaces and/or uploading detailed process parameter data to the central computer for real-time analysis.

CZ silicon furnace manufacturers are also developing hardware to allow crystal growth in the presence of a magnetic field and from a continuously replenished melt. These modified CZ processes offer potential for more uniform crystal chemistry and increased process productivity and yield.

Crystal Evaluation

After the crystal is grown, but before it is shaped, it is evaluated to verify that it complies with certain generic and code-specific material requirements. These evaluations include the following.

Perfection Evaluation. This operation ensures that only single-crystal DF silicon passes to the shaping operations. Visual inspection of the crystal surface can determine gross deviations from single-crystal structure, such as grain boundaries and crystallographic twinning. These are caused by improper thermal conditions or foreign particulate matter impinging upon the solid-liquid interface during body growth. A subtler "structural" defect in the grown ingot is crystallographic slip. This is a series of adjacent dislocation defects that form when adjacent planes of atoms within the crystal shift with respect to each other in response to internal or external stresses. The slip defect is detected by etching the crystal with a chromic-hydrofluoric acid mixture that makes the slipped regions distinguishable from DF material.

Electrical Evaluation. The thermodynamic nature of the CZ process causes a nonuniform distribution of dopant atoms and, therefore, electrical resistivity within the crystal body. This evaluation characterizes the resistivity of the

crystal in terms of its longitudinal and radial values. The ingot is analyzed by means of a four-point probe method in which a linear array of electrodes contacts the ingot surface. A constant current is forced through the two outer electrodes and the voltage is measured across the two inner electrodes. The measured voltage can be used to determine the resistivity of the small volume of material directly under the probes.

Other Evaluations. Oxygen and carbon are unavoidably present in all CZ-grown silicon crystal. Interstitial oxygen is present in the range of 10 to 25 parts per million, and substitutional carbon is present in the range of 0 to 3 parts per million. The major source of oxygen is the fused silica crucible, which is slowly dissolved during the growth process by its contact with the molten silicon. The major sources of carbon are the polycrystalline silicon raw material and the graphitic hot-zone components in the CZ furnace.

The nominal concentration, longitudinal and radial distributions, and chemical state of these impurities have become areas of intense interest and importance in recent years, particularly for VLSI-grade silicon materials. The effects of oxygen depend upon the initial oxygen concentration and the thermal history of the material before and during device fabrication. The role of carbon, acting alone or in conjunction with other impurities, is less clearly understood. At present, however, it is generally accepted that its concentration should be kept to a minimum.

Specialized growth process programs incorporating variations of certain primary growth parameters are used to control the concentration and distribution of oxygen and carbon in the as-grown crystal. The presence of interstitial oxygen and substitutional carbon is measured by infrared absorption on a polished slice or slug sample. Several commercial test systems are available for this measurement. No crystal evaluation is complete without a knowledge of the level and distribution of these impurities. The presence of these impurities is therefore measured on a routine basis.

Crystal and Wafer Shaping

The process of converting a crystal ingot into a wafer form begins by grinding the evaluated crystal into a cylindrical shape of the appropriate diameter. This is done on a center-type machine using diamond grinding wheels and a flood of coolant. A diamond wheel is used because it minimizes damage to the crystal lattice, stays sharp, and wears very slowly.

The next step involves locating and grinding a primary reference flat along the crystal length. The flat corresponds to a specific crystal plane and is located by x-ray or optical techniques while the crystal is fixtured. With Laue x-ray methods, the flat can be located to an angular tolerance of ± 30 minutes. The fixtured crystal is then transferred to another machine where the reference flat is produced by a diamond grinding wheel. A secondary reference flat is also located and ground to identify crystal orientation and doping according to standards prescribed by the Semiconductor Equipment and Materials Institute.

In the next step, the crystal is shaped into a wafer, using an inside-diameter sawing operation that also establishes several wafer parameters, including surface orientation, thickness, taper, and bow. Surface orientation is determined by x-ray diffractometer methods within a tolerance of ± 30 minutes. Thickness is initially established during slicing and altered later in subsequent shaping operations. Taper and bow are also created during the sawing operation.

After sawing is completed, a special diamond wheel grinds a radius onto the wafer edge. This is done to minimize the production of edge chips during wafer fabrication.

For VLSI applications, the sawed wafers must be processed through a mechanical two-sided lapping operation. This produces a wafer with flatness uniform to within 2 microns and helps ensure that wafer flatness requirements are satisfied in subsequent shaping processes.

The initial shaping operations leave the surface and edges of the wafer lightly contaminated and work-damaged, the degree of damage depending on machine

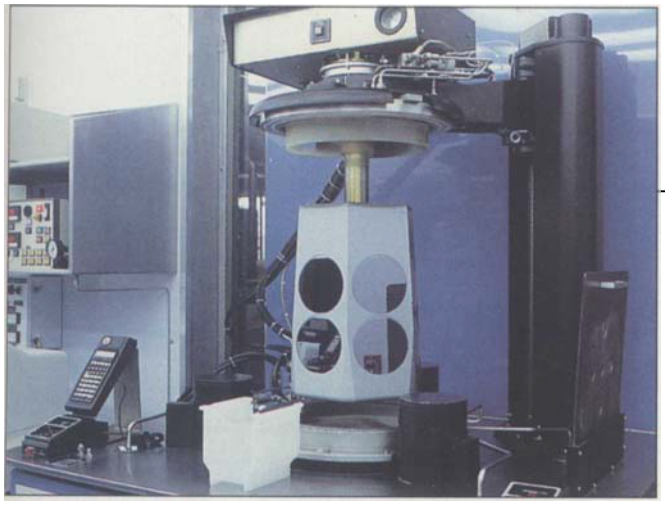

Figure 6. A reactor commonly used in the process of epitaxial deposition is this radiantly heated barrel reactor, which uses infrared radiation to heat the substrates.

conditions. The work damage is removed by means of chemical etching, either acid or alkaline, with a stock removal of 0.2 to 1.0 mils.

Polishing, the final step in shaping, provides the reflective, featureless surface necessary for device fabrication (Figure 1). For VLSI applications, the surface must also have a high degree of flatness for subsequent photolithographic processing. Flatness specifications generally run to less than 5 microns total indicated runout. For the polishing operation, the wafers are mounted in a fixture and rotated against a pad under high pressure in the presence of a polishing slurry. The polishing slurry is a special mixture of colloidal silicon dioxide particles in an aqueous hydroxide solution. The amount of stock removed during polishing is nominally 1 mil.

Wafers must be absolutely clean before epitaxial deposition can take place. Consequently, all oxides, metallics and organics must first be removed from the surface. Cleaning methods include chemical sprays and dips, and brush and high-pressure water jet scrubbing. Inadequate cleaning will result in contaminants and/or structural defects within the epitaxial layer that can adversely affect device performance.

Epitaxial Deposition

The epitaxial layer is a thin, single crystal formed on the surface of a polished wafer. Although many of its characteristics are indistinguishable from the polished wafer or the substrate crystal (atomic structure and orientation are identical), the epitaxial layer does not necessarily contain the same trace impurities, dopants, resistivity variations, and crystalline imperfections found in grown crystals. These distinctions can be used to significant advantage in the design and fabrication of VLSI circuits.

Hardware and Processes. Epitaxial deposition takes place within a piece of equipment called a reactor. In its 26 years of epitaxial production, AT&T has used many different types of reactors, both commercial and internally designed. One recent type of reactor (Figure 6), called the radiantly heated barrel (RHB) heats the silicon substrates by infrared radiation. The reactor is microprocessor-controlled, and all gas flows are controlled automatically.

To start the epitaxial process, polished wafers are loaded vertically onto a graphite susceptor, which provides mechanical support for the wafers during deposition. The reactor is closed and dry nitrogen is introduced to purge the reactor chamber of air and moisture. The nitrogen flow is then discontinued and hydrogen is introduced as the reactive ambient. The chamber contents are heated to about 1200°C for a short in-place etch, in which gaseous HCl amounting to about 1 to 2 percent of the hydrogen flow is introduced into the reactor. The gas etches a small amount of silicon from the substrate surface without destroying its polish. The purpose of the etch is to remove damaged lattice sites on the surface, ensuring minimum crystalline defects in the epitaxial layer.

After the HCl etch, the reactor temperature is adjusted to layer-deposition conditions and the gaseous silicon and dopant sources are introduced. Potential sources of silicon are $SiHCl_3$, SiH_2Cl_2, and $SiCl_4$. The dopants are generally B_2H_6 or AsH_3. Following deposition, the reactor is cooled and the wafers are removed for evaluation. The nature of epitaxial deposition and the requirements for device fabrication necessitate a rapid and continuous feedback of evaluation results to ensure a controlled, precise, and cost-effective process.

To obtain the characteristics desired in an epitaxial wafer, many considerations must be weighed in designing the process. In bipolar production, buried layer pattern replication, thickness uniformity, and autodoping are important factors. For metal oxide semiconductor (MOS) processing, the critical epitaxial parameters are car-

rier density control, surface quality, perfection, and purity; thickness specifications are less stringent and there is no buried layer.

In addition to satisfying needs for carrier concentration, thickness, surface perfection, and radial and in-depth variations, the epitaxial wafer must meet all criteria for polished wafer physical characteristics. These include bow, flatness, nonlinear thickness variation, parallelism, and all other dimensional criteria.

In processing epitaxial material for linear and digital bipolar devices, one of the most restrictive requirements is in replicating the buried layer pattern. The accuracy of this replication depends largely on the process temperature. For linear bipolar devices, this dictates the use of $SiCl_4$ and a deposition temperature of over 1200°C. Thickness uniformity of the epitaxial layer is also a challenge in processing bipolar devices, since these wafers generally require a spread of less than 1 micron. This requirement applies both to variations within a wafer and to variations among wafers. Uniformity within a wafer depends on susceptor design and gas flow patterns. Among wafers, uniformity is determined by reactor gas flow and control of reactor rotation.

Whereas thickness uniformity is largely dependent on flow patterns in the reactor, carrier concentration uniformity is often a matter of temperature. For temperature control purposes, an RHB reactor is divided into three zones, with the center zone serving as control for the end zones. Carrier concentration is regulated by monitoring postepitaxial concentration evaluation data and making appropriate temperature adjustments to the end zones.

In addition to intentional doping from the reactor source, wafers are subject to autodoping, a phenomenon common in epitaxy. Autodoping describes the supplemental doping of wafers from other impurity atoms present in the reactor. These atoms may come from highly doped substrate wafers being processed, or from diffused areas such as buried layers. However, the buried layer is only a temporary source of impurity atoms vaporized during the heating and etching portion of the process preceding deposition. Once the silicon layer has been deposited, the temporary source is sealed over and the vaporization halts.

On the other hand, the back surface of a substrate wafer is a continuous source of dopant atoms. While this source can be controlled by using a nitride or oxide back coating, such an approach involves additional technology and cost. Careful epitaxial process design can, in some cases, avoid this investment.

MOS device designs call for a lightly doped p- or n-type epitaxial layer on a heavily doped p- or n-type substrate. In the 1970s, AT&T was the first company to manufacture MOS dynamic random-access memories (DRAMs) using epitaxial wafers. Today this process is highly refined and controlled. All wafers are laser-marked prior to epitaxial processing, and highly automated evaluation uses optical character readers to associate test data with individual wafers.

Epitaxial Evaluation

The epitaxial layer adds certain physical and electrical characteristics to a wafer that must be considered in the design and processing of integrated circuits. For example, carrier density, or concentration, affects implants, diffusions, and final chip probe parametrics and yields.

Carrier density is the number of dopant atoms in a cubic centimeter of the epitaxial layer. As a rule, this concentration is extremely low, in the range of parts per billion, and is governed by the physical and chemical structure established in the epitaxial layer on an atomic scale. In manufacturing microelectronic devices, it is essential that carrier concentration be rigorously controlled. Since epitaxial deposition is a semicontinuous batch process, variations in carrier density from run to run can result in large volumes of defective epitaxial wafers. Consequently, methods of monitoring carrier density are both numerous and extensive.

Four-Point Probe Control. The classic approach to controlling carrier density is the four-point probe. This test method is direct and useful in those epitaxial structures where the conductivity of the layer is the opposite of that

of the substrate, such as p on n type or n on p type. This test has several shortcomings, however. Very few VLSI epitaxial structures are formed on substrates with an opposing conductivity. Hence, in those applications where the four-point probe is used, a control wafer is required. This wafer is run through the process for the sole purpose of testing and is later recycled or scrapped. A control wafer not only adds to the operational expense, but also occupies a reactor position that could otherwise be used for actual product.

Spreading Resistance. A more sophisticated approach for measuring carrier density is the spreading resistance test. On first examination, this test appears simple. In fact, it is a complex and exacting technique requiring specialized training and instrumentation. The test is based on the concept that the resistance of a small point contact is directly related to the resistivity of a specially prepared silicon surface and indirectly to the radius of contact of a flat circular probe. The stability of the radius of contact is a key factor in controlling the measurement of carrier density by spreading resistance. Metal-to-silicon contacts are greatly affected by slight changes to the silicon surface and the contact surface. The surface finish, crystal orientation, conductivity type, time out of the reactor, and ambient conditions to which the silicon is exposed all affect the electrical contact radius. The probe itself must be specially prepared and frequently calibrated using silicon samples of known surface condition and resistivity. The calibration samples must have surfaces as similar as possible to the wafers being measured. Because spreading resistance is a calibrated technique that relies on standard references, carrier density is not derived from first principles but is deduced from comparison with calibration samples.

Diode V-C Test. Although the spreading resistance test produces rapid measurements, it does not provide the accuracy and precision necessary to monitor carrier density in MOS epitaxial wafers. Since the threshold voltage of many MOS devices depends on the doping density or carrier density of the epitaxial layer, the carrier density parameter must be determined accurately. The most accurate method has been measurement by planar diode voltage-capacitance (V-C) testing. However, this test has a number of pronounced disadvantages.

Testing by voltage capacitance is destructive, labor intensive, and requires 8 to 12 hours to produce results. The planar diode is an actual device that must be fabricated in a product wafer. This entails oxidation, photolithography, diffusion, and multiple etching steps. Only the wafer upon which the diode is fabricated is probed for the voltage capacitance test, after which the wafer is no longer usable.

Once the diode has been fabricated, the probing is rapid. To be tested, the diode must be well-defined and have a low leakage current, high breakdown voltage, and low forward resistance. If any of these attributes are missing, errors in measurement will be introduced and the diode will be unacceptable for probing.

Mercury Probe. A new test developed by AT&T for measuring carrier density is the mercury probe voltage-capacitance method. With this method, the dopant density can be measured to a degree previously obtainable only by destructive and labor-intensive tests. Using special surface treatments developed and patented by AT&T, the contact of mercury to the epitaxial surface produces a Schottky barrier diode. The Schottky contact is established by using a vacuum to draw mercury to the wafer surface through a well-defined orifice. Rapid, nondestructive determinations of carrier density can then be made by measuring the voltage-capacitance characteristics of the reverse-biased diode.

Mercury probe testing has several economic advantages: it releases the high percentage of reactor capacity formerly required for control wafers; it eliminates the expense involved in scrapping or recycling control wafers after testing; it is not labor intensive; it provides high accuracy and precision; it increases chip yield through more careful control of carrier density; and because it tests product wafers directly rather than through a control wafer, it can screen good product from defective, thus

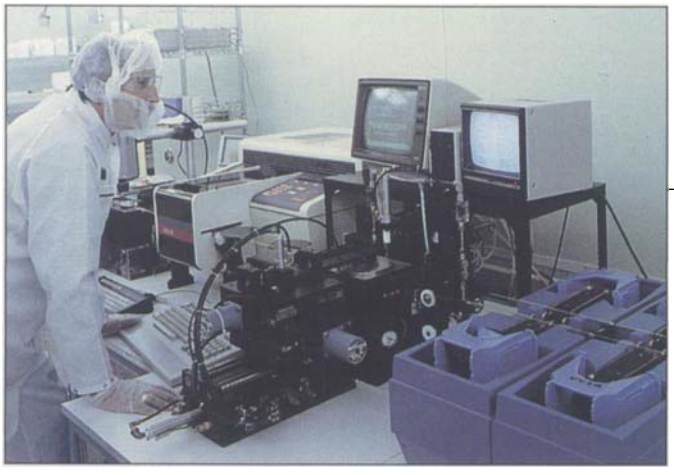

Figure 7. This instrument is part of a new test set developed by AT&T for measuring carrier density. It is based on the mercury-probe voltage-capacitance method.

increasing epitaxial yield. During testing, each wafer is handled by cassette transfer.

Wafer flats are oriented, and standard laser marks are read and recorded. Carrier density is measured either at the center or at five points, including the center and four 90° edge locations, which makes radial gradient determinations readily available. The wafers are automatically sorted into accept and reject cassettes according to programmed criteria. Typical output includes the laser mark identification, conductivity type, the center carrier density, the radial carrier density, in-depth carrier density variation, and disposition. These features are established by electronics and computer control techniques that represent the most precise and reliable package of voltage capacitance testing equipment ever assembled (see Figure 7).

Layer Thickness—Fourier Transform Infrared Interferometry. Another important characteristic that must be considered in device fabrication is the thickness and uniformity of the epitaxial layer. Here, thickness is dictated by the device being processed. It may range from less than a micron to more than 100 microns, with values less than 25 microns being the most common. Specifications for thickness uniformity typically range from ± 13 percent to ± 3.5 percent. Bipolar devices with oxide isolation have very thin epitaxial layers, and some have only submicron thicknesses. Uniformity is most critical in these very thin layers and is also a most challenging parameter to control.

The standard technique for measuring epitaxial thickness is based on Fourier transform infrared interferometry. AT&T first introduced this instrumentation into epitaxial production in the early 1970s. Various designs are now widespread throughout AT&T, offering a number of options in output presentation and wafer handling.

Basically, the instrument consists of a Michelson interferometer with an infrared source and a computer to control the test and perform calculations. The system produces and examines an interferogram created by impinging infrared radiation on the surface of the epitaxial wafer. By analyzing the intensity of the detected radiation, the interference pattern can be related back to the difference in optical paths and, therefore, layer thicknesses.

Surface. For MOS device manufacture, the epitaxial layer is deposited directly on a polished wafer. In bipolar manufacture, subdiffused buried layers are formed in the substrate prior to deposition. The buried layer consists of regions on the substrate that have been ion-implanted with dopants.

The buried layer may serve a variety of purposes. It provides a low resistivity path in the collector of digital bipolar devices, serves as a source of up-diffusion in forming junctions, or functions as the emitter in linear bipolar devices. Since any distortion of the buried layer during deposition will cause a misalignment of photolithography, the epitaxial process is designed and controlled so that buried layer patterns are accurately replicated and visible on the layer surface. Wafers with buried layer patterns are inspected in a dark area under a high-intensity light and also with Nomarski interference contrast microscopy.

Unpatterned epitaxial wafers, such as those used for MOS VLSI technologies, are inspected with a scanning laser system. The laser light, both reflected and scattered, from the epitaxial surface is collected by photomultiplier detectors. The signals detected by the photomultipliers are analyzed by computer. Within a matter of seconds, 100 percent of the wafer surface is scrutinized and a judgment

is made concerning the epitaxial wafer's acceptance or rejection. This entire operation is quantitative and automated.

Perfection and purity are also frequently analyzed by using appropriate instrumentation such as scanning electron microscopy, transmission electron microscopy, Auger spectroscopy, neutron activation analysis, secondary ion mass spectroscopy, electron spectroscopy for chemical analysis, electron microprobe, laser emission microprobe, cryogenic Fourier transform infrared, and other techniques.

The presence of impurity precipitates and other crystalline imperfections is routinely monitored on a microscopic level through selective etching. Anodic etching is also used to discern those defects that are electrically active. Although destructive, these etching tests are performed on a routine basis.

AT&T has been a leader in the development of production measurement technology. The methods developed to characterize epitaxial wafers reflect measurement techniques largely initiated and implemented by AT&T technologists, for example, Fourier-transform infrared thickness measurements, scanning laser inspection systems, and mercury probe capacitance-voltage testing. The advanced development of production measurement technologies has led to a detailed understanding of wafer characteristics. This understanding, coupled with feedback from device technologists, has led to high yields and high-quality epitaxial wafers which are custom-tailored to chip production yield and performance, whether the product is a megabit DRAM or a planar diode. The objective is to provide the ideal material for the device being fabricated. This is possible only through extensive process and quality control as well as the constant interaction of silicon materials specialists and device fabrication engineers.

Biographies (continued)

from crystal to epitaxial wafers, and for developing new test techniques and instruments. He received a B.S. degree in chemistry from Lafayette College in 1969 and an M.S. degree in materials science from Lehigh University in 1975. He joined AT&T in 1969. ***Raymond E. Reusser*** *is Intellectual Property Licensing and Management manager at AT&T, Liberty Corners, New Jersey. Since joining AT&T in 1963, he has worked on engineering research, semiconductor materials engineering, strategic planning, and bipolar chip manufacturing and process control. He received a B.S. degree from Purdue University in 1963 and an M.S. from Lehigh University in 1967.* ***George Williams*** *is a consulting member of technical staff at the AT&T Engineering Research Center, Princeton, New Jersey, assigned to the Thermal and Computational Engineering group in the Semiconductor Process Technology department. He began his AT&T career in 1971. He received a bachelor's degree in mechanical engineering from The City College of New York in 1965 and Sc.M. and Ph.D. degrees in mechanical engineering from Brown University in 1968 and 1971.*

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