REPORT:

A NETWORK-INTERFACE CHIP FOR ISDN TERMINALS

P. K. Govind *and* ***Glen E. Offord*** *are members of the technical staff at AT&T Bell Laboratories in Allentown, Pa.* ***Lisa J. Piper*** *is a member of the technical staff in the Consumer Products Division of AT&T Information Systems in Holmdel, N.J. Mr. Govind is a senior product planner for communication devices in the Customer Service Laboratory. He received an M.S. and Ph.D. in physics from the University of Colorado. He joined AT&T in 1981. Mr. Offord is in the Customer Product VLSI Design Department and specializes in VLSI design. He joined AT&T in 1970 with a B.S.E.E. from the University of Florida. Ms. Piper is a system designer and VLSI specialist in a terminal development laboratory. She joined AT&T in 1981. She has a B.S.E.E. from Purdue University and an M.S.E.E. from Ohio State University.*

Introduction

A new integrated circuit designed by AT&T enables digital telephones, terminals, personal computers, and workstations to access simultaneously the voice and data services of the Integrated Services Digital Network (ISDN).[1]

The chip meets the CCITT (International Telegraph and Telephone Consultative Committee) physical link 2B + D standard for terminating a four-wire line. The line consists of a transmit and receive pair that may form a passive bus supporting up to eight terminals. This off-the-shelf integrated circuit (IC), a member of the UNITE™ family of devices—designated T7250A—terminates the ISDN basic rate interface (BRI) in terminal equipment.

The BRI is also known as the 2B + D interface at the S/T (subscriber/termination) reference point (Figure 1). It is through the BRI that voice, data, telemetry, facsimile, and other digital services that ISDN provides are accessed by subscriber terminals. This report describes how the UNITE IC works and can be used to build ISDN basic-access terminals.

Standards

The IC's design conforms to the BRI specifications in the CCITT's I.430 Recommendation.[2] Time multiplexed 2B + D transmissions at the S/T interface consist of two 64 kilobits per second (kb/s) B channels and one 16 kb/s D channel (Panel 1). Line transmissions occur at 192 kb/s, with 144 kb/s for user information (2B + D) and 48 kb/s for framing, control and synchronization. The I.430 voltage and impedance requirements are met when a simple four-wire line interface circuit is connected.

Point-to-point and point-to-multipoint (passive bus) arrangements are supported as are procedures for activation/deactivation, contention resolution, and priority. The IC also supports a multiframing mechanism that's expected to be adopted in the next I.430 revision.

Cost-effective design features of the UNITE IC simplify the design of ISDN basic access integrated voice/data terminals. Programmable features, for example, allow many devices to be interfaced easily. Separate pins are available for inputting B1 and B2 channel information that is to be transmitted to the network.

The chip's HDLC (high-level data-link control) formatter processes D-channel data. Sixteen-byte buffers allow efficient processing of D-channel transmit and receive data queues.

Basic Data Flow

Figure 2 shows the major parts of the IC: the *four-wire line transceiver, 2B + D core, HDLC formatter, and the microprocessor interface and control.* Chip operation is controlled via the microprocessor interface using 16 programmable registers listed in Table I. The IC also has a versatile programmable timer for general system applications.

The 2B + D data stream is received from the network in alternate space inversion line code. In this line-coding scheme, a binary "1" is represented by the absence of a pulse,

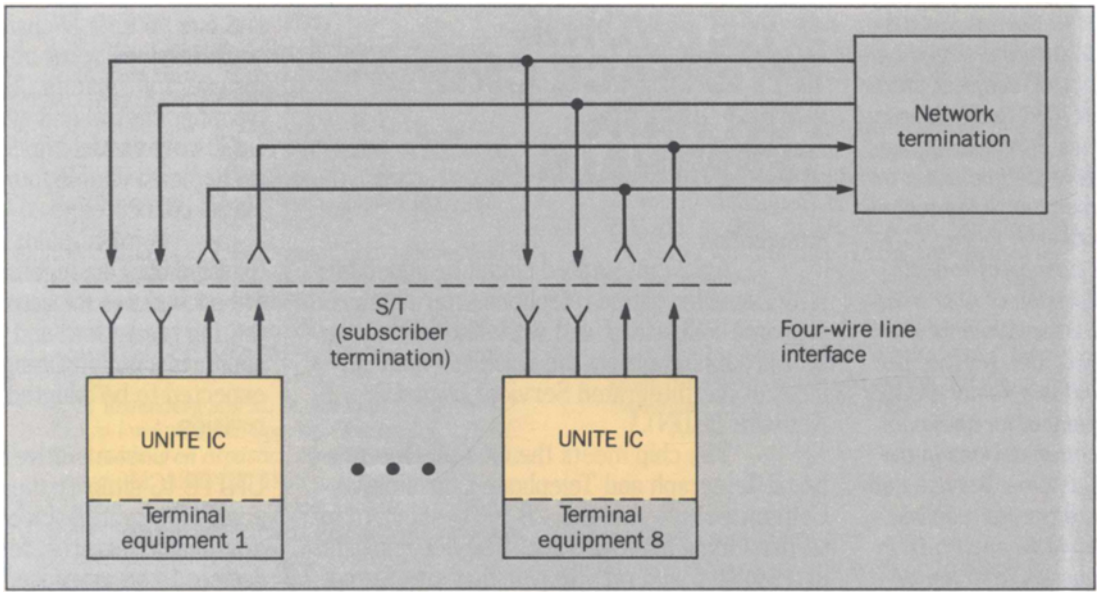


Figure 1. Subscriber/ termination (S/T) reference point for ISDN basic access subscriber terminals.

and a binary "0" (or space) is represented by alternating positive and negative pulses. The line receiver provides filtering and converts the bipolar line data to unipolar binary bit streams that represent data from the positive rail and the negative rail. The bit streams are passed to the 2B + D core, which derives timing signals from them and generates a single 192 kb/s bit stream.

The received 2B + D bit stream is passed directly to the terminal equipment via a single pin. Programmable clock and synchronization signals permit easy extraction of the two B channels. D-channel data are passed to the HDLC formatter for frame-level processing. The HDLC formatter stores D-channel data in a 16-byte queue. The microprocessor controlling the UNITE IC retrieves the data through register 3 of the IC. D-channel queues may contain level 2 and level 3 information, i.e., signaling messages or packet data. In addition, S-channel messages, newly defined in the I.430 and providing one-bit-per received frame, are stored in register 7.

The 2B + D data transmitted to the network follow the reverse path. D-channel data to be transmitted to the network are entered through register 3 of the microprocessor interface and are passed to a 16-byte transmit queue. The HDLC formatter processes data from the queue and passes them to the 2B + D core. B-channel information is sent to the 2B + D core via dedicated input pins.

Data from these pins are sampled relative to the B1 and B2 clocks provided by the receiver portion of the 2B + D core. The 2B + D core also handles the processing of Q-

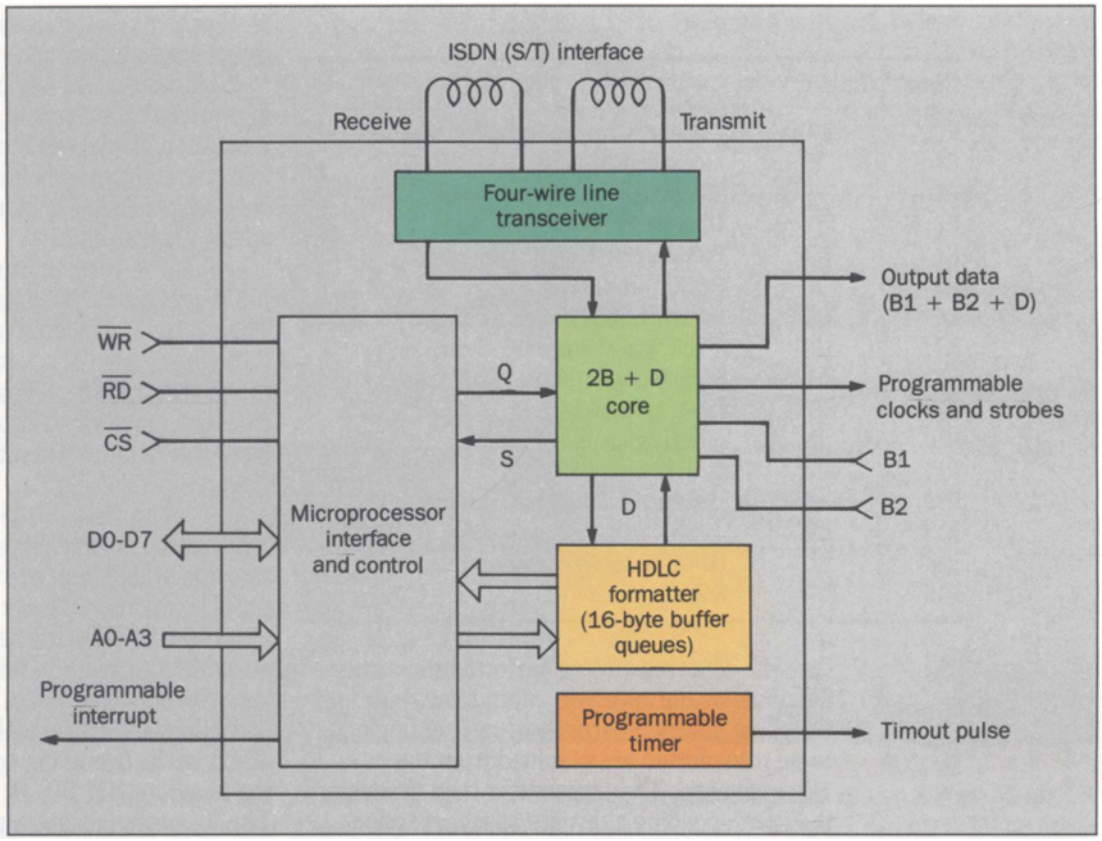


Figure 2. Architecture of the AT&T UNITE integrated circuit (T7250A) showing the primary data paths, inputs, and outputs.

channel data that are provided for multiframing (TE→NT). The Q channel provides a signaling capability. One Q bit is permitted in every fifth frame. Q-channel data are entered through register 11 of the microprocessor interface. The use of Q bits as a signaling channel is optional in the TE. The 2B + D core formats the user data into the I.430 192 kb/s frame and passes binary encoded 192 kb/s bit streams to the transceiver. The line transmitter then creates the alternate space inversion line code and transmits the information.

Four-Wire Line Transceiver

The four-wire line transceiver consists of a receiver and a transmitter that are transformer coupled to the S/T line interface (Figure 3). The receiver converts the bipolar line-code signals to unipolar binary bit streams that contain user data and framing information. The bit streams go to the 2B + D core for further processing.

Table I. Register Overview

Name	Read/Write	Function
R0	R/W	Chip/hardware configuration register
R1	R	Line interface status
R2	R/W	Transmitter control register
R3	R/W	D-channel data byte
R4	R/W	Hardware configuration register
R5	R	HDLC receiver status
R6	R/W	Interrupt trigger levels for D-channel queues
R7	R	Multiframe status and S-channel queues
R8	R/W	S/T interface control
R9	R/W	Interrupt masks
R10	R	Interrupt status
R11	R/W	Q-channel data and status
R12	R/W	Loopback and transmit ones control
R13	R/W	Timer configuration control
R14	R	HDLC transmitter queue status
R15	R/W	Software resets

The transmitter performs the same functions as the receiver, but in reverse order. Outgoing binary bit streams representing data to be transmitted are obtained from the 2B + D core. The transmitter then produces the corresponding alternate space inversion line code.

2B + D Core

The 2B + D core is the heart of the UNITE IC. Figure 4 shows its major parts. The timing recovery circuit is a digital phase-locked loop that derives the 192-kHz master clock signal from received data. (Clock jitter limits specified in I.430 are met.) The signal is fed to the receive formatter.

The receive formatter extracts timing and synchronization information from the binary bit streams of data that come from the line receiver. It then converts the bit streams into a single bit stream. This bit stream is sent to external system devices; to the multiframing, priority mechanism, and contention resolution blocks; and to the internal HDLC formatter. Programmable clock and strobe signals are produced to identify the B1, B2, S, Q, and D-channel data.

The receive formatter also reports the I.430 specified INFO-state that is received. This status is available to the microprocessor through register 1, allowing the microprocessor to monitor activation/deactivation requests from the network. A programmable interrupt can be generated when the INFO-state changes.

The transmit formatter of the 2B + D core handles the formatting of binary streams of data that are passed to the transmitter. The microprocessor may specify that a particular INFO-state be transmitted. This gives the flexibility to initiate activation/deactivation procedures. Data formatting for normal operation (INFO 3) involves constructing the 48-bit serial frame (as specified in I.430) from the separate B1, B2, D, and Q data sources. The formatted data are passed to the line interface transmitter for transmission to the network.

The transmit and receive formatters are capable of exchanging the information on the B1 and B2 channels. This feature allows designers to connect a device to a particular channel without limiting its use to that channel. The exchange feature is controlled through register 4.

Contention resolution as specified in I.430 is supported. When transmitting on the D channel, the 2B + D core compares the received D-echo bit with the previously trans-

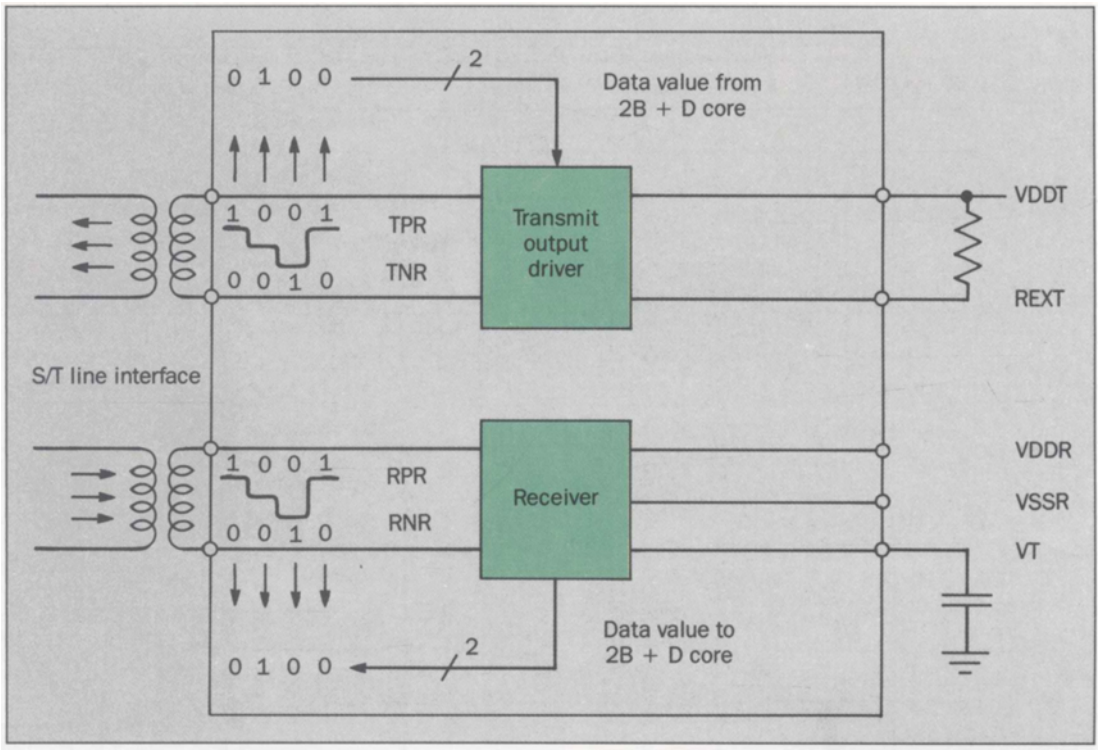


Figure 3. Block diagram of the four-wire line transceiver.

mitted D bit. If they are not the same, D-channel transmission is immediately terminated. A programmable interrupt is generated to alert the microprocessor.

The priority mechanism ensures that all terminals in a passive-bus arrangement have equal access to the D channel. There are two priority classes: signaling and data. Signaling is given high priority; data are given low priority. Within each class, the priority mechanism is completely automatic.

Multiframing is also handled by the 2B + D core. The receive formatter determines whether multiframing is present. If it is, the transmit formatter will place the Q bits in the appropriate location of the proper 48-bit frames. Four-bit nibbles of Q-channel data are loaded by the microprocessor through register 11. This register also provides operational status on the number of bits that have been transmitted, and when a complete nibble (one multiframe) has been transmitted. A nibble transmission can generate an interrupt. Proper operation of the multiframing mechanism may be verified by reading register 7. Received S-bits (one S-bit per frame, NT→TE) are also available in register 7 every five frames. An alternate mode presents four bits every multiframe (20 frames), where each of the four bits is a majority vote of five sequential S bits.

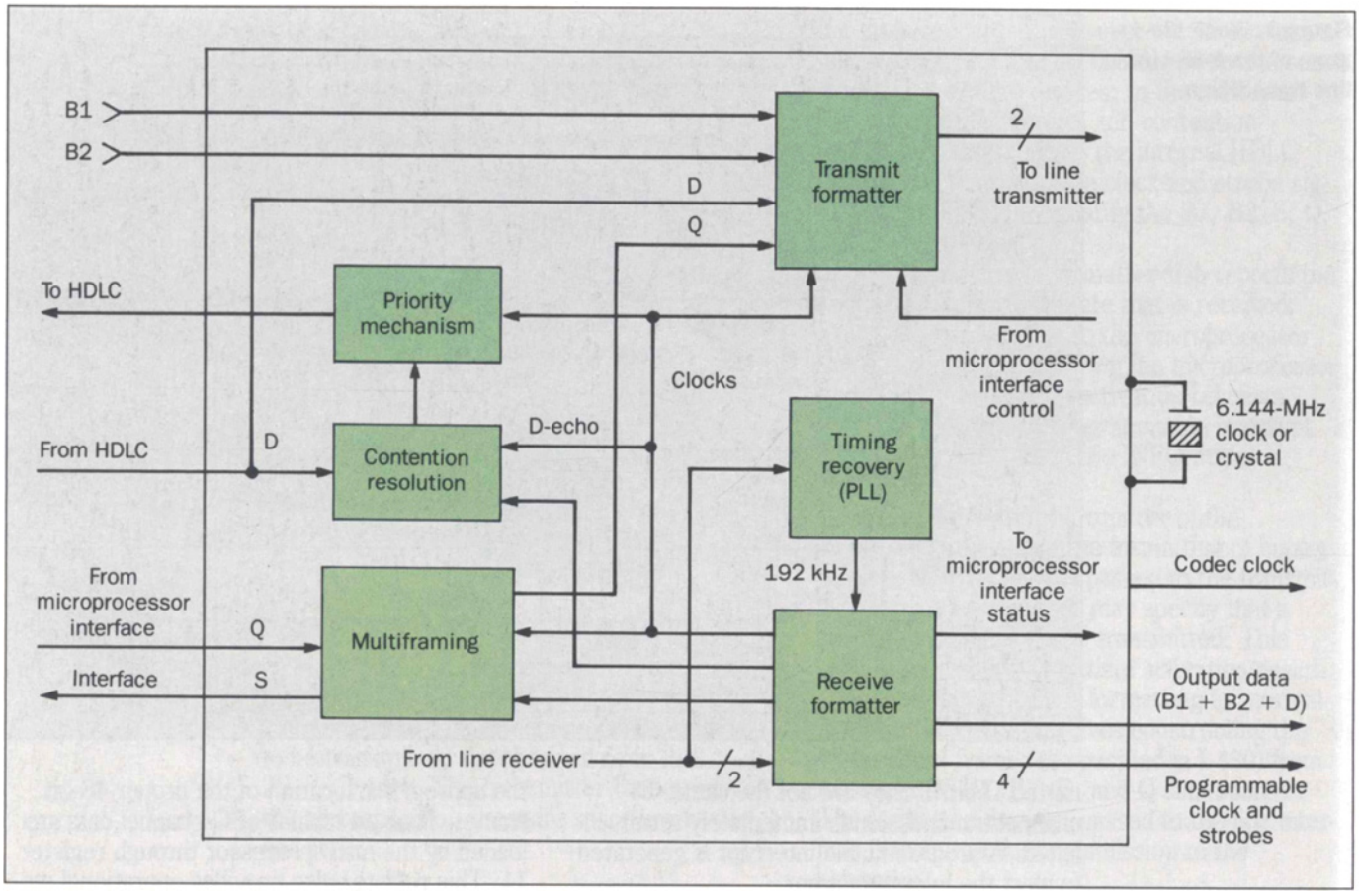


Figure 4. Block diagram of the 2B + D core.

HDLC Formatter

I.430 specifies that HDLC formatting must be used for all D-channel transmissions. The UNITE IC contains an internal HDLC formatter that handles this automatically. Figure 5 is a block diagram of the HDLC formatter, which performs the standard HDLC functions and more.

Standard HDLC receive functions include flag detection and deletion, zero-bit deletion, and CRC (cyclic redundancy check) checking. In addition to the standard functions, the incoming serial data are converted to 8-bit bytes and stored in a 16-byte queue. The microprocessor retrieves queued data through register 3. The HDLC formatter also provides status information for each frame and for the receive queue. Multiple frames are allowed in the queue. An end-of-frame (EOF) status is set for each frame when a closing flag is detected.

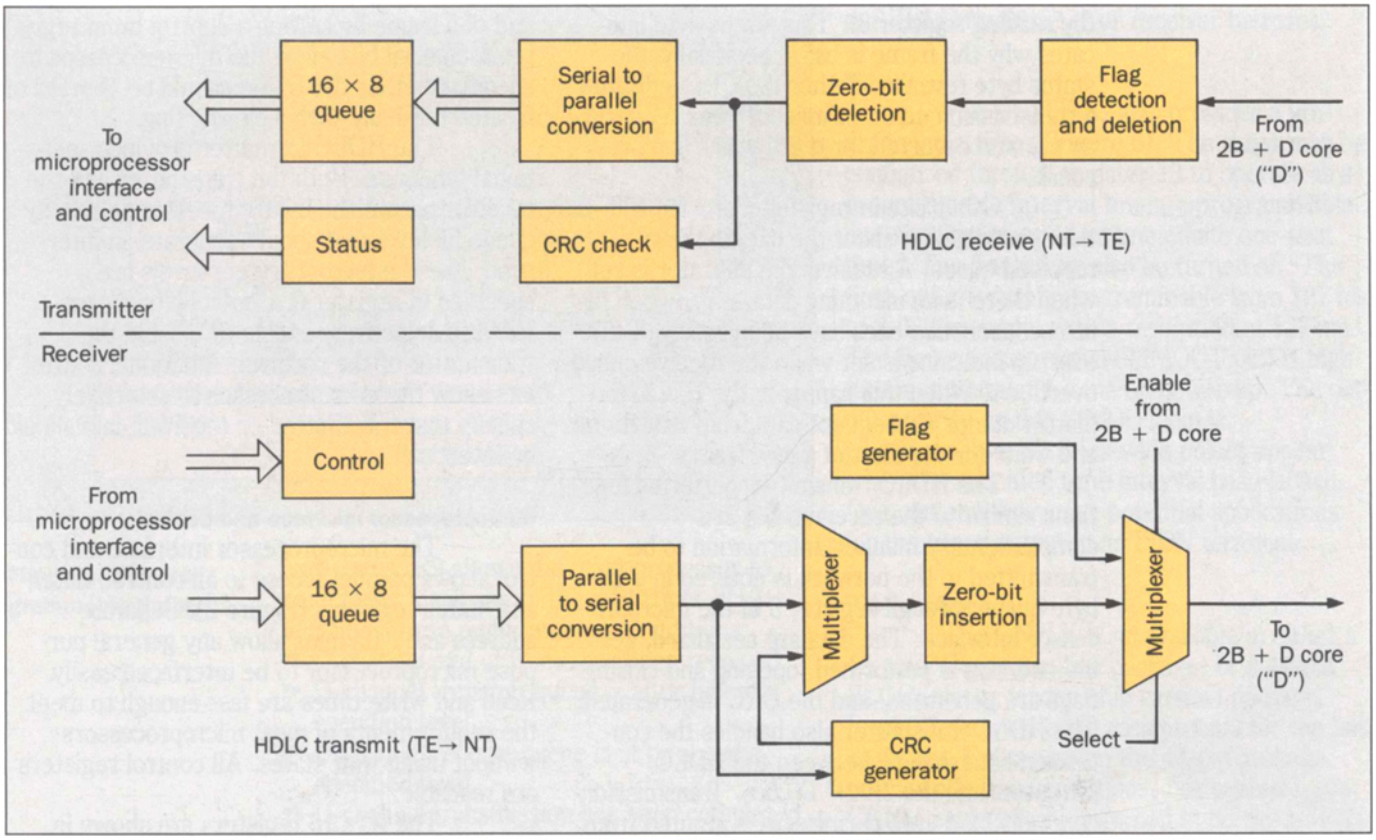


Figure 5. Block diagram of the HDLC formatter.

A programmable interrupt can be generated to alert the microprocessor.

The receiver design allows very efficient processing of multiple frames in the queue. A global status register (register 5) provides queue status for all received frames. An EOF (end of frame) status byte is stored in the receive queue to provide information specific to each frame.

Register 5 reports the number of bytes in the received queue up to the first end of frame. If there is no EOF status byte in the queue, register 5 reports the number of bytes in the queue. This novel design eliminates the need for the software to monitor an EOF status for every data byte in the queue. By reading register 5, the software knows whether end-of-frame processing is required and it knows exactly where the end of frame status exists in the data queue. This minimizes the number of processor reads and permits the processor to utilize block moves.

The EOF status byte is retrieved from the data queue as the last byte of every frame

(by reading register 3). This status byte indicates why the frame is bad. Specifically, the status byte reveals whether the CRC indicated a transmission error, or an abort was received, an overrun occurred, or there was a bad byte count.

Other bits in register 5 provide additional information about the data in the received queue. A receive-idle indicator is set when there is no incoming data, e.g., when fifteen consecutive ones have been received. An overrun indicator is set when the receive queue overflows. When this happens, the HDLC formatter dumps subsequent data from that frame and waits for the start of a new frame.

The HDLC transmitter performs functions similar to the receiver, but in a complementary manner. Information to be transmitted to the network is entered in a 16-byte queue through register 3 of the microprocessor interface. The data are serialized, zero bit insertion is performed, opening and closing flags are generated, and the CRC is generated. The HDLC transmitter also handles the contention handshaking between the HDLC formatter and the 2B + D core. Transmission is not enabled until permission is granted from the 2B + D core.

The HDLC transmitter will request permission to transmit from the 2B + D core when there are data in the queue. Transmission stops when an entire frame has been transmitted. An interrupt is generated after the last bit of the closing flag has been transmitted. This allows the microprocessor to keep track of frames that have been transmitted. If access to the D channel is lost, the microprocessor then knows which frame should be retransmitted.

Multiple frames may be entered in the queue. The microprocessor must indicate the end of a frame by setting a control bit in register 2. Special bits allow the microprocessor to specify whether the frame should be aborted or treated normally with a closing flag.

The HDLC formatter provides additional functions. Both the transmitter and the receiver permit the microprocessor to specify a queue fill level that should generate an interrupt. These interrupt trigger levels are specified in register 6. Control bits are provided to selectively enable or disable the transmitter or the receiver. Additional control bits allow the microprocessor to selectively specify that transmitted or received data should be inverted.

Microprocessor Interface and Control

The microprocessor interface and control allows parallel access to all control, data, and status registers (Figure 2). Separate address and data lines allow any general purpose microprocessor to be interfaced easily. Read and write times are fast enough to meet the requirements of most microprocessors without using wait states. All control registers are readable.

The IC's 16 registers are shown in Table I. Most register functions have already been discussed; a few others will now be described.

Register R4 contains hardware configuration parameters. The microprocessor may configure the polarity of the timer and interrupt signals through this register. This register also provides programmable control of clock and strobe signals. Having software control of hardware output signals minimizes the external logic that is required to interface the UNITE IC to peripheral devices.

R9 and R10 provide interrupt control

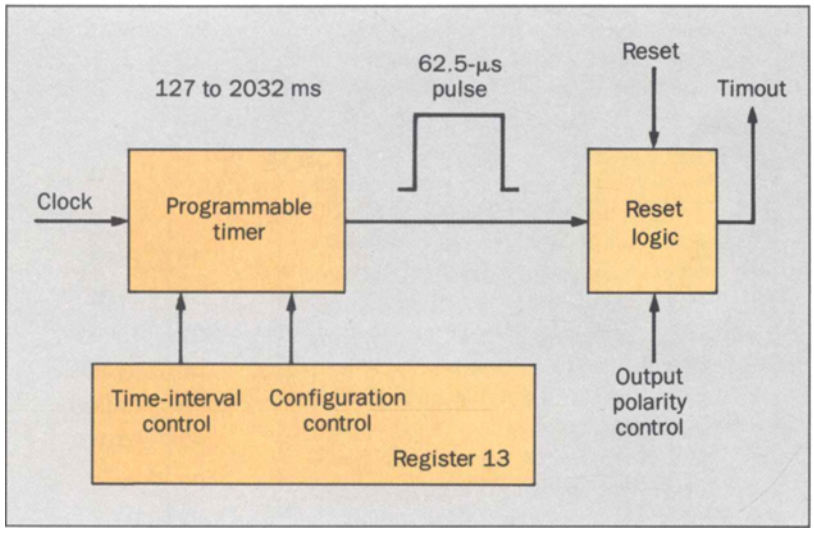


Figure 6. The programmable timer.

and status. R9 allows the microprocessor to selectively mask any of the interrupts. R10 identifies these eight interrupt conditions:

- D-channel end of frame has been received
- D-channel transmit queue is at or below a specified level
- D-channel receive queue is at or above a specified level
- D-channel transmission has been completed
- S-channel data are available
- Q-channel multiframe has been completed
- The received I.430 info-state has changed
- D-channel access has been lost.

R12 contains loopback controls. Local and remote loopbacks are provided for the B1, B2, and D channels. Loopback modes are useful during system tests. R12 also allows the microprocessor to specify an all-ones transmission on B1 and B2 channels.

R15 contains software resets. The microprocessor may specify that the entire chip be reset. It may also selectively specify that the HDLC transmitter or receiver be reset.

Timer

The UNITE IC also provides a programmable timer (Figure 6). The timer may be configured through register 13 to operate as a programmable interval timer, a programmable one-shot timer, or as an immediate one-shot timer. The timer may also be turned off. The time-out interval is programmable from 127 ms to 2.032 seconds, with a resolution of 127 ms. The timer output signal (TIMOUT pin) is high for a minimum of 1.4 ms on power-up. The output polarity on the TIMOUT pin is programmable. 62.5-µs-wide pulses appear when the specified time interval has elapsed. One can envision many potential applications for the timer output in an ISDN terminal.

Pin Functions

The UNITE IC is available in either a 40-pin DIP (dual in-line package) or a 44-pin PLCC (plastic leaded chip carrier) package. Figure 7 shows the pin assignments for the two packages. Extra pins on the 44-pin package provide additional functions. For example, pin CKDM could be programmed to be the 16-kHz D-channel clock or to be a free-running 8-kHz clock. Pin 28 provides the 6.144-MHz clock or the 192-kHz clock for system use.

Most pins have been discussed, so we will briefly describe functionally related groups; refer to the DIP diagram in Figure 7.

Pins 1-4 (VDDT, TNR, REXT, TPR) all belong to the line transmitter. TPR and TNR are the transformer connections. REXT is for setting the transmitter output current and VDDT is the dedicated power pin.

Pins 5 and 6 (TXB1 and TXB2) are inputs for the B-channel information that is to

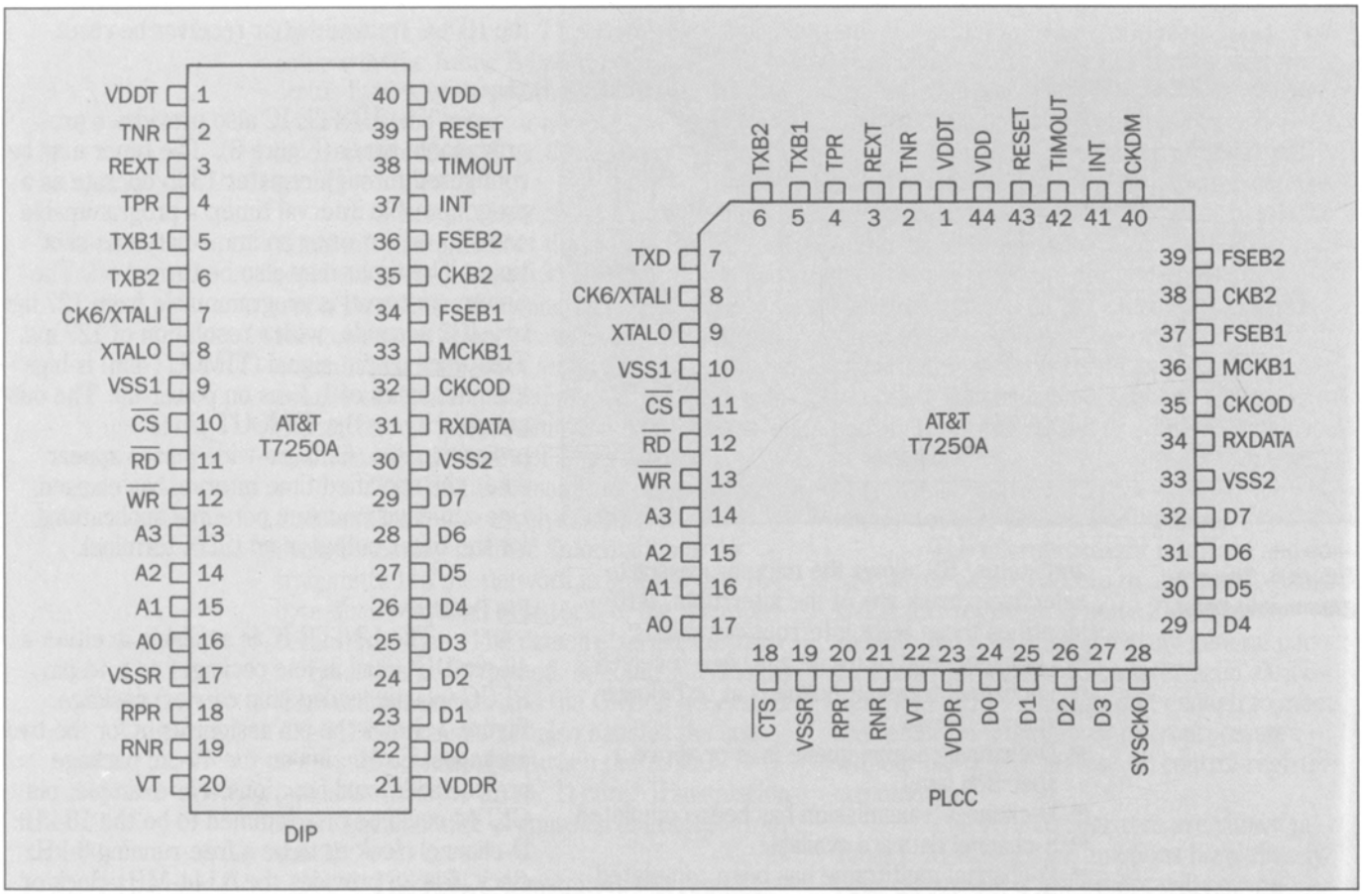


Figure 7. Pin assignments of the UNITE IC are shown for a 40-pin DIP (dual in-line package) and a 44-pin PLCC (plastic leaded chip carrier).

be transmitted to the NT.

Pins 7-8 (CK6/XTALI and XTALO) provide direct connections to a crystal. Alternatively, the CK6/XTALI pin may be driven by an external clock source at 6.144 MHz.

Pins 9, 30, and 40 provide grounds and power. Pin 9 (VSS1) is the ground reference for input buffers and other internal logic. Pin 30 (VSS2) is the ground reference for the output buffers. Pin 40 (VDD) is the power input for all the digital logic.

Pins 10-16 ($\overline{CS}$, $\overline{RD}$, $\overline{WR}$, A0-A3), pins 22-29 (D0-D7) and pin 37 (INT) form the microprocessor interface.

Pins 17-21 (VSSR, RPR, RNR, VT, and VDDR) are inputs to the line receiver. RPR and RNR are the transformer connections. The VT input allows for an external decoupling capacitor to filter noise from the receiver's voltage reference level. Separate power and ground pins (VDDR and VSSR) for the receiver minimize noise problems.

Panel 1. ISDN (2B + D) Basics

The promise of an ISDN as a "digital pipe" for global information exchange is based on a nonproprietary open architecture of international standards. The CCITT has defined ISDN as a communications network evolving from the present telephone network. The goal of ISDN is to provide end-to-end digital connections worldwide, in support of voice and nonvoice services to which users have access via a limited set of standard multipurpose user-network interfaces.

Service capabilities are defined across a user-network interface by subdividing the information capacity into channels. User information is carried in 64 kb/s bearer channels, called B channels. Control information (signaling) for the B channels is carried in a separate 16 kb/s data channel, called the D channel. Fundamental to ISDN is the customer control of service features via the D channel. Thus, when customers get bandwidth (B) on demand via the D channel, the D channel can be viewed as a dialing channel. When two B channels and a D channel are combined, the user-to-network interface is called a 2B + D basic access subscriber/termination (S/T) interface.

The CCITT has published the technical specifications for the S/T interface in its October 1985 Red Book Recommendation I.430, with some revisions made in 1986. Two-way digital communication will take place over existing telephone wire pairs. There is no need to convert digital information to analog form before it can move over phone lines. Since digitized voice signals will be transmitted like digital data signals, it is possible to send both voice and data digitally on the same set of wires in interleaved time slices. Hence, most distinctions between voice and data communications will disappear in ISDN.

The basic access service in ISDN operates at a bit stream rate of 192 kb/s, with 144 kb/s of bandwidth reserved for the 2B + D multiplexing, and 48 kb/s of bandwidth reserved for control and recovery of the multiplexed B and D channels.

Up to eight 2B + D nodes may be interconnected to support distributed processing across an ISDN interface as the demand for networking telephones and terminals grows. A priority mechanism for access to the D channel among the nodes is specified in the I.430 standard.

The RJ-45 minimodular connector is likely to be approved as the physical interface for IDSN connections. It is the eight-wire version of the familiar RJ-11 telephone jack and plug used widely in the United States. Four of the eight leads of the RJ-45 will provide bidirectional communications between the terminal equipment (TE) and the network termination (NT). The same four leads may also provide remote power transfer from NT to TE; the remaining four leads may be used for auxiliary power as needed.

Pin 31 (RXDATA) contains the 2B + D serial bit stream that is received from the NT.

Pins 32-36 (CKCOD, MCKB1, FSEB1, CKB2, and FSEB2) provide the programmable clock and strobe signals associated with the B1 and B2 channel information. All clock and strobe signals are synchronized to the 2.048-MHz clock (CKCOD) to reduce codec noise problems.

Pin 38 (TIMOUT) is the timer output. This signal is always high on power-up.

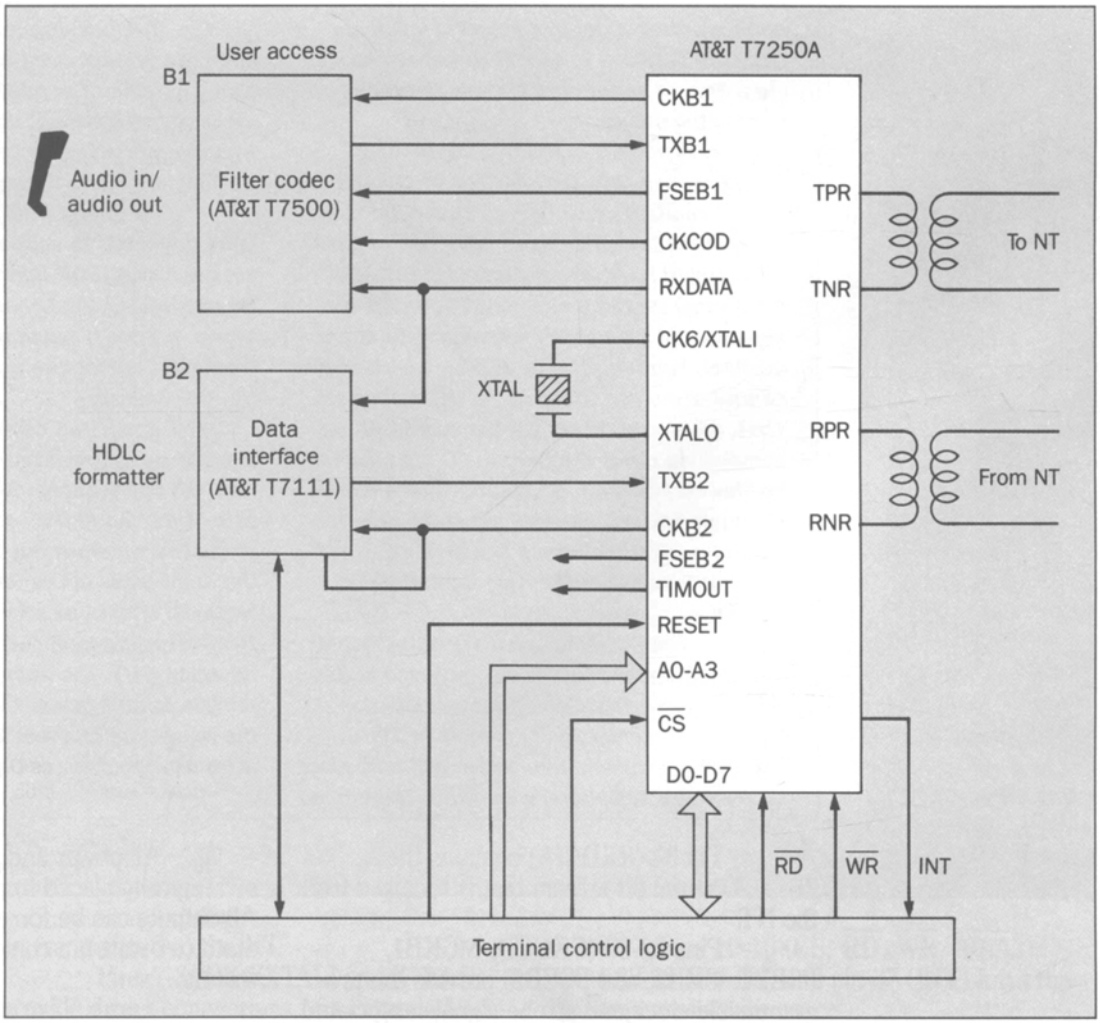
Pin 39 is RESET; a high on it resets the entire chip and restores all default settings.

All power and ground pins have been strategically placed to reduce noise problems. All outputs can be forced to a high-impedance state (tri-state), a convenience for board-level testing.

Putting the UNITE IC to Work

Figure 8 shows how the UNITE IC can be connected in an ISDN integrated voice and data application. The B1 channel is connected to a codec for voice. The B2 channel is connected to an HDLC formatter for data. The UNITE chip combines the B-channel voice and data with the D-channel signaling/data. Other

Figure 8. This application of the UNITE IC shows it with an AT&T T7500 codec connected to the B1 channel and an AT&T T7111 HDLC formatter connected to the B2 channel.



framing and synchronization are added, after which the data stream is transmitted to the NT.

With this hardware configuration, voice could also be transmitted and received over B2 by requesting the UNITE IC to internally exchange B1 and B2 information.

Programmable clock and strobe signals are automatically configured for the devices shown, during power-up and reset. CKCOD is programmed as a 2.048-MHz clock. FSEB1 is programmed as a strobe to meet the timing requirements of the AT&T T7500 codec. MCKB1 is programmed as a continuous 192-kHz clock. Alternatively, MCKB1 may be programmed as a clock for B1 data. FSEB1 (and FSEB2 as well) can be programmed as an enable signal, which is active for the duration of the B1(B2) time slot. The exact timing of FSEB1 (FSEB2) is also programmable.

Terminal control logic can be very simple. Minimally, this would include a microprocessor of some sort. It might also include memory, address decoding logic, and an interrupt controller. Terminal design may be simplified by using the 6.144-MHz UNITE output as the system clock. The on-chip power-up reset is also available for system use.

Summary

The UNITE IC is easy to use, and its cost-effective features are versatile enough to allow it to fit in virtually any system. Strobes and clocks are programmable so that the IC can be interfaced easily to many data handling devices, such as codecs and serial communication controllers. Separate pins are provided for B-channel data that are to be transmitted to the network. Separate address and data buses and a programmable interrupt polarity make the UNITE IC compatible with most microprocessors. All interrupt conditions are selectively maskable.

There are other features that also make the UNITE chip attractive to system designers. Sixteen-byte buffers in the HDLC formatter provide efficient processing of D-channel data in both directions of transmission. A sophisticated queue design maximizes the throughput for D-channel information.

A common codec master clock signal of 2.048-MHz is provided and all clocks and strobes are synchronized to it. Carefully placed power and ground pins minimize noise problems. These system-level assets should reduce development times and produce better products.

References

1. "Integrated Services Digital Network," *AT&T Technical Journal*, Vol. 65, No. 1, January/February 1986, pp. 1-88.
2. CCITT Study Group XVIII I Series Recommendation I.430, Draft Specification, 1986.

(Manuscript received October 15, 1986)