THE TECHNOLOGY OF INTERCONNECTION

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The key role of interconnection technology is to make it possible for designers to exploit fully new and developing device and manufacturing technologies such as very large scale integration (VLSI) and surface mount technology to produce feature- and function-rich systems at lower cost, in smaller volumes with shorter design intervals. Interconnection media, assembly technology, and computer-aided engineering and design (CAE/D) tools have been developed in concert with VLSI and have permitted designers to make about a ten-fold reduction in the cost of system interconnections and a ten-fold improvement in system reliability in the decade 1976–1986. Application of the Fastech® interconnection system, together with CAE/D, has contributed to reducing design interval by a factor of three and to increasing designer productivity five-fold in this period. These improvements were obtained by closely coupling development of interconnection technology to device development, systems design, and manufacturing requirements.

Origin of Interconnection Technology

What is now called interconnection technology had its origin in significant advances made during the 1960s in the materials and processes used to interconnect electronic components. Key developments were printed wiring technology, automated assembly processes (such as wave soldering and numerically controlled wiring), thin-film hybrid circuits, and highly reliable separable connectors. These technologies, when applied together, allowed a major step forward in the architecture of electronic systems. It became possible to build batch-fabricated, inexpensive, reliable, and maintainable electronic subsystems. Much progress has been made in the technological foundations of interconnec-

Focus on Interconnections

This issue of the *AT&T Technical Journal* examines the technology of electronic interconnections. Hoover, Harrod, and Cohen lead off with an overview and review the origins of the field, the forces that are driving advances in the technology, and the relationships among interconnection design, device development, system design, and manufacturing.

In "Fundamental Interconnection Issues," Franzon et al. analyze the growing dominance of interconnections in determining system performance and cost. Higher system performance, they predict, will be obtained by focusing advanced technology development on system-level, multichip packaging and interconnection. In addition, just as device technologies have reduced the intrinsic power-delay products of devices, so too will system macrointegration, through new technologies and architectures, seek lower intrinsic interconnection switching energy.

In "Interconnection Media," Giffels et al. describe the media used at each level in the interconnection hierarchy from integrated circuit package to circuit pack. They examine the effects of new demands on each level, and discuss the developments that will provide the new capabilities.

In "Interconnection System Requirements and Modeling," Pinnel and Knausenberger explore traditional levels of interconnection from integrated circuit chip packages to frames. They show how the interconnection levels relate and how they must be improved simultaneously to achieve full performance and cost benefits.

In "Computer-Aided Engineering and Design for Interconnection Technology," Rosenthal and Dishman describe the application of vertically integrated design and manufacturing elements to the complete hierarchy of interconnection levels—the integrated circuit package, circuit pack, backplane, multibackplane unit, frame, and system.

In "Reliability Evaluation of Interconnection Products," Cohen et al. describe several new reliability evaluation methods and tools and give specific examples of how they are used to design reliability into new interconnection products. The methods include early identification of risk sites and stress factors, design of failure-mode-specific test vehicles, and efficient execution of accelerated test programs through computer-controlled data-acquisition systems.

Finally, in "Systems Packaging," Ambekar et al. discuss the Fastech® integrated packaging system, which gives AT&T designers standardized packaging options that shorten the design process and provide economies of scale. The Fastech system has been used in AT&T products, the authors note, since the mid-1970s and will continue to be used well into the 1990s.

tions since the early 1960s to improve density, reliability, performance, and cost. However, now as then, many of the fundamental properties of electronic systems are determined by the characteristics of the interconnection technologies employed.

Driving Forces

Interconnection technology is shaped by three external driving forces: silicon integrated circuit technology, automated systems for assembly and testing, and the fundamental architectures of electronic systems. Most of the "electronic functionality" of current systems is embedded in silicon integrated circuits (ICs). The connections between silicon ICs are provided by interconnection media which must be closely matched to the characteristics of the silicon ICs. Some important parameters are density (number of connections per unit area), connection lengths, characteristic impedances, inductances, and propagation speeds. These parameters must all be tailored to the particular types of ICs being interconnected.

Automated assembly and testing is required for cost-effective and high-quality manufacture of electronic systems. These manufacturing technologies impose requirements on interconnections which often must be traded against system performance requirements. For example, to optimize silicon IC performance, the size of all interconnections must be minimized. To optimize manufacturing, interconnections must be large enough to allow reliable and high-yield assembly operations, to provide test access, and to allow repair and maintenance.

Finally, system architectures shape interconnection needs. In telecommunication systems, there are many distinct classes of subsystems, each with its own interconnection requirements. For example, systems are often controlled by a central high-performance computer where high-speed interconnections are paramount—the switches that do the work of interconnecting telephone circuits demand high-density packaging and well-controlled impedances. The line interfaces are slower-speed circuits which are built in large numbers and thus require low-cost, high-quality manufacture.

These three driving forces are rapidly evolving, and consequently, interconnection technology is also evolving. System designers continue to find that the most cost-effective and highest-performance systems minimize the numbers of plug-in circuit cards by increasing the amount of circuitry per card. The net effect is to increase the packaging density of the system. (An important exception to this trend is small, single-board systems with moderate performance requirements where other factors—low cost, simplicity, ease of change—dominate.)

The increase in density is primarily paced by silicon technology, where unprecedented gains in scale of integration have occurred. The number of components per silicon circuit has increased more than 100-fold over the past 10 years. Increasing scale of integration at the chip level increases the number of external connections which the chip package must provide. (This relationship will be discussed in detail in other articles in this issue.)

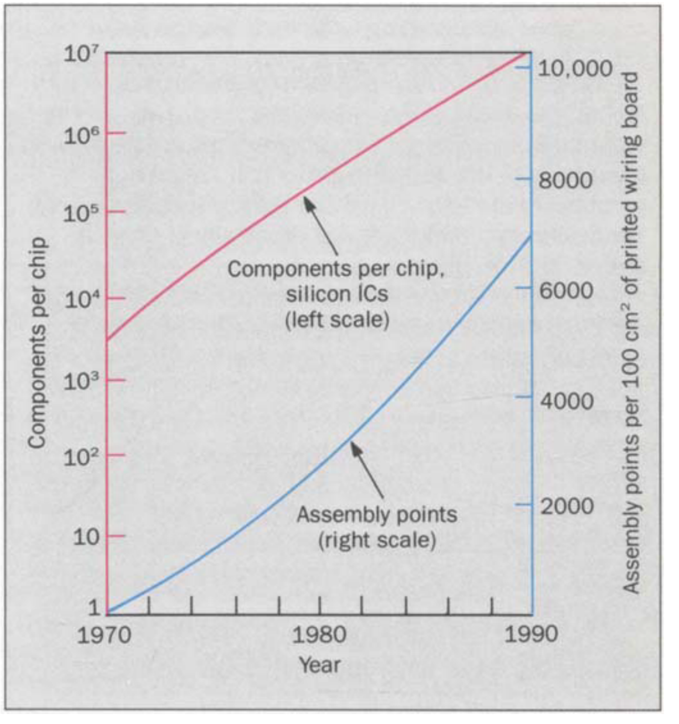

Figure 1. The history of silicon integrated circuit scale of integration and its effect on interconnection density.

The higher performance and higher input/output requirements of current-generation chips have helped establish a fundamental change in assembly technology—the transition from wave-soldered, through-hole assembly to higher density surface-mount technology. This change in assembly method will impact all components. Devices no longer will have wire-like leads that are soldered into holes in printed wiring boards with minimum spaces of 100 mils. Surface-mount assemblies achieve higher interconnection densities by reducing the separation between device leads down to 25 mils and by eliminating space-consuming drilled holes. Many surface-mount assemblies are in manufacture,

Table I. Interconnection Limits for Telecommunication Systems

	Typical limits for plug-in circuit packs			
Pacing technologies	**1970**	**1978**	**1986**	**Early 1990s**
Circuit pack size, in^2	50	100	200	200
Layers of printed wiring	2	6	8	14
Line widths, mils	25	7	6	4
Connections (number of connected device terminals)	100	2000	9000	16,000
External input/outputs	80	300	600	2000
Logic gates	10^2	10^4	10^5	10^6

but the transition to widespread use will take time because of the enormous task of converting tens of thousands of electronic component types to surface-mount configurations.

Until recently, system speeds have not been seriously limited by the bandwidth available in printed wiring, hybrid circuits, or backplane connectors. Emerging systems, such as high-speed switches and fiber-optic communications systems, will require interconnections with controlled characteristic impedance, increased connector bandwidth, and improved control of crosstalk.

All of these design trends lead to increased density of the interconnection media. Product quality and reliability are specified for today's products, and these specifications must be met to realize product cost and marketability. For designs using high scale of integration and surface-mount technology, system hardware reliability and quality are determined primarily by the reliability of interconnect media and assembly processes. Increased density requires that more points located closer together be interconnected on each board, and this leads to new and more rigorous requirements for reliable assembly. For example, circuit packs using surface-mount technology usually go through several thermal treatments in assembly; thus solder surfaces and board cover coats must be carefully controlled to get the required level of product reliability. This imposes special requirements on both the media and assembly processes to produce a reliable product.

The most stringent quality and reliability requirements on interconnection media and assembly processes derive from requirements for economical manufacture. Today's dense circuit packs and hybrid integrated circuits are assembled on automated lines. For these lines to be efficient, first-pass circuit pack yield must be very high—typically greater than 99 percent. A simple calculation shows that the quality of each component on a pack with 200 components must exceed 0.99995 to get a first-pass yield of 0.99. Such a pack typically has 5000 or more points that must be reliably joined. While it is inappropriate to calculate an assembly reliability requirement per joint by the same means used for components, it is nevertheless clear that assembly process quality and reliability must be very high.

Metrics

It is important to understand the relationships between scale of integration and the requirements on interconnection density. Figure 1 shows the well known history of scale of integration for silicon integrated circuits. For the leading-edge technology, the maximum number of components per chip increases by a factor of 100 per decade. Circuits are usually described in terms of numbers of gates. For a given technology, the number of gates is proportional to the number of components. The number of pinouts per chip is roughly proportional to the square root of the number of gates for random logic and to a lower power for functional designs.

As the scale of integration and number of devices

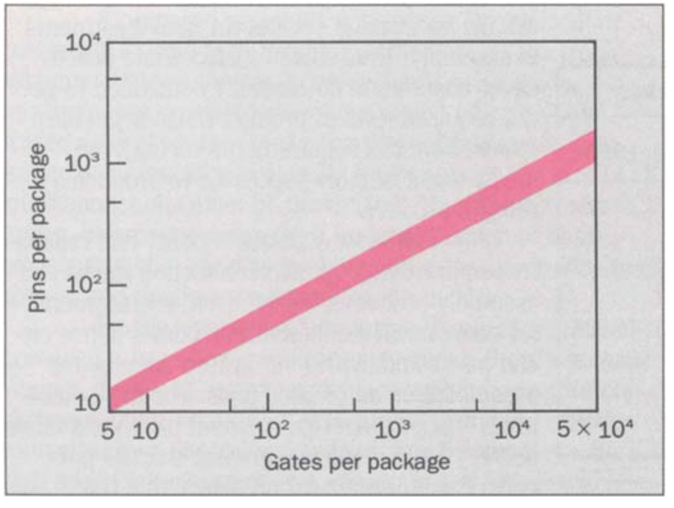

Figure 2. Pins per package versus gates per package.

per pack increase, the number of pins interconnected on each pack increases. Figure 1 also shows data, derived from our computer-aided design (CAD) systems, on how the number of interconnections per 100 square inches of circuit pack has increased under this impetus, with a projection to 1990.

Table I shows the effects over time of driving forces on the size and complexity of plug-in circuit packs. Forward-looking systems built in 1970 used small circuit packs (50 in^2) containing about 100 logic gates. By 1986, the typical packs in forward-looking systems had grown in area by 4 times, in interconnection layers by 4 times, in interconnections (connected device terminals) by 90 times, and in number of logic gates by 1000 times. As the projection for the early 1990s shows, the evolutionary pace is not expected to slow.

System Design Process

The interconnection design process is driven by system design and partitioning choices, so it is necessary to start with an understanding of how system design is done. In design, there are trade-offs between the cost and performance of interconnections on the one hand, and device choices, architecture, and the time to get the design into manufacture and onto the market on the other hand.

System design begins with the development of an electrical circuit which, with software or firmware, provides the required features and functions at a target cost. Other system characteristics such as the architecture, the integrated circuit technology and scale of integration (e.g., MOS technology and 1.75-micron geometry), and quality and reliability are also specified. The next step is to decompose or partition the electrical circuit into blocks to be realized in new or existing integrated circuits (ICs), hybrid integrated circuits (HICs), and circuit packs in such a way as to meet performance requirements and to minimize the total cost of devices, interconnections, assembly, and test.

Partitioning is driven by many factors. In channel banks and line circuits for switching systems, the functional units are defined by strategies on modularity and system provisioning, or particular features requirements. The design goal is to realize a functional unit at lowest cost. In other cases, the designer's goal is to partition a large circuit onto chips, hybrid integrated circuits, circuit packs, and backplanes to maximize system performance. This process is guided by the designer's insight on how system performance and cost vary with IC scale of integration. (Analytical tools to help in system decomposition or synthesis are just beginning to appear.) This complex task must also take into account the time available to get the system to market, since IC costs fall and scale of integration increases rapidly with time.

Rent's Rule

Rent's rule is a relationship which can be used to show how interconnections are distributed among chips, HICs, circuit packs, and backplanes as a function of the number of gates included in each. For random logic, Rent's rule specifies that p, the number of pins per package or partition, is a function of the number of gates g in the

Table II. Distribution of Interconnection for 10^5-Gate Circuit, Random Logic

	Gates per IC		
Interconnections	**100**	**1000**	**10,000**
On silicon	100,000	187,400	196,000
On printed wiring	40,000	12,600	4000

package according to the equation $p = kg^a$, where k is in the range from 3 to 6 and a is typically in the range from 0.45 to 0.55. This rule was empirically developed by Rent at IBM. The half-power dependency can be shown to apply for partitions of a randomly interconnected circuit with an exponential distribution of interconnection lengths.

Rent's relationship has been found to apply remarkably well over a very large range of circuit sizes, as shown in Figure 2. Given this fact and the cost and reliability of each type of interconnection, it is possible to demonstrate the savings in cost and improvements in reliability attainable by increasing IC scale of integration.

Fundamental Trade-offs

Interconnection Costs. We now demonstrate the effects of increasing scale of integration on cost and reliability. The distributions of interconnections obtained by partitioning a circuit with 10^5 gates into ICs with 100, 1000, and 10,000 gates per chip, obtained by applying Rent's rule (with $k = 4$, $a = 0.5$), are as shown in Table II.

Note in the table that increasing IC scale of integration by a factor of 100 moves 90 percent of the external interconnections onto silicon. Increasing the scale of integration requires denser interconnection media that are more expensive per unit area, but which may lower the total interconnection cost, since the total number of external interconnections decreases. Figure 3 provides the data needed for the cost trade-off. It shows that interconnections on silicon are one to two orders of magnitude

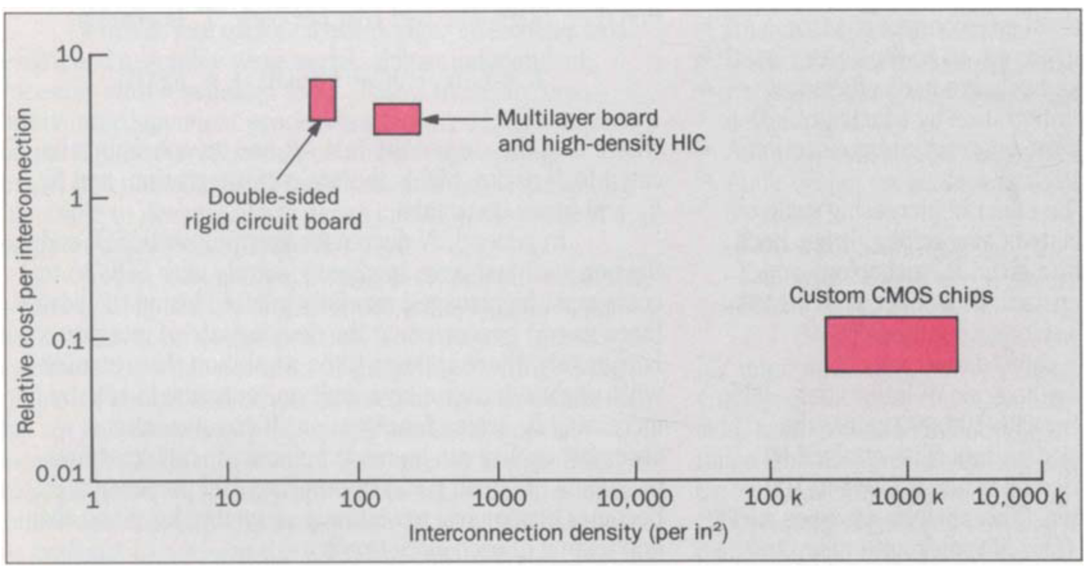

Figure 3. Data for a cost trade-off. Cost per interconnection decreases greatly as interconnections are transferred to silicon, here represented by complementary metal-oxide-semiconductor (CMOS) chips.

Table III. Effect of Increasing Scale of Integration on System Reliability

	Gates per IC		
	100	1000	10,000
Number of ICs	1,000	100	10
IC FIT count, total	50,000	5,000	500
Numer of external interconnections	40,000	12,600	4,000
Interconnection FIT count, total	4,000	750	200
System FIT count	54,000	5,750	700

cheaper than those on printed wiring boards or HICs, so the cost for the interconnections transferred onto silicon is strongly reduced. Figure 3 also shows that the *cost per interconnection* for the external interconnections that remain may decrease slightly as we go to the denser multilayer or hybrid media, if the media are used efficiently. Hence, increasing scale of integration by a factor of 100 can eliminate 90 percent of the external interconnections and 90 percent of interconnection cost.

System Reliability. The effect of increasing scale of integration on circuit reliability is also strong. It has been found that IC FIT count, for a given IC technology and manufacturer, is roughly constant, independent of the number of gates per chip. (FIT stands for failures in 10^9 hours.) Hence, system FIT count due to devices is reduced in inverse proportion to scale of integration. Table III summarizes, for a system with 100,000 gates, the effects of interconnection system reliability attained by increasing scale of integration by factors of 10 and 100 from a level of 100 gates/chip. This analysis assumes a FIT count of 50 for all the ICs. This is appropriate today and conservative for the earlier systems. FIT counts for printed wiring products, appropriate to the board types required at the various levels of integration, have been used.

It must be kept in mind that this is an idealized example where a given circuit is partitioned into uniform-sized chips, whereas in practice we have a mix of chips with varying scales of integration, surface-mounted devices, and so forth. Few systems manage to get all of the circuits onto a few VLSI chips, and a large circuit pack typically uses 50 or more low-scale-of-integration chips and components. When the FIT count for 50 such components is added to that for the interconnection and VLSI devices, the total is in the range of 3000 to 5000 FITs.

Test Cost. As we have shown, improvements in system quality and reliability are obtained by increasing scale of integration and packaging more components per circuit pack. However, as the number of gates per circuit pack is increased, circuit pack complexity increases and the number of packs to be tested decreases. The capital cost of circuit pack test equipment is large and must be amortized over the number of packs in a given generation of production (i.e., SOI). The test cost per pack, T, is given by

$$T = C/N + K = k_1(\text{SOI}) + k_2 f(\text{SOI})$$

where C is the cost of the test set and its operation allocated to N packs, SOI is the scale of integration, and K, k_1, and k_2 are constants.

In general, N decreases inversely with SOI and k_2, the per pack test cost, increases sharply with SOI, so test costs must be managed carefully to avoid losing the advantages gained by increasing the device scale of integration. Fortunately, there appears to be a solution that removes what might otherwise be a limit on reduction in cost by increasing IC scale of integration. If component and assembly quality can be made sufficiently high that first-pass yield of circuit packs approaches 100 percent, it becomes economical to test only at system level and abandon testing of each circuit pack.

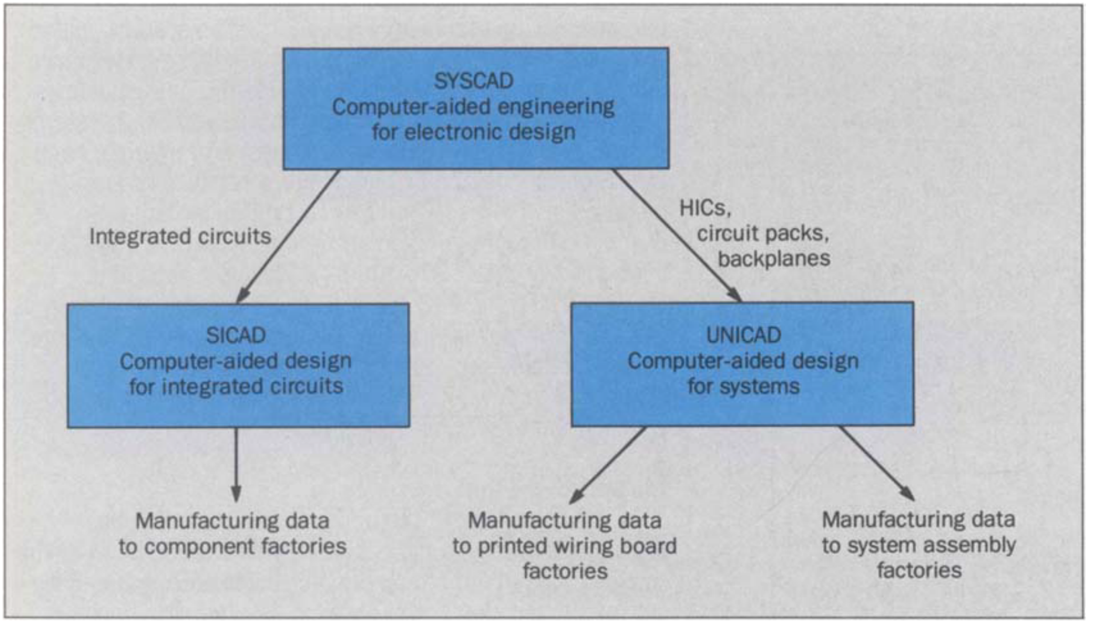

Figure 4. Functions and flow of information in computer-aided systems.

Interconnection Design Process

Fifteen years ago, circuit design, interconnection design, and assembly were serial, almost independent, processes with few design tools. Today, these are completely interdependent processes supported by a complete computer-based system that combines engineering, design, and manufacturing functions. Indeed, it would be impossible to design today's dense circuit packs without a computer-aided design system.

Today, cost and performance considerations of the various system partitioning schemes are evaluated in parallel in the system design process. The designer must determine the characteristics of the printed wiring (e.g., number of layers) and connectors required to assemble the chip set and the other devices, and must make device placements taking into account heat release and air flow, crosstalk between wiring paths and in connectors, orientation for solderability, and many other factors. CAE/D tools are available to perform the following functions:

- Simulate design for functionality and margins
- Analyze design for testability
- Determine thermal performance
- Estimate interconnection density required (layers, design rules)
- Analyze crosstalk performance of proposed routing
- Audit design for adherance to design for manufacturability rules:
  –Path width/clearance
  –Part orientation
  –Solder mask design.

CAE/D systems requirements are driven by the IC, interconnection, and manufacturing technologies employed. These systems, which started as layout design aids, have expanded in both directions and now span the range from design capture and simulation to programs that automatically drive printed wiring board manufacture, choose components and download instructions to insertion machines, and drive machines that test completed circuit

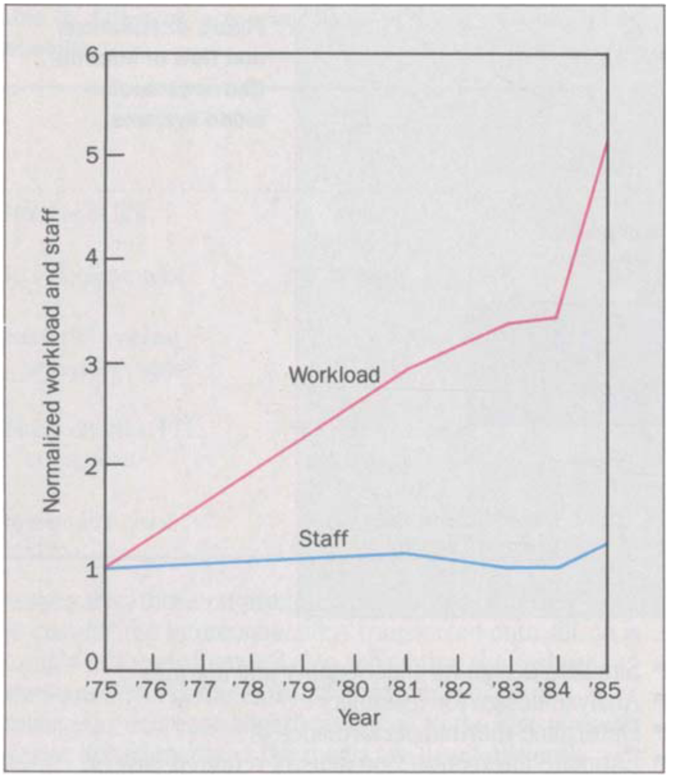

Figure 5. Workload and staff as measures of productivity.

packs. The functions and flow of information in these systems are shown in Figure 4.

Standard System Packaging

As previous sections have outlined, interconnection technology spans a wide variety of disciplines, ranging from basic materials technologies to computer-aided interconnection design. To provide optimal benefits to system designers, all of the parameters of interconnection technology must be treated in an integrated fashion to allow appropriate technology trade-offs to be made. Within AT&T, an integrated, standardized packaging system has been established as a framework for the development of interconnection technology elements. The system, called the Fastech® integrated electronic packaging system, provides a full set of CAE/D tools, standards, and guidelines as well as hardware for packaging and assembling systems. In general, these systems are composed of multiple circuit packs interconnected by one or more backplanes and mounted in shelves. The Fastech system, which is described in more detail in a subsequent article,[1] has been used in more than 150 systems and is now applied in almost all large new AT&T systems. Adopting its standards leads to economy of scale in printed wiring board and connector manufacture, speeds development, assures adherence to development intervals, and makes a major contribution to system reliability.

The Role of the Physical Designer

The scope of the physical designer's job has greatly increased over the past 10 years. In addition to the complex jobs of interconnections, thermal design, and layout mentioned above, the physical designer has become responsible for much of the product realization process. Thus, the physical designer usually has the key responsibility for system hardware cost, for ensuring the use of standard components, for testability, for manufacturability, and for introduction to production and manufacture. The job requires interactions with the system designers, software and firmware developers, component suppliers, drafting and documentation, and the manufacturing organizations.

The combination of integrated CAE/D tools and the Fastech packaging system has led to remarkable increases in physical design productivity over this period. Figure 5 shows the design workload, measured by a number of circuit pack designs times the terminals interconnected per pack, versus the size of the design engineering staff. Note that there is a five-fold increase in designer productivity over the period shown. This model does not attempt to measure the additional work required because of additional constraints and increased complexity and therefore understates the workload and the productivity gain.

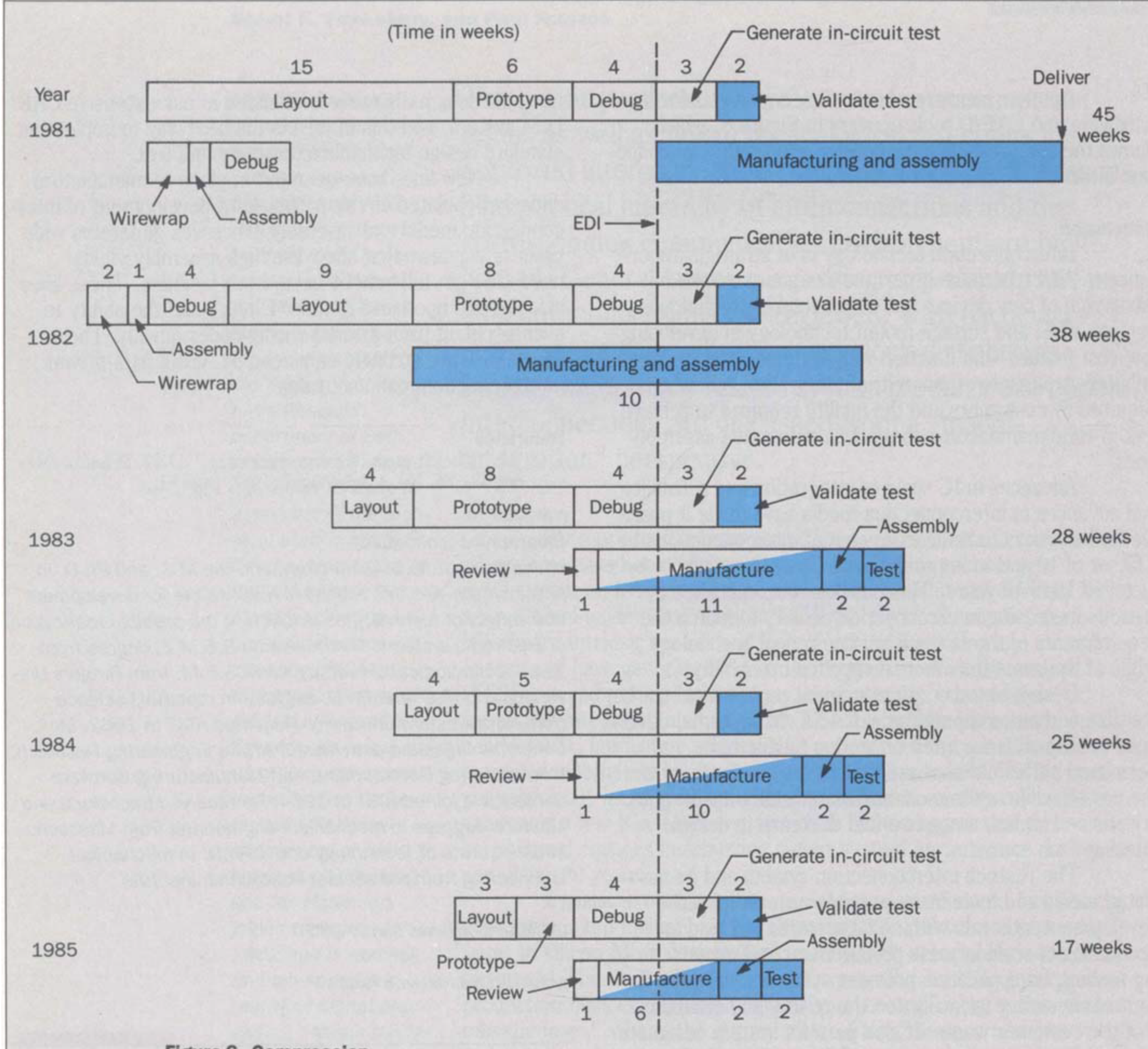

Figure 6. Compression of design and product introduction intervals.

Another measure of the efficiency of standardized hardware and CAE/D tools appears in Figure 6, which shows the compression of the design and product introduction intervals at one major location.

Conclusion

Interconnection technology is of strategic importance to AT&T because it permits designers to take full advantage of new devices and manufacturing techniques such as VLSI and surface-mount technology in developing low-cost feature- and function-rich systems. It also contributes strongly to attainment of the system reliability required by customers and the quality required to achieve just-in-time manufacture on modern automated assembly lines.

Advances in IC scale of integration and reliability and advances in interconnection media have made it possible for designers to reduce the cost of interconnections by a factor of 10 and to improve the circuit total reliability by a factor of 10 in 10 years. This has been accomplished by steadily increasing interconnection density to match the requirements of the ICs and surface-mount technology while at the same time increasing circuit reliability.

Design of today's dense circuit packs would not be possible without computer aids. CAE/D/M systems, developed in step with the interconnection media, have permitted a five-fold increase in designer productivity over the period while accommodating many additional design criteria and audits, and a two-fold decrease in design interval.

The Fastech interconnection system and its associated media and tools make possible reduced product development intervals with no false starts and lead to economies of scale in parts procurement and manufacturing tooling. Its application provides system developers the control necessary to guarantee the quality and reliability that the customer wants. It also permits system designers to meet requirements for compatibility with modern automated manufacturing. A subtle but important point is that the interconnection technology program makes possible a common design discipline embedded in our extensive CAE/D/M system, and this in turn is the best way to implement standard design for manufacturability and test.

New lines have been put in place to manufacture densely populated circuit packs. Joint development of interconnection media and assembly processes generates wide process windows that allow the high assembly yields needed to get full benefit from these facilities. These lines also depend upon just-in-time delivery and the ability to change circuit pack printed wiring codes quickly. These capabilities are strongly enhanced by AT&T data-driven interconnection manufacturing.

Reference

1. S. M. Ambekar et al., "System Packaging," *AT&T Technical Journal*, Vol. 66, No. 4, July/August 1987, page 81.

Biographies (continued)

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