INTERCONNECTION MEDIA

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The growth of scale of integration in semiconductors, coupled with the increasing speed and complexity of electronic systems, is placing demands in terms of packaging density and speed on the capabilities of the interconnections. This paper separates the interconnection system into a hierarchy of levels—from IC package to circuit pack—and describes the media used at each level in the hierarchy. It also describes the effect of the new demands on each level and discusses the developments to provide the required new capabilities.

Perspective

With the continuing increases that occur in the silicon scale of integration (SOI) and operating speeds used in electronic systems, the interconnections play an ever more important role in determining a system's ultimate capabilities. (Panel 1 defines all acronyms used in this paper.) In this issue's introductory paper,[1] Hoover describes the migration of interconnections toward the chip because of increased SOI. Offsetting this migration is the tendency of system complexity to grow as designers take advantage of the increased reliability and functional possibilities opened up by higher integration. As a result, the demands on the interconnection media increase with time at every level of interconnection in leading-edge systems.

In the quest for ultimate packaging density and system performance, the complete integration of a system function on a single silicon wafer is a goal that remains to be achieved. Among the formidable problems have been yield and power dissipation. An alternate approach is a new packaging technology, called advanced VLSI packaging (AVP),[2] that is being developed at AT&T Bell Laboratories. (VLSI stands for very-large-scale integration.)

With AVP, unpackaged chips are mounted directly on a silicon wafer substrate that can interconnect many chips without incurring the limits on operating speed imposed by more conventional system-packaging technology. Because AVP uses polymer dielectric layers, copper conductors, and short interconnecting paths on the silicon

Panel 1. Acronyms in This Paper

AVP	advanced VLSI packaging
BMPM	board-mounted power module
CAD	computer-aided design
CBIC	complementary bipolar integrated circuit
CC	chip carrier
CCB	controlled collapse bonding
CMOS	complementary metal-oxide semiconductor
DIP	dual in-line package
FEA	finite-element analysis
HIC	hybrid integrated circuit
HPC	high-performance connector
I/O	input/output
JEDEC	Joint Electron Device Engineering Council
LDCC	leaded ceramic chip carrier
LLCC	leadless ceramic chip carrier
MAC	multifiber array connector
MLB	multilayer board
PGA	pin-grid array
PLCC	leaded plastic chip carrier
PWB	printed-wiring board
RTV	room-temperature vulcanizing
SEM	standard electronic module
SIP	single in-line package
SM	surface mount
SO	small outline
SOI	scale of integration
TAB	tape automated bonding
TGU	terminal grounding unit
TH	through hole
VLSI	very-large-scale integration

substrate, it offers the possibility of reducing system size by a factor of seven and power dissipation by 30 percent, while operating speed can be three times higher.

The subject of this paper, however, is the more typical case of large electronic systems that exhibit a hierarchy of interconnection levels.[3] The lowest level, on the silicon IC (integrated circuit) itself, provides all the internal connections between elements and organizes the external connections into regular arrays. Usually, the IC chip is packaged to provide protection and easy attachment to the next level of interconnection.

Generally, the packaged chip is mounted—with other components—directly on the printed wiring board (PWB). But often, an intermediate level of interconnection is useful, either to gain increased density or provide a smaller testable unit. This level of interconnection may be either on a ceramic module, a small PWB, or an AVP substrate.

One could mount packaged single chips directly on the board or use combinations of chips, modules, and other components. Either way, the trends in device packaging impose increasing demands on the interconnection capabilities of the PWB.

Usually, the PWB is part of a larger functional system that uses a hardware packaging system, such as the Fastech® electronic packaging system.[3] To simplify system assembly and repair, the PWB is connectorized so it can be readily plugged in or unplugged when necessary. The performance needs that drive the demands on the printed wiring also drive the connector requirements to higher pin counts and higher speed capability. In addition, the increasing application of photonics has created a need for pluggable optical connections.

Device Packages

Because of the recent proliferation of package types—both for through-hole (TH) and surface mounting (SM) to PWBs, a wide variety of package types now can be selected for semiconductor devices. Figure 1 presents some of the more popular package types and their range of available I/O (input/output) pins.

The through-hole types, which cover the I/O range from 8 through 300 pins, include the older dual in-line package (DIP) and the newer pin-grid array (PGA). The availability of new SM packages has expanded greatly,

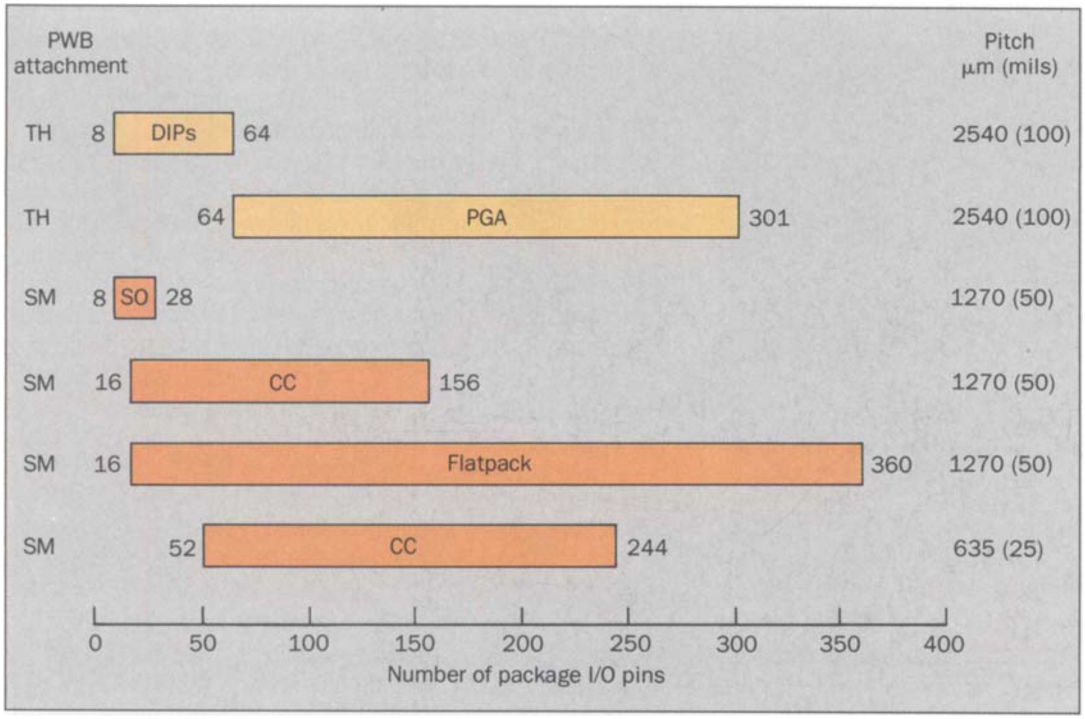


Figure 1. Input/output (I/O) ranges for current types of semiconductor packages. CC = chip carrier; PGA = pin-grid array; SM = surface mount; SO = small outline; TH = through hole.

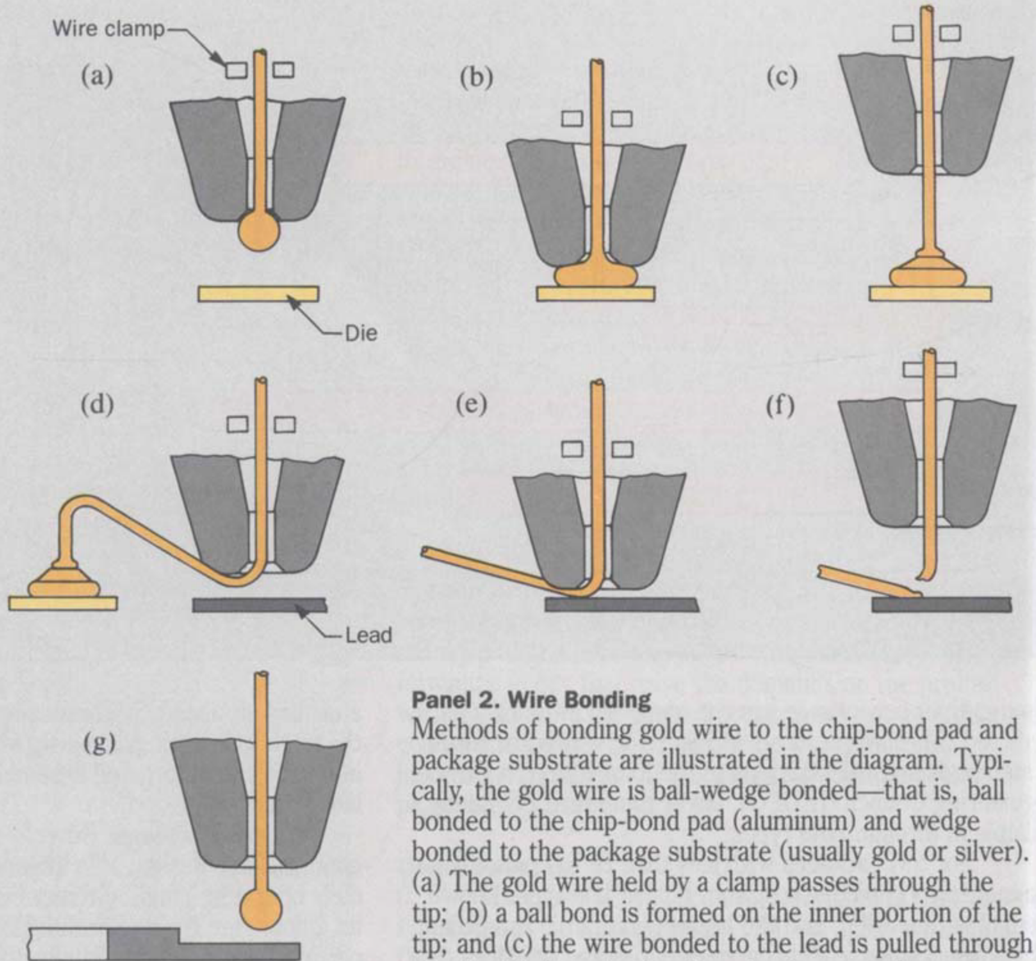
although their acceptance has not advanced as quickly as predicted. The SM packages in Figure 1, which are based on standards and registrations of the Joint Electron Device Engineering Council (JEDEC), cover the entire I/O range available in through-hole types.

For SM packages with less than 28 I/O pins, the designer has a choice of a plastic, dual in-line type, known as small outline (SO), and the hermetic ceramic and plastic quad types, known as chip carriers (CCs) and flatpacks. CC packages are available in leaded plastic (PLCC) and leaded ceramic (LDCC) for mounting to PWBs, or leadless ceramic (LLCC) for socketing or mounting to boards with a matching thermal coefficient of expansion (TCE). Leads may be of different geometric form ("J" and gull wing) and pitch (1.27 and 0.635 mm, or 50 and 25 mils).

Packages designed for high performance are ceramic based, usually hermetically sealed. Low cost drives the need for plastic packages, which are typically handled in batches on automated assembly equipment to minimize labor costs.

Package Design. Several considerations enter into good package design. It is important to keep the silicon die's operating-junction temperature low enough to prevent its failure rate from exceeding the acceptable limit for a particular application. Usually, this requires considering not only the packaged device, but also its environment—which includes such factors as ambient temperature, board power dissipation, air flow velocity, and heat sinking.

With the increasing speed of today's circuits and their potentially reduced noise margins, package design has become a more important factor in electrical performance. Among the package parameters that affect



Panel 2. Wire Bonding
Methods of bonding gold wire to the chip-bond pad and package substrate are illustrated in the diagram. Typically, the gold wire is ball-wedge bonded—that is, ball bonded to the chip-bond pad (aluminum) and wedge bonded to the package substrate (usually gold or silver). (a) The gold wire held by a clamp passes through the tip; (b) a ball bond is formed on the inner portion of the tip; and (c) the wire bonded to the lead is pulled through the tip. (d) A wedge bond can be done anywhere on a 360-degree arc around the ball bond, (e) using the outer portion of the tip. (f) The clamp closes, breaks the wire, and prepares the wire tail for (g) forming the new ball with either a hydrogen flame or electronic spark.

performance are the resistance and inductance of power and ground pins, inductance and capacitance of signal leads, and impedance matching.

As the size of semiconductor chips increases, the mismatch in the TCE of materials that are used in package construction is a potential cause of failure. Analysts have developed sophisticated stress models and introduced computer aids, such as finite-element analysis, to increase their ability to characterize thermal stresses and deformations throughout the plastic package. With these tools, one can quickly evaluate the effect of design changes on stress-related failure.

Chip Connection. In packaging, chip connection consists of two steps:

1. The back of the die is attached mechanically and sometimes electrically to an appropriate mounting surface, such as a ceramic substrate, multilayer ceramic-package piece part, or metal lead frame. The two common die-bonding methods are hard solders (typically, gold-silicon eutectic) and polymers (epoxy and polyimide). Silver-filled epoxy adhesives are of major interest today as die-bond materials. The silver filler (typically flakes) makes the epoxy both electrically conductive—for low resistance between the die and the substrate—and thermally conductive—to allow a good thermal path between the die and the rest of the package.
2. The bond pads on the circuit side of the die are connected electrically to the package. The three common methods of connecting to the chip-bond pads are: wire bonding (see Panel 2); tape automated bonding (TAB); and "flip-chip" solder bonding, which is also called controlled collapse bonding (CCB). All three are used extensively for all levels of chip complexity up to VLSI.

Package Fabrication Technologies. Generally, single-chip packages are based on either refractory ceramic technology or metal lead frames and molded plastics. Ceramic packages are usually used for state-of-the-art devices that require maximum reliability or many signal, power, ground,

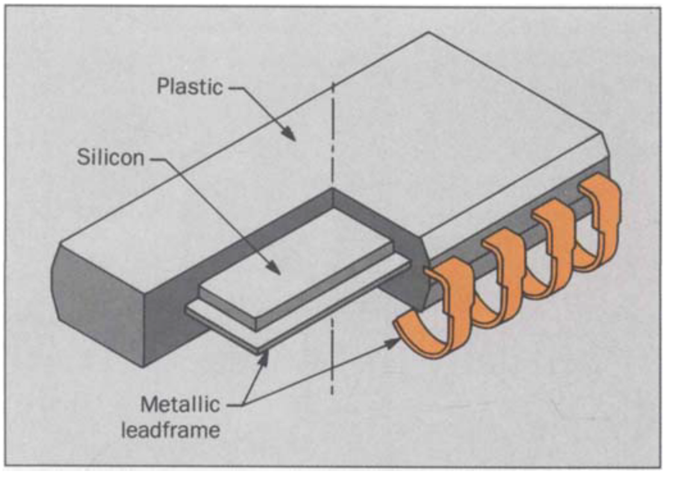


Figure 2. Cross section of a plastic small-outline package.

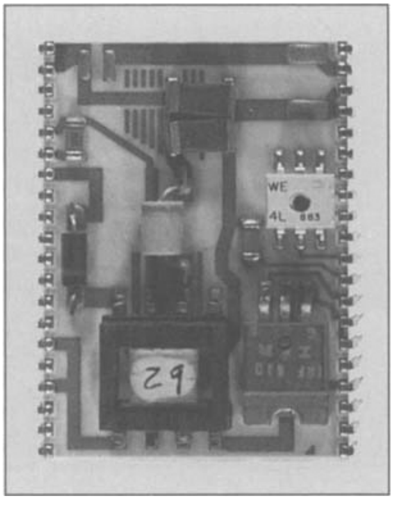
and sealing layers. Plastic packaging is usually better for more mature products where cost is paramount and hermeticity is not required.

Until recently, plastic had implied lower reliability. Now, however, plastic technology has improved and is highly reliable with proper process control. Figure 2 shows a cross section of a plastic, small-outline type package. The polymer used most commonly for IC packaging is epoxy.

Novolac epoxies generally are preferred because their higher functionality imparts better heat resistance. Fillers are added to the resin to improve its mechanical strength and reduce its TCE, thus reducing its shrinkage after molding.

Future Trends in Packages. Undoubtedly, the pin counts of packages will continue to increase with increasing silicon capability. Alumina-ceramic packages will dominate the high-performance VLSI packaging technology until factors—such as its high dielectric constant, modest thermal conductivity, or cost—force a change to

Figure 3. The board-mounted power module, a thick-film hybrid integrated circuit.



other contending materials. The need for higher packing density on the PWB level will drive the package design toward smaller lead pitches [≤ 0.635 mm (25 mils)].

If chip integration keeps pace with decreasing feature size, today's chip interconnection technologies, especially wire bonding, will be challenged by I/O counts above 200. TAB and flip-chip bonding will be revisited to assess their future in VLSI packaging. Both technologies, especially TAB with its pretestability features, lend themselves to hybrids. But flip-chip bonding has the advantage of a very low inductance connection to the package and the capability for a high-density, area-array interconnection. It is the method of choice in the AVP technology.

Intermediate Level Interconnections

In the most common system packaging, the IC package is mounted directly to a PWB using through-hole leads or surface-mount technology. The chip itself occupies only a small fraction of the area of the package, whose size is governed primarily by the required lead pitch for attachment to the PWB. Often, a better approach uses an intermediate level of interconnection on a separate substrate of ceramic, epoxy-glass, or—for AVP—silicon.

The resulting hybrid integrated circuit (HIC) or module is intermediate between a single-chip package and a PWB in three ways.

- The HIC's overall dimensions are normally 1 to 10 cm, generally larger than a single-chip package but smaller than a PWB.
- A HIC is intermediate in function, able to contain more than one chip but normally not as many as a PWB. The ability to test an intermediate module is a significant advantage when the PWB might contain hundreds of ICs.
- The HIC's feature dimensions are intermediate. On a ceramic hybrid circuit, for example, 0.051-cm (2-mil) line widths and spaces are standard. As a result, a higher packing density is possible on the substrate,[4] which eventually means fewer PWBs, backplanes, and cabinets are needed for a given function.

Ceramic Hybrids. Techniques for fabricating components on ceramic hybrids are divided into two groups:

- *Thin-film processes* consist mainly of blanket coating of thin metal layers in a vacuum system, followed by photolithographic pattern generation. Besides conductors, thin-film processes can be used to create resistors and capacitors based on tantalum deposition.
- *Thick-film processes* use screen printing to deposit and pattern material, followed by firing to establish adhesion and burn off unwanted volatile material.

Using these processes, we can form conductors and resistors or deposit dielectric layers for thick-film capacitors or multilayer circuits.

Once fabricated, the value of most hybrid components cannot be changed. However, thin- and thick-film resistors can be trimmed with lasers to increase their value. A laser beam, under software control, can selectively vaporize a thin line of resistor material to increase the current path, thus increasing the resistance value. Circuits on an operating HIC can thus be tuned *in situ* with a precision not otherwise attainable.

Thick- and thin-film techniques can be combined on the same circuit. First, gold thick-film crossunders are deposited, followed by thick-film glaze-insulating pads. Then, thin-film components, including crossovers, are fabricated. By using this technique, along with circuitry on the back of the ceramic, we can fabricate three-dimensional ceramic hybrids.

Assembly and packaging. A variety of components—including silicon ICs, chip capacitors, transformers, inductors, and optoisolators—can be attached to thin- or thick-film HICs.

Sealed-junction, beam-leaded CBIC (complementary bipolar IC) devices are bonded to the HIC using thermocompression. This process involves solid-state diffusion of gold on beam leads and HIC metalization, under heat (about 300°C) and pressure.

Low-power CMOS (complementary metal-oxide semiconductor) and some high-voltage CBIC devices are attached with die- and wire-bonding techniques similar to those used in the IC packaging described previously.

Packaged ICs, chip capacitors, transformers, inductors, optoisolators, and external leads are reflow soldered to the HIC. Soldering can be done on one or both sides of the HIC, typically using a solder of 60-percent tin, 40-percent lead (60 Sn/40 Pb). Usually, pure rosin flux is used to assure high reliability (prevent corrosion and metal migration). Cleaning processes remove all ionic impurities and prepare the HIC surface for encapsulation.

Typically, thin-film HICs are encapsulated in Dow Corning 36550 RTV silicone rubber to provide corrosion protection for silicon ICs and all film elements: conductors, resistors, capacitors, crossovers, etc. (RTV rubber cures at room temperature.) Depending on the application, RTV-coated HICs are further packaged with a snap-on cover or sealed in a plastic case with silicone potting compound.

Thick-film HICs, such as the board-mounted power module (BMPM) in Figure 3, also use RTV rubber as the encapsulant for silicon devices, and are further packaged in shells using silicone potting compound.

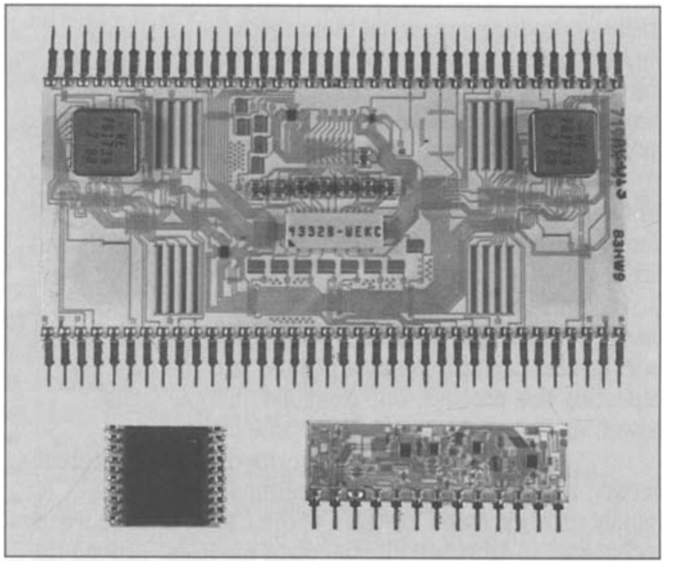


Figure 4. Ceramic hybrid integrated circuits. Currently manufactured are leaded dual and single in-line packages (DIP and SIP) and surface-mount (SM) forms. The photograph shows a DIP, top; SIP, bottom right; and SM, bottom left.

HICs are available in DIP, single in-line package (SIP), or surface-mount configurations. Figure 4 shows examples of currently manufactured ceramic HICs in both leaded (DIP and SIP) and surface-mount forms.

Multilayer structures on ceramic. Additional circuitry can be added to thin-film ceramic hybrids by building alternate layers of polymer and metal patterns. These hybrids are known as POLYHICs.[5]

Figure 5 illustrates the process sequence. Vias placed selectively in the polymer interconnect successive metal layers. (A *via* is a vertical electrical conductor that connects between conductors on two different levels in a layered structure.) A photosensitive polymer, based on triazine, is used so that patterns and vias can be formed with photolithography. The polymer then is cured thermally to produce a material that meets the reliability requirements for hybrids. The POLYHIC structure produces smaller circuit sizes, increased interconnection density, and enhanced electrical characteristics, compared to conventional ceramic hybrids.

Multilayer thick-film structures have also been fabricated for military applications that require high circuit density (Figure 6). First, a conductor layer is printed and fired on the ceramic substrate. Then, two layers of glaze (to minimize pinholes) are printed and fired. To form vias, openings are left in the glaze. When the conductor for the next level is printed, metal is printed into the vias. By repeating this process, one can build multiple signal, power, and ground layers on the same circuit.

Printed Wiring Modules. Intermediate-level interconnection need not be limited to a ceramic hybrid circuit. A rapidly growing trend in AT&T is the use of printed wiring technology to fabricate intermediate modules. Among the reasons for this trend are superior electrical performance, better dimensional stability during processing, capability for multiple signal layers, and cost advantages of batch fabrication in large panels [typically 45.7 by 61 cm (18 by 24 inches)].

Factors that contribute to the improved electrical performance are the lower dielectric constant (4.5 versus 10)—which reduces lead capacitance and propagation delay—and better power and ground-plane coverage.

Printed wiring modules are compatible with either surface-mounted or through-hole components. If desired, the TCE of a printed wiring module can be tailored to match its components by introducing low expansion metal composites during construction.

For example, Figure 7 shows the WE® 32001 module, which packaged the first-generation WE 32000 chip set. Its power and ground planes were made from copper-invar-copper sandwich material to achieve the TCE match needed for solder joint reliability during extended thermal cycling. ("Invar" is an iron-nickel alloy with a near-zero TCE.)

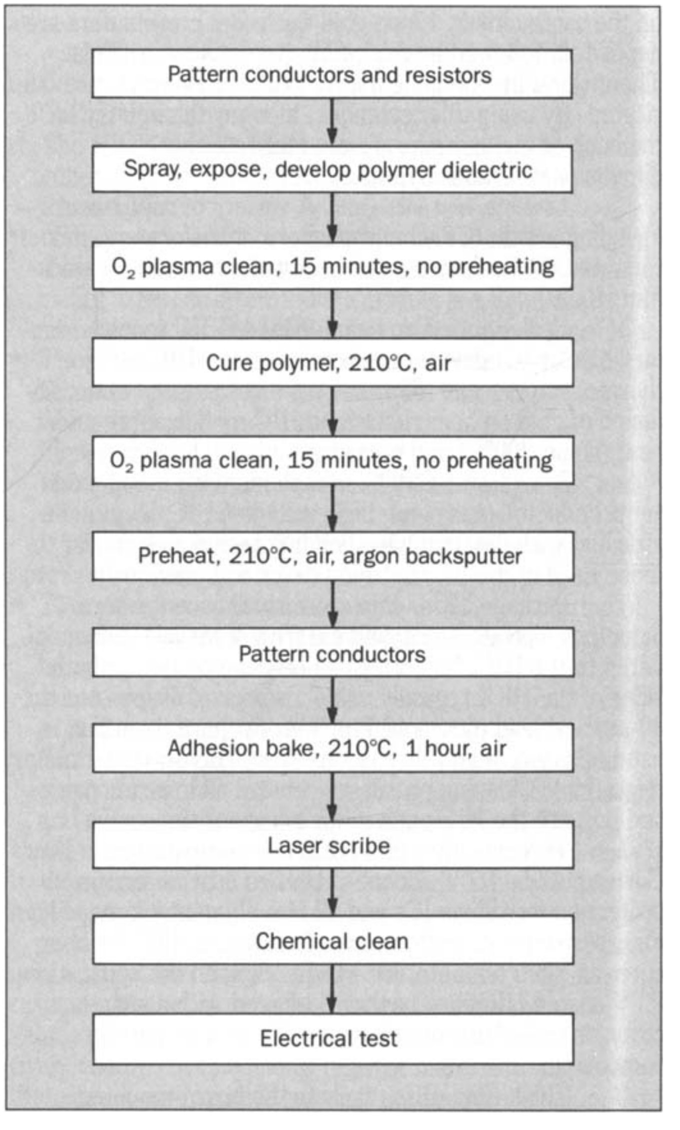


Figure 5. Steps for building a POLYHIC, a hybrid integrated circuit that has alternate layers of polymer and metal patterns.

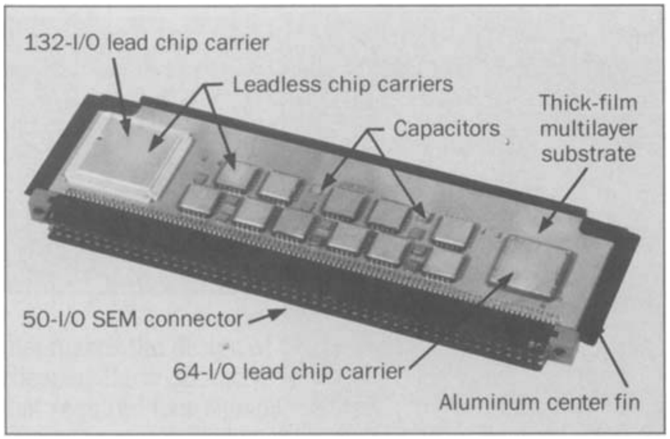


Figure 6. Standard electronic module (SEM) with a thick-film multilayer substrate. I/O = input/output.

The printed wiring module can be pinned (as is the WE 32001 module) or designed with leads for surface mounting to a circuit pack.

Silicon Wafer Substrates. A new multichip packaging technology,[2] called advanced VSLI packaging, uses a silicon wafer as the substrate on which unpackaged chips are mounted. AVP overcomes many of the limitations of more conventional packaging.

Figure 8 shows a cross section that demonstrates some of AVP's features. Power and ground planes are solid copper on either side of the substrate. Polyimide dielectric material separates two levels of copper signal wiring from each other and from the power plane. Signal line widths and spaces are 10 μm (0.4 mils) or more, affording ample interconnection capability with relatively easy wafer-scale lithography. The chips are flip-chip bonded, providing a very-low-inductance electrical connection.

Because of the low noise capability and low capacitance of the interconnections, very-high-speed switching is possible. It is estimated[2] that synchronous clock frequencies above 50 MHz should be possible with a wafer complexity of over a million logic gates.

AVP will undoubtedly be an important interconnection technology in future high-performance systems.

Printed Wiring Technology

Along with its growing applicability as a hybrid substrate, printed wiring has long served as the medium of choice at both the second (circuit pack) and third (backplane) levels of interconnection. The demands on printed wiring have grown as the trend to higher speed and scale of integration has proceeded unabated. These demands arise from the need for:

- Packages with higher I/Os on finer pitch
- More surface-mount packages
- Larger boards
- Increased concern with signal-propagation properties
- Much greater interconnection demand.

To meet these needs, the development of technology and computer-aided design (CAD) tools has been closely coupled in a partnership to provide the system designer not only needed PWB technology but also the ability to use its new features.

The growth of surface mounting is forcing major changes in the form of printed wiring. The surface-mount-pad features on the board, which are typically on 1.27-mm (50-mil) centers, pose significant blocks to use of the mounting layer for laying out circuit traces. For many circuits, this means a double-sided board is not a valid choice.

In addition, the need for higher interconnection density and better electrical performance is driving more applications to multilayer boards. Here, too, surface-mounting pads interfere with surface routing, and a dedicated surface layer for pads and fanout pattern is coming into wider use. The fanout pattern connects the pads to an array of through vias that can access any of the interior layers. These fanout vias can be smaller than component mounting holes, contributing to the interconnection density advantage of surface mounting.

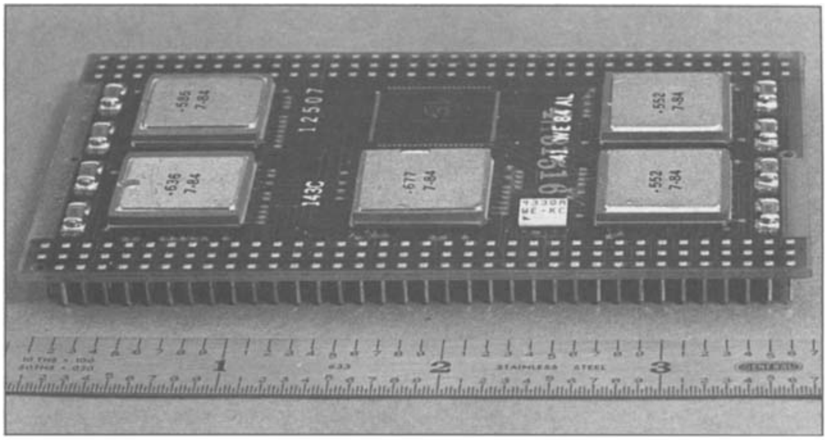


Figure 7. The WE 32001 module contains AT&T's first 32-bit microprocessor and associated clock and memory circuit.

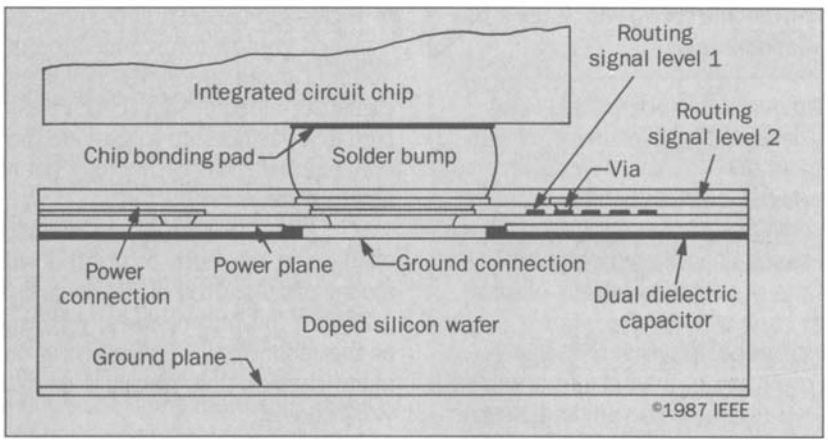


Figure 8. Advanced VSLI packaging (AVP) uses a silicon wafer as the interconnection substrate. (From reference 2; reproduced with permission.)

Other PWB technology developments that are driven by the need for higher density include buried and semi-buried vias, precision feature definition and placement, and improved solder masks.

Buried and Semi-buried Vias. A buried via connects two adjacent interior layers in a multilayer board (MLB), without obstructing other layers (Figure 9), and is formed between those layers before the MLB is laminated. Two advantages arise:

- The buried via can have a smaller diameter, because it penetrates less material.
- The space above and below the via on other layers can be used again.

If its diameter is reduced enough, the buried via can even avoid interfering with adjacent paths on the layers it interconnects. This via, known as a microvia, allows the most efficient use of routing resources on the board.

A powerful microvia router has been developed

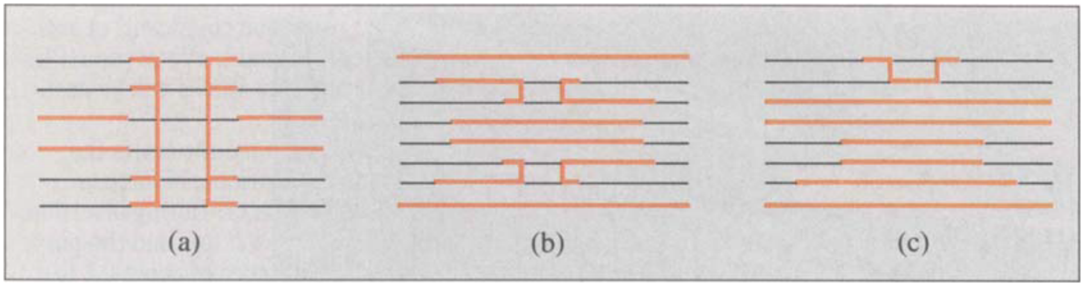


Figure 9. Vias interconnect circuits on various layers of a printed wiring board. (a) Through via; (b) buried via; and (c) semi-buried via.

that makes the design of microvia boards simpler and cheaper. Because microvia routing is efficient, a design that required four signal layers using conventional through vias often can be reduced to two signal layers with microvias.

A semi-buried via, one that connects a surface layer to the layer immediately below (Figure 9), is of great use in connecting directly from a surface-mount footprint to the underlying signal layer, without interfering with other layers. This type of via is essential for high-density, two-sided surface attachment, where fanout vias originate from both sides of the board.

Two approaches to forming a semi-buried via are being pursued:

- Drilling with a laser.
- Use of a dielectric coating layer in which the vias are formed with photolithography. Later, the surface is metalized and patterned.

Fine Features and Manufacturing Precision. Just as finer surface features are required for surface attachment, the dimensions of interconnecting lines and spaces are also shrinking under the demand for higher packaging density. Tighter manufacturing precision is required, not only for successful manufacture of the board, but also for later placement of packages during assembly. Fine-feature definition is not enough. Fine features must also be placed with accuracy for the total manufacturing process from board fabrication to final assembly and test.

New methods of maintaining the required precision have been developed and are now being introduced into the board manufacturing process. As a result, microvia boards will be easier to make. Tighter tolerances on finished boards are possible with the same methods, and a systems approach to manufacturing precision is planned that will propagate the improvements to every stage of manufacture.

Solder Mask Developments. The finer features on surface-mount boards require a precisely defined and registered solder mask. A lower cost process that uses a photo-definable, liquid solder mask has been developed and is now being introduced. This material, which is processed completely in aqueous solutions, meets corporate objectives to reduce the use of halogenated solvents wherever possible.

Future Needs and Developments. Most likely, the trend to higher speed electronics will continue, which will require greater attention to the propagation properties of a printed wiring board. With attention to conductor width and dielectric thickness, we can control impedance. Autoclave lamination, which is now being developed, has significantly improved thickness predictability. Materials with lower dielectric constant will help to reduce propagation delay and line capacitance.

The trend to surface mount is clear and will most likely continue to two-sided mounting, because the density advantages are so compelling. Then, the semi-buried via will be a necessity, as described above. But through vias will also be needed to interconnect the two surfaces, although a way must be found to reduce the blockage they create. A promising technique for doing this is now being developed, using dielectric layers that are defined with photolithography.

Connectors

In this issue, a paper by Ambekar et al.[3] describes the connector system that is used in the Fastech integrated packaging system. This connector system has evolved significantly during the past decade in response to expanding and broadening customer needs, as well as the application of advances in the contact material and lubricant technology.

More recently, new technological forces that act on the designers of communication systems have accelerated the evolution process. Among these forces are the continuing trends toward higher speed, more circuit-pack I/O pins, and increased use of photonics. We are now addressing these needs.

High-Performance Connector. Currently, the development of a six-column, 300 I/O pin, high-performance connector (HPC) is nearing completion. In this new design, the six individual columns of the connector are separated by a series of metal ground planes and form a stripline-type structure. These interstitial ground planes (or blades) extend out from the face of the connector. As the circuit pack is inserted, the blades bisect the space between the columns of backplane pins. When the circuit pack is fully inserted, the blades make electrical connection to the surface of the backplane through a special piece of backplane hardware called the terminal grounding unit (TGU).

Three small double-sided flex circuits carry the individual signal paths and ground from the rear of each contact socket to corresponding points on the circuit pack. Specially designed coaxial pin headers make the final connections between the flex circuits and the circuit pack.

Models of this new coax-like, high-performance connector have been built and evaluated. For 1-volt reference pulses with a 1-ns rise time, the worst-case crosstalk into an idle position in the connector is less than 50 mV. In addition, the HPC exhibits a reflection coefficient of less than 4 percent in a 50-ohm environment. Prototype HPCs manufactured at AT&T's Kansas City Works will be available before the end of 1987.

Higher I/O Connectors. What currently limits the number of connector I/O pins is the frictional force required to mate the individual contacts. During insertion, the nominal contact force between each tine and the pin (0.3 to 0.4 lb) generates frictional forces of about 0.1 to 0.3 lb. These friction forces, as well as the initial force required to spread the tines, must be overcome during insertion of the circuit pack and, hence, lead to an upper limit on the size of the connector (number of I/O pins). With the current latch design, the 400-pin 963R connector is at the upper limit. However, reliability studies done the last several years suggest that we can reduce the nominal, as well as end-of-life, contact force to 0.1 lb without sacrificing reliability. These studies open the way to 963-connector designs with more than 400 I/O pins.

Optical Connectors. The increasing use of photonics in communications systems has led to the development of an optical connector option[6] for the Fastech packaging system. The design, called the 9630 multifiber array connector (MAC), currently provides up to 12 optical fiber connections from a circuit pack through the backplane. Figure 10 shows the MAC module mounted in the center of a circuit pack between two 100-pin 963C connectors.

The MAC uses the well-established, silicon V-groove chip technology that was originally developed for splicing optical cables. Fibers in the circuit-pack portion of the connector are terminated in one set of chips, while those in the backplane terminate in another chip set. An unusual feature of the connector module is its floating alignment sleeve that automatically captures and aligns the precision chips as the circuit pack is inserted and latched into position.

Development of an 18-fiber version of the MAC is nearing completion, and a single-mode version is under development with a projected average loss of 1 dB.

The MAC is compatible with Fastech packaging

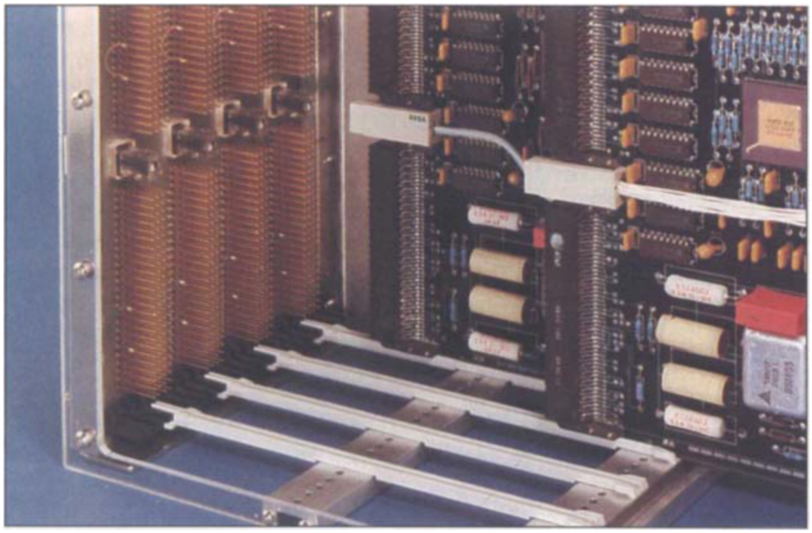


Figure 10. The multifiber array connector (MAC), right, can connect a circuit pack to 12 multimode optical fibers.

and can be used with a variety of 963 connectors. Thus, it provides a major technology extension without making existing hardware obsolete.

Connectors for Future Needs. As additional Fastech packaging options are developed for future communication systems, the connector family will continue to evolve. Until now, the original 3.175-mm grid used in Fastech packaging has remained intact and served well. However, because future systems will require more I/O pins per circuit pack than the existing 963 family can provide easily, denser connectors will be needed. To meet this need, connector designs with grids as low as 1.27 mm (48.8 mils) are being explored today.

Besides the increased densities, even higher performance capabilities will be required of connectors; namely, they must be compatible with pulses that have rise times of 0.3 to 0.6 ns.

The use of optical interconnections within Fastech packaging will also continue to grow. The connector system developed for the next decade will become more modular and allow graceful mixing of optical, electronic, and power connections.

Summary

This paper has examined the interconnection systems that are typically used in electronic system packaging. The interconnection technologies and the forces exerted on them by advancing electronic technology have been described.

Major thrusts in electronic systems include higher speed, higher levels of integration, optoelectronics, and more dense packaging. New capabilities in interconnections will be required and are being developed to provide AT&T systems designers with the means to put together the cost-effective, high-performance systems of tomorrow.

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Biographies (continued)

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