REPORT:

Charles W. Rosenthal *and* ***John M. Dishman*** *are with AT&T Bell Laboratories. Mr. Rosenthal is head of the Computer Aids Systems Department in Whippany, New Jersey. He is responsible for establishing computer-aided engineering and design requirements for new interconnection technology, overall testing of the CAE/D process, and development of automatic interconnection routers, audits, analyses, and fabrication machine outputs. He joined AT&T in 1951 after obtaining a B.E. in electrical engineering from City College of New York and a M.S. in engineering science and applied physics from Harvard University. Mr. Dishman is head of the Interconnection and Power CAE/D Department in Piscataway, New Jersey. He is responsible for providing computer-aided engineering, design,* (continued on page 69)

COMPUTER-AIDED ENGINEERING AND DESIGN FOR INTERCONNECTION TECHNOLOGY

Introduction

The vertical integration of the design and manufacturing elements of AT&T provides the right environment for developing and using an end-to-end computer-aided design process. We have applied this process to the design of the complete hierarchy of interconnection levels[1]—the integrated circuit (IC) package, circuit pack, backplane, multibackplane unit, frame, and system. Computer aids are available for the initial design phases (computer-aided engineering, or CAE) and the follow-on, detailed design phases and interfaces to manufacturing (computer-aided design, including computer-aided test design, or CAD.) The computer-aided design process has been in use throughout the AT&T R&D community for many years,[2] and it is steadily enhanced to increase its benefits.

Objectives of CAE/CAD for Interconnection Technology

From the start of our work in the late 1950s, the development of CAE and CAD tools has been guided by several objectives:

- CAE/CAD must assist in the design of all elements of the interconnection hierarchy, from packages through frames.
- CAE/CAD must be tightly integrated into a complete system solution for interconnection, with the technologies essential to AT&T and with the quality, reliability, and assembly characteristics required of other system elements.
- CAE/CAD must directly support the printed wiring board and the assembly, wire, and test factories through flexible assignment and reassignment of tasks been design and factory organizations, incorporation of design-for-manufacturability, test, repair, and other rules in the synthesis and the checking phases of all designs, aids for direct incorporation in factory processes, and provision of electronic interfaces to the factories to avoid costly and error-prone regeneration of data.
- CAE/CAD must advance in synchronism with the new AT&T technologies made available to designers.[3] The new technology and CAE/CAD features must be coordinated to bring out the best balance of both, and they must continue to be in balance as they evolve. Furthermore, technologies of unique or strategic value to AT&T must be supported irrespective of their value to vendor markets. We are motivated primarily by the importance of internal markets, not just the general or special needs of the vendor market.
- CAE/CAD must provide tools for the leading edge AT&T technologies and projects. This requires the use of leading-edge algorithms, software, and hardware. The most advanced techniques are used for system, circuit, and mechanical simulation; for automatic layout with parts placement and interconnection routers; for component catalogs, design data bases, and trouble report tracking; for processors, displays, and networks; and for human interfaces.
- CAE/CAD must, each year, increase its con-

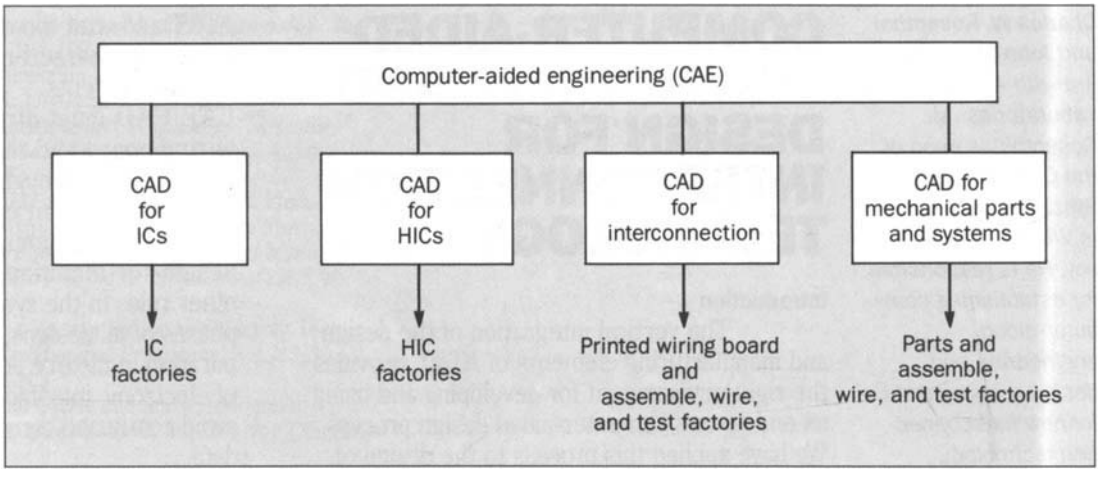


Figure 1. Architecture of AT&T CAE/CAD.

tribution to the bottom line of the design process. It must reduce intervals, reduce costs, improve quality, and allow more complex designs to be processed.

Strategy to Achieve Goals

To achieve its objectives, AT&T established corporate development teams focused on satisfying the internal CAE/CAD requirements. These teams work cooperatively with those working on aids for the factories (computer-aided manufacture, or CAM) to provide an end-to-end computer-aided process for design and manufacturing. The priority-ordered CAE/CAD requirements are developed by planning teams whose recommendations and work programs are guided by corporate steering committees representing technology, project, and factory organizations. This enhances our ability to match our customers' needs in a timely fashion and to maintain a long-term research and development program. In addition, collocation of developers and users and the exchange of personnel increases cross-fertilization of ideas and experience.

Also contributing to meeting our objectives is the use of an open architecture for the CAE/CAD system. It contains well-defined data file interfaces to factory systems and well-defined access points for vendor facilities. We incorporate the best of what is available outside with aids unique to AT&T. The core of the system is of AT&T design and implementation, but there are several external systems that have been used to advantage by exchanging data through the access points. In fact, we actively evaluate vendor systems to assess our own relative position in the CAE/CAD field and have chosen choose vendor products, such as mechanical design systems and simulation accelerators for wide use.

AT&T CAE/CAD for Interconnection

Architecture. The architecture of our system is depicted in Figure 1. The structure uses a common front end for the design steps which are independent of the eventual physical realization. In these first steps, the designers

are given the freedom to withhold, make, and change assignments of functions to physical blocks. Pure logic and function can be synthesized and entered in the system. These can be checked, simulated, analyzed and drawn by the CAE tools. As the design is made more explicit, in a top-down process, data are drawn from electronic catalogs describing components or reusable units and integrated into the design file. The component data can be transferred to the factories for checks on availability, usability, and price. When designers are satisfied with the performance and features of their work, the CAE tools provide aids for generating files that control the fabrication of discrete wire models.

The CAE tools enhance the circuit designers' and physical designers' abilities to provide high-performance and high-quality designs. The logic/function checking tools help avoid most of the errors that could occur. The errors avoided in this stage of design decrease the interval for design and make the next stages easier and less costly.

When the functional/circuit design is correct, and its elements have been assigned to physical blocks, the detailed physical design can begin. The information conveyed is generally a list of available components, their physical characteristics, and the connections that must be made among them to achieve the design's intent.

If some or all of the design is to be realized as an IC, the design intent file is transferred to the IC designers. They will employ a set of aids for IC layout and documentation.

If hybrid integrated circuits (HICs), printed wiring boards (PWBs), or mechanical parts are needed, the relevant portions of the design file are transferred to the appropriate designers. This article will henceforth concern itself primarily with the design process aids for PWBs and mechanical equipment.

The mechanical portions of a system consist of carriers for supporting and interconnecting electronic subassemblies.[1] The carrier can be a frame or cabinet or enclosure which stretches floor to ceiling or can be a telephone set fitting in the palm of a hand. There is a shelf or unit to fit within the frame or cabinet; one or more circuit packs fit within a unit and usually many ICs, HICs, or discrete components are interconnected on a circuit pack.

At the outset of the design process, we must select the technology to be employed. Because telecommunications systems have a large span of environmental, performance, and user characteristics, the designers must have a large choice of technologies. The computer aids handle these mechanical technologies and assist the designers in making the choice which optimizes benefits and costs. In the physical design of parts, the aids incorporate design-for-manufacturability rules derived by design and manufacturing engineers. Adherence to these rules will ensure the lowest-cost/highest-yield products for the manufacturing facilities in the factory. If the designer deviates from the accepted design rules, that fact is graphically brought to the designer's attention for correction or for the negotiation of an exception. The principle is to establish design rules, a flexible means for incorporating them in the synthesis stage of automatic design, and a means to audit for adherence after design is complete.

When this procedure is followed, the designs will go to the factories with 100 percent accuracy and not require review or correction. This principle applies to mechanical and electronic CAD for equipment, PWBs,

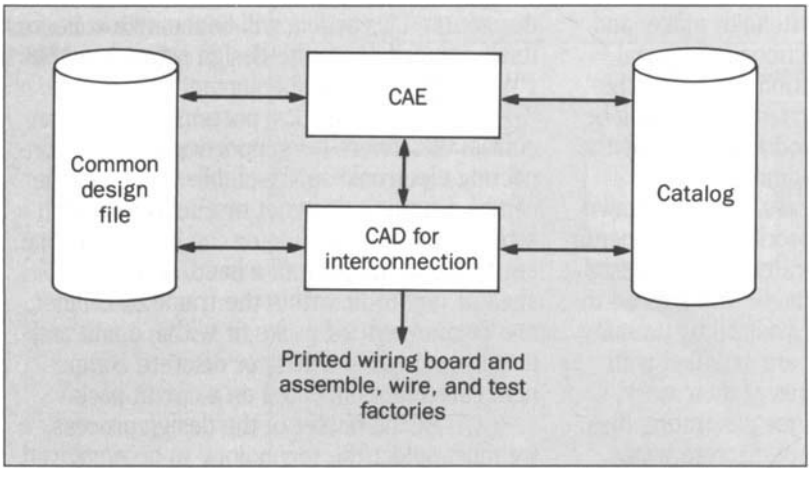


Figure 2. AT&T CAE/CAD for interconnection.

HICs, and ICs.

The CAD tools accept the design intent data and assist in the detailed layout and then the generation of data for our factories. In the case of PWBs, the intent data are the identities of the parts, descriptions of the interconnections to be made among the terminals of the parts (called nets), and descriptions of the parts. The part descriptions are retrieved from a catalog. The role of the catalog is depicted in Figure 2, a more detailed view of the CAE front end and the CAD aids for PWBs. The catalog is a key element in our process, because it allows the sharing of data about common components and reusable units throughout AT&T.

For common parts, there is a corporate team to enter, verify, and distribute data throughout AT&T. The data include the logical, timing, simulation, physical, availability, reliability, and cost attributes of each component. These data are gathered from many corporate sources and their values aligned before they are presented to the CAE/CAD applications. The gathering and alignment functions are a difficult and continuing task to ensure quality. In instances where a complete set of data is not available, the catalog will include a subset. Where a component is not needed throughout AT&T, its data can be captured for a locale, a project, or a single design.

Once data for a component are retrieved from the catalog for, say CAE, it is retained within the design. It is not necessary to retrieve more data from the catalog until the CAD phase or the point at which data are sent to the factory. One retrieval during the CAD phase will extract all additional data needed for the CAD phase. Similarly, additional data are extracted once for manufacturing.

A single repository data base, the common design file, or CDF, is used for CAE and CAD. The data content in the CDF is adequate for all the programs in the design process, all technologies, and all levels of interconnection from package to system. The amount of data in the CDF for a design will increase as the design moves through the CAE and then CAD processes. Programs in the process extract data from the CDF, process it, and return it to the CDF with value added. By this means, the CDF serves as a data bus for our system. It ensures that a path is available among all application programs, and it ensures that adherence to its dictionary will enable communication among all present and future application programs.

The Major Design Process Functions.

Computer-aided engineering. In CAE, we provide features for design capture of behavioral, structural, or logic descriptions of systems and circuits using hardware description languages or graphical representations. A system can be represented and then success-

fully decomposed into smaller blocks as its constituents are designed or specified in a top-down design process that is fully abstract and functional without the need for coupling to physical realization. The more detailed logical/functional decomposition will ultimately refer to the companion physical decomposition. To assist circuit data entry and understanding of drawings, we represent repeated patterns (like memories), buses, and highways in compressed notation. Our principal system functions have addressed logic circuits. The features for analog and mixed analogic-logic circuits are now being developed.

Among the first design tasks is the selection of the specific group of components for a system. This is done by query, using key words, on the attributes of components in the catalog. The designer, the project component administrator, and the factory engineers will select the components for a specific system on the basis of features, performance, cost, and availability. Thereafter, as each subcircuit, such as a circuit pack, is designed or captured, its data file of components is sent electronically to the factory Manufacturing Resource Planning (MRP) system for advance ordering. If a design is initiated which calls for components outside the agreed-to list, there are flags to indicate the condition; thereafter, corrections or exception agreements are needed. An acceptable list of components and potential substitutes is electronically sent to factory engineers to start orders and planning for assembly.

Checks are automatically run on the captured circuit to diagnose typographical and syntactical errors including one-terminal nets, duplicate names, and illegal names. Errors are reported graphically for interactive viewing and correction or in listings for off-line analysis and either interactive or batch correction. The checked circuit schematic diagram can be drawn interactively or a hard-copy drawing can be made for off-line examination.

When the above errors are eliminated, the designers can simulate the design's behavior using logic and timing simulators.[4-6] The simulation is accelerated by using one or more real devices when the device complexity could overwhelm either the running of the simulation or the preparation of accurate models for them. During simulation, the input and output data are saved in temporally ordered files. The results are voluminous and very complicated. A complete examination would be like looking for needles in a haystack. The designer wants only to examine patterns of signals that confirm desired operation and indicate undesired operation of the system. To locate these patterns, the data can be automatically searched for specified patterns or combinations of patterns of the signals. These are displayed for the designer at the interactive workstation. Using the simulation programs, designers obtain the test patterns which will be used by factory engineers to test the circuit for acceptable performance. The file of test patterns is sent to the factory for their use in one of the prespecified test sets.[7]

To this point in the process, the treatment has been primarily of logical/functional design. With these verified as satisfying the requirements, it is necessary to partition the functions among specific portions of the physical hierarchy—so much goes to this frame, so much to the next; within the frame there is further partitioning to units, then to circuit packs, and finally to packages and ICs. Focusing on the circuit pack, at the conclusion of partitioning, its printed board, connector, and all its

components have been identified. Furthermore, because the functions have been partitioned, we also know what interconnections must be made among the components. We must now determine where the components will be placed on the board and how they will be connected.

Placement of components is an important means of ensuring the realization of a circuit's performance. With this in mind, we provide the engineers with automatic means for placing components. The placement of components must satisfy many objectives including providing space for short interconnections, adherence to temperature constraints, limiting electromagnetic coupling and interference, and arrangement of components for easy assembly. Several algorithms, optimization criteria, weighting parameters, and interactive displays are available to help designers meet the objectives. The multicolor displays and responsive editors can be used to tune the placement for unusual conditions. When placement cannot achieve its objectives, earlier steps in the design process must be redone so that all objectives can be met.

The next step, for many projects, is to build models of the designs. There are three types of easy-to-build discrete wire models: wire-wrap, quick-connect and Multiwire (registered trademark of Kollmorgen Corp.) systems. The data to wire each of these models can be generated readily by the CAE software. A fast modeling facility at the Network Software Center, Lisle, Illinois, uses these files to return fully wrapped boards in 2 to 4 days.

If the electrical, thermal, or mechanical performance of a discrete wire model is not adequate, we can accelerate the CAD activities and design a printed wire model. Sometimes these employ simpler design rules to speed the process. Early test of a model's features and performance compresses the design process by enhancing verification or the identification of errors in requirements or design. Changes in the early phases of design are invariably easier and cheaper to make than the same ones at intermediate or final design phases.

At the conclusion of the CAE stage the accumulated design and component data are transferred to the CAD tools. The data transfer is in a standard file defined for two-way communication. The CAE-to-CAD direction transfers design intent (components and interconnections) plus component placement if desired. The CAD-to-CAE direction (back annotation) transfers final placement information or interchanges of equivalent terminals or elements, or substitutions of equivalent components to be included in the schematic diagram.

Mechanical CAD. In parallel with the circuit pack design, mechanical engineers and designers conceptualize piece parts as well as the overall equipment design. This includes frames with their associated shelves or units into which the circuit packs are placed and the backplanes. Also included is the interunit and interframe wiring: cables, wiring harnesses, and associated connectors.

The overall mechanical design involves several different factors, all of which have to be optimized to ensure satisfactory performance at the lowest cost. Interference analysis addresses the issue of parts clearing one another, structural analysis considers internal stress on individual parts and systems of parts, and thermal analysis ensures that sensitive components are not overheated. Electrical

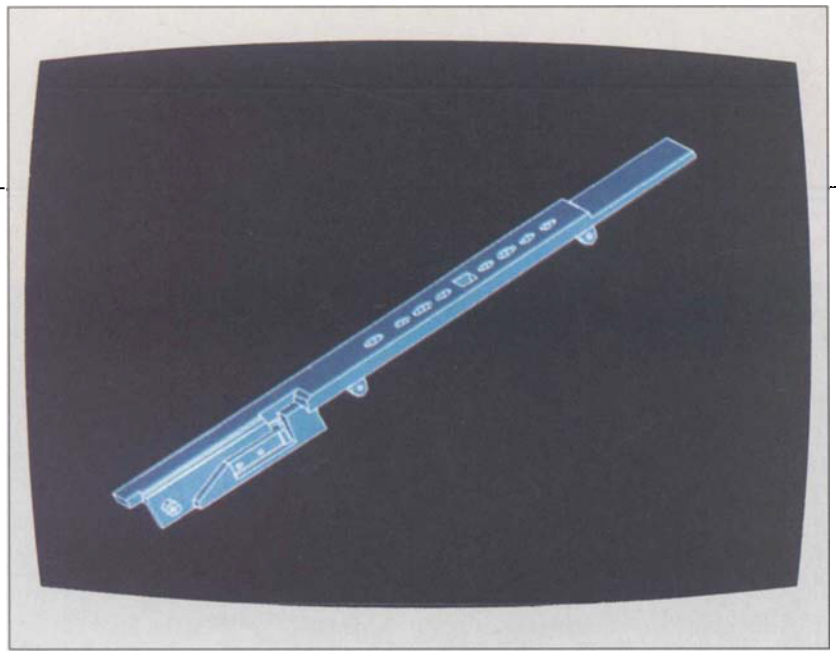


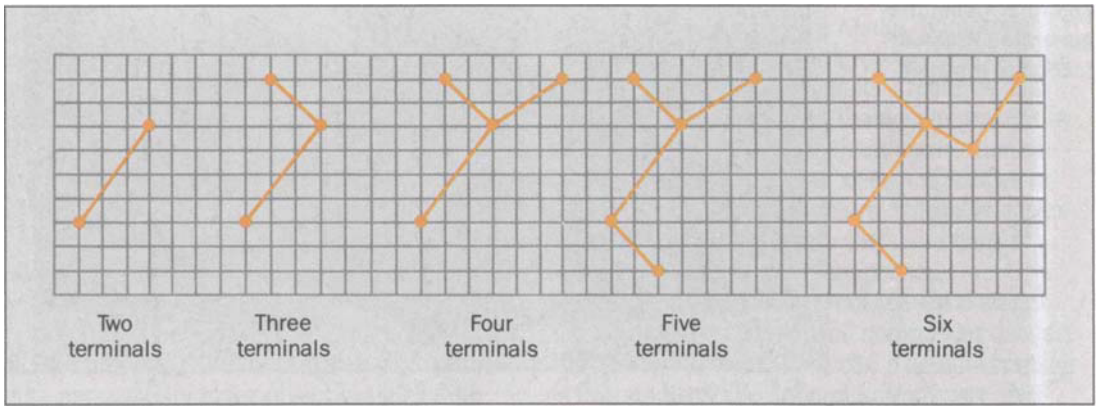
Figure 3. Computer-generated Fastech® faceplate drawing.

analysis is also a part of this intrinsically mechanically oriented process, since it is vital to ensure that electrical interference (i.e., crosstalk) is not excessive in connectors, cables, and the circuit packs themselves, especially for performance-driven applications.

CAD tools in support of the mechanical design process are for the most part purchased from outside vendors, customized for particular needs of the AT&T design community, and integrated with various networking and special-purpose software. Examples include GEOMOD® software (from SDRC Corp.) for solid modeling and conceptualization, ANSYS® software (from Swanson Analysis Systems Corp.) for finite-element analysis of structural and thermal constraints, and UNIGRAPHICS® software (from McDonnell-Douglas Corp.) for documentation and visualization of intrinsically three-dimensional objects. UNIGRAPHICS software is the standard mechanical design computer tool within the AT&T engineering and design communities and by mid-1986 had been deployed throughout AT&T. Customized software, developed internally, has been deployed to perform audits of individual piece parts [e.g., customized faceplates for circuit packs (Figure 3)] to ensure that the designer has recognized the factories' economic and manufacturability constraints.

Finally, electronic files from the final design of individual piece parts and systems of mechanical assemblies are passed electronically to factories. The files are used to generate work documents for those assembling the equipment, or to directly drive numerically controlled machinery for shaping, molding, or bending mechanical parts in the factory. The electronic data are used to control laser scribing machines and inspection machines to eliminate silk screening of nomenclature and monitoring of manufactured product for conformance to design specifications. In addition, product engineers can view the information in three dimensions (e.g., using UNIGRAPHICS) and add value to it in terms of adjustments to make designs more manufacturable. Simultaneous viewing of such data by both product and design engineers, who are usually separated by large distances geographically, leads to a streamlined product realization process by enhancing the dialog between the two participants.

Figure 4. Minimal spanning trees for nets.



Computer-aided design. In the design of an interconnection product, we anticipate the manufacturing process by adhering to rules that ensure achievement of targets for quality, reliability, cost, and performance. These rules are the joint responsibility of product engineers from manufacturing, marketing, and design. We have codified a structure for rules which allows them to be stored and distributed electronically, like data for components. Making them widely available leads to incorporation of the rules into the computer-aids programs. This helps enforce the rules in several ways: automatic design programs use the rules as conditions on the selections made, editing programs obey the rules when changes are made, and auditing programs identify violations of rules. The use of design rules is as vital to a product's design for manufacturability as the use of reliable, available, and cost-effective components. Rules therefore provide a capability not generally found in vendor systems. In the process we use, it is necessary to select design rules and enter them into standard files.

Circuit pack layout. Let us return to consideration of the PWB. The components have been placed, so we know the positions of all terminals and we know the interconnections among terminals needed to obtain the circuit specified. Furthermore, the design rules will specify the technology, that is, the widths of paths; sizes of holes, lands, and vias; clearance of features; number and type of layers; and other characteristics.

Before starting the interconnection routing, we analyze the potential crowding in the available space on the board. The analyses are done to avoid starting the design of all the specific interconnections when it may be impossible to complete them in the available space. Routing all the interconnections takes a relatively long time and large computer resources. The analysis helps avoid fruitless, expensive attempts. The analysis is based on direct point-to-point connections of terminals in each net (a net is the set of terminals which are electrically and logically equivalent). For nets with more than one terminal, the interconnection pattern is the minimal spanning tree, i.e., the net graph, without loops, that connects all terminals in a way that yields the least interconnection distances (Figure 4). The dis-

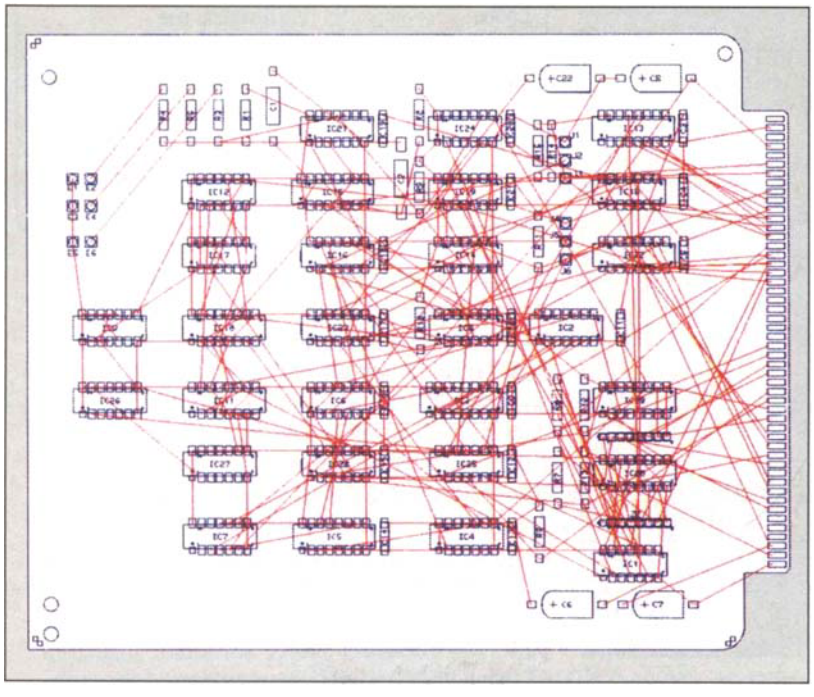


Figure 5. Computer-generated display of minimal spanning trees for simple circuit.

play of all the minimal spanning trees for a simple circuit is shown in Figure 5. All the trees for a more complex circuit would be difficult to discern, therefore the display can portray nets in groups selected by the designer.

Congestion of interconnections is estimated to occur where the trees' branches overlap most. Another estimate is made by drawing vertical lines at equal intervals (say every one-tenth inch) across the board and counting the number of crossing branches for each line. The same can be done for vertical lines. These counts, plotted in Figure 6, show where connections will be densest and where there may be too many for the board. If there are too many it is necessary to return to the placement program for a new arrangement or to use the interactive graphical facilities to move a few components and relieve the congestion.

A positive analysis will be followed by the use of an automatic router. Its task is to complete the hundreds or thousands of connections while obeying the design rules. Our routers are based on the cell expansion algorithm invented by C. Y. Lee[8] and elegantly coded by J. H. Condon and K. Thompson. A connection between two terminals does not follow a straight-line path but meanders along orthogonal directions to remain outside design-rule clearances from pre-existing paths and terminals. The path will also go up and down among the layers to get through congested areas.

The algorithm orders the connections by length and, starting with the shortest, in one method, traces paths for them sequentially until all are done or the earlier ones occupy space in a pattern that blocks later ones. By reordering the connections and starting anew or by strategically removing early connections and continuing, it is possible to complete more total connections. The goal is to complete all connections, so the reordering and strategic removal steps may be executed several times. Routing and rerouting require large computer resources, but are effective because their cost is less than that of the equivalent human effort.

Human operators are brought in when a few incomplete connections remain or when logical or electrical conditions require tracing paths in ways that the algorithms cannot handle. The operators are provided with interactive color displays of the existing connections and prompts depicting the incomplete ones. They use editing features to complete one connection at a time.

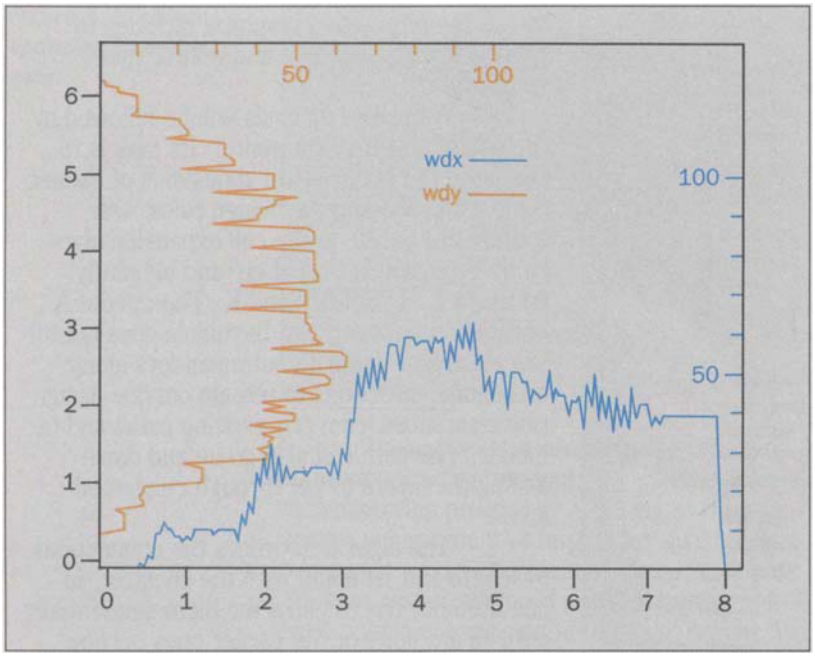


Figure 6. Interconnection histograms for simple circuit.

When all connections are traced, the layout is complete. The design is carefully audited using an array of programs that check correctness of:

- *Logic function.* Connectivity must be as the circuit requires, and there must be no explicit loops.
- *Performance.* Connection lengths must not be excessive.
- *Mechanics.* Clearances must be adequate.
- *Electrical.* Crosstalk must be within bounds.
- *Manufacturability.* Proper test sites must be available, feature sizes must be adequate, hole sizes must be standard.

A complete list of audits is in Table I. When the design passes all the audits it will be manufacturable in the AT&T factories.

The complete design is represented by the data accumulated in the CDF. The data therein are used to generate the fabrication tools for manufacturing and testing the bare board and the circuit pack. For the bare boards and backplanes, we produce data files which control: machines generating artwork for the PWB layers, the solder mask protective coat, the surface mount device solder pads, and the nomenclature; machines that insert backplane pins; testers that locate shorts or opens; and automatic drill machines. For the assembly of packs or backplanes, we produce files for: component sequencing before automatic insertion of through-hole devices; insertion of through-hole and "on-sertion" of surface mount devices; and in-circuit test generation.[7] These files can be supplemented by a flexible suite of drawings which depicts the artwork, stocklists, notes, tables, mechanical parts, details of assembly such as components' locations with their reference designations, and assembled product.

Table I. Audits, Analyses, and Reports of a Final Design

Functional	
Connectivity	Parallelism
Crosstalk	Segments:
Impedance	Electrical
Lengths	Thermal
Loops	Terminal use
Manufacturable	
Clearance:	Bare board testability
Metal	Hole characteristics
Solder mask	In-circuit testability
Nomenclature	Part layout

Electronic design transfer. The CDF is placed under version control when the design data are released for factory use. The control process is a single source of all product design information which also monitors the distribution of data to factories. For example, the artwork drill and test files are sent electronically to the Richmond Works from design locations that stretch from Massachusetts to Colorado. There they automatically enter the

Table II. Principal CAE/CAD Environments

Features	CAE Environment	CAD Physical Design Environment	CAD Manufacturing Data Environment
Original	TSO/mainframe	TSO/mainframe	TSO/IMS/mainframe
Current		UNIX®/mainframe	
	UNIX/microcomputer	UNIX/microcomputer	
	Workstation	Workstation	
	UNIX/minicomputer	UNIX/minicomputer	
	UNIX/mainframe	UNIX/mainframe	UNIX/minicomputer
	VMS*/minicomputer		VMS/minicomputer
	Special purpose	Special purpose	
	Accelerator	Accelerator	

*Registered trademark of Digital Equipment Corp.

Richmond Automatic Tracking System.[9] Transmission errors are automatically reported to the design organization for rapid correction. Minimal checks of designs are required because of the execution of the audits described above. The designs transmitted are highly manufacturable; less than 5 percent have transmission errors, design rule violations, or scrambled data.

For the assembly factories, which are widely distributed, we transfer data for the factory processes, as described above, and for Manufacturing Resource Planning. In addition to the assembly data described above, we control the flow of early stocklists and bills of materials received from the CAE system. At this stage, data are added which describe the interconnections at the unit and frame level.

For factory data, we have access control to limit the individuals able to review and modify the critical information. As designs evolve, the successive data for series and issues are identified and controlled. Electronic control ensures that changes are not confused, unnecessary product is not produced, and product is produced in adequate quantities. A critical part of this portion of the process is configuration control, which associates the files for the parts of a system that go together.

Hardware/Software Computing Environment. The functions described under "Design Process Functions" run in a varied environment of operating systems, micro-, mini-, and maxiprocessors, and displays. This is because the development of functions started at different times with different customer bases. The variety of hardware and operating systems is shown in Table II.

We are well on the way toward our goal of exclusive use of the UNIX® operating system with the core hardware/networking architecture shown in Figure 7. This architecture supports all the CAE/CAD functions effectively.

Use of CAE/CAD in AT&T

The features described are used at all R&D locations that design interconnection product. The vast majority or our designs are made with our aids; this practice places AT&T at the leading edge of CAE/CAD users. There are seven mainframe installations of the original TSO-based process. There are also several hundred design stations using mini- and microcomputer installations with the current environment. The mainframe and stand-alone installations communicate over links in local and wide area networks. Several hundred engineers and design engineering staff support people are regular users. Files for several thousand PWB designs flow to the factories each year.

Quantitative reviews of our CAE/CAD processes show a significant increase in the

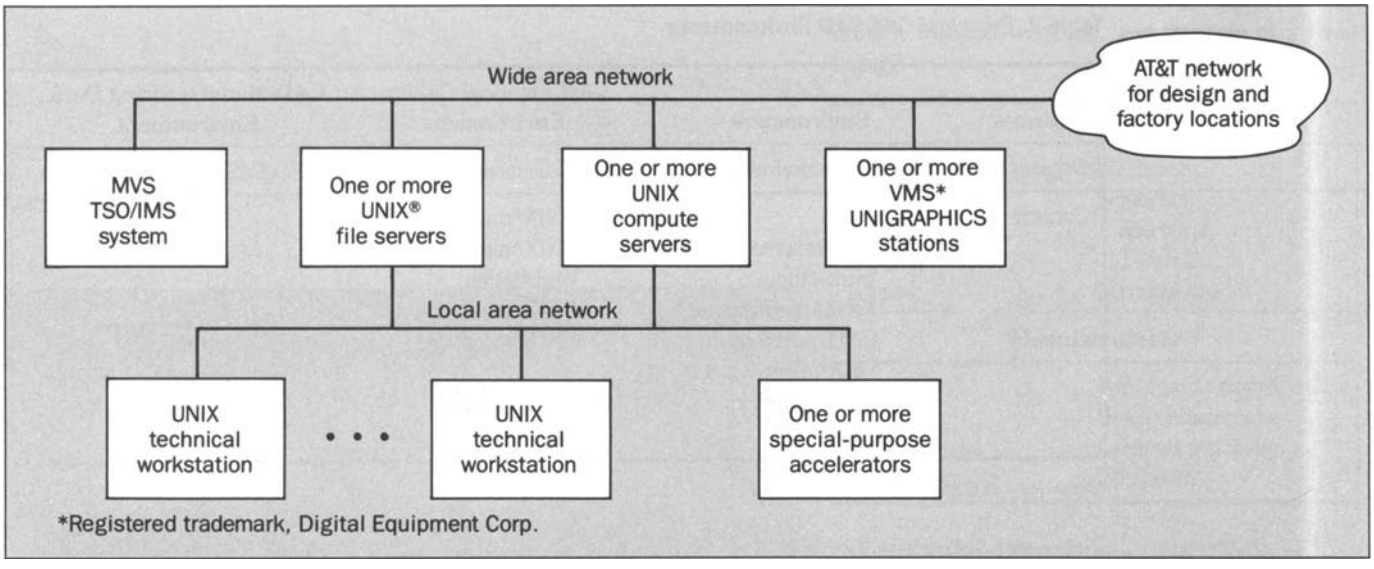


Figure 7. CAE/CAD hardware/networking core architecture.

productivity of designers, an avoidance of costs, and an increase in quality. We can cite three examples. Traditionally the front-end design is done manually and hand-drawn design information is given to the physical design staff. It takes more than a week to complete and correct the data before the physical design staff can start the layout process. When the CAE system is used, this interval reduces to 1/2 day. We estimate that, over the last 12 years, the physical design load has grown over five-fold because of changes in design complexity, number of designs, and tasks carried out. Yet over this interval, the staff has remained constant and the quality of design has increased. Finally, when design information was transferred manually to the Richmond works the probability of a file being wrong was 65 percent. Through the use of electronic, monitored files which have been audited beforehand the error rate has been reduced to 5 percent and is still declining. The higher quality, lower cost, and shorter intervals we seek with CAE/CAD are being achieved in a technology era in which design complexity obviates the use of traditional manual methods.

Future Directions of CAE/CAD

The prime driving force for our development of new features is the need to support AT&T technology, design processes, and factory processes. Through vertical integration, we plan for the unique, frequently proprietary, technologies and processes used in AT&T. We can provide CAE/CAD for these processes and technologies in synchronism with their introduction within AT&T. Indeed, by providing ad hoc modifications to current CAE/CAD, we accelerate experiments with new technologies and processes and we analyze their benefits, shortening the interval before they are introduced.

Another continuous stimulant to our developing CAE/CAD is the rapid evolution of processors, displays, networks, and software. These put larger resources in our hands at lower costs. We will continue to work to put these benefits in the hands of our customers. The distributed core architecture described earlier will support our development with minimum disturbance and maximum benefit to our customers.

The span of responsibility is very large for an end-to-end process—from initial system design aids to aids for introducing design data in the factories. The variety of technologies, projects, and factories served is also very large. The still-unfilled need to totally integrate electronic and mechanical design remains a goal. A major challenge for us is to develop a

smooth process for this market base. The use of the UNIX operating system, improved local- and wide-area networking, common design file definitions, and a user community that wants a common approach will enhance our ability to provide a smooth AT&T process.

Engineers are confronted with more difficult design decisions because of the greater variety of technologies available and the need to design for high-quality products. We take it as our goal to assist engineers by devising aids to help them make choices. We are studying and experimenting with aids as simple as spreadsheet programs and as complex as expert systems. From these will shortly come useful tools. The challenge of CAE/CAD for interconnection technology continues unabated as the technology evolves to serve telecommunications systems.

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and manufacturing tools for mechanical product realization for all of AT&T and in particular for energy systems and electronic power. He received a B.S. degree from Georgia Institute of Technology and M.S. and Ph.D. degrees from Carnegie Mellon University. He joined AT&T in 1967.

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