REPORT:

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SYSTEMS PACKAGING

Introduction

The packaging of an electronic system is the translation of the system designer's concepts into physical realities. Packaging is a major engineering consideration which addresses every element in the system's makeup, from the fundamental material and circuit technologies to manufacturing and final testing strategies. The packaging scheme implemented for a particular system is termed its physical design. The physical design process is descriptive of the methods used to "package" an electronic system.

Developers and manufacturers can realize important advantages if the physical design of a variety of different systems can be based on a common set of standardized building blocks without inhibiting the electronic function of the systems. By using proven building blocks, systems can be developed at lower cost and with less technological risk. The systems can be more readily manufactured, and costs will be reduced by economies of scale.

Partitioning and Assembly

A successful packaging system must satisfy the demands imposed by the system design. Reduced to simplest terms, the physical realization of a system results in providing low-cost, functional, and reliable interconnections among all of the system elements—from transistor-to-transistor connections within integrated circuit chips up to the system's connections to its power sources. The physical elements shown in Figure 1 help illustrate the course of partitioning an electronic system.

The partitioning process is one of assigning logic elements (gates, flip-flops, microprocessors, memory elements, etc.) to the optimal electronic building blocks. These building blocks include silicon integrated circuit chips, multichip modules, circuit packs, backplanes, and cabinets.

The system interconnections, i.e., the wiring paths among components, occur at each building block level. For large systems, these interconnections can be described in the following hierarchy:

- Level 0: Chip-level interconnections
- Level 1: Chip package and hybrid circuits
- Level 2: Printed wiring circuit cards
- Level 3: Back panel (printed and discrete wire)
- Level 4: Intracabinet wiring and cabling
- Level 5: Intercabinet connections.

These interconnections are shown schematically in Figure 2.

Small systems, and even some large ones, apply fewer interconnection levels. Personal computers, for example, may have only levels 0, 1, and 2.

The performance, reliability, and maintainability of electronic systems (especially in the case of large systems) are determined by three key factors: system architecture, integrated circuit technology, and the physical partitioning of the system into a hierarchy of interconnection levels. One of the key AT&T methodologies which addresses the partitioning and assembly elements in the last four interconnection levels is the Fastech® integrated packaging system. The Fastech system consists of circuit packs, connectors, shelf hardware, computer-aided design and documentation, application engineering, system prototyping technology, and automated manu-

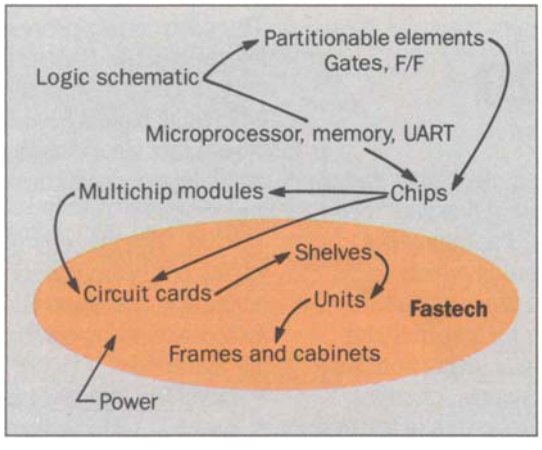

Figure 1. The course of logic partitioning of an electronic system.

facturing technology. It is currently being used in over 150 of AT&T's recently developed telecommunication and computing systems.

The goal of the Fastech system from its inception was to establish a flexible, widely used, and economically attractive interconnection system to address interconnection levels 2 through 5. The challenges were: (1) to pick the "right" standards, and (2) to make the system provide significant advantages to prospective users, thereby ensuring its widespread use and high-volume manufacture.

Standardization Goals

By addressing physical design issues in a standardized and well-characterized manner, the electronic system developers are freed to concentrate on system architecture and IC technology issues and the manufacturing engineers are able to move further down the manufacturing learning curve while maintaining high quality.

In the increasingly competitive telecommunications and computer business, improved productivity can be obtained by aggressively pursuing three paths:[1]

1. Computer-aided design and manufacture (CAD/CAM)
2. Design for manufacturability
3. Factory automation.

The common characteristic that binds these three together is consistency.

The first of these paths, CAD/CAM, has consistency at its very foundation. Once design rules have been established, their uniform application using CAD tools provides an efficient translation from design intent into a product ready for manufacture. The use of a similar set of CAM tools in production minimizes the sporadic defects that tie up a production line. Thus, CAD/CAM provides for productivity improvements in both the design-transfer and the manufacturing processes.

The inherent advantages of CAD/CAM can be offset, however, if the design rules are not carefully thought through. Thus, the principles of design for manufacturability must be applied. It is essential that product designs reflect the capabilities of existing or planned manufacturing and testing facilities. The margins set for manufacturing processes are just as critical as those set for the product itself. Equal attention to both will yield a further improvement in productivity.

Factory automation presents the most obvious means for improved consistency in manufacture. If the automated process is properly characterized and the interaction with the previous elements—CAD/CAM and design for manufacture—is well managed, the results can yield substantial productivity gains. Other engineering factors are involved as well, but the proper interaction of these planning elements is essential in realizing consistency.

The Fastech system is an example of

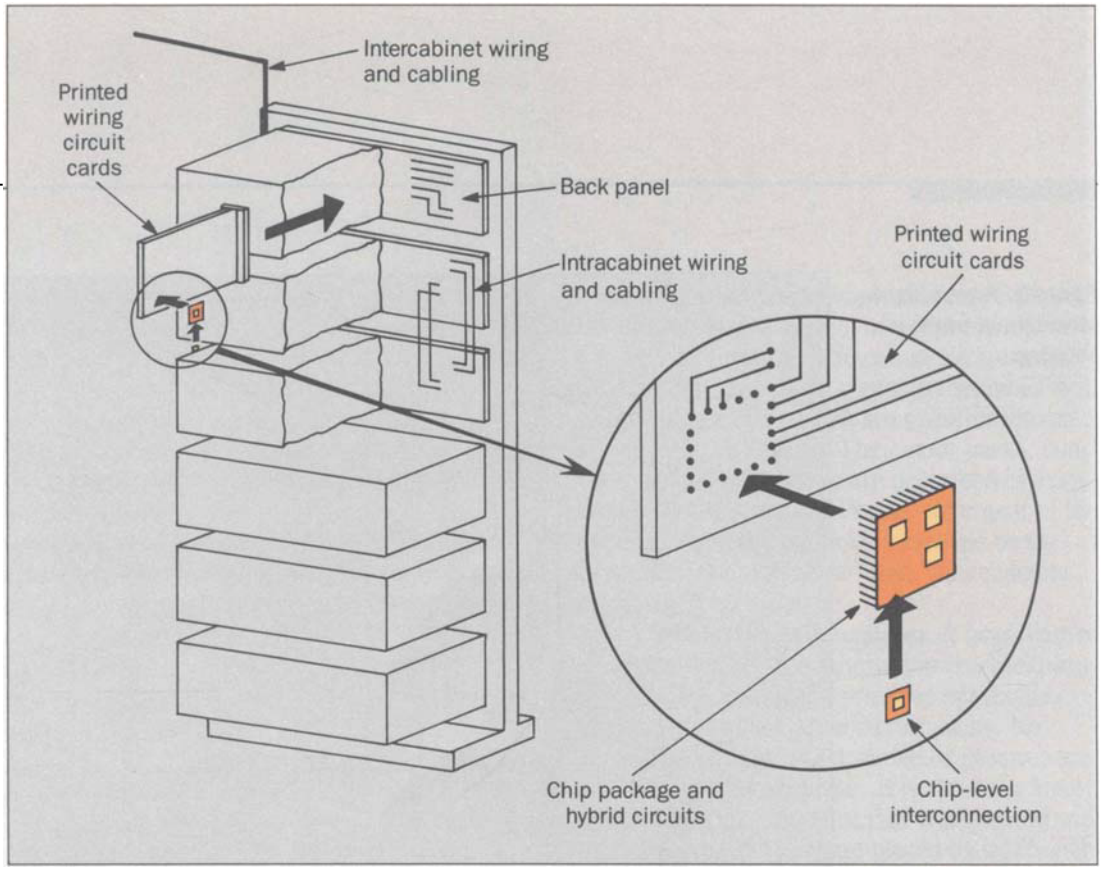

Figure 2. The interconnection hierarchy, from chip to system.

the application of the foregoing principles. From its inception, the system represented a design process undertaken with consideration for the manufacturing process. Its development proceeded in a coherent, systematic manner to define a generic physical structure that could be adapted to many product types. Developed in the mid-1970s, the Fastech system has since been used in the manufacture of some of AT&T's newest products: the 5ESS™ digital switching system, System 75 digital PBX, 3B20 computer, SL undersea fiber cable system, and FT Series G high-speed lightwave system. The rapid pace of development in integrated circuit technology and in integrated circuit packaging has been easily accommodated in the Fastech system. Integrated-circuit-level issues are addressed at interconnection levels 0 and 1. Because Fastech standards primarily address interconnection levels 2 to 4, the packaging system is relatively immune to changing integrated circuit technology. Of course, this is true only up to a certain point. A later section of this article will discuss how some of the newer integrated circuit technologies will impact the physical design of systems.

Establishing a Standard

The Fastech system was designed to provide advantages to the system developers and manufacturers, and thus to invite its use. The widespread acceptance of the Fastech system is based on several key features:

- *Flexibility*. Packaging options are provided to span a wide range of applications. Designers do not feel restricted by too narrow a standard.
- *Reliability*. A very reliable bifurcated connector system has been coupled with a carefully

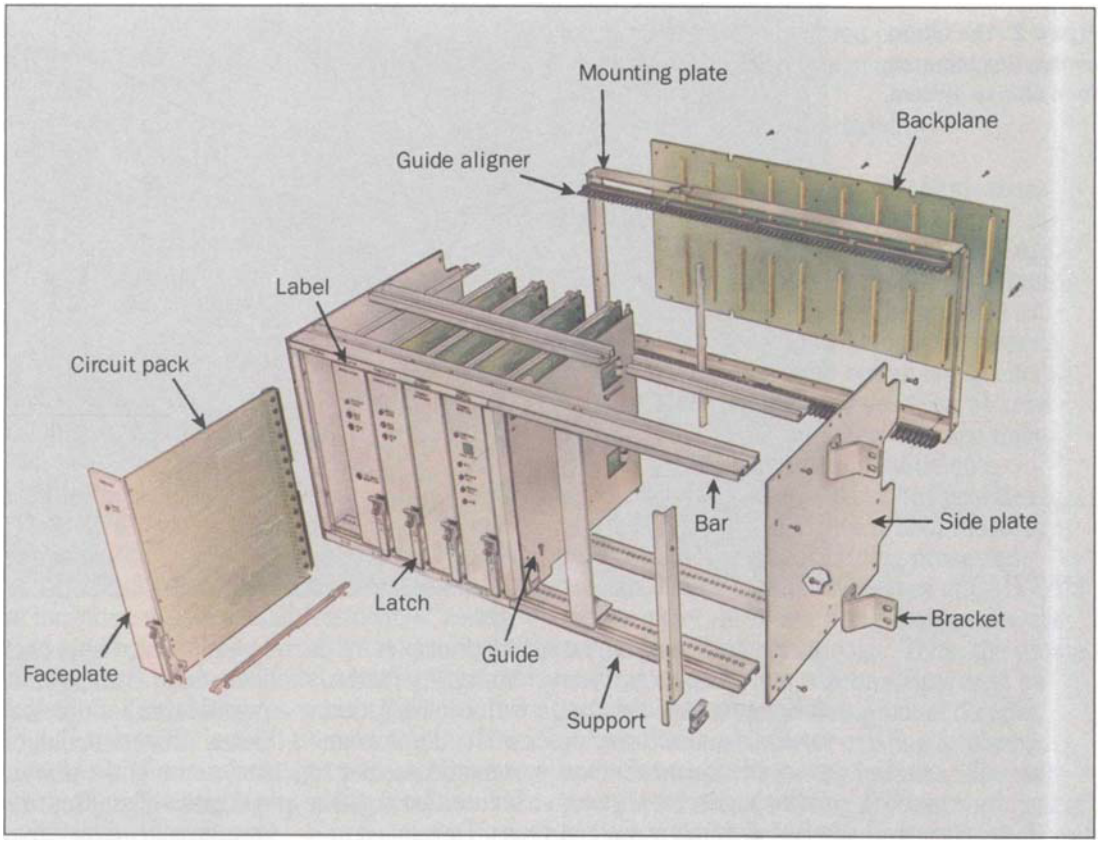

Figure 3. A representative circuit pack housing.

designed and characterized hardware system. The result has been the most trouble-free interconnection hardware ever provided to system developers. There are currently over 2 billion connector contacts in service.

- *Support.* The hardware elements are available off-the-shelf to developers. Very detailed application engineering information is published on the basis of thermal, electrical, and mechanical characterization. Prototyping (breadboarding) technology and hardware are also provided.
- *Economy.* Economies of scale result from the manufacturing quantities made possible by the large number of users. Development economies result from a centralized design and support effort. Manufacturing development and support is less expensive because the technology is common to numerous factories.
- *Development Intervals.* Since the manufacturability and reliability of the hardware are known factors, uncertainty is eliminated from system development schedules. AT&T

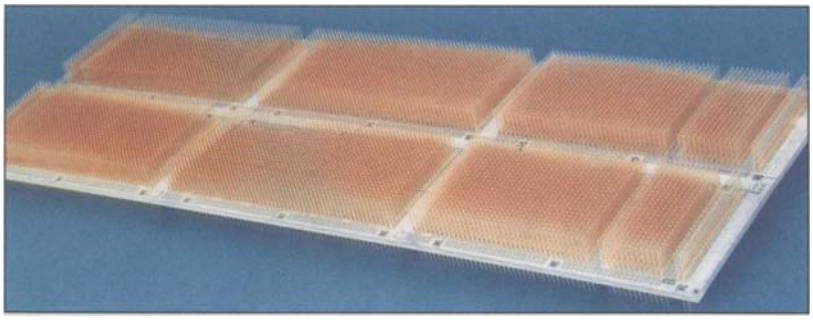

Figure 4. A compliant-pin backplane contains press-fit pins on a 0.125-inch grid.

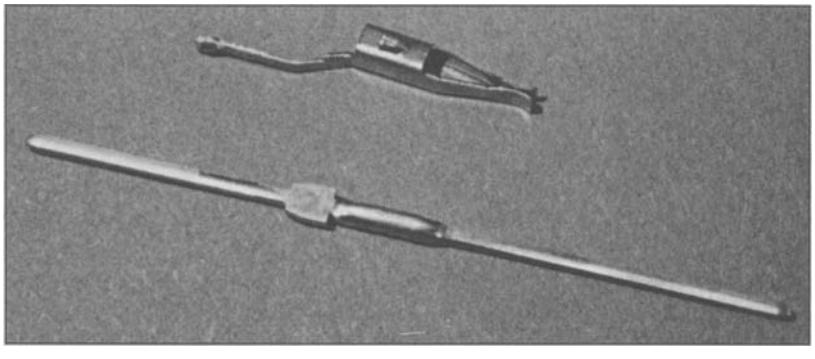

Figure 5. Circuit pack connector (top) and the mating compliant pin.

has manufacturing technology in hand, applications engineering is readily available, and detailed performance information is already known. As a result, system physical design intervals are reduced by 50 percent or more.

Physical Design Concepts

The Fastech system hardware family covers a broad range of options in circuit pack sizes, pin-out densities, and shelf configurations. These options, however, all stem from a small set of parts and a common design concept.

The exploded view of Figure 3 illustrates the physical design of a representative circuit pack housing. The circuit pack connectors contain receptacle contacts that mate with 25-mil-square pins which are press-fit into an epoxy glass backplane. The circuit packs, connectors, and backplanes are described in more detail in later sections. Proper alignment of the circuit card to the pin field is assured by the parts labeled "card guide" and "guide aligner" in Figure 3.

Compliant-Pin Backplanes. A large degree of design flexibility is inherent in the backplane system. The backplane provides interconnections between functional circuit packs. No electrical devices, either active or passive, are attached to the backplane. It is strictly a level 3 interconnection structure that is populated with press-fit pins. All pins are placed on 0.125-inch-grid positions; however, only those columns of pins required for mating with circuit card connectors or other connectors need be installed. Interconnections among pins in the backplane can be provided by any combination of printed wiring (double-sided or multilayer), manual wiring, automatic wire-wrap, and backplane cables.

On the circuit pack side, three lengths of pins are provided to allow the sequencing of electrical connections to the circuit cards. This is particularly useful when circuit packs must be inserted or removed while the rest of the system remains in operation. In such cases, it is advantageous to make ground, power, and signal connections in that order.

A backplane arranged to accommodate up to forty-two 8-inch-high circuit cards is illustrated in Figure 4. This backplane is approximately 24 inches wide and contains a full complement of 10,800 pins.

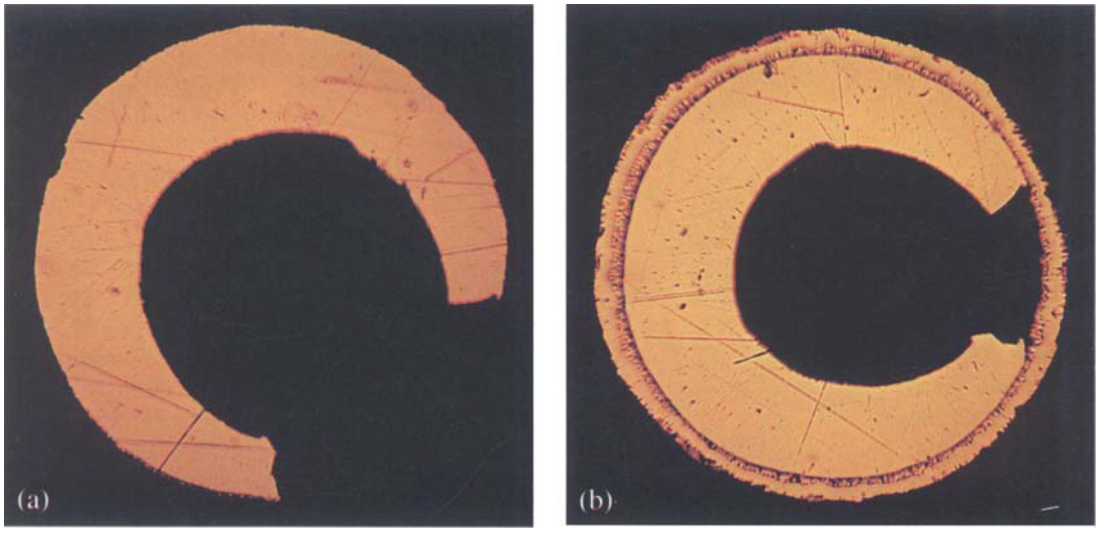

Figure 6. Photomicrographs of a compliant-pin cross section (a) before and (b) after insertion.

Compliant Pins and Connectors. The reliability of the compliant pin-to-backplane interface has been established by AT&T studies over the past 10 years.[2,3,4]

Experience has been accumulated with over 2 billion pins manufactured to AT&T specifications. The compliant region is in the center section of the pin shown in Figure 5. The large square shoulder section of the pin appears on the circuit pack side of the backplane and is provided to aid the insertion process. Also shown in Figure 5 is the contact which is the basis for Fastech system connectors.

A cross-section view of the compliant section before and after insertion is shown in Figure 6. The compression of the pin and the intimate contact between the pin and the surrounding plated-through hole are clearly shown. This gas-tight interface provides a very reliable electrical contact.

The circuit card connectors that mate with the compliant pins use bifurcated contacts as shown in Figure 5. The contacts are assembled into various plastic housings to provide a family of circuit pack connectors. The connector family is modular in two dimensions. Nominal heights of 4 and 8 inches are available. The connectors provide variable numbers of pin-outs by adding additional columns of backplane pins. Connectors are available to mate with two, three, four, six, and eight columns of pins. The eight-column connector provides 400 pin-outs on an 8-inch-high circuit pack.

The lower-density connectors, with two or three columns of contacts, are attached to circuit packs by heat staking. Electrical connections are made by wave soldering the terminals of the connector contacts into plated-through holes in the circuit packs at the same time as other through-hole-mounted components are soldered to the circuit packs.

The higher-density connectors, with four, six, and eight columns of contacts, are screwed to the circuit cards. Electrical connec-

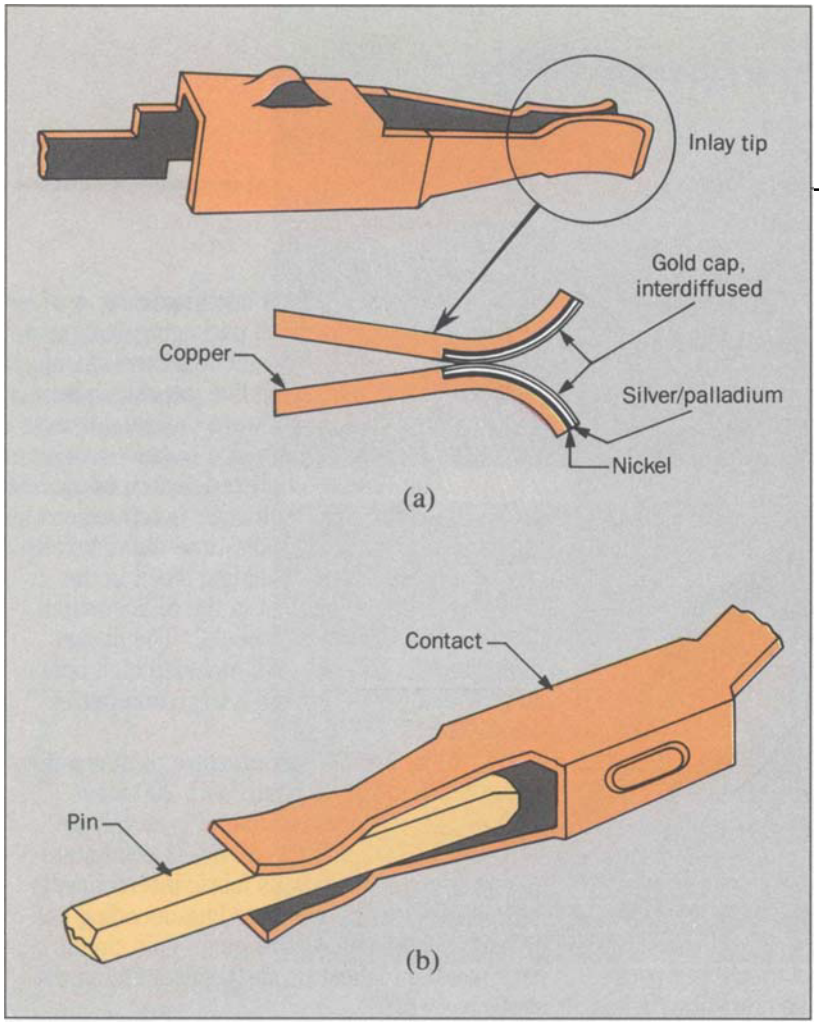

Figure 7. Copper connector contains inlays of nickel, silver/palladium, and gold (a). The inserted pin (b) contacts these layers.

tions are made in a separate mass-soldering operation which attaches terminals of the connector to their corresponding lands on the circuit packs.

The connector contact is bifurcated to provide two points of contact with the backplane pin (Figure 7). The wiping action of the contacts as the pin enters minimizes the chances of contaminants lodging between contact surfaces. Also, any insulating film that might be present is broken up, and a clean contact surface is thus provided. This dual-contact design thus ensures low contact resistance and high contact reliability. A contact force of 100 to 150 grams is expected over the life of the connector.

The base metal used in the contact is CDA 725, an alloy of 80 percent copper, 9 percent nickel, and 2 percent tin. This alloy was chosen because it offers a good balance of qualities required in a contact. These are formability, good spring characteristics, solderability, conductivity, and reasonable cost. Originally, the contact area of the terminal was electroplated with gold hardened with cobalt. However, the plated surface has been replaced with an inlay of diffused gold. This is a sandwich of materials consisting of an underliner of nickel, an alloy core composed of palladium and silver, and a cap of gold that has been interdiffused to produce an alloy with a nominal gold content at the surface.

Circuit Packs. The Fastech standards encompass a family of circuit pack sizes. The selection of a proper circuit pack size is an important system partitioning decision that can have a major influence on the reliability, maintainability, and manufacturability of the system. Figure 8 shows the range of circuit pack sizes offered by Fastech technology and the maximum pin-out capability for each circuit pack height. The electrical function that is being partitioned has a strong influence on appropriate circuit pack size. Typically, those system elements that are performance-oriented tend to avoid the delays and distortion associated with signals that are transmitted through multiple circuit packs, and therefore tend to partition into the larger circuit packs. The smaller-sized packs tend to be used in those portions of the system in which small failure groups are important. Other factors, such as overall physical size restrictions and manufacturing complexities, must also be considered. The Fastech packaging system offers pack sizes to accom-

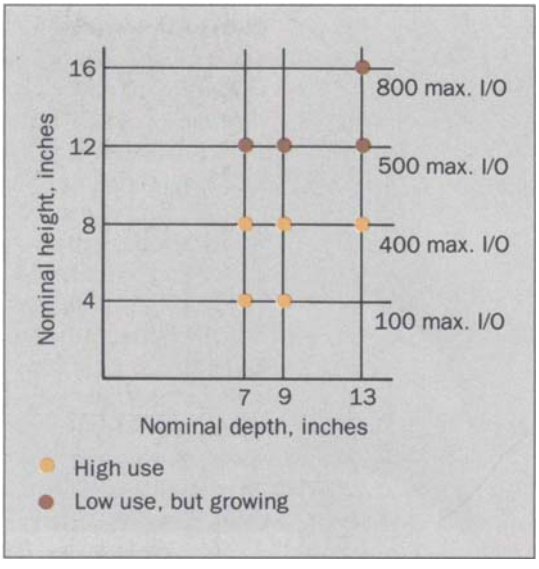

Figure 8. Fastech circuit-pack sizes and their maximum pin-out capacity.

modate a wide variety of partitioning needs, yet retains a commonality of design that permits factories to utilize many of the same production facilities for the various-size packs.

Circuit packs may be fabricated in a variety of printed wiring technologies. Choice of circuit pack technology is dictated by many factors, including cost, electrical performance, thermal performance, and interconnection density. Fastech designs are currently supported in the following circuit pack styles:

1. Double-sided epoxy-glass board
2. Four-layer multilayer board
3. Six-layer multilayer board
4. Multiwire® board (registered trademark Kollmorgen Corp.)
5. Wire-wrap board
6. Quick-connect board.

The last two board styles are designed for rapid system breadboarding and are available as off-the-shelf parts to be wired by the user.

Two examples of circuit packs designed with the Fastech packaging system are the 5ESS switch time-multiplexed-switch fabric pack and the analog line interface pack shown in Figure 9. They were designed using the standard 8-by-13-inch size board.

The time-multiplexed-switch fabric pack is an eight-layer multilayer board which functions as a 62-by-32 port time-multiplexed switch and serves as a building block in the growable 192-by-192 port in the 5ESS switch communication module model 2. The design requirements for this pack included high operating speed (65 MHz) and a large number of input/outputs (400).

The analog line interface pack is a double-sided rigid circuit board with 200 input/outputs and requires the use of high voltage (300 V dc) to control the 32-by-32 solid-state analog switch fabric. This fabric interconnects subscriber lines to digital coding-decoding and service circuits such as ringing. This circuit pack has the highest production volume in the system.

Connector Assembly

The high-density connectors, which have four, six, or eight columns of contacts, provide up to 64 pin-outs per inch of circuit pack height. Because these connectors are surface-mounted to the board, they require a different manufacturing process than the low- and medium-density through-hole-mounted connectors. High-density connectors are assembled to the circuit board after the component-soldering operation. They are physically connected to the circuit board with self-tapping screws and are electrically connected by soldering the tails of the connector contacts to corresponding pads on both sides of the circuit board.

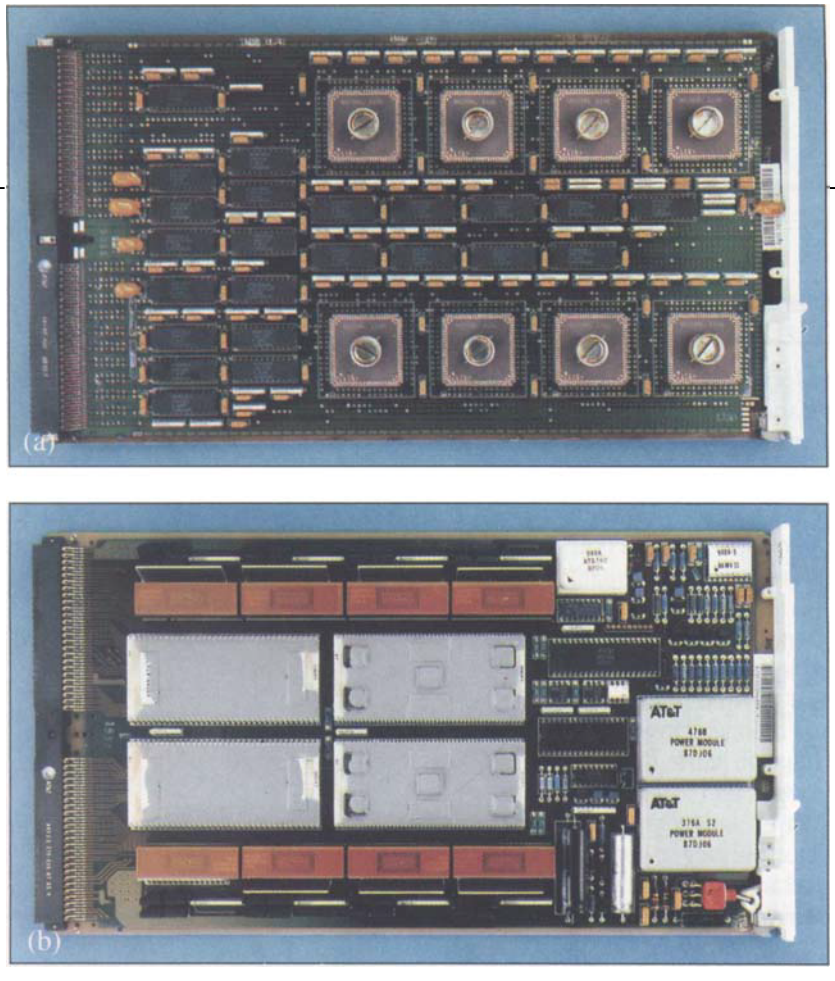

Figure 9. Examples of circuit packs designed with the Fastech packaging system: (a) time-multiplexed-switch fabric pack, (b) analog line interface pack.

The need for a reliable, stress-free solder joint dictated that a noncontact soldering process be used. This requirement, coupled with the need for visual inspection of the solder joints, led to the research and development of a new soldering process called "convection heating with solder addition." This process heats the surfaces to be soldered simultaneously while solder is added to the joint area.[5]

Work in the area of convection heating and in the design of a new solder-feed mechanism was undertaken to develop a process that would continuously produce reliable solder connections at a low cost while providing the following:

1. Rapid heating of the soldering area to soldering temperature.
2. Maintenance of near-constant temperature during the soldering cycle.
3. Confinement of heating to the soldering area.
4. Maintenance of the board temperature below critical values.
5. Consistent production of reliable, sight-inspectable solder fillets.
6. Optimization of the soldering cycle time to maximize output.

The convection-heating process and the solder-feeding mechanism were implemented in a facility for soldering surface-mounted connectors to Fastech boards. The convection-heated, reflow-soldering system consists of a board-holding fixture attached to a shuttle, two heating modules, a solder-feeding

Table I. Electrical Characterization of Circuit Packs

Circuit pack style	Characteristic impedance, ohms	Propagation delay, ns/ft	Signal rise time, ns	Bandwidth, MHz	Maximum intralayer pulse crosstalk (near-end), %	Maximum interlayer pulse crosstalk (near-end), %
Wire wrap	125 ± 50	1.4	2.0	250		40
	160 ± 35	1.3	1.8	278		35
Double-sided	150 ± 20	1.5	2.6	190	21	39
(epoxy)	150 ± 20	1.5	2.6	190	24	34
Six-layer multilayer	75 ± 30	1.8	2.5	200	40	32
board (external	70 ± 35	1.8	2.5	200	46	16
power/ground)						
Six-layer multilayer	85 ± 25	1.8, 1.5*	1.8	278	22	16
board (internal	75 ± 15	1.8, 1.5*	1.8	278	26	14
power/ground or						
surface routing)						

*Values pertain to surface routing.

NOTE: The upper entries for the wire-wrap data apply to Milene® (trademark of W. L. Gore & Assoc.) insulation; the lower entries apply to Teflon® (trademark of Dupont) insulation. The upper entries for all other circuit pack styles apply to conductor width of 8 mils and spacing of 9 mils; the lower entries apply to 12-mil width and 13-mil spacing.

mechanism for each module, and a central control cabinet.

Electrical and Thermal Characterization

The development of a standardized physical design made possible a comprehensive effort at electrical characterization. The goal of this effort was to provide a complete electrical characterization of the Fastech system so that the system and circuit designers could predict the performance of their designs.

Studies have been made on the electrical properties of Fastech connectors, cables, and circuit packs. The transmission properties of the connector family were studied and found to be adequate for the circuit pack needs of most present development projects—that is, those with signal rise times of 1 ns or greater or with bandwidths of 400 MHz or less. Another study showed the stability of the electrical connection from the circuit pack to the backplane through the connector. Changes of less than 0.80 milliohm were observed over the lifetime of the connector (200 insertions and withdrawals). Studies of pulse transmission properties (characteristic impedance, propagation delay, rise time, and bandwidth) were made for Fastech circuit pack styles. Detailed evaluation of crosstalk properties, which are strongly geometry-dependent, became possible.

Table I is adapted from Reference 6,

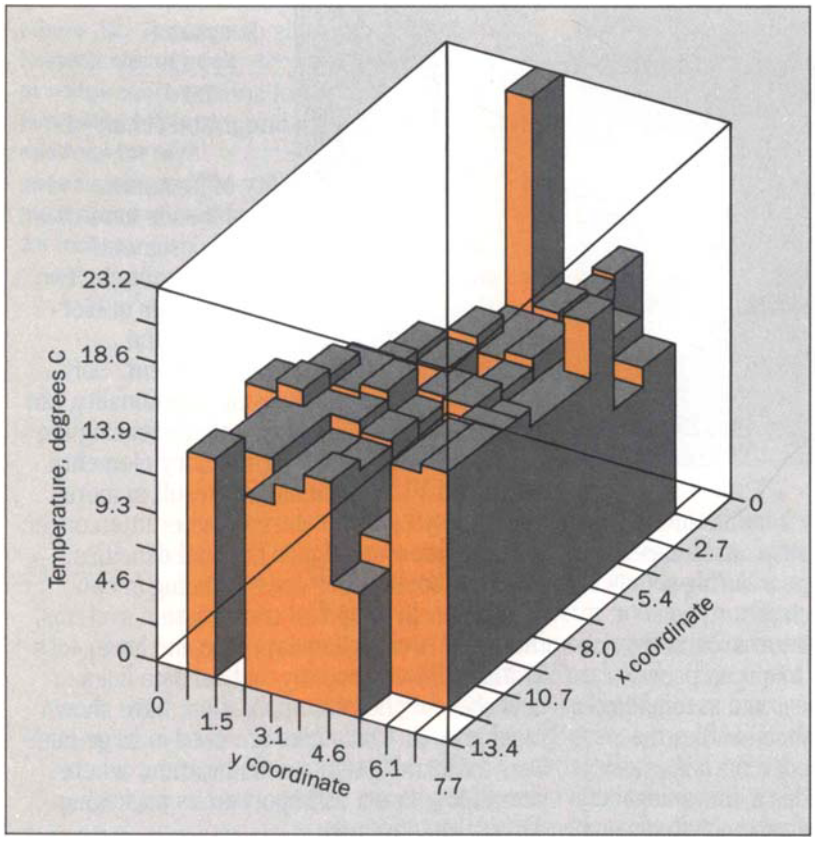

Figure 10. Representative thermal information produced by computer-aided design system.

which presents theoretical results and scaling laws that extend the application of the crosstalk results to arbitrary pulse signals, periodic signals, and random signals. The material has been used to help choose an appropriate circuit pack style, and to estimate crosstalk (either manually or for post-routing analysis, using the CAD system), conductor capacitance and inductance, and the effects of proposed new dielectrics or geometries.

Similarly, an earlier study on current-carrying capacity was applied and extended to encompass all the Fastech system styles of printed wiring. Once again, the standardization associated with the Fastech system made this detailed analysis feasible.

The standardization inherent in Fastech hardware provides an opportunity for generalized thermal characterization. (There is a good analogy to the electrical characterization described above.) An extensive program of analytical and experimental work was carried out by a thermal design task group formed of representatives from most AT&T R&D locations. The results of the work have been incorporated in the thermal design chapter of the Fastech System Guidelines. The main body of the thermal design chapter consists of charts and graphs that allow thermal designers to predict component temperature rises in equipment frames of varying configurations. The effects of varying a large number of parameters can be evaluated. For example, charts are provided to relate temperature rises (using forced convection cooling) to power density, circuit pack spacing, location on the circuit pack, channel height, presence or absence of baffles, nonuniform heating conditions, board depth, presence or absence of covers, altitude, and air velocity.

Much of the information available in charts is also embodied in a system of computer aids to thermal design. In addition to computer simulation capabilities, an extensive set of experimental test facilities has been established. The Fastech system thermal test laboratory allows simulation of specific hardware configurations found in actual frame designs. CAD tools can predict the circuit pack's thermal performance before the pack is actually constructed. Figure 10 shows an example of thermal information generated by the

Figure 11. Standard Fastech multifiber array connector for lightwave communication systems.

CAD system. This information allows the circuit designer to identify "hot spots" and evaluate alternative component placements.

Prototyping Aids

One of the primary benefits of the Fastech packaging system is the assistance that is offered to system developers during prototype development. A Fastech prototype assembly shop provides fast-turnaround service for assembly of connectors to circuit packs, inserting pins into backplanes, and assembling complete shelf units. This shop handles the small quantities that are needed for laboratory development and also provides a convenient setting for investigating new assembly tools and techniques.

The prototype shop also provides a variety of prototyping tools that are needed during laboratory development. These items are available "off the shelf" and include such commonly used items as extender boards and wire-wrap boards.

Evolution of the Fastech System

The technological forces acting on the designers of electronic systems are well known. Among these forces are:

1. Increasing demands on system functionality
2. Explosive growth of software
3. Rapidly advancing integrated circuit technology
4. Increasing applicability of photonics.

These technological trends have concrete implications for physical designers. Systems obtain increased functionality by two methods—by increasing the number of electronic elements and by increasing the performance (speed) of each element. Software also provides increasing functionality, but at the inevitable cost of greatly increasing the number of semiconductor memory elements. Advanced VLSI technologies result in more compact systems, requiring higher interconnection densities and higher thermal densities. Photonic applications are advancing in two directions. In long-haul transmission systems, the trend is to higher-data-rate and lower-loss systems. More recently, optical data links, a new class of photonic application, have shown rapid growth. Data links are used in large numbers for intrasystem communication, where overall loss is not as important as packaging density and low cost.

The technological changes described above affect all system designs. Competitive systems cannot be built from outdated technology.

If Fastech is to retain its position as a widely used AT&T packaging standard, it must provide on a continuing basis for the incorporation of new technologies. The challenge to the developers of Fastech is to define an evolutionary path which retains as much compatibility with the previous system as possible. Three examples of recent extensions to Fastech illus-

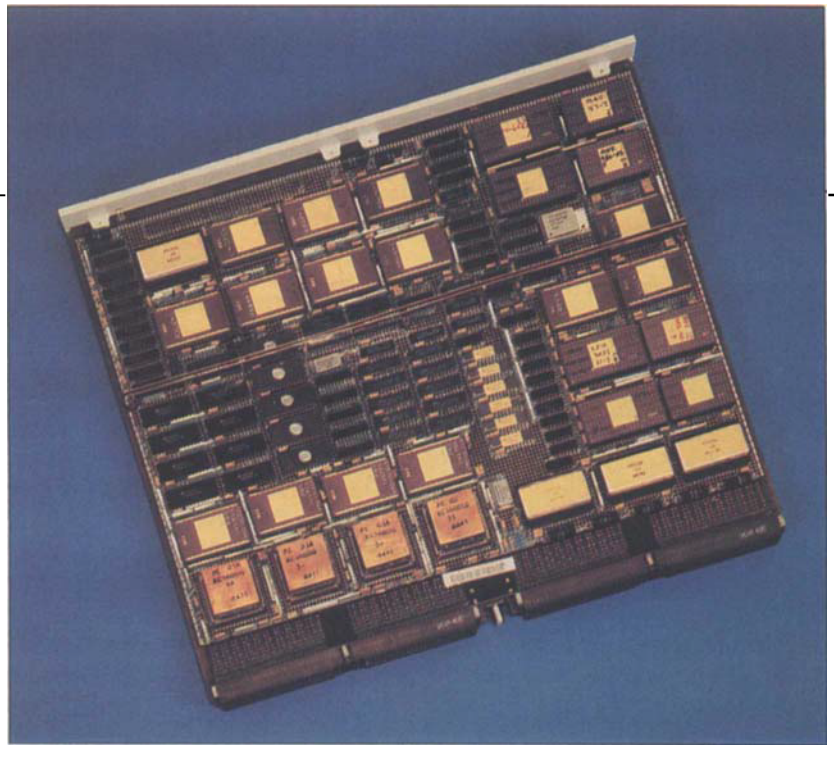

Figure 12. The largest Fastech circuit pack provides short, well-controlled interconnections for high speed systems. The pack measures 16 by 13 inches.

trate this strategy. The first example (Figure 11) shows an optical multifiber-array connector (MAC) which has become a standard Fastech offering. A single connector housing provides up to 18 low-loss multimode connections from a circuit pack through the backplane. The fibers can be either individual jacketed fibers or can be fiber ribbon arrays. Because the MAC is compatible with all existing Fastech connectors, circuit packs, insertion levers, and shelves, it provides a major technology extension without making previous hardware obsolete. The second example (Figure 12) illustrates the largest Fastech circuit pack, which is roughly 16 by 13 inches. The driving force for the large circuit pack was electrical performance. In some high-speed systems, the interconnection delays introduced by connections between adjacent circuit packs can hamper system performance. The 16-inch-high circuit pack allows the design of short, well controlled interconnections among key circuit elements.

The third example (Figure 13) emphasizes the flexibility of Fastech to incorporate additions within its interconnection system to accommodate varying system needs. This example is the hardware designed by Fastech to be used in the 5ESS integrated services line unit (ISLU).

The 5ESS ISLU is an integrated analog and digital line unit which can handle high traffic most economically as well as enhance the 5ESS switch with the ability of establishing customer interface into ISDN. It can accommodate the high traffic volume by supplying each subscriber with dedicated circuitry, in addition to allowing the flexibility to change the customer interface from analog to digital as customer needs change. These abilities are the inherent features of a single-line packaging strategy.

The packaging system designed for 5ESS ISLU represents the ability in Fastech to package a system that is different from the standard 23-inch-shelf configuration. The

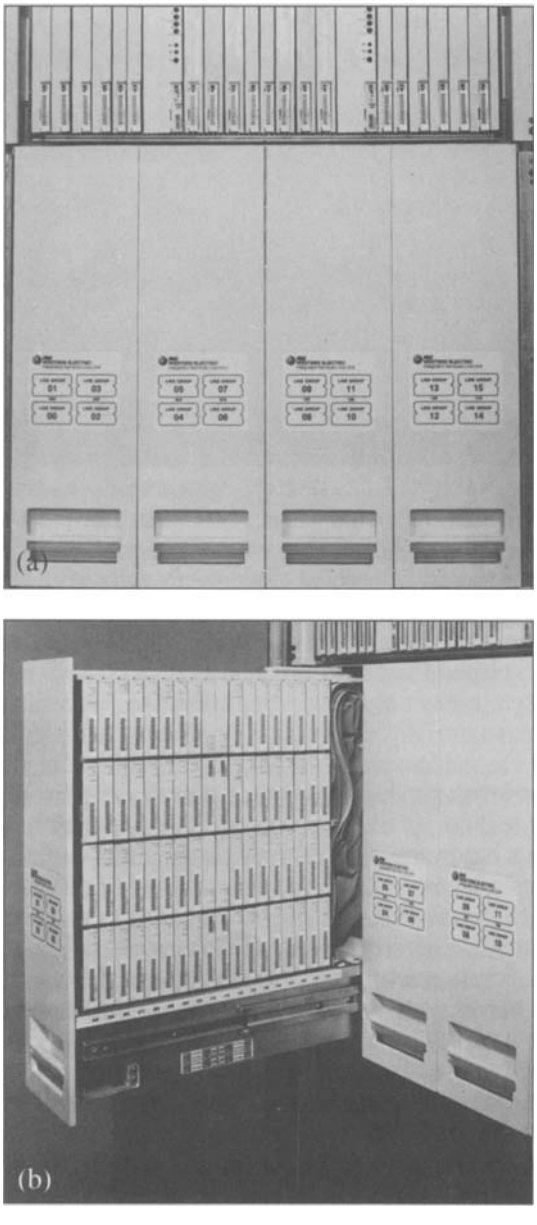

Figure 13. Integrated services line unit for the 5ESS switch was designed in a drawer configuration (a). Each drawer (b) can hold 128 circuit packs.

nature of the architecture proposed for ISLU dictated the packaging scheme most suitable for a single-line system in order to optimize on single line reliability (because the most critical reliability requirement that the ISLU must satisfy is the downtime of a single line) and, at the same time, provide versatility within the overall system.

Because single-line rather than multiple-line packaging was required in the ISLU, the best approach was to package the unit in a "drawer configuration," in which small individual circuit packs could be assigned to each customer. Circuit pack size is 2.5 by 3.5 inches. Each drawer can support 128 circuit packs. Four drawers compose a unit, which thus houses a total of 512 circuit packs per unit. Each drawer has umbilical cabling attached so that as a drawer is accessed (pulled out of the cabinet frame on slides), the system remains alive during craftsperson interface. Thus if an individually packaged line circuit fails, the craftsperson can immediately replace it without affecting other customers. Such a packaging scheme can be applied effectively to other systems that require individual line interface circuits. Another advantage to drawer-type packaging is that it is the most space-efficient method of providing the single-line circuit design.

Summary

The physical design of an electronic system requires careful consideration of every element of the system's make-up. Each packaging option must be examined in terms of cost, performance, reliability, and manufacturability. The goal of the Fastech integrated packaging system is to provide AT&T designers with proven standardized packaging options

that can shorten the design process and provides economies of scale. The Fastech system has been used in AT&T products since the mid 1970s and will continue to be used well into the 1990s. The longevity of the system is testimony to the usefulness of carefully chosen design standards. Eventually, advances in device technology will create packaging needs that cannot be accommodated by the existing Fastech system. Increasing circuit pack input-output, increasing power consumption, the increasing use of fiber optics, the need for more sophisticated thermal management, and the need for faster signal speeds are all well established trends. AT&T will continue, however, to develop new packaging systems that maintain the high level of productivity and quality established by the Fastech integrated packaging system.

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system from 1978 to 1986. He received a M.S. in mechanical engineering from Stanford University in 1979. Ms. Cole is supervisor of the Fastech System Technology Group. She is responsible for design and development of hardware elements for the Fastech packaging system. She received a B.S. in mechanical engineering from Tuskegee University and the M.S. in engineering science and mechanics from Georgia Institute of Technology. She joined AT&T in 1980.

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