REPORT:

BASIC ACCESS NETWORK TERMINATION CHIP FOR ISDN 4-WIRE LOOPS

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Introduction

In this article, we describe an AT&T CMOS chip, the T7252, which simplifies the line interface design on the network side of a four-wire ISDN basic access subscriber loop. (CMOS stands for complementary metal oxide semiconductor; ISDN is the Integrated Services Digital Network.) Called UNITS (*user to network interface termination for switches*), the T7252 implements the CCITT (International Telegraph and Telephone Consultative Committee) I.430 Layer 1 physical link "2B + D" standard.[1] This customer premises subscriber loop provides integrated voice and data transmission at 192 kilobits per second (kb/s) on separate transmit and receive twisted pairs. The basic transmission interface supports two 64-kb/s B channels and one 16-kb/s D channel, with 48 kb/s used for framing, control, link maintenance, and synchronization. (B stands for bearer channel; D stands for demand channel.)

The network end of a subscriber loop is called an NT (network termination). The loop may form a passive bus supporting up to eight terminal endpoints (TEs). (See Figure 1.)

ISDN standards define several reference points and functional groups. The "S" reference point is a subscriber side demarcation point for basic access at 192 kb/s. NT1 and NT2 provide NT functions, connecting the subscriber to the network. NT2 provides subscriber side termination. NT1 provides access to the network. NT2 can provide switching functions; NT1 cannot. NT1 provides Layer 1 bit multiplexing only.

The UNITS chip is tailored to the NT application, typically a line card in a digital switch such as a private branch exchange (PBX) or a Class 5 central office (CO). A companion chip, T7250A, called the UNITE™ chip and separately optimized for TEs (e.g., digital telephones, terminals, and personal computers), was profiled in an earlier article in the *AT&T Technical Journal*.[2] For a general review of ISDN concepts, see *AT&T Technical Journal*, Vol. 65, No. 1,[3] and Appendix A of this article.

Highlights

The UNITS chip has many system-level assets that minimize component count, board space, development time, and cost. Some features that are valuable to *hardware* designers are:

- A flexible microprocessor interface with 16 programmable on-chip registers.
- Fully adaptive timing circuit for all link configurations.
- Multi-framing support for physical link (Layer 1) maintenance.
- Power-down mode of operation.
- High-impedance outputs for board-level testing.
- Two data transport highways with assignable time slots for voice or data transfer.
- Speed selection on the serial highways from 256 kHz (4 time slots) to 4.096 MHz (64 time slots).
- Suitable for NT1 and NT2 applications.

Features valuable to *software* designers include:

- Maskable interrupt conditions.

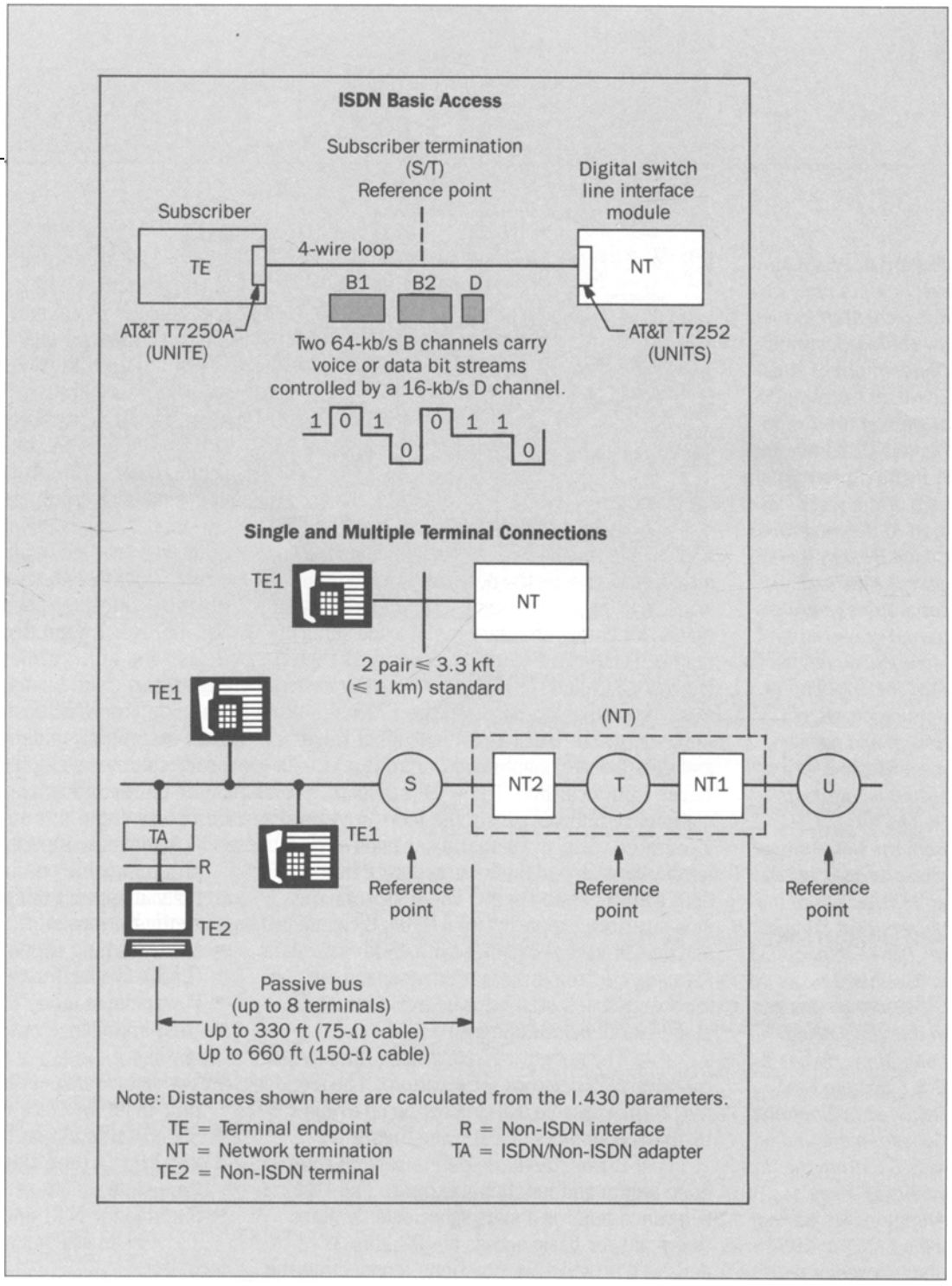


Figure 1. ISDN basic access. The "T" reference point separates the NT2 and NT1 functional groups. Phone terminals can connect to the network at the S or T reference point. Because electrical interface is identical at S or T, the symbol "S/T" is frequently used. The "U" reference point identifies the network side.

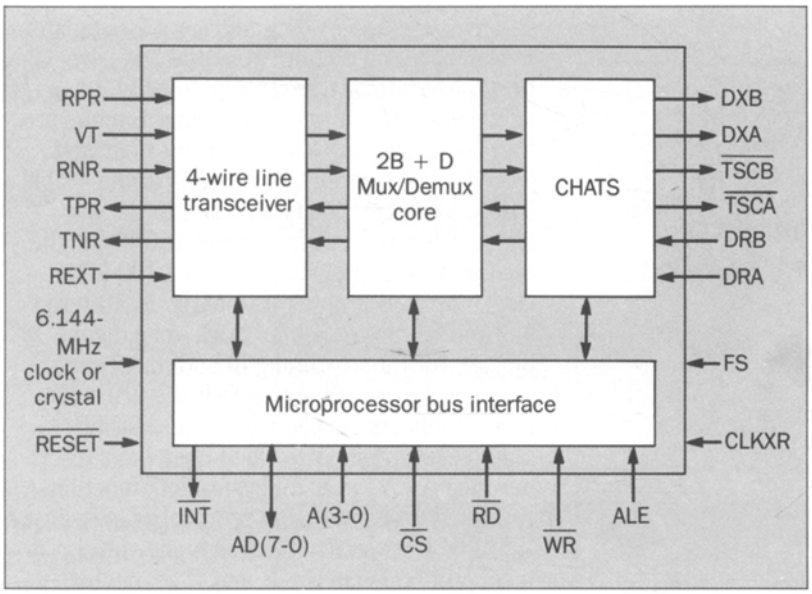


Figure 2. Building blocks of the AT&T *UNITS chip for ISDN*. CHATS stands for Concentration Highway access for time slots.

- Fourteen different loopback modes.
- Programmable control of B- and D-channel time slots.
- Read/write control of a memory-mapped register set.

Building Blocks

System interface flexibility is achieved on the T7252 UNITS chip by using four building blocks: the *4-wire line transceiver*, the *2B + D multiplex/demultiplex core*, the *Concentration Highway access time slot* (CHATS) interchange, and the *microprocessor bus interface*. (See Figure 2.)

The *4-wire line transceiver* handles time-multiplexed 2B + D transmissions to and from the 4-wire physical link. The *2B + D core* transfers data back and forth between the 4-wire line transceiver block and the CHATS block. The core interprets the stream received from the line transceiver and separates the B-channel and D-channel bits. Conversely, the 2B + D core inserts B-channel and D-channel bits obtained from the CHATS block into link frames, then sends them to the line transceiver interface for transmission to the subscriber.

The *CHATS* block provides access to the serial transport highways that carry B-channel and D-channel time slots. The highway interchange can be configured to meet a variety of system interfaces. Each channel is assigned a time slot under microprocessor control. The *microprocessor bus interface* is the window through which the UNITS chip is controlled. Chip operation is programmed using the 16 registers listed in Table I.

Four-Wire Line Transceiver

The 4-wire line transceiver interface (Figure 3) supports the encoding and decoding of the 2B + D stream in the alternate space inversion line-code signal format. In this line coding scheme, a binary "1" is represented by the absence of a pulse, and a binary "0" (or space) is represented by alternating positive and negative pulses.

Transmission occurs over four wires, normally twisted pair cable composed of 26-gauge wire, between the NT and the TE(s). The transceiver interface contains an analog transmitter and receiver, which are to be connected to external transformers. The line-driver circuit collects the 2B + D signals from the multiplex/demultiplex core, frames the channels, and transmits the stream to the TE(s).

The line-receiver circuit performs filtering, timing recovery, frame synchronization,

Table I. UNITS Chip: Register Overview

Name	Read/Write	Function
R0	R/W	Highway Configuration—Transmit Highway
R1	R/W	Highway Configuration—Receive Highway
R2	R/W	Time Slot Offset—Transmit Highway Data
R3	R/W	Time Slot Offset—Receive Highway Data
R4	R/W	Loopback & Exchange Control
R5	W	Transmit Data Exchange
R6	R	Receive Data Exchange
R7	R/W	Interrupt Masks & Time Slot control
R8	R/W	Multiframe—S & Q bits
R9	R/W	Transmit B1 Channel Time Slot
R10	R/W	Transmit B2 Channel Time Slot
R11	R/W	Transmit D Channel Time Slot
R12	R/W	Receive B1 Channel Time Slot
R13	R/W	Receive B2 Channel Time Slot
R14	R/W	Receive D Channel Time Slot
R15	R	Interrupt Status

and threshold slicing, recovering the 2B + D signals from the TE(s) and passing them to the core. In conformance with the CCITT I.430 Recommendation, the transceiver supports point-to-point as well as point-to-multipoint (passive bus) applications. Multiframe and activation/deactivation procedures are also provided under microprocessor control. Adaptive signal processing on incoming line signals ensures reliable operation for all allowed link configurations over commonly used twisted wire pairs.

2B + D Multiplex/Demultiplex Core

The 2B + D multiplex/demultiplex core (Figure 4) receives the 192-kb/s subscriber stream from the line receiver and extracts the B- and D-channel information. The channels are saved in holding registers for transfer to time slots on one of two serial highways (described later). Conversely, to send 2B + D information to the subscriber line, the bits are first received from one of the two highways, placed in designated bit positions of the 48-bit basic-access frame, then routed to the line transmitter for transmission at 192 kb/s. The multiplex/demultiplex core uses a 192-kHz clock, derived from a 6.144-MHz ± 100 parts per million (ppm) master clock via a digital divider, for its link timing in both directions.

It is worth noting that the 2B + D core is only concerned with time-division-multiplexed transport of bits over the subscriber loop (i.e., Layer 1 physical link functions). It doesn't do higher level protocol processing on any B or D channel. It leaves higher level protocol processing in the B and D channels to circuits external to the chip.

CHATS Interchange

The *Concentration Highway* is a dual transport interface that carries serial bit streams back and forth between the UNITS chip and the switching system. Two pairs of transmit and receive paths on the Concentration Highway are realized using eight signals, grouped as follows:

- Clock group: CLKXR, FS
- Transport Group A: DXA, DRA, $\overline{\text{TSCA}}$
- Transport Group B: DXB, DRB, $\overline{\text{TSCB}}$.

The highway is a time-division-multiplexed (TDM) bus that can be configured to meet a variety of system interfaces.

Data is transmitted (DX) or received (DR) on either one of two transport groups: "A" or "B." The user-supplied clock rate (CLKXR) determines the number of eight-bit

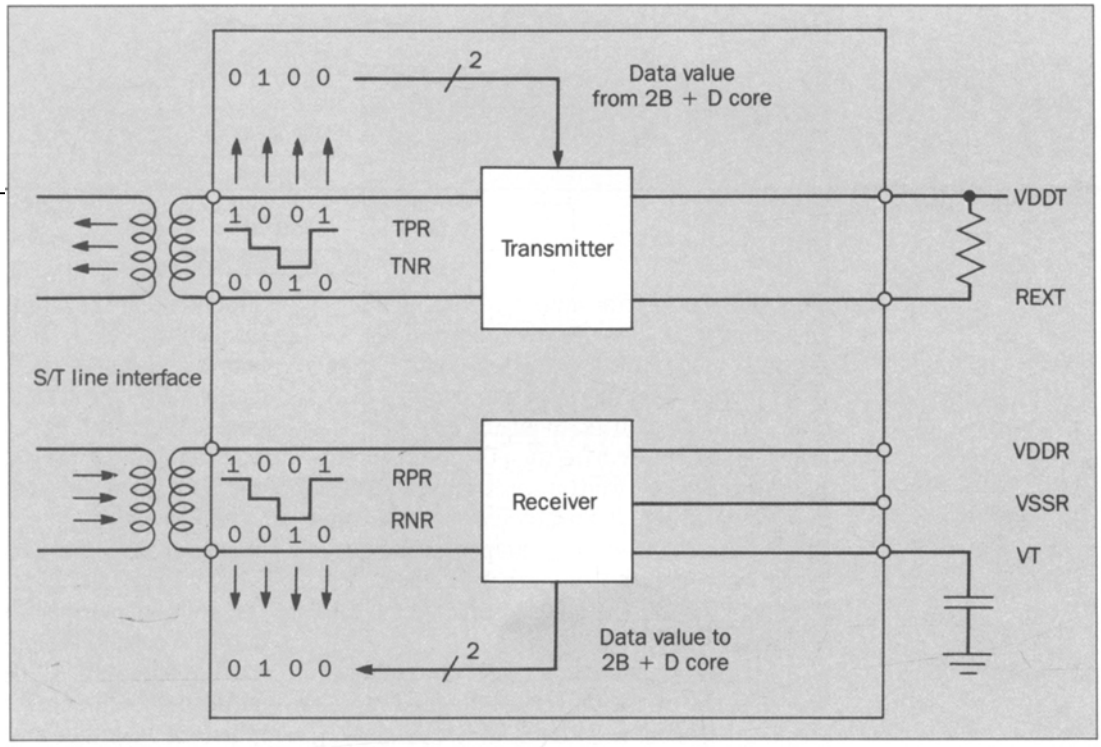


Figure 3. Block diagram of the 4-wire line transceiver.

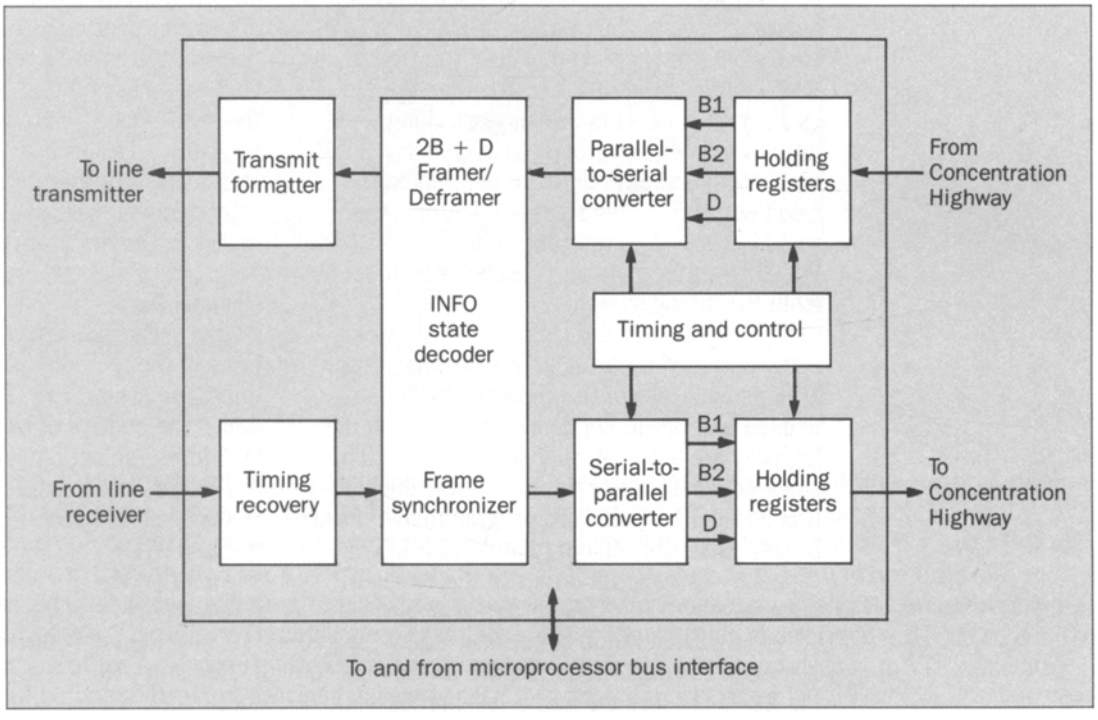


Figure 4. Block diagram of the 2B + D multiplex/demultiplex core.

time slots on the transmit or receive paths. Individual time slots are referenced to the frame synchronization pulse (FS), which is an 8-kHz signal. Time-slot control signals $\overline{\text{TSCA}}$ and $\overline{\text{TSCB}}$ can be used to enable optional external buffers to drive the DXA or DXB output lines. Having two transport groups allows substantial design flexibility. For example, both groups may be used to accommodate increased traffic, or one of the groups may be used as a "hot standby" for the other to provide fail-safe operation.

The transmission speed on the highway depends on the bit rate of the highway clock. For example, with a 2.048-MHz clock, 32 time slots are supported in each direction of each serial pair; with a 4.096-MHz clock, 64 time slots are supported in either direction on each transport group (A or B). With a 256-kHz clock, four time slots are supported in either direction on either group. CHATS derives the highway speed directly from the number of clock edges between frame-synchronization pulses. Time slots are programmable for the B1, B2, and D transmit/receive paths to and from the digital switch.

Note that the D-channel time slots carry only two meaningful bits because of the 16-kb/s data rate of the D channel. The six unused bits of the D-channel time slot on the highway are automatically set to "ones." The clock edges used to sample highway information and the FS pulse are programmable, as are bit and time-slot offsets relative to FS. The capability to swap the order of the bits in a highway time slot is also programmable.

Channel time slots received by the *system input steering* circuit (Figure 5) are sent to the 2B + D core for frame-level processing and transmission to the subscriber. In the other direction, data received from the subscriber through the 2B + D core is sent to the system output steering circuit for transmission to the digital switching system. Transmit and receive time slot control is programmed via the highway configuration registers through the microprocessor interface.

Microprocessor Bus Interface

The microprocessor bus interface (Figure 6) allows parallel, asynchronous input/output access to the on-chip registers that control the operation of the device. A general-purpose microprocessor can read or write the registers via either multiplexed or demultiplexed address and data lines, at the designer's discretion. During a register read, bytes to be transmitted to the microprocessor bus are latched, ensuring that changes occurring within the read cycle will not affect data on the bus. Register accesses are sufficiently fast that wait states are rarely required. The hardware interrupt signal may be enabled or disabled using bit masks in the interrupt control register.

Register Bank

The on-chip registers occupy 16 locations in the memory map of the controlling microprocessor. The registers are accessed under the control of the following signals:

- Address select (A0-A3 or AD0-AD3)
- Address latch enable (ALE)
- Chip select ($\overline{\text{CS}}$)
- Read ($\overline{\text{RD}}$)
- Write ($\overline{\text{WR}}$)
- Data (AD0-AD7).

Register functions are shown in Table I. Registers R0-R4 specify operational parameters (clock edges, synchronization offsets, loop control, and channel-insertion control) for the

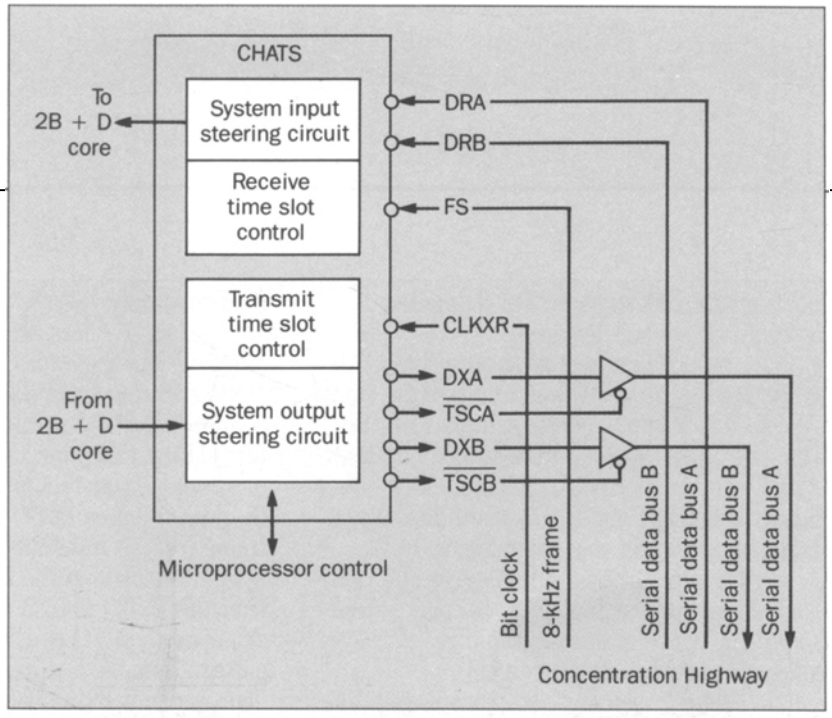


Figure 5. Block diagram of the Concentration Highway access for time slots (CHATS) interchange.

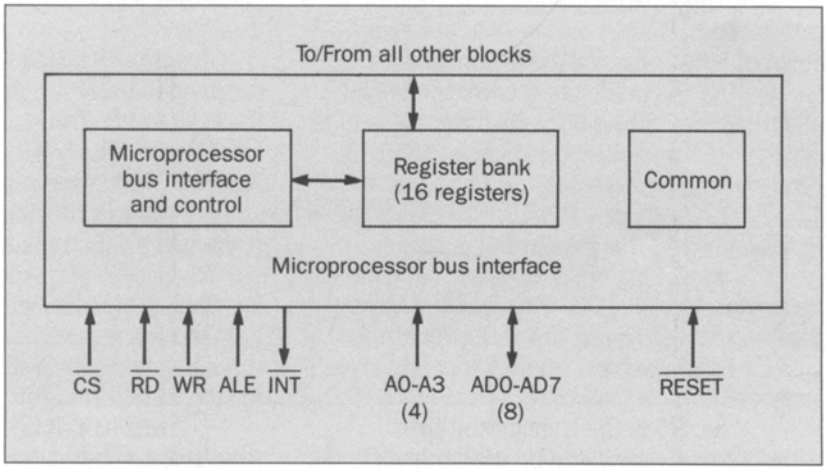


Figure 6. Microprocessor bus interface.

dual Concentration Highway transmit and receive paths. Registers R5 and R6 allow the microprocessor to insert or remove channel information directly. For example, they can be used during chip testing or to place one of the channels (B1, B2, or D) under microprocessor, rather than hardware, control. Interrupt masks and other control are provided in register R7. Four bits in register R8 supply the "Q bits" received in the last multiframe interval, with another four bits controlling the NT-to-TE "S" channel (a multiframe consists of twenty 48-bit frames). Registers R9-R14 are time-slot and highway-transport-group assignment registers for transmitting and receiving B1-, B2-, and D-channel information. Register R15 is the interrupt status register.

The following sections highlight the

functions of each register. For a detailed description, consult Reference 4.

R0. R0 contains programmable fields to specify the *frame edge* parameter (the transition of CLKXR on which to sample FS), the Concentration Highway transmitted-bit offset (range—0-7 bit periods), transmit clock edge (rising or falling), and the transmit leading bit (least significant or most significant first).

R1. R1 contains the received-bit offset, clock edge, and leading bit fields, plus a *fixed timing bit*, which alters the sampling characteristics of the 4-wire line receiver.

R2. R2 specifies the transmitted time-slot offset bits (with a range of 0-63 time slots), the soft reset bit, and the power up/down or active/standby mode control bits.

R3. R3 holds the received time-slot offset and the OPEN bit, which can be used to disable the Concentration Highway when changing register contents. R3 also has a TEST bit, which puts the T7252 UNITS into a special mode for manufacturing purposes.

R4. R4 contains loopback and data-exchange control fields. Fourteen different loopback modes to test link integrity at the CCITT-recommended reference points are supported.

R5. R5 is the transmitted-byte exchange register. It can be used to supply the B1-, B2- or D-channel byte to be transmitted to the 4-wire link. When D-channel bytes are exchanged, only the two least significant bits of each byte are meaningful. R5 is a write-only register. When it is read, it returns internal test points for chip verification after fabrication.

R6. R6 is the received-byte exchange register. It can be used to extract the B1-, B2-, or D-channel bits received from the link. It is read-only.

R7. R7 contains bit fields to specify interrupt masks and to select the transmitted "INFO" frame type. The following interrupt conditions can be masked by bits in this register: (1) the ORed sum of all conditions, (2) missing or extra bipolar line code violations, (3) new received INFO state, (4) start of multiframe (on the transmit side), and (5) new 4-bit Q field received in the last multiframe. The transmit INFO field in R7 specifies whether all zeros or an INFO 0, INFO 2, or INFO 4 frame pattern is to be transmitted. (See Appendix A.) The transmit INFO field can be used to synchronize the line side of multiple T7252 devices.

R8. R8 supplies the four Q bits received in the last multiframe. It also holds the S bits to be transmitted in the next four link frames. The S bits can be written and read; the Q bits are read-only.

R9-R11. R9-R11 contain the Concentration Highway transmit time-slot number and bus-enable bits (transport group A or B) for B1, B2, and D channels. The UNITS chip will not transmit in a given time slot if two or all three channels are inadvertently programmed for the same time slot.

R12-R14. R12-R14 contain the receive time-slot number, a bus-selection bit, and a bus-enable bit for each channel. Only one bus (A or B) can be selected per channel. If two or all three channels are set to the same time slot, the input pin(s) are ignored, causing all ones to be received.

R15. R15 collects the interrupt bits and the received signal field. The interrupt conditions are defined as described for R7 above, and each interrupt-status bit is set to one when the corresponding event occurs. Sta-

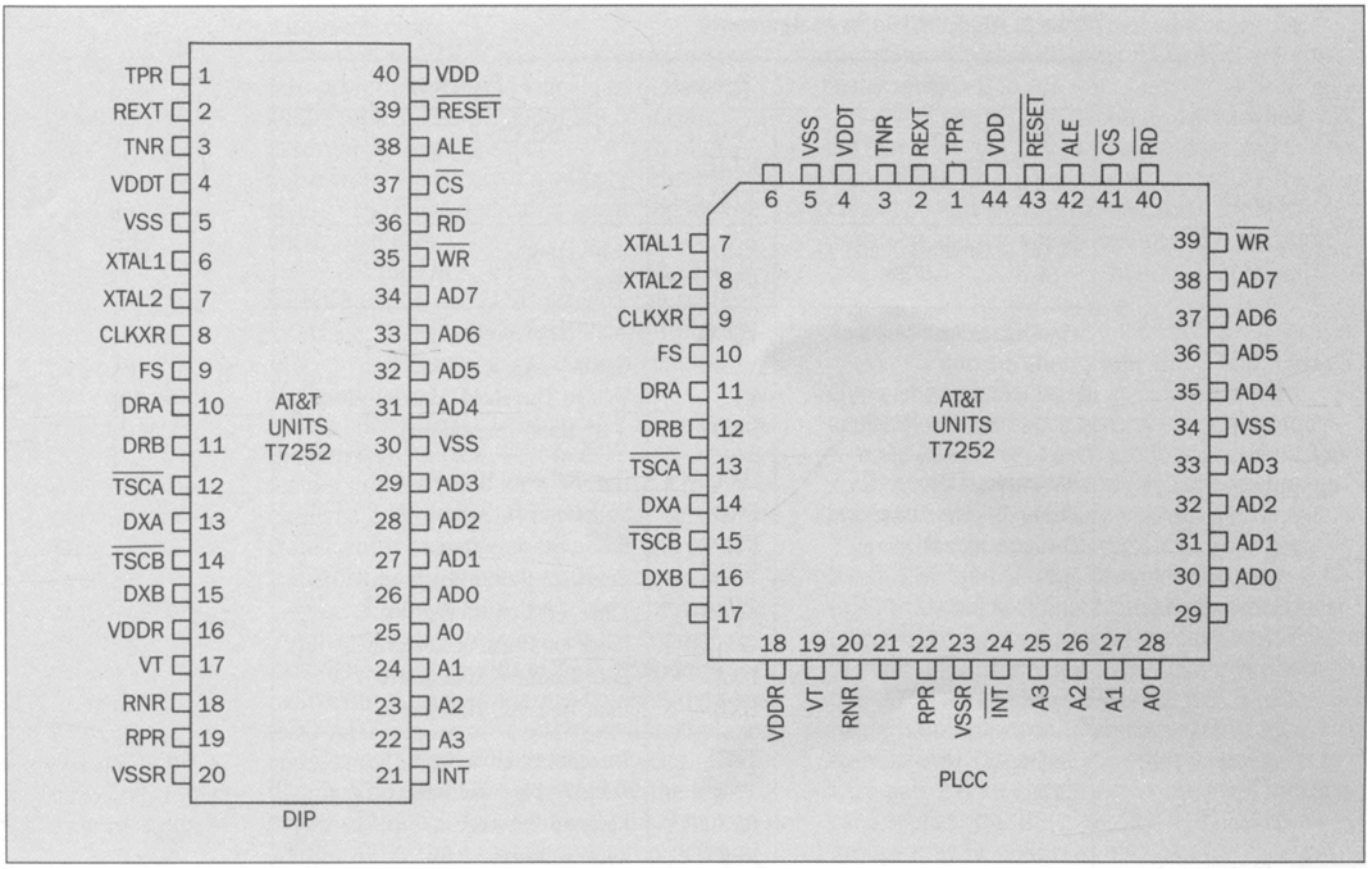


Figure 7. Pin assignments of the UNITS chip for a 40-pin DIP (dual in-line package) and a 44-pin PLCC (plastic leaded chip carrier).

tus bits are set whether or not the mask bits are programmed in register R7. The received signal field reports arrival of INFO 0, INFO 1, or INFO 3 frames from the subscriber end.

Pin Functions

The UNITS chip is available in either a 40-pin DIP (dual in-line package) or a 44-pin PLCC (plastic leaded chip carrier). Figure 7 shows the pin assignments for the two packages. Four pins in the 44-pin package are unused. We will briefly describe the functionally related groups of pins listed in Table II.

Pins CK6/XTAL1 and XTAL2 provide direct connections to a 6.144-MHz crystal. Alternatively, the CK6/XTAL1 pin may be driven at CMOS logic levels by an external clock source at 6.144 MHz. The overall stability of the 6.144-MHz signal must be ± 100 ppm.

Pins VDD and VSS provide the power input and ground reference for all digital logic

Table II. AT&T UNITS Pin Assignments

Group	Symbol	Function
Chip Clock	CK6/ XTAL1 XTAL2	6.144-MHz Clock
Power & Ground (Digital)	VDD VSS	+5V Power Ground
Power & Ground (Analog)	VDDR VSSR VT VDDT	+5V (Line Receiver) Ground (Line Receiver) Voltage Threshold (Line Receiver) +5V (Line Transmitter)
System Interface (Time-division-multiplexed Concentration Highway)	DRA DRB FS $\overline{\text{TSCA}}$ $\overline{\text{TSCB}}$ CLKXR DXA DXB	Data Receive, Highway A Data Receive, Highway B Frame Synchronization Time Slot Control Highway A Time Slot Control Highway B Clock for Transmit/Receive Data Transmit, Highway A Data Transmit, Highway B
4-wire "S/T" line interface	TPR TNR REXT RPR RNR	Transmit Positive Rail Transmit Negative Rail Resistor, External Receive Positive Rail Receive Negative Rail
Microprocessor interface	$\overline{\text{RD}}$ $\overline{\text{WR}}$ $\overline{\text{CS}}$ $\overline{\text{INT}}$ $\overline{\text{RESET}}$ A0-A3 AD0-AD7 ALE	Read Write Chip Select Interrupt Reset Address Bus Address/Data Bus Address Latch Enable

within the chip.

Pins VDDR and VSSR provide separate power and ground signals to the analog line receiver. The VT input pin connects to an external decoupling capacitor, which filters noise from the receiver's voltage reference level. VDDT is a dedicated power pin for the line transmitter.

Pins DRA, DRB, FS, $\overline{\text{TSCA}}$, $\overline{\text{TSCB}}$, CLKXR, DXA and DXB provide the system interface. These eight signals constitute the time-division-multiplexed *Concentration Highway*.

Pins TPR, TNR and REXT belong to the line transmitter. TPR and TNR are transformer connections. REXT connects to an external 2-kilohm (kΩ) resistor for setting the transformer output current. RPR and RNR are transformer connections to the line receiver.

Pins $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, and ALE provide the microprocessor bus interface control signals. The eight pins AD0-AD7 provide a bidirectional, non-inverting, tri-state data bus. AD0-AD7 can be used either as a multiplexed address/data bus or as a data-only bus. The data bus direction is controlled by the logic states of the $\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ pins. On read or write cycles, the controlling microprocessor can send address information synchronized to the ALE signal. On a read cycle, bytes are sent to the microprocessor on the data bus. On a write cycle, bytes are received from the microprocessor. When chip select ($\overline{\text{CS}}$) is not active, the AD0-AD7 pins are placed in a high-impedance state.

Pins A0-A3 are the address leads to control the chip from a microprocessor using separate (demultiplexed) address and data lines. The ALE pin is strapped to a logic high when A0-A3 are used. When addresses are multiplexed with data, pins AD0-AD3 are normally strapped to A0-A3.

The $\overline{\text{INT}}$ pin becomes active when certain interrupt conditions are detected by the chip. The $\overline{\text{RESET}}$ pin is used to restore the chip logic and all internal registers to their power-up default values before chip operation can begin.

Application Example

Figure 8 shows how the T7252 UNITS chip can be connected in an ISDN line card application to support several subscriber loops. In most line cards, there are four sections: *subscriber port(s)*, *microcontroller*, *highway timing generator*, and a *switching network matrix*.

Beginning with the subscriber port, the T7252 UNITS chip provides the basic (2B + D) bidirectional transmission interface to a subscriber loop. Each loop may have one to eight TEs connected to it. On a given loop, two AT&T 2718AM transformers (2.5 to 1 turns ratio) are used. One connects to the transmit wire pair and the other to the receive wire pair. When eight T7252s are used in a line card application, the eight 2B + D channel groups may be collected into 24 time slots on the Concentration Highway.

The highway timing generator section provides the two timing control signals, FS and CLKXR, for the highway. The frame synchronization pulse must be 8 kHz ± 100 ppm with a maximum jitter of 160 nanoseconds (ns) to meet the specifications in the I.430 standard. The CLKXR speed is at the discretion of the user. For example, when a 2.048-MHz clock is provided, the highway carries thirty-two 8-bit time slots.

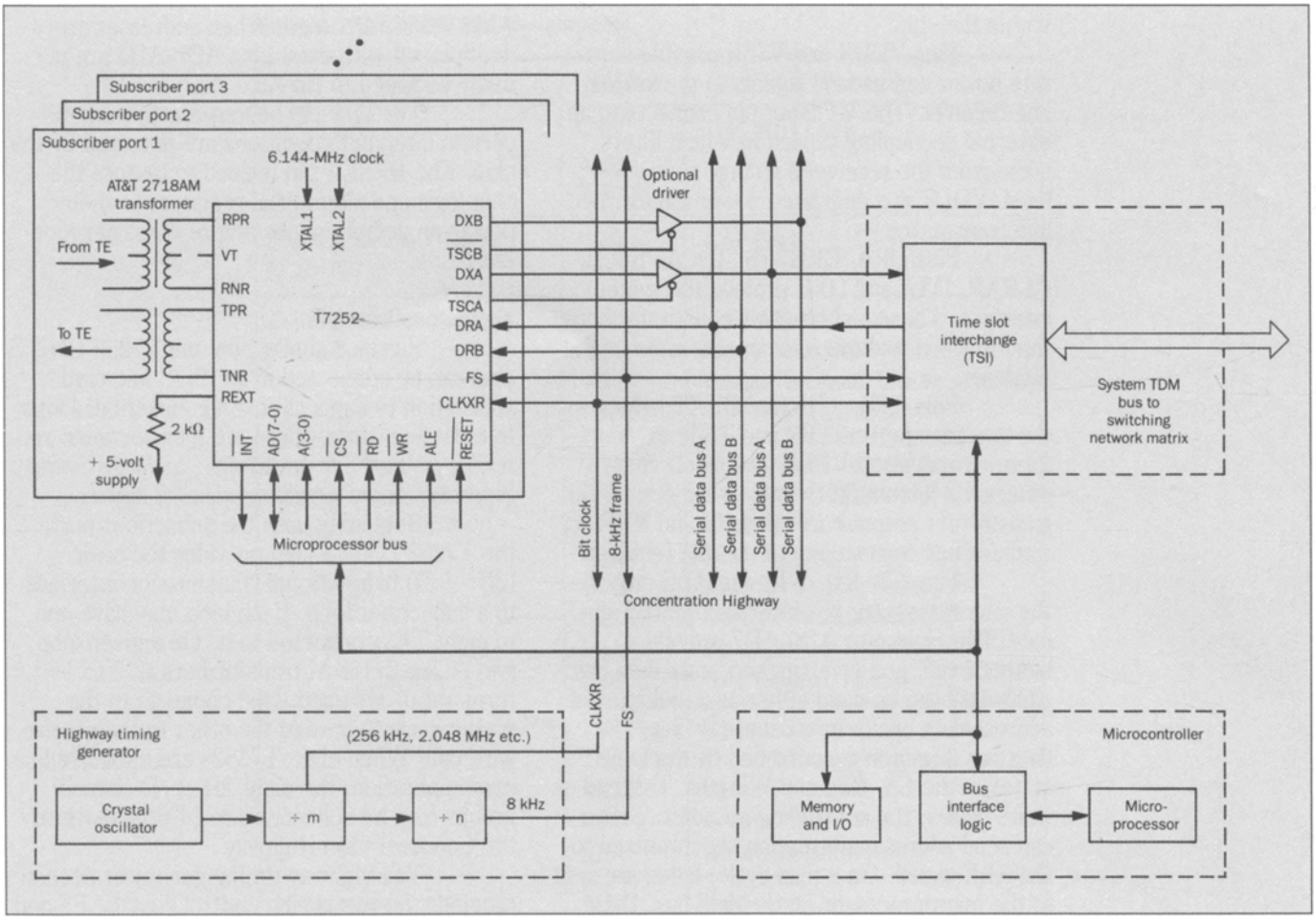


Figure 8. Connection example for the T7252 network termination chip on an ISDN line card.

The microcontroller section consists of a generic microprocessor, bus interface logic and associated memory, and input/output functions. The T7252 device operation is controlled and monitored by the microcontroller section.

Most line card applications use a switching network matrix to establish connection paths and exchange voice or data channels between subscriber ports and the digital switch. Full discussion of switched network operation is beyond the scope of this article. However, to illustrate the Concentration Highway interface in a digital switching environment, we have shown a simple time slot interchange (TSI) block. The TSI block connects the Concentration Highway of the UNITS chips to the system TDM switching matrix. Subscriber port operation and TSI functions are supervised by the microcontroller.

Another way to accomplish a TSI function would be to use a dual-port RAM, a serial-to-parallel bit shifter, a parallel-to-serial bit shifter, and a bit/time slot counter. The dual-port RAM contains two "mailboxes." The transmit mailbox holds bytes to be sent to the highway in channel time slots. The receive mailbox stores bytes received from the highway time slots. The parallel-to-serial shifter output connects to the DRA input on the UNITS chips. The serial-to-parallel shifter input connects to the DXA output on the UNITS chips.

Summary

The T7252 UNITS chip handles the network termination functions for one ISDN basic rate 4-wire subscriber loop. Typical applications include PBX line cards, line concentrators, high-speed multiplexers, and NT1 interfaces (for 4-wire to 2-wire conversion).

Chip operation is controlled easily by a microprocessor. The T7252 connects to a 4-wire subscriber loop via a pair of isolating transformers to meet the electrical requirements of the CCITT-recommended I.430 standard. As many as eight ISDN terminals may be connected to form a passive bus served by one UNITS chip. Adaptive receiver circuitry allows device operation in all configurations of the subscriber loop. The multiframing capability of the UNITS chip permits the use of the "S" and "Q" channels for physical link (Layer 1) maintenance.

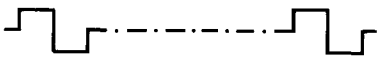
The system interface to a digital switch is achieved via the Concentration Highway. This serial highway transports the B- and D-channel information in 8-bit time slots on two transmit and receive paths. Time slot assignments and the bit transport sequence are programmable. Several T7252 devices (typically 8 to 12) may be connected to the highway at the system interface.

In addition to its many cost-saving features, the T7252 UNITS chip consumes a meager 85 milliwatts (mW) of power during normal operation. In the low power mode, the power consumption is about 22 mW.

References

1. CCITT Study Group XVIII I-Series Recommendation I.430, Draft Specification, 1986.
2. P. K. Govind, G. E. Offord, and L. J. Piper, "A Network-Interface Chip for ISDN Terminals," *AT&T Technical Journal*, Vol. 66, No. 2, March/April 1987, pp. 27-39.
3. "Integrated Services Digital Network," *AT&T Technical Journal*, Vol. 65, No. 1, January/February 1986, pp. 1-55.
4. Data Sheet—T7252 ISDN Basic Access User Network Interface Termination for Switches (UNITS), AT&T Technologies, Allentown, Pennsylvania, 1987.

Table A. Activation/Deactivation Sequence

Signals from NT to TE	Signals from TE to NT
INFO 0 No signal.	**INFO 0** No signal.
INFO 2 Frame with all bits of B, D, and D-echo channels set to binary ZERO. Bit A set to binary ZERO. N and L bits set according to the normal coding rules.	**INFO 1** A continuous signal with the pattern: Positive ZERO, Negative ZERO, six ONES, Positive ZERO, Negative ZERO, etc. 
INFO 4 Frames with operational data on B, D, and D-echo channels. Bit A set to binary ONE.	**INFO 3** Synchronized frames with operational data on B and D channels.

Appendix A.: What's in an I.430 (2B + D) frame?

The I.430 Recommendation of the CCITT describes the physical link (Layer 1) at the "S" or "T" reference point between ISDN terminal endpoints (TE) and a Network Termination (NT).[1] Specifications include voltage levels, impedance templates, bit timing, and coding. The frame structure (see Figure A-1) defined by I.430 has the following characteristics:

- 192-kb/s full-duplex signal grouped into "2B + D" time-multiplexed frames of 48 bits (frame period = 250 μs).
- Alternate space inversion (pseudo-ternary) line code.
- Framing by code violation at the F-bit.
- Multiframing by the combination of the F_A bit and the M bit; S-bit channel and Q-bit channel for Layer 1 maintenance.
- Echo back to the TE of the D bit received by the NT.
- Nominal two-bit offset of the relative bit positions of NT→TE and TE→NT frames.

In the bit stream transmitted from the TE to the NT, four bits are used for framing (F and F_A, each with a dc balancing bit L), eight "L" bits are used to balance the 32 B-channel bits, and four bits are D-channel bits. Conversely, for the NT-to-TE transmission, four bits (F with balancing bit L, F_A, and N) are used for framing, one "M" bit marks the start of a 20-frame multiframe, four "E" bits form an echo channel for retransmission of the D-channel bits received from the terminal, one "L" bit is used to balance the contents of the entire frame, and one bit (A) is set to one when bit synchronization is achieved between TE and NT. One "S" bit remains as an NT-to-TE channel. With a zero-length subscriber loop, the TE-to-NT stream is delayed by two bit times relative to NT-to-TE frames.

The alternate space inversion (ASI) line code used for the 2B + D transmission is

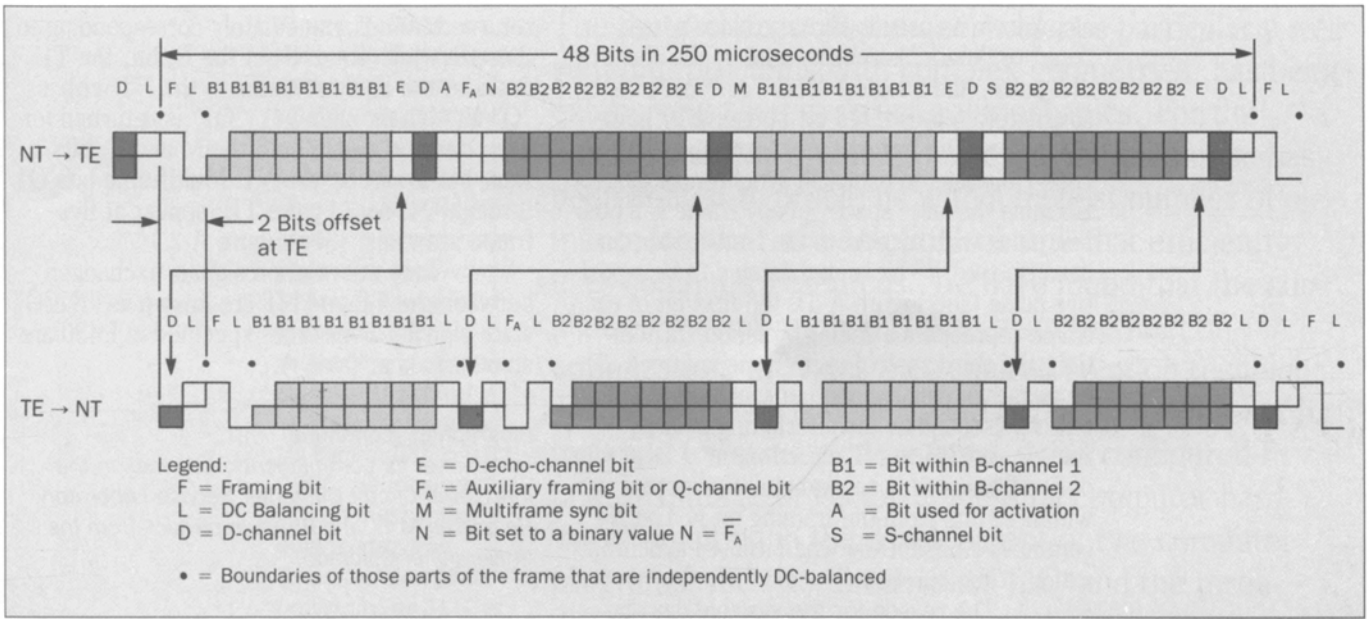


Figure A-1. I.430 frame structure.

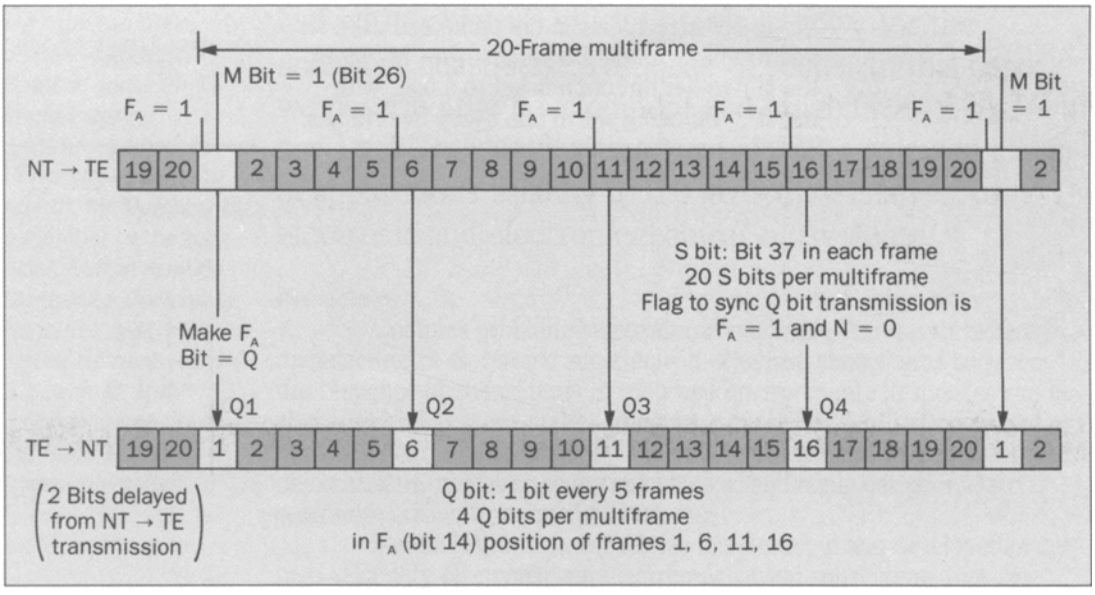


Figure A-2. Multiframing—S and Q channels.

also known as pseudo-ternary, since a logic "one" or "mark" is represented by the absence of a pulse, and a logical "zero" or "space" is alternately represented by a positive or negative pulse. The framing procedure uses line-code violations to establish synchronization. Because the last "space" of any frame is a positive pulse with respect to the transmitter, and because the "F" bit is also defined to be a positive pulse (see Figure A-1), the first bit of each frame represents a coding violation. In addition, the third zero of each frame is forced to be negative, causing another violation. All other pulses follow the alternating polarity rule. In the TE-to-NT direction, in at least four of five frames, this second violation occurs within 13 bits from the framing bit F. The NT continues transmitting when it loses synchronization at the receiver.

The reason for the variable distribution of the second line-code violation in the TE-to-NT stream lies in the technique used for multiframing. Every 20 frames, the "M" bit in the NT-to-TE direction is set to a one, with the "F_A" bit being set to one every five frames. The TE recognizes these states and, in returned frames immediately corresponding to those in which the NT set the F_A bit, the TE replaces the F_A bit it sends to the NT with a "Q" bit (Q1 through Q4). "Q1" is returned for each frame in which both the M and F_A bits were set to one by the NT. Multiframe bits Q1 through Q4, sent by the TE, appear at five-frame intervals. (See Figure A-2.)

Line information signals exchanged between the TE and NT are known as "INFO" state signals. Sequences specified in I.430 are summarized in Table A.

Biographies (continued)

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