AUTOMATED VISUAL INSPECTION OF SOLDER BUMPS

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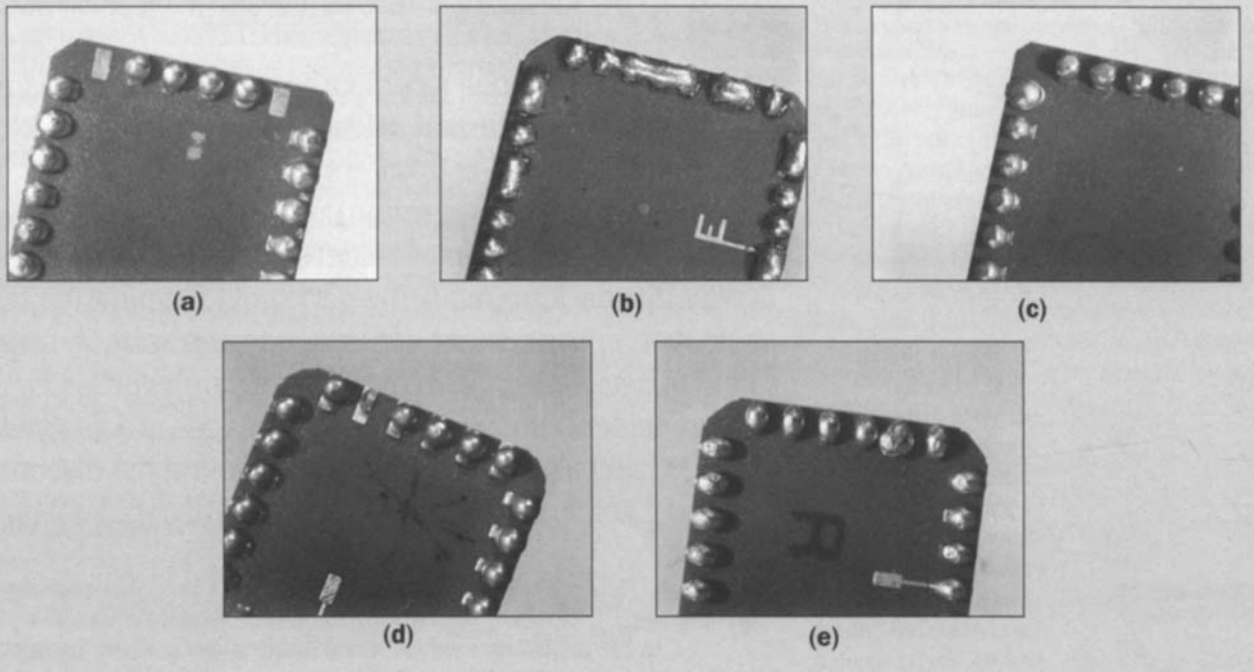
This paper describes a computer vision technique for automated inspection of solder bumps on leadless chip carriers and metallized wafers for advanced VLSI (very-large-scale integration) packaging. It is based on high-contrast imaging of soldered surfaces against a reflective background using dark-field illumination for selective enhancement of surface topography. A bright-field image is also used for resolving ambiguities in image understanding. Gray-scale images are analyzed using vision algorithms to detect topographic discontinuities of soldered surfaces and to identify solder-bump defects.

Introduction

In the electronics industry, soldering is the primary means of interconnecting components on printed wiring boards. Visual inspection of these soldered surfaces is a crucial step in the manufacturing process. Automated inspection and process control can ensure that products of the highest quality come off the production line. An automated process can also eliminate human factors that affect reliability, such as fatigue, boredom, and inconsistency of judgment, and create a more consistent inspection process with repeatable inspection results. Besides improving the quality and reliability of final products, automated visual inspection has the potential to improve process yield and generate cost savings.

The *advanced VLSI packaging* (AVP) technology under development at AT&T Bell Laboratories involves a process known as flip-chip solder assembly. In this process, solder is applied to the contact pads of chip and substrate wafers by evaporation through a metal mask before reflow assembly.[1-4] For *gated-diode cross-point* (GDX) devices in 5ESS® switching systems, spherical solder preforms are attached directly to the metallized pads of leadless chip carriers. These solder-bumped chip carriers are then surface-mounted on ceramic substrates of hybrid-integrated-circuit modules.

When inspecting solder bumps, we must be able to detect and classify defective solder bumps on chips, substrates, and chip carriers.



Panel 1. Types of Defects

- *Missing Bump.* The absence of a solder bump on a contact pad that may or may not be completely tinned (dewetted or nonwet pads). This defect invariably creates an electrical open circuit. (a)
- *Solder Bridging.* An extraneous soldered connection between two adjacent bumps, causing an electrical short circuit. (b)
- *Squashed Bump.* A solder bump with considerably less height than an average bump. Such a bump may not make an electrical contact with the corresponding surface after device placement. Even if a contact is made, it is likely to be a poor electrical contact with high resistance at the junction.
- *Excess Solder or Overflow.* A large solder bump extending beyond the outer extremities of the pad. This defect may cause undesirable interconnection of a pad with metallized traces during reflow attachment. (c)
- *Poor Wetting.* An untinned contact pad at the base of a solder bump. (d)
- *Near-Short.* Close proximity of two adjacent bumps. This defect has a high probability of causing solder bridging during final reflow. (e)
- *Splatter or Debris.* Adhesion of isolated globules of solder to the chip or substrate surface.
- *Cold Solder.* A solder bump with a high degree of surface roughness resembling a polyhedral shape and a pre-reflow surface condition. A probable cause is lack of adequate heating.
- *Surface Discoloration.* A solder bump with a dull and lusterless appearance (grainy, frosty, tarnished, or oxidized surface texture). This defect can be caused by process malfunctions, excessive rework, or presence of flux, dirt, or other contaminants.
- *Holes and Cavities.* Soldered surfaces with cracks, cavities, craters, or other kinds of shape-related deformations because of vibrations or probing during reflow or immediately thereafter.

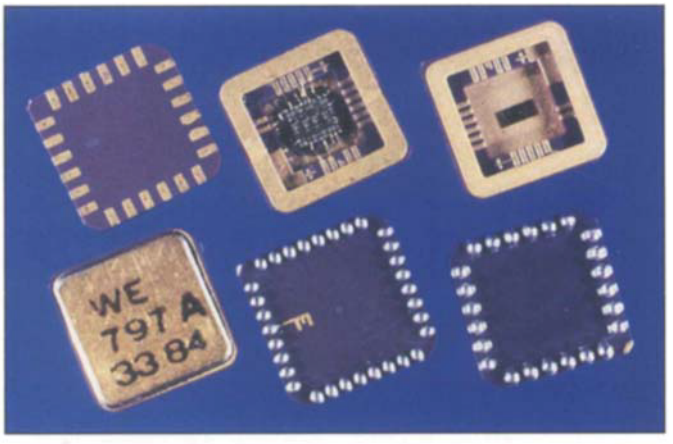


Figure 1. GDX chip carriers in various stages of manufacturing. Top row (left to right): chip carriers with gold pads before solder-bumping, after wire-bonding, and before chip-bonding operations. Bottom row (left to right): the top surface of the chip carrier after lid sealing and the bottom surface with 32 and 24 solder bumps, respectively.

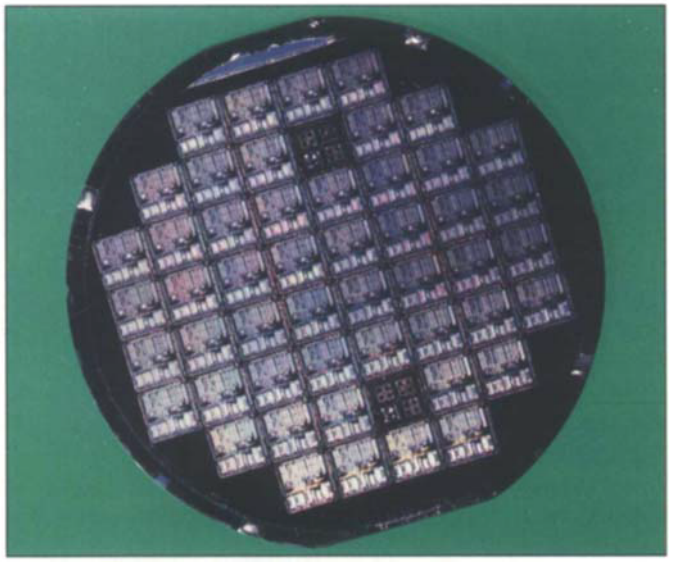


Figure 2. An AVP wafer. Solder bumps are located on the peripheral regions of the chips.

In particular, detecting missing bumps and solder bridging is of prime importance. The devices discussed in this paper have linear arrays of solder bumps around the peripheral regions. A GDX device contains solder bumps attached to gold pads on a dark-gray ceramic surface (Figure 1). A typical AVP wafer contains 3000 to 12,000 microscopic solder bumps on 100 × 100-micrometer (μm) pads on 200-μm centers (Figure 2). The inspection requirements and dimensional specifications of these devices are shown in Table I.

The most commonly observed defects related to solder bumps are presented in Panel 1. Some of these defects can only be distinguished by subtle differences in gray scale and texture because of a rough and discontinuous surface topography. This makes automatic defect classification difficult.

The major technical challenge of this application is to create images of microscopic, specular (mirror-like), and irregular surfaces on a specular background with enough contrast to be interpreted. We need to enhance the surface defects, while avoiding artifacts in the image caused by specularities. This is a major constraint in the design of the optical and illumination setup for solder-bump inspection.

Furthermore, the inspection criteria for acceptance and classification are highly subjective and the typical geometrical signatures of solder-bump defects are not well defined. This implies the need for complex algorithms, optical assemblies, and expensive computational hardware for image acquisition and processing.

But, speed and cost are always important factors. To satisfy process reliability and time requirements, we need a simple setup for image acquisition, and simple image processing algorithms that can be executed at a high speed with a special-purpose hardware processor. This dichotomy can be resolved by using a special-purpose optical "front-end," for acquiring high-contrast and high-resolution images with little ambiguity in the information content, to allow for the application of simple vision algorithms.

The Design Approach

Automated visual inspection of solder bumps is a new area of research. Blanz et al. have recently reported a

Table I. Mechanical Dimensions and Inspection Requirements

Requirements	Advanced VLSI Packaging Process	Gated-Diode Cross-Point Process
Pad size	100 × 100 μm	500 × 1000 μm
Bump height	50 μm	600 μm
Shape of bump	Hemispherical	Spherical
Bumps per device	100 to 150	24 or 32
Solder composition	95 Pb/5 Sn	40 Pb/60 Sn
Scene background	Silicon wafer	Ceramic substrate
Inspection throughput	300 bumps/min	1200 bumps/min
Vision system cost*	$ 20,000	$ 15,000

*Does not include cost of equipment for material handling.

technique of projecting shadows of solder bumps using oblique illumination.[5] Using a camera at an oblique viewing angle from the opposite direction, each bump and its shadow are imaged as adjoining elliptical blobs. The shadows are analyzed using Hough transforms. This technique is useful for determining the presence and the height of a bump. However, if the shadows extend into regions containing solder bridging, it may create erroneous results.

The problem of solder-bump inspection has a lot in common with the problem of lead-through-hole solder-joint inspection, which has been the subject of several studies in the past. Solder-joint techniques reported in the literature include:

- A knowledge-based expert system and a minimum-distance classifier by Bartlett et al.[6]
- A range-mapping technique using structured lighting, by Nakagawa.[7]
- An optical filtering technique, using colored illumination matched against the color of the solder masks and the circuit traces of the printed-wiring board, by McIntosh.[8]
- An infra-red technique to study the time characteristics of thermal signatures of solder joints during heating and cooling periods, by Vanzetti.[9]
- An x-ray-based technique for the investigation of the internal structures of solder joints, by Juha.[10]

Many of these techniques require complex inspection setups, have long cycle times, and are quite expensive. A detailed analysis of these techniques is beyond the scope of this paper.

The technique presented in this paper uses a traditional approach of imaging solder bumps using visible light and detecting surface defects using visual means. (This method is also described in U.S. Patent No. 4,688,939, issued on Aug. 25, 1987 to R. Ray and assigned to AT&T Technologies, Inc.) The three-dimensional (3D) shapes of soldered surfaces are inferred from the visual signatures of the specularities, commonly known as *image highlights*, using directed illumination at high and low angles of incidence. The major advantages of this technique are:

- A system operator can verify defects, if needed; methods using x-ray or infrared techniques can not.
- Solder-bump images can be processed at a high speed using a low-cost vision processor.
- No complex, costly, or unconventional optical setup is required.
- With minor changes, this approach can be extended to other applications involving the inspection of soldered surfaces.

In this approach, however, there are some basic assumptions:

- The scene in the background is a planar surface.
- All solder bumps are of equal height and are equally spaced.
- Topographical variations in the scene are only due to the presence of soldered surfaces and not to any other components.

It is also assumed that the viewing direction is perpendicular to the plane of the wafer or chip carrier and the size of the bump is much smaller than the viewing distance. This minimizes perspective distortion, occlusion, or depth-of-focus problems, and thus, image coordinates can be directly related to the corresponding object coordinates without correcting for spatial distortions.

Design of the Illumination System. This method uses illumination techniques to enhance topographical features of solder bumps in the acquired images. The complexity of algorithmic processing can be greatly reduced if input images have good quality and contrast. Lighting parameters, such as directionality and spatial distributions, are

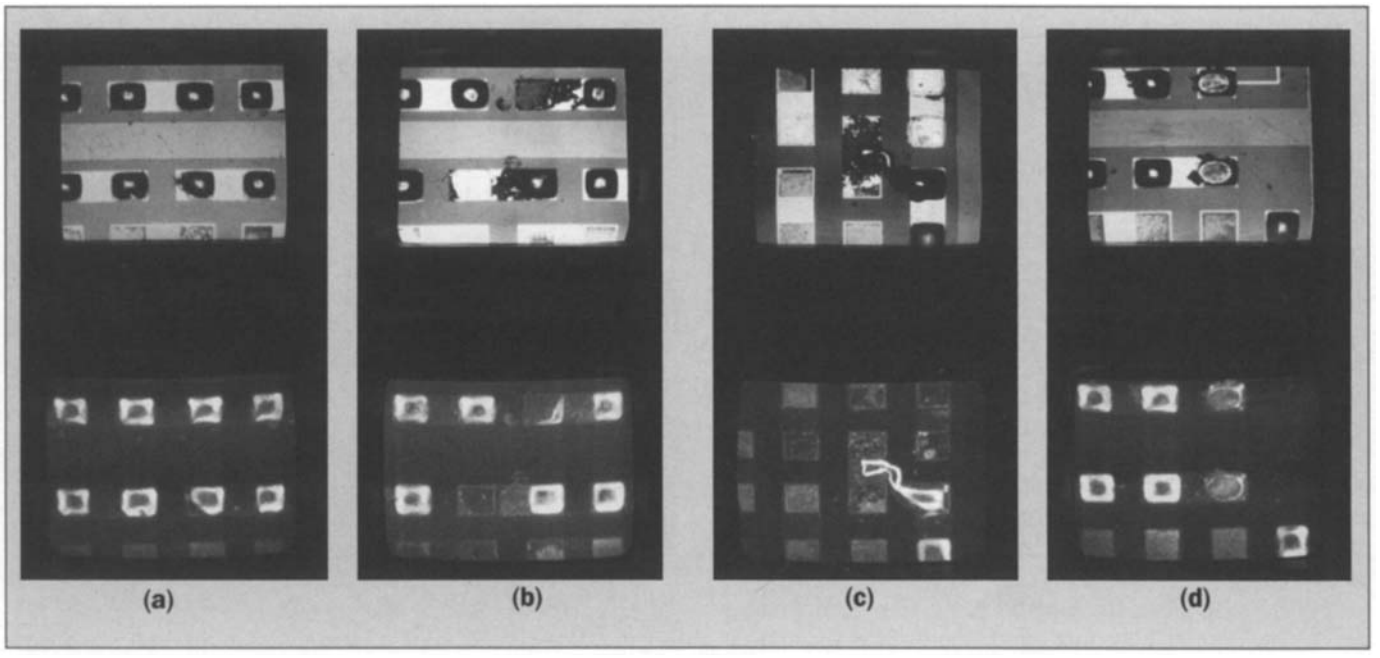


Figure 3. Gray-scale images of defective AVP solder bumps, under bright-field (top of each picture) and dark-field illumination (bottom of each picture): (a) poor wetting, (b) missing bumps, (c) solder bridging, and (d) squashed bumps.

the key ingredients in producing good-quality images of soldered surfaces.

Experiments to study the relative merits of various illumination schemes for solder-bump inspection were also performed. An extended and diffuse light source of circular symmetry provides uniform, shadow-free illumination. This helps to avoid creating spurious artifacts in the image, including the formation of distorted visual signatures of bumps due to excessive image saturation.

Under bright-field illumination, when the light is projected downwards directly from above, the top surface of a solder bump appears as bright as a pad with no bump (Figure 3) because of the specular reflectance characteristics of solder and the equally reflective properties of a gold pad. It is difficult to distinguish between these two surfaces simply based on the intensities in these bright-field images. Other qualitative image features, such as shape and texture, need to be evaluated for correct classification.

With bright-field illumination, the curved surface of a solder bump reflects incident light away from the camera, thereby appearing as a dark patch in the image. This causes ambiguities in feature interpretation and image understanding. For example, a dark line in the image between two dark blobs may be caused by solder bridging between two bumps, or it may simply be a circuit pattern on the wafer surface adjoining the bumps (Figure 3).

Most defects analyzed in this report appear as sharp and discontinuous changes in surface topography. The presence of such a surface can be easily verified by projecting light at a grazing incidence, such that the incident light is in a plane normal to the viewing axis. Under this scheme of dark-field illumination, the solder surface that is at a steep gradient with respect to the plane of incidence scatters light toward the camera and creates a bright highlight in the image, as illustrated in Figure 4 for a chip carrier. For a missing bump or a planar surface, the direct passage of light is not obstructed by any elevated surface

structure, and hence, no light is reflected toward the viewer (Figure 5a).

Solder bridging can also be clearly detected using dark-field illumination as a set of nearly parallel lines terminated by two annular blobs at the two ends. These lines correspond to the high topographical gradients of the solder surface causing the bridging (Figure 5b). A ring light, used to illuminate soldered surfaces uniformly at a near-grazing incidence from all sides, helps to detect solder bridgings, irrespective of their location, geometry, and orientation on a 2D plane.

Dark-field illumination also emphasizes ridges, grooves, and other surface discontinuities. By eliminating the planar background, this technique minimizes the probability of confusion between a 3D soldered region and a planar, metallized surface patch on this background. Some subtle defects (e.g., poor wetting) may not be resolved from an image obtained with dark-field illumination. In addition, any defect located in the darker regions of this image, for example at the top part of a solder-bump, may not be discernible. This creates an ambiguity that can be resolved by processing a second image of the same site

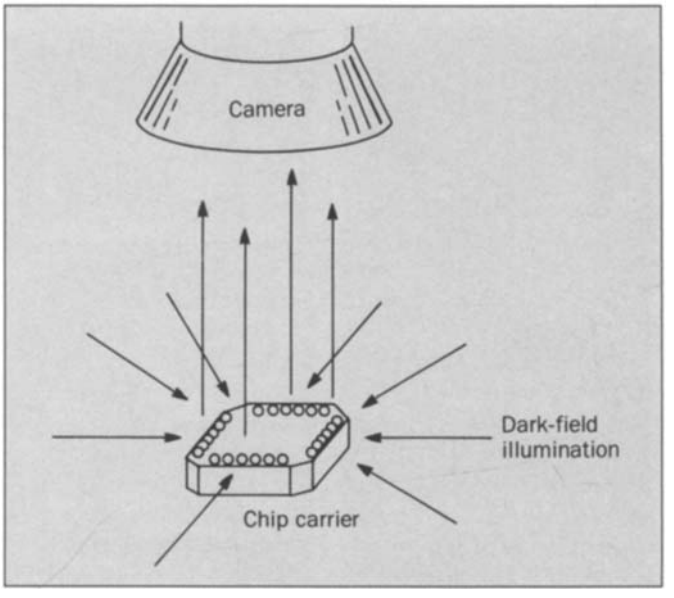


Figure 4. Dark-field imaging of solder bumps on a GDX chip carrier.

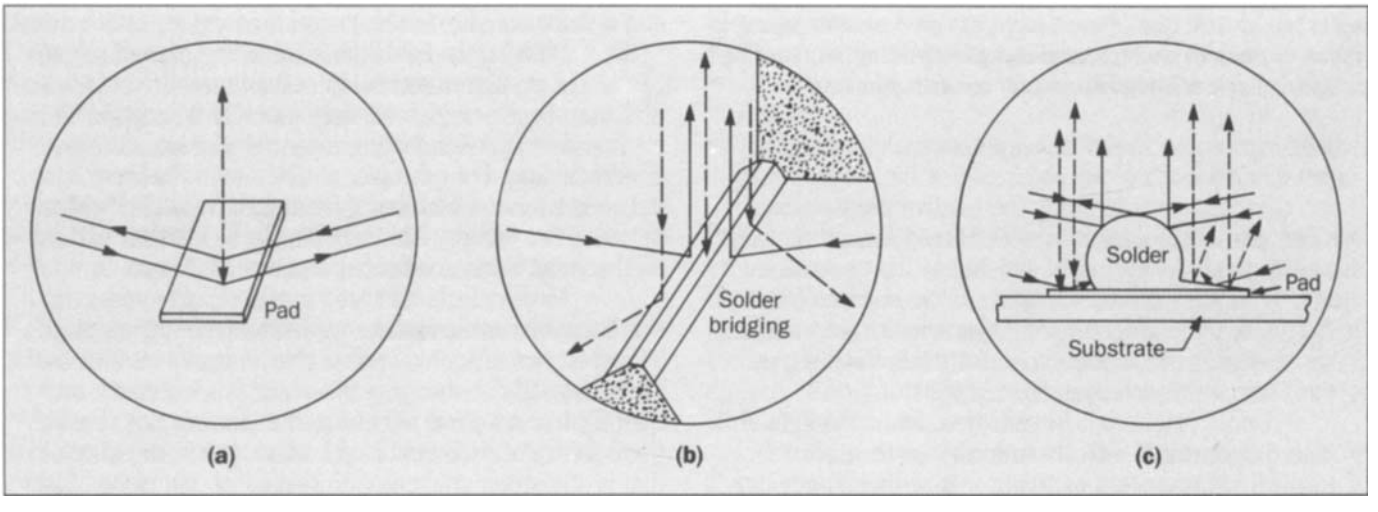


Figure 5. Reflection characteristics of (a) a pad with no bump, (b) solder bridging and (c) a poorly wetted pad. Dashed lines = bright-field illumination; solid lines = dark-field illumination.

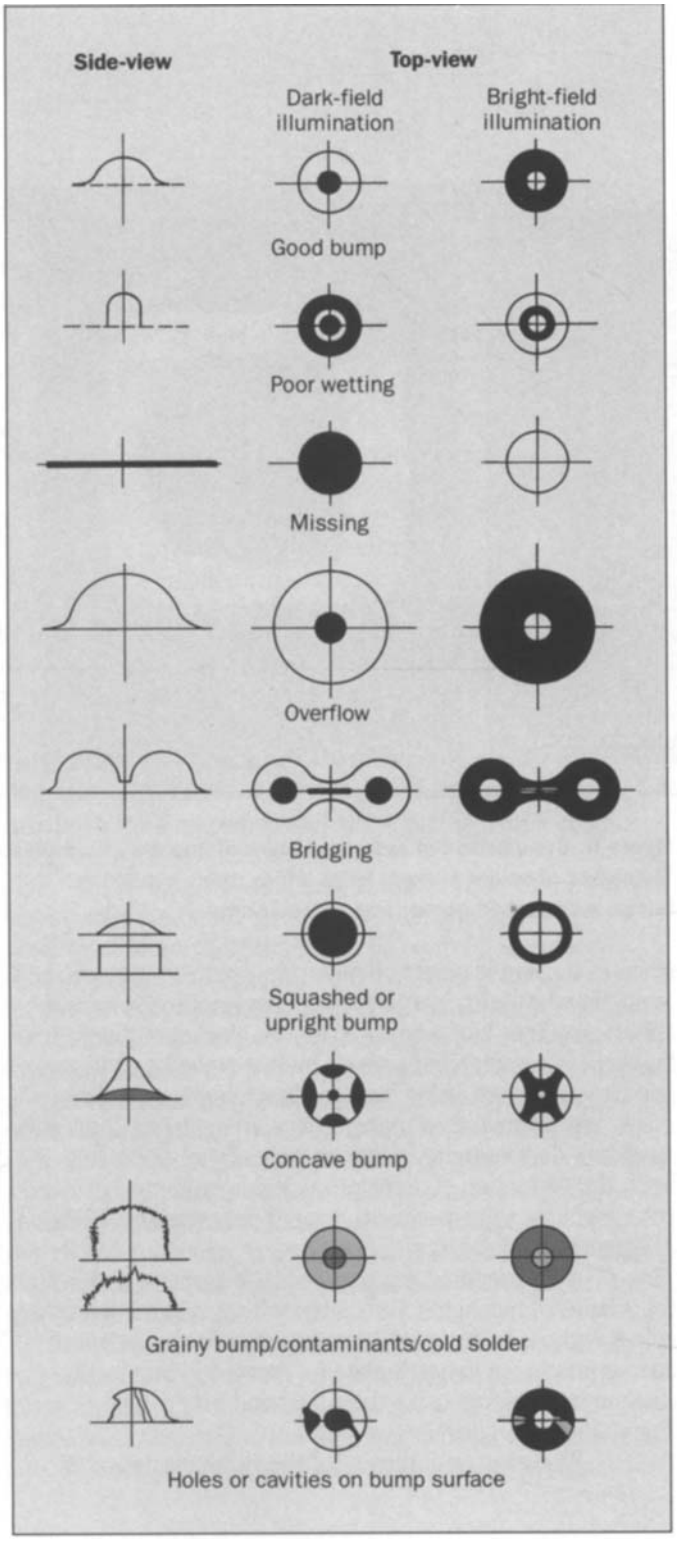


Figure 6. Visual signatures of defects under bright and dark-field illuminations. Background surface texture appears in these images around the outer periphery of the bright-field highlights (not shown).

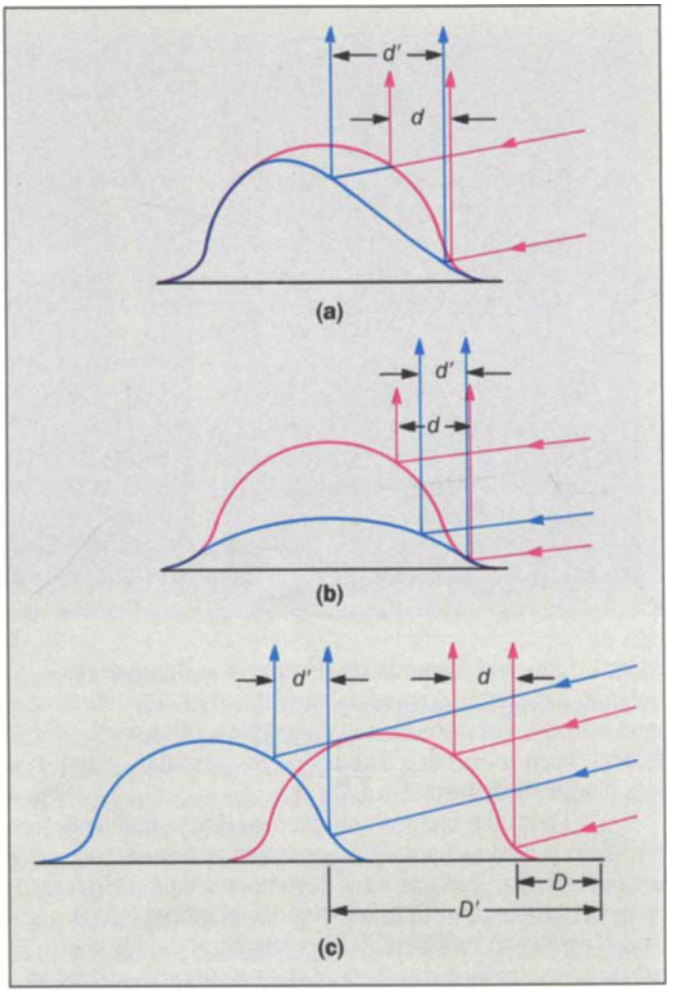


Figure 7. Spatial parameters of image highlights as a function of (a) the surface curvature of a bump ($d < d'$), (b) the planarity of the top surface ($d > d'$), and (c) the location of the bump on a pad ($d = d'$, $D \neq D'$).

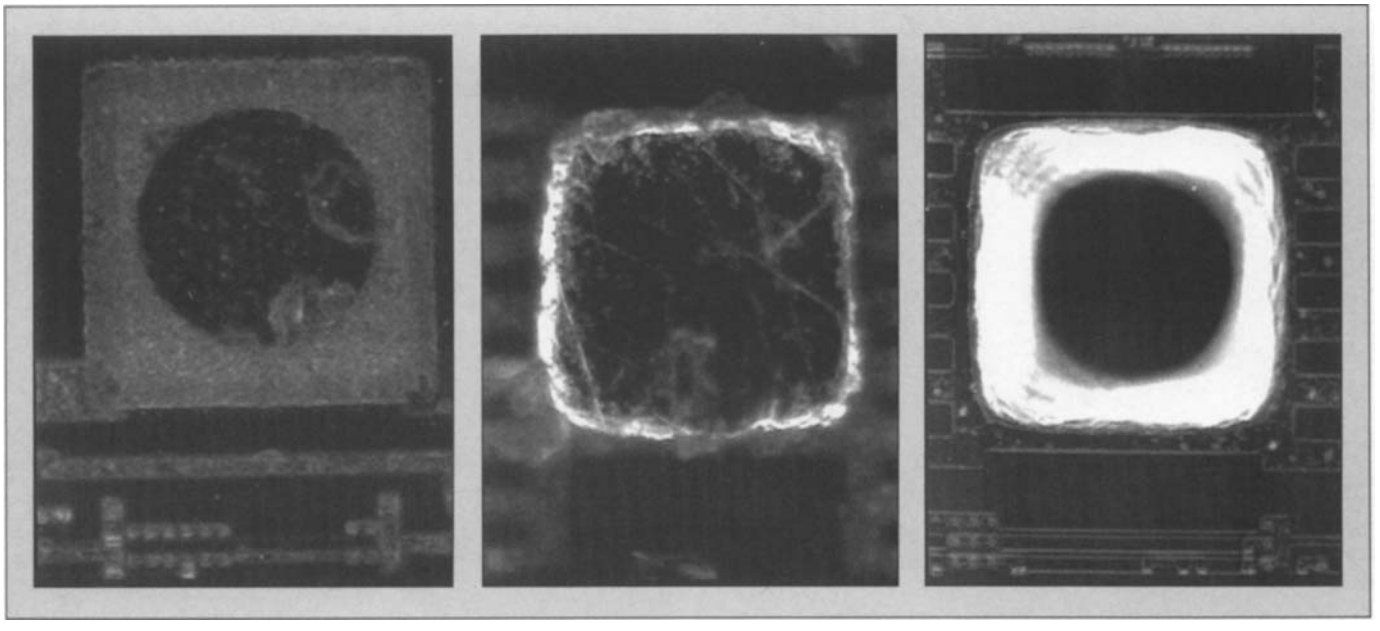


Figure 8. Comparison of inner and outer diameters of annular highlights of solder bumps. From left to right: a missing bump, a squashed bump, and a good bump.

under bright-field illumination (Figure 5c). However, this ambiguity is related to nonfatal defects, such as craters or poor wetting. For detection and classification of fatal defects, such as missing bumps or solder bridging, dark-field illumination is quite sufficient.

Thus, the images produced by bright-field and dark-field techniques are quasi-complementary. For a smooth specular surface, dark regions in a dark-field image generally correspond to bright regions in a bright-field image, as shown in Figure 3. Topographical details are enhanced by dark-field, whereas printed texture on planar regions is enhanced by bright-field. However, neither of these two techniques is sufficient for detecting all fatal and nonfatal defects. The two images together can form a complete set that has the potential for displaying all externally visible solder-bump defects.

Visual Signatures of Image Highlights. For a smooth surface, the shape of the highlight depends on the shape of the light source, the illumination and imaging geometries, and the surface curvature. A ring light, axially symmetric around the optical axis of the camera and parallel to the plane of the wafer or the chip carrier, creates a ring-shaped highlight of uniform width and uniform brightness from a spherical solder-bump surface. Under ideal conditions, this highlight is completely bounded by two smooth, continuous and closed curves. If the incident beam impinges on a crack, pit, or any other topographical irregularity, it creates an abrupt discontinuity in this annular shape. For a ring light, the formation of an elliptical highlight instead of a circular highlight implies smooth spatial deformations in the 3D-structure of the workpiece.

This property can be used to determine *a priori* the shapes of highlights associated with good and defective solder bumps. In our study, we determined typical visual characteristics of image highlights corresponding to various surface defects using dark-field and bright-field illuminations (Figure 6).

The average intensity of the highlight indicates

the surface-finish characteristics of the solder bump, its microstructure, and its metallurgical constituents. The highlight created by a cold solder appears less bright in comparison to a good bump. A bump that has undergone excessive rework may also appear dull because of excessive flux contents.

The surface curvature of a solder bump (a spheroidal segment) is a function of its height above a given plane if its diameter at the base is held constant. The width of the annular shape of this highlight depends on the surface curvature of the solder-fillet (Figure 7a). The outer diameter indicates poor wetting (i.e., a bump segment of a smaller cross-section) whereas the inner diameter conveys information about the planarity of the top surface of a soldered region (Figure 7b). The extremities of the outer ring also indicate the relative displacement of the bump with respect to the pad, if the pad locations and pad geometries are programmed into the vision system before inspection through a CAD (computer-aided design) interface (Figure 7c). Figure 8 shows typical visual signatures of a missing bump, a squashed bump, and a good bump using dark-field illumination.

Spectral Contents of Illumination. A reflectance analysis is performed to determine how the spectral composition of incident light affects the contrast of solder-bump images. The specular reflectance of solder alloy is measured experimentally using a Perkin Elmer Model 330 spectrophotometer. Two solder samples are used for experimentation: one corresponding to a solder bar of 40-percent lead and 60-percent tin (40 Pb/60 Sn), and the other corresponding to reflowed solder paste. A third sample prepared from an unsoldered silicon wafer coated with a polyimide dielectric material is also studied. Figure 9 shows the measured values of specular reflectance over the visible spectrum, normalized with respect to the specular reflectance of a highly polished aluminum mirror at a wavelength of 0.8 μm

This plot clearly shows that the reflectance of the two solder samples closely match each other and the maximum intensity differential between the wafer and the solder samples corresponds to the wavelength range of 0.45 to 0.55 μm. The emissivity of a typical fluorescent light source

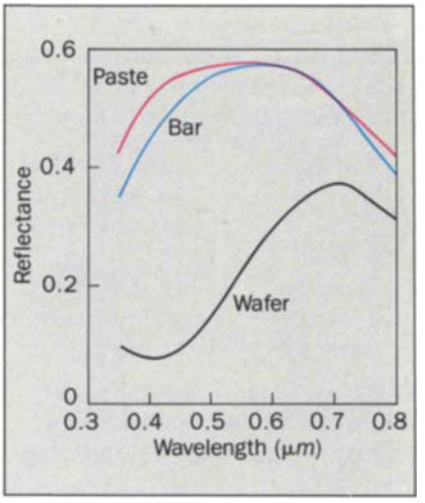


Figure 9. Specular reflectance of reflowed solder bar, solder paste, and a silicon wafer as a function of wavelength of incident light.

peaks in this blue-green region of the visible spectrum. Besides, a fluorescent source also provides uniform illumination, which is essential for this inspection task.

System Architecture

Figure 10 shows the principal components of the AVP inspection system including:

- A vision processor
- A computer-controlled *xy* table
- A solid-state camera
- An automatic wafer handler
- A "flat-finder
- An AT&T PC 6300.

The input/output devices include a PC 6300 terminal screen with keyboard, a line printer, and a black-and-white television monitor. The vision controller consists of a Motorola 68000-based central processing unit (CPU), operating at a clock rate of 12 MHz, four 256 × 256 × 8-bit frame buffers, 64 kilobytes (Kbytes) of on-board static random access memory (SRAM), and a systolic array processor for high-speed execution of vision algorithms. The table controller uses an Intel 8085 microprocessor; the wafer handler uses four Z-80 microprocessors. These controllers are interfaced with the PC 6300 and with one another through multiple asynchronous serial communication links.

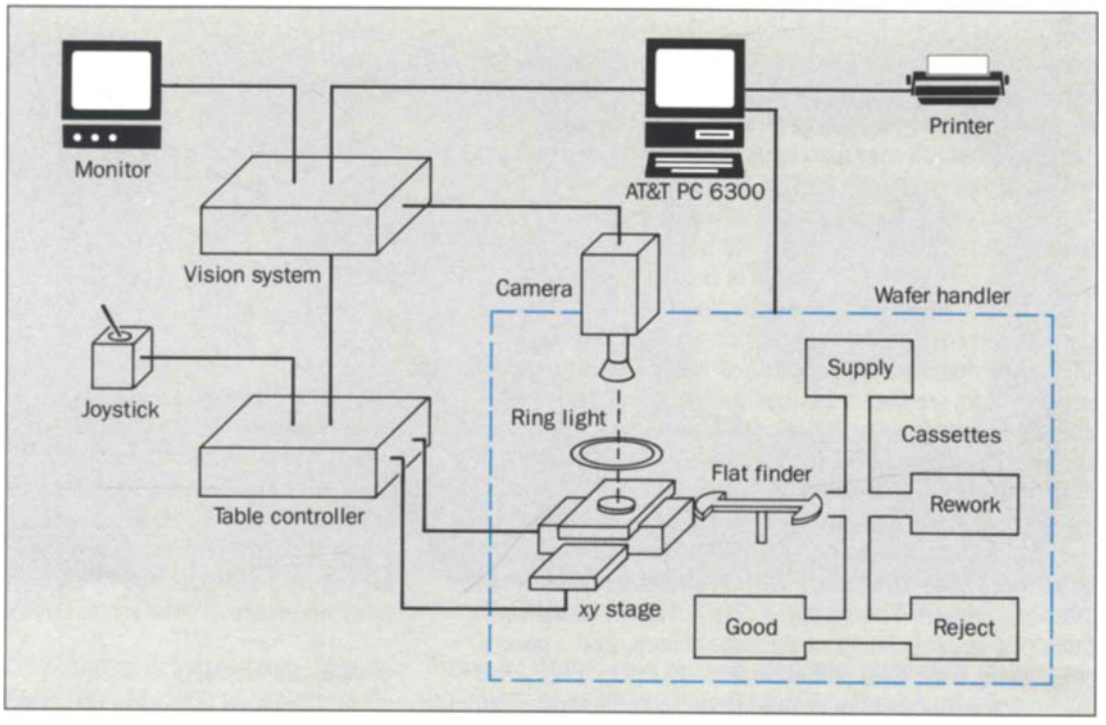


Figure 10. System configuration for AVP inspection.

For reliable inspection, solder bumps should always be positioned by the *xy* table within predefined rectangular windows, with the linear array of the bumps approximately parallel to the top and bottom edges of the window. The required placement accuracy for AVP inspection is 50 μm. This is done by automatic pre-alignment of the wafer, which is placed on an alignment chuck and a flat finder to obtain a positioning accuracy of 50 μm and a rotational accuracy of 0.2 degrees. To achieve precise alignment, the magnitudes of translational and rotational offsets are then computed by the vision system based on two fiducial (reference) locations before inspection. We correct for these offsets during inspection by applying mathematical transforms for rigid-body translation and rotation to the solder-bump coordinates.

For each lot code, a data file is generated, edited, and stored by the system operator during system training. The file contains the code number, the locations of the bumps, the window size, and the various thresholds for image processing and defect classification. These data are automatically downloaded into system memory for automated inspection.

The integrated system architecture for the GDX inspection system consists of

- A vision controller
- A robot controller and a multi-axis robot arm with dual suction-cup grippers for simultaneous loading and unloading of chip carriers
- A solid-state camera.

The GDX chip-carrier inspection system uses a fluorescent ring light to illuminate solder bumps from the side at an incidence angle of 80 degrees with respect to the optical axis of the camera. A second light source is also used to illuminate these bumps from above. We use only one source at a time for image capture and additional processing.

System Resolution. In the AVP inspection system, four pixels are allocated for reliable detection of a 25-μm defect to ascertain highly repeatable performance by the inspection system. For a 256 × 256-pixel image, this cor-

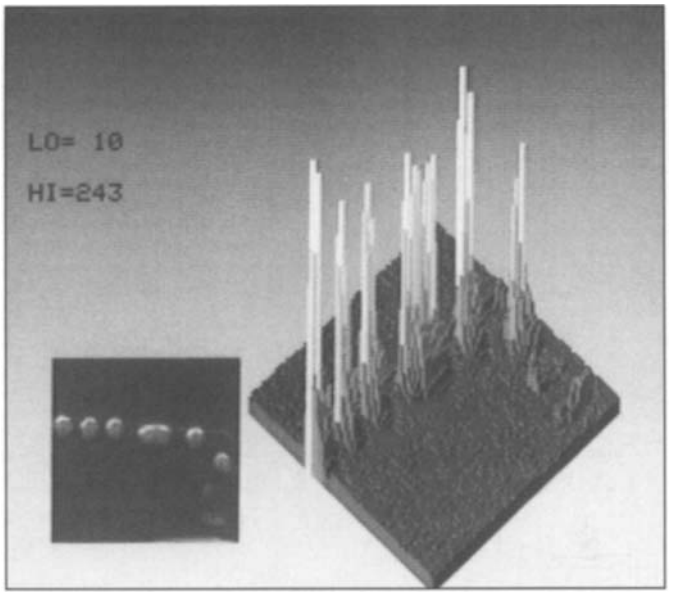


Figure 11. A 3D intensity map of defective solder bumps.

responds to a field of view of 1.5 × 1.5 mm, which is only a small fraction of the total cross-section of an AVP chip. This implies an additional part-indexing scheme (step and repeat operations) for presenting all bumps on all four edges of the chip to the camera. For parts presentation, we use a high-precision *xy* stage with a maximum travel of 150 mm per axis at a resolution of 0.33 μm per step.

The GDX inspection system uses a lower magnification for the optical assembly because the solder bumps and the associated defects are comparatively larger than in the AVP system. Here, the entire chip carrier with all its solder bumps is included in the field of view of the camera. Because all the bumps are captured in a single image, there is considerable speed advantage over the AVP inspection system. Technical specifications of the two inspection systems are shown in Table II.

Table II. Performance Specifications

System Specifications	Advanced VLSI Packaging Process	Gated-Diode Cross-Point Process
Spatial resolution	6.3 μm/pixel	50 μm/pixel
Field of view	1.5 × 1.5 mm	12.8 × 12.8 mm
Number of images/ device	12–28	1
Placement accuracy	50 μm	250 μm
Cycle time	320 bumps/min	1850 bumps/min

Vision Algorithms

In this section, we present the vision algorithms for acquiring and processing solder-bump images.

Image Acquisition. A gray-scale image of solder bumps appropriately highlighted by the illumination system is captured by the imaging device. The solid-state camera can provide images at the rate of 30 frames per second for digitization. When triggered by an input signal, an image is digitized as a 256 × 256 × 8-bit intensity array and stored in the image memory. A typical intensity pattern of a chip carrier containing shorted and missing solder bumps is shown in Figure 11.

Contrast Enhancement. The captured image is processed using an intensity threshold to remove the background from the image. The residual gray-scale contents are normalized to improve image contrast by stretching the intensity histogram of the image. This is done by computing the minimum and maximum intensities of the image, determining a scale factor for intensity conversion, and then mapping the intensities between these two limits into a gray-scale domain of [0,255] using this scale factor.

Windowing. Preprogrammed, rectangular windows are positioned around each segment of the processed image enclosing a linear array of solder bumps on the periphery of the chips. A window should be large enough to accommodate parts-positioning tolerance.

Figure 12a shows two software-controlled windows on a processed image enclosing arrays of solder bumps at the adjacent edges of two neighboring chips on an AVP wafer. Software-controlled windows on a GDX chip carrier are shown in Figure 12b.

Feature Extraction. We reduce the dimensionality of the background to reduce computational complexity and to speed up processing. Many simple image features are considered for extracting information from the visual signatures, because of their potential for rapid computation

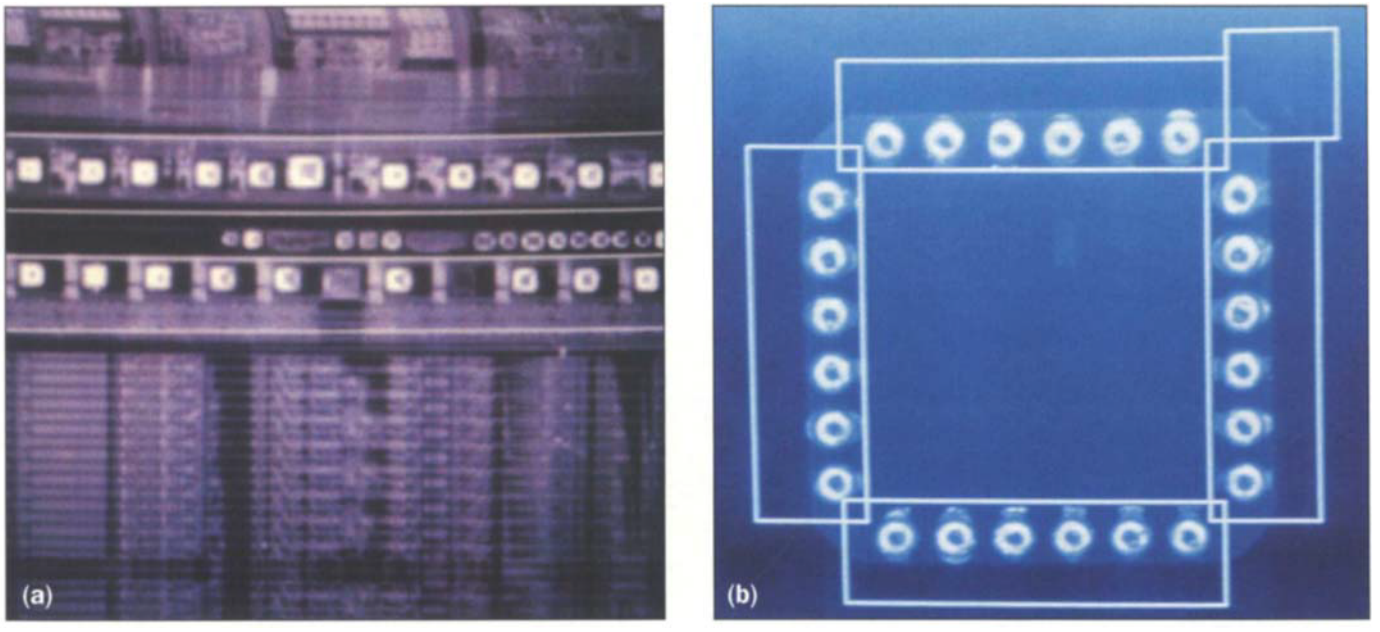


Figure 12. Digitized images of (a) AVP and (b) GDX solder bumps enclosed by windows. The small window in the top-right corner of the device in (b) is used for the detection of solder debris and for the verification of device registration on the inspection fixture.

with special-purpose hardware. These features are:

- Low-pass filtered bidirectional intensity projections
- Average brightness of the image highlights and abrupt changes in brightness
- Local curvatures of the highlights
- Location and inner and outer diameters of these highlights.

For scenes such as those in Figure 12, new intensity maps are created by integrating the gray-scale intensities along each column of the image frame inside each window. This is known as column projection of intensities. The peaks and valleys of the column projection correspond to the solder bumps and the gaps between, respectively. To detect the presence of defects that may not be evident from column projections, we create and analyze row projections as well. These bidirectional intensity projections are then smoothed by convolving them with a one-dimensional, low-pass filter to remove noise before any further investigations. Examples of column projections as graphic overlays on the dark-field images of solder bumps and row projections on bright-field images are shown in Figure 13.

Feature Interpretation and Decision Making. Defective solder bumps are identified by analyzing the spatial characteristics of the individual features. The profiles of the intensity projections are analyzed by determining the width and average height of the peaks and comparing them with expected values. A missing bump is characterized by a missing peak or a low peak in the column projection. An abnormally wide peak indicates solder bridging.

The width of a peak in the column projection is also an indicator of solder overflow or a near-short condition. The average height of a peak indicates overflow, cold solder, or frosty or contaminated bumps. Similarly, the width of a valley is examined to detect missing bumps, splatter, near-shorts, or poor wetting. The width and height of peaks and the number of peaks in the row projection of bright-field images indicate poor wetting and overflow.

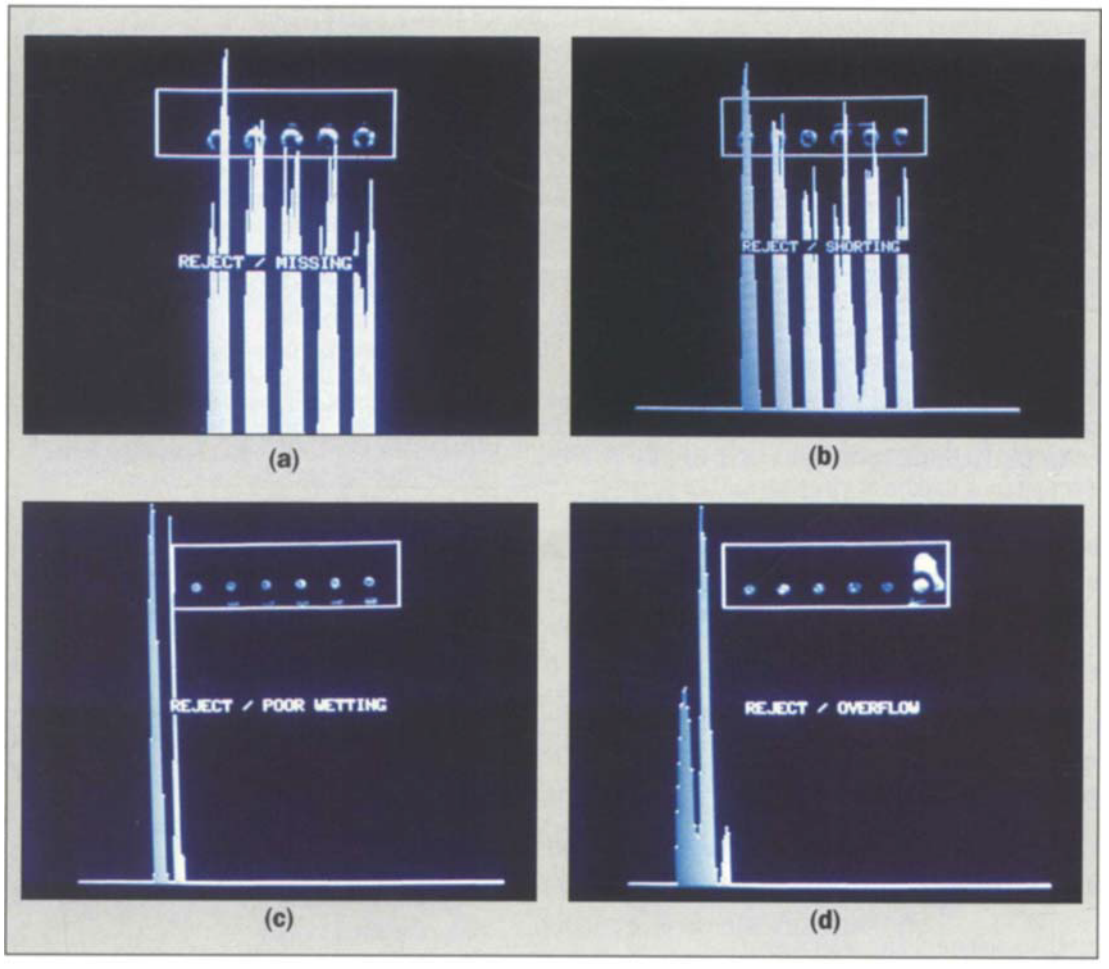


Figure 13. Intensity projections of GDX solder bumps: (a) missing bump, (b) bridging, (c) poor wetting, and (d) solder overflow.

Discussion

This paper has focused on technical issues related to the illumination and imaging of solder bumps. Visual signatures of solder-bump defects under various illumination schemes are characterized for efficient identification and classification of defects during automatic inspection. Fatal solder-bump defects, such as missing bumps and solder bridging, can be detected and classified reliably by dark-field imaging techniques. However, various nonfatal defects confined to planar regions can be detected only by processing a secondary image acquired under bright-field illumination. This technique helps to resolve any ambiguities in one image by using a second image for verification. The additional time involved can be significantly reduced if most of the processing is performed on the high-contrast, dark-field images and only a few preselected regions of the bright-field image are examined for further details. If cycle time constraints do not permit the acquisition and processing of a second image, dark-field illumination is preferred, because of its high contrast and superior capabilities in detecting fatal defects.

Our inspection results show that, for a scene con-

taining specular objects, image contrast is more dependent on illumination geometry than the wavelength of the incident light. These also show that this inspection technique is capable of detecting visible solder-bump defects including cosmetic defects, with a very low false-acceptance rate.

An automation system with such performance characteristics gives the process engineer a consistent means of verifying quality. If this information is correlated with yield, more significant data can be fed back into the process.

The GDX solder-bump inspection systems currently in operation at AT&T Microelectronics' Reading Works have had a significant impact on the production process. The number of outgoing GDX devices with defects related to solder bumps (per million devices tested) has dropped by a factor on the order of 10^2 within a period of six to eight months, to a defect statistic considered quite insignificant by most quality-control standards. This is because of a combined effect of reliable inspection and improved process control.

Although solder-bump inspection has been the subject of our study, this method may also be applicable to problems such as lead-through-hole solder joint, post-solder surface-mount, and solder-paste inspection. It can also extend beyond solder-related applications to the inspection of 3D surface topography of metallic parts and specular components.

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