SYNTHESIS OF HIGH-QUALITY ULTRA-THIN GATE OXIDES FOR ULSI APPLICATIONS

Pradip K. Roy and Ashok K. Sinha

Pradip K. Roy *is a member of technical staff in the VLSI Processing Technology Department at AT&T Bell Laboratories, Allentown, Pennsylvania. He works on process development for ultra-thin oxides and characterization of the oxide-semiconductor interface in VLSI/ULSI technology. He received a B.S. from the Indian Institute of Technology, Kharagpur, an M.S. from the University of Alberta, and a Ph.D. from Columbia University, all in material science and technology. He joined AT&T in 1982.*

Ashok K. Sinha *is vice president of the Manufacturing Technology Development Division of SEMATECH Corporation, Austin Texas, on loan from AT&T Bell Laboratories. He is responsible for development of manufacturable process modules and their integration, testing, and assembly. He has* (continued on page 174)

A critical challenge in achieving ultra-large-scale-integration (ULSI) is growing ultra-thin oxides with low defect (D_o) and interface trap (Q_{it}) densities and generating a planar stress-free silicon/oxide (Si-SiO_2) interface. This paper describes the fabrication of a thin, multilayered, stacked SiO_2 structure with such characteristics. The dramatic improvement in the quality of these stacked oxides has been achieved through a novel synthesis of a three-step process that involves growing, depositing, and growing SiO_2 layers on silicon substrates by thermal oxidation, chemical vapor deposition, and densification/oxidation, respectively. These oxides have an ideal combination of low defect and interface trap densities. The Si-SiO_2 interface generated during the synthesis is structurally superior. Oxides of this high quality are needed—with shallow junctions and fine-line geometries—to produce scaled-down devices that can be integrated into ULSI circuits with multilevel interconnects.

Introduction

The pervasiveness of silicon-based semiconductors in electronic systems is a result of the unique ability of single-crystal silicon to grow thermally an amorphous stoichiometric oxide with an interface (transition zone) only a few atomic layers wide. Metal-oxide-silicon field-effect transistors (MOSFETs) are used in circuits ranging from memories to microprocessors to custom logic circuits for functions such as echo cancellation, voice recognition, data encryption, and high-definition television. Indeed, the power of silicon circuits is limited only by their size or the level of integration.

A major hurdle to achieving ultra-large-scale-integration (ULSI—more than 10 million transistors on a chip) has been the inability of process technologists to grow ultra-thin oxides with low defect

Panel 1. Symbols and Abbreviations

D_o	defect density, cm^{-2}
DRAM	dynamic random-access memory
F_{bd}	breakdown field, MV/cm
FOX	field oxide
FTIR	Fourier transform infrared spectroscopy
HCl	hydrochloric acid
HF	hydroflouric acid
H_2O_2	hydrogen peroxide
H_2SO_4	sulfuric acid
LOCOS	local oxidation of silicon
LPCVD	low-pressure chemical vapor deposition
Mb	megabit
MOS	metal-oxide-semiconductor
NH_4OH	ammonium hydroxide
N_{mi}	mobile-ion concentration, cm^{-2}
ONO	oxide-nitride-oxide
Q_f	fixed charge, cm^{-2}
Q_{it}	interface trapped charge, cm^{-2}
RTA	rapid thermal anneal
RTO	rapid thermal oxidation
Si	silicon
SiH_4	silane
SiO_2	silicon dioxide
SiO_xN_y	silicon oxynitride
Si_3N_4	silicon nitride
SRAM	static random-access memory
TCA	trichloroethane
TCE	trichloroethylene
TEM	transmission electron microscopy
TEOS	tetraethyl orthosilicate
TOX	thin oxide
ULSI	ultra-large-scale integration
V_D, V_G	drain and gate voltages
V_{FB}	flat-band voltage, V
VLSI	very large scale integration
XRMD	x-ray microdiffraction
Δ_{FB}	flat-band shift, V

density and atomically sharp interface. Combined with shallow junctions and fine-line geometries, such high-quality ultra-thin oxides will make possible scaled-down devices for integration into ULSI circuits through multilevel interconnects.

This paper describes the synthesis of a thin multilayer stacked oxide structure that should allow us to build circuits with physical features measuring less than 0.5 micrometer (μm). Moreover, the new process introduces the concept of stress relief at virtual interfaces. Stress relief should dramatically reduce defect density in other thin insulators as well. It should therefore be useful in many diverse applications, such as charge-storage capacitors, charge-coupled devices, three-dimensional integrated circuits, and heterostructures composed of dissimilar semiconductor layers.

Driving Force behind Stacked Oxide Structure

As metal-oxide-semiconductor (MOS) technology continues to advance and feature sizes shrink, a scaling down in the vertical dimension also occurs. Critical to the success of these advanced devices is a reliable and high-quality gate dielectric with a low defect density (D_o) and a high breakdown field strength (F_{bd}) that retains its quality during advanced processing.[1] Previous reviews[2] indicate that, with careful processing, such as use of RCA-type pregate oxidation cleanup and 2 to 5 percent chlorine-bearing species [hydrochloric acid (HCl), trichloroethane (TCA), or trichloroethylene (TCE)] in the oxidant during oxide growth, D_o and the breakdown strength of the gate dielectric can be greatly improved. In addition, workers have reported various fine-tuning procedures in the oxidation process, such as multistep processing (dry-wet-dry oxidation)[3] and growth-modified oxidation by insertion of several *in situ* perturbations, such as a high-temperature Cl^- getter and a stress-relief annealing treatment that generates oxides with D_o in the range of 0.8 to 2.0 cm^{-2}.

As the oxide gets thinner [(less than 150 angstroms (Å)], the quality of the oxide (SiO_2)—even under

the best possible external growth conditions—is limited by natural viscoelastic compressive stress[4] generated in SiO_2 at temperatures below 1000°C and by the thermal expansion mismatch between silicon and SiO_2. With a multilayered oxide-nitride (SiO_2-Si_3N_4) dielectric, Watanabe et al.[5] achieved a genuine lowering of D_o in the range of 0.2 to 0.5 cm^{-2}. However, the Si_3N_4-SiO_2 interface is invariably associated with a high density of interface states[6] (Q_{it}) that cannot be annealed out easily because the Si_3N_4 layer is impervious to diffusion of oxidizing species. These multilayered dielectrics are unsuitable as gate dielectrics in advanced CMOS ICs, because the interface states can cause charge-induced shift in threshold voltage and can reduce channel conductance[7] during operation.

The concept of stacking thermally grown and chemical-vapor-deposited (CVD) SiO_2 is borne out by the multilayered SiO_2-Si_3N_4 structure. The interface between grown and deposited SiO_2 layers is virtual,[8] but serves the same purpose as the real interface in SiO_2-Si_3N_4 structures; that is, it reduces D_o by misaligning defects across the interface. More important, the interface traps in stacked oxide structure can be removed easily by an oxidizing anneal, since the top deposited SiO_2 layer, unlike the Si_3N_4 film, is transparent to oxidizing species—that is, transports them by diffusion. The stacking concept can be applied to any dual dielectric structure $(SiO)_2$ plus another dielectric) with similar results as long as the top dielectric is transparent to the oxidizing species. This allows us to grow a structurally superior third oxide layer during a subsequent oxidizing anneal.

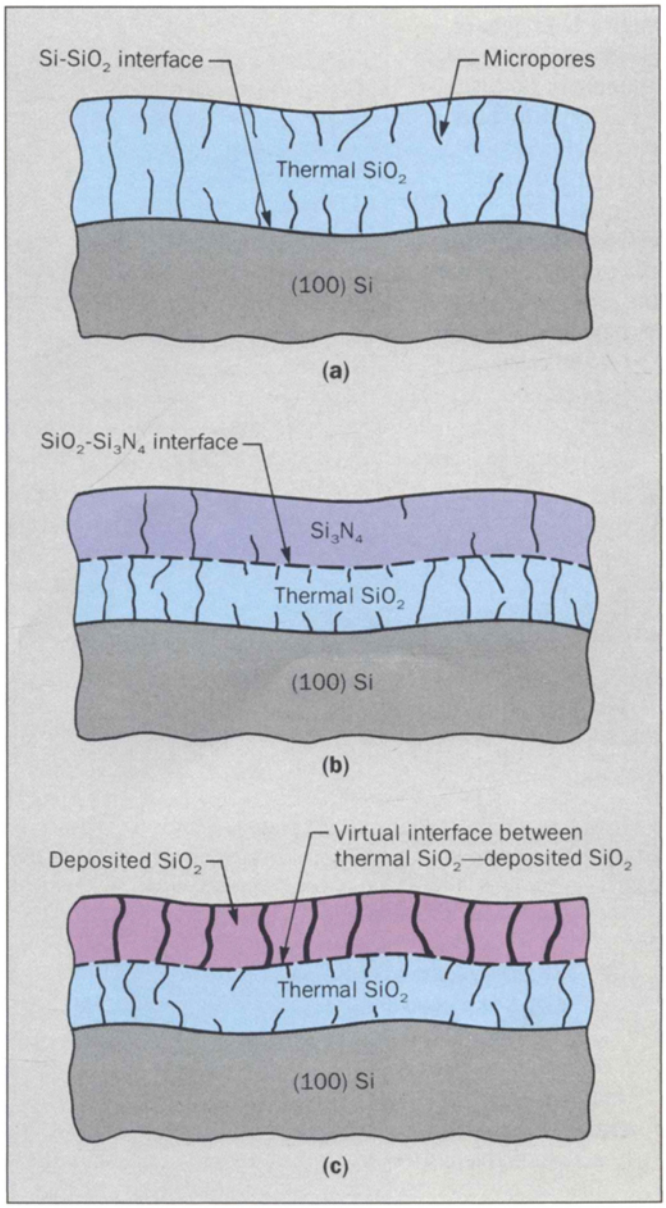

Figure 1. Micropores in SiO_2 films with and without interface layers. (a) Thermal SiO_2; defect density D_{os}. (b) SiO_2-Si_3N_4 dual dielectric; defect density D_{ob}. (c) Stacked SiO_2; defect density D_{oc}. Effective density D_{ob}, $D_{oc} \ll D_{os}$.

Background on Stacked Oxide Process Design

Major factors contributing to defects in thin-oxide gate dielectrics are growth-induced micropores and the

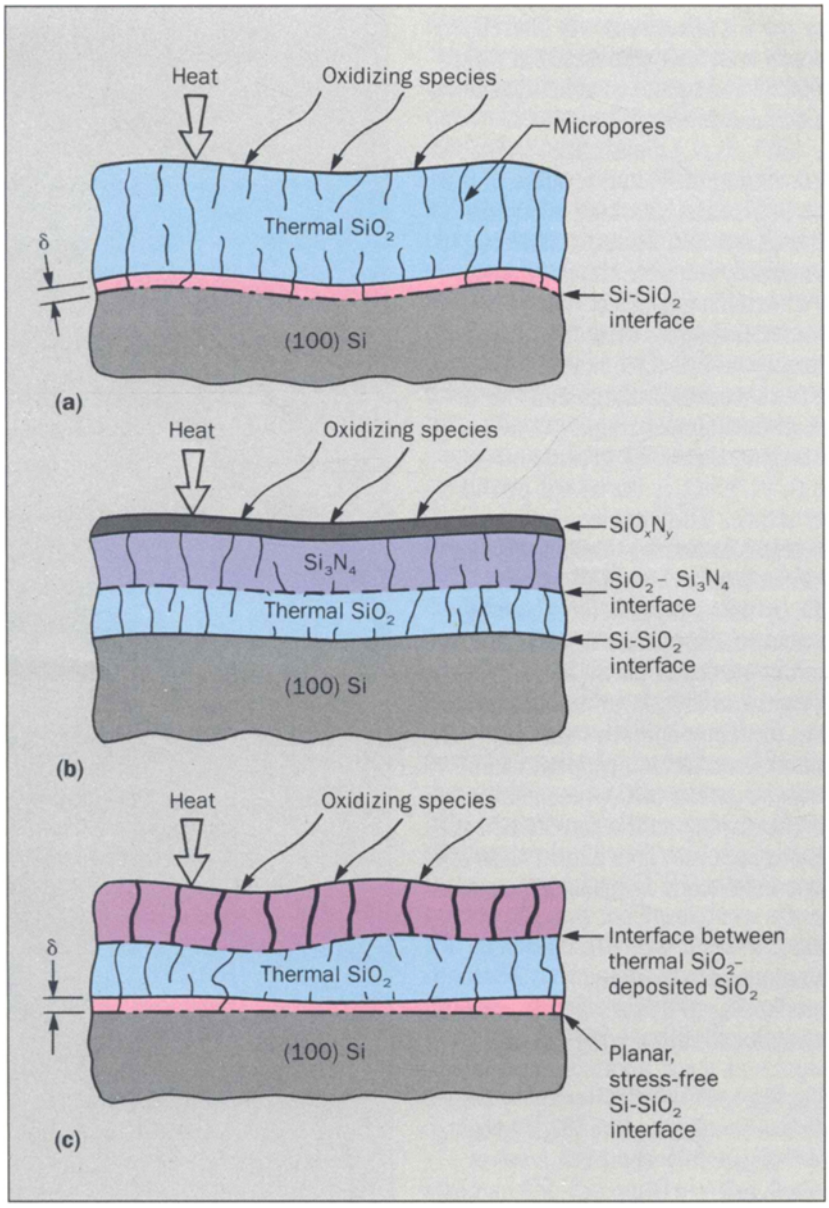

Figure 2. Effects of oxidizing densification annealing: (a) SiO_2 films, (b) SiO_2-Si_3N_4 dual dielectric, (c) thermal SiO_2 and deposited SiO_2 stacked films. The dimension δ indicates the movement of the Si-SiO_2 interface during densification annealing.

intrinsic stress within the oxide layer.[9,10] The micropores are 10 to 25 Å in diameter, with an average separation of about 100 Å. The pores form at energetically favored sites (such as heterogeneities created by localized contaminants, ion-damaged areas, dislocation pileups, and other defect areas) on the silicon surface as a result of retarded oxidation in these sites. The pores grow outward as oxidation continues to consume silicon around the pore. Thus, a network of micropores usually exists in SiO_2 (shown schematically in Figure 1a). The micropore network forms potential short-circuit paths for diffusional mass transport and for current leakage.

In addition, the stress within a SiO_2 layer, often accentuated by complex device geometries and processing, usually increases both the size and density of the micropores. Therefore, in developing thin dielectrics with ultralow D_o, one not only has to reduce initial D_o, but also reduce local stress-gradients near the Si-SiO_2 interface by providing a stress-accommodating layer, such as an interface within the dielectric that acts as a stress cushion and defect sink. Figure 1b and c shows schematic representations of an interface layer that reduces the effective D_o by misaligning the micropores and other interconnecting defects.

During densification/oxidation annealing (at 850 to 1150°C) in Si-SiO_2 structures, the oxide grows with the inward advance of the Si-SiO_2 interface (δ) from the reaction of silicon with the incoming oxidizing species[11] to which the SiO_2 layer is transparent. The newly formed Si-SiO_2 interface, in this case, virtually mimics the interface before the densification anneal, as shown schematically in Figure 2a. The Si-SiO_2 interface in a Si_3N_4-SiO_2 dual-dielectric structure, on the other hand, remains virtually intact during an oxidizing anneal (Figure 2b) because the Si_3N_4 layer is opaque to the diffusional transport of the oxidant and only the top layer of the Si_3N_4 film gets oxidized to form a silicon oxynitride (SiO_xN_y) layer.[12] The top deposited SiO_2 layer in a stacked oxide structure,[8] unlike Si_3N_4, is transparent to the diffusional

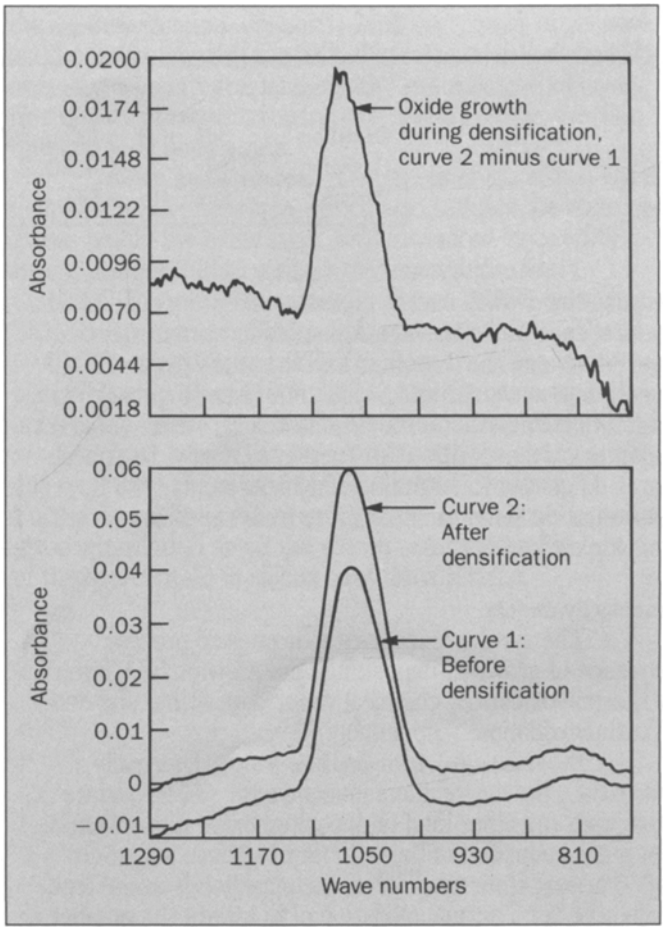

Figure 3. FTIR absorbance spectra for stacked thermal SiO_2 and TEOS SiO_2 composite oxide films before and after densification.

transport of the oxidizing species. During a densification anneal, the SiO_2 growth occurs by the interfacial reaction of the oxidizing species and silicon with a simultaneous densification of the top deposited layer.

Table I. Reactions and Conditions for LPCVD

Type	Reaction	Conditions
Oxidation	$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$	300—450°C, 0.2—0.5 torr
Oxidation	$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2$	300—450°C, 0.2—0.5 torr
Pyrolysis	$Si(OC_2H_5)_4 \rightarrow SiO_2$ + by-products	600—750°C, 0.2—0.5 torr

The newly grown SiO_2 is structurally superior because the growth occurs in near-equilibrium condition in the presence of a stress-accommodating virtual interface layer[13] between the deposited and thermally grown SiO_2 layers. The newly formed Si-SiO_2 interface (Figure 2c) is structurally smoother with very little local stress variation and interfacial asperities.[14,15] Furthermore, the interface states do get annealed during densification, and the stacked oxide structures therefore have superior charge-trapping characteristics.

Process Synthesis

The synthesis involves a three-step process sequence of growing, depositing, and growing SiO_2 layers by thermal oxidation, chemical vapor deposition, and densification/oxidation, respectively.

The First Layer—Thermally Grown SiO_2. Thermally grown SiO_2 passivates the semiconductor silicon surface more than any other kind of deposited oxide film. *Passivation* is the reduction of the number of surface states (10^{15} cm^{-2}) arising from unsatisfied chemical bonds at the free surface of Si.[9] Thermal oxidation of Si lowers the number of dangling bonds to about 10^{10} states/cm^2 with the formation of a very stable SiO_2, and the first layer of the stacked oxide therefore is grown thermally.

The silicon surface oxidizes by reaction with the oxidant as the oxidant migrates inward. Thus, the silicon surface is constantly renewed by oxidation and many of the surface and bulk defects are removed. Normally, thermal energy drives the oxidant through the growing SiO_2 layer, but oxidation can be enhanced by photon flux[16] or electric field.[17] Oxidation can be carried out in a conventional hot-wall atmospheric-type furnace[18] or by rapid thermal processing (RTP)[19] using lasers, electron beams, or incoherent halogen lamps as the heat source for very short, high-temperature treatment.

The Second Deposited SiO_2 Layer. The passivation of a silicon surface is no longer critical after the growth of the first SiO_2 layer, and surface-state generation is minimized[20] when the deposited second SiO_2 layer is stacked on the first grown layer. More importantly, the second layer must be deposited rather than grown if it is to form a virtual interface[8] that reduces effective D_o and acts as a stress-accommodating layer.

Thin SiO_2 films are usually deposited by low-pressure chemical vapor deposition (LPCVD) methods from oxidation of silane (SiH_4) with oxygen or nitrous oxide (N_2O) or from pyrolysis of tetraethyl orthosilicate [TEOS, $Si(OC_2H_5)_4$]. The reactions are listed in Table I. These LPCVD methods generate conformal coverage with reproducibly uniform thickness. CVD reactions can be enhanced—and, therefore, deposition temperature can be lowered—for specialized VLSI processing by dissociating the reactant molecules by the following LPCVD methods:

- Plasma-enhanced (PE) CVD[21]
- Electron cyclotron resonance (ECR) plasma-enchanced CVD[22]
- Photochemically induced (PH) CVD[23]
- Laser-activated (L) CVD.[24]

The Third Grown Layer—Oxidation/Densification. The final step of the synthesis is to grow a third SiO_2 layer underneath the first grown layer by an oxidizing reaction at the interface. This occurs

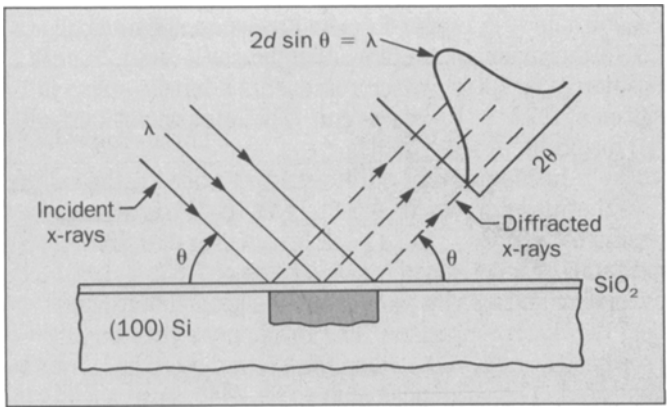

Figure 4. Si (400) diffracted peak profile in SiO_2-Si structure under Bragg diffraction condition.

during densification annealing in mild oxidizing conditions.[8]

The densification anneal is usually performed in an atmospheric hot-wall (750 to 900°C) furnace. However, rapid thermal annealing (RTA)[25] can also be used in a short, high-temperature (1000 to 1150°C) cycle in a mild oxidizing atmosphere diluted by nitrogen or argon gas. During densification, the third oxide layer grows under near-equilibrium conditions in the presence of a stress-accommodating virtual interface layer that serves as a defect sink. Two events occur: traps get annealed out and a planar and stress-free[8] Si-SiO_2 interface is formed by the newly grown SiO_2.

Results and Discussion

The results of measurements on the three-layer, ultra-thin gate oxide are discussed below.

Oxide Thickness. In-process oxide thickness measurements were made by ellipsometry (λ = 5461 Å)[26] and were confirmed by the Fourier transform infrared (FTIR) Si-O absorbance spectra[27] of the 1100 cm^{-1} band. Figure 3 shows typical FTIR Si-O spectra for the stacked-oxide structure before and after densification. The difference spectrum (area) is a direct measure of SiO_2 growth (δ) during densification. The Si-O 1100 cm^{-1} peak areas have a 1:1 correlation with the SiO_2 thickness measured by ellipsometry. The integral peak width[27] is a measure of oxide film quality in terms of micropore density within the SiO_2 film and Si-O bond strain.

Stress Measurements. The stress in the silicon layer near the Si-SiO_2 interface, which also reflects the state of stress within the oxide layer, was measured by Si (400) Bragg peak profiling[13] using x-ray microdiffraction (XRMD). Figure 4 schematically shows XRMD on a Si-SiO_2 structure under Bragg diffraction conditions. The Si (400) 2θ peak position is a direct measure of the interplanar spacing (d) of (400) planes. Any deviation from the unstressed value of $2\theta_o$ is a measure of lattice dilatation ($d - d_o$ or Δd), which can be converted to the stress in silicon (σ_{Si}) from the elastic stiffness values of silicon.[28] Furthermore, the peak breadth in the Si (400) peak profile gives information about the silicon substructure[8] in terms of the defect state in silicon near the interface.

$$\sigma_{Si} = \frac{E}{1-\upsilon}\epsilon = \frac{E}{1-\upsilon}\frac{\Delta d}{d_o} = \frac{E}{1-\nu}\left(\frac{\sin\theta_o}{\sin\theta} - 1\right)$$

where E = modulus of elasticity
ν = Poisson's ratio
ϵ = relative lattice strain

$\frac{E}{1-\upsilon}$ = 2.26×10^{12} dynes/cm^2 for (100) Si

$2\theta_o$ = 69.1975 for Si (400) unstressed crystal

Figure 5 shows the Si (400) 2θ peak profiles of the stacked SiO_2 film at various stages of the synthesis.

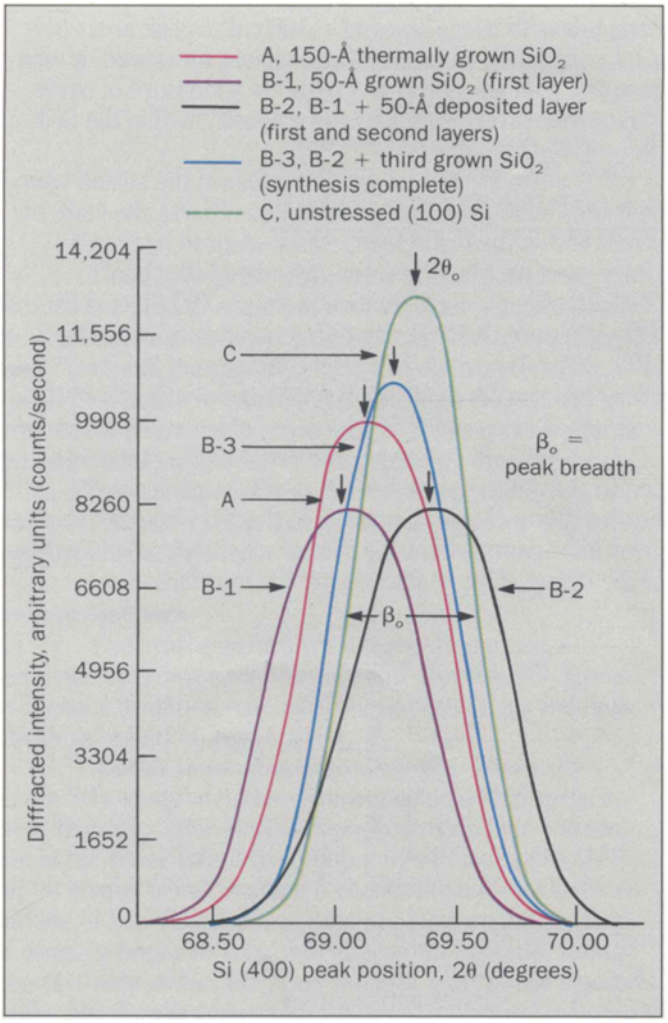

Figure 5. XRMD Si (400) peak position profile in (100) Si-SiO_2 structure for stacked oxide films (150 Å) at various stages of processing. Peak position indicates σ, peak broadening indicates substructure, and peak area indicates microtexture.

Peak profile A in Figure 5 corresponds to conventional 150-Å thermally grown film and indicates a (400) 2θ peak position of 69.1000°, which represents a tensile stress in silicon of 2.72×10^9 dynes/cm². The integral peak breadth (β) for profile A is 0.7450°.

In comparison, during stacked oxide synthesis, the first thermally grown 50-Å SiO_2 layer (B-1) has a peak position at 68.9260° and a peak broadening of 0.7520°, indicating respectively a tensile stress of 7.83×10^9 dynes/cm² and a slight worsening in silicon substructure near the Si-SiO_2 interface. The Bragg peak gets slightly broader ($\beta = 0.7700°$) when the second 50-Å SiO_2 layer is deposited. The large peak shift to 69.2440° corresponds to a mild compression of -0.91×10^9 dynes/cm² as a result of stacking and stress accommodation by the virtual interface (B-2). After oxidation/densification annealing and the formation of a newly grown SiO_2 layer, the Si (400) peak position corresponds to a nearly zero-stress value (0.20×10^9 dynes/cm²). The simultaneous reduction in peak broadening to a value of 0.7250 Å indicates a superior substructure of silicon near the interface (B-3). Profile B-3 almost mimics profile C for unstressed (100) Si crystal, indicating that the Si-SiO_2 interface generated by this new oxidation process is stress-free.

Table II summarizes the Si (400) Bragg peak profiling results and the calculated stress data in silicon near the interface for various gate oxide thicknesses used in different technologies. Table II also gives the peak profile data at various phases of synthesis.

Lattice Imaging of the Si-SiO_2 Interface. In a transmission electron microscope (TEM), forming an observable image depends upon two interrelated processes: interaction of electrons with the specimen and transfer of the interaction to a photographic plate by the objective and image-forming lenses.[29] In the high-resolution imaging mode, the objective lens of the TEM brings the various diffracted beams to interference in the image plane. As a consequence, a lattice image, which is simply an electron interferogram, is formed. The contrast in the image is due

Table II. Stress from Si (400) Peak Profile

Oxide processing	Nominal thickness (Å)	Si (400) peak profile		Stress in Si
		Position (2θ°)	Width (β°)	(10^9 dynes/cm^2)
Conventional thermal SiO_2	50	68.9260	0.7580	7.83
	100	69.0200	0.7520	4.75
	125	60.0400	0.7460	3.50
	150	69.1000	0.7400	2.71
	250	69.1400	0.7360	1.58
Stacked oxide (grown/deposited) predensification	50/30	69.2400	0.7750	−0.91
	50/50	69.2500	0.7650	−1.20
	100/100	69.3240	0.7580	−3.61
Stacked oxide (grown/deposited/grown) postdensification	100 → 50/30/20	69.1750	0.7400	0.48
	125 → 50/30/45	69.1820	0.7300	0.48
	150 → 50/50/50	69.1930	0.7250	0.20
	250 → 100/100/50	69.2050	0.7120	−0.44
Si (100) unstressed		69.1975	0.7000	0

either to electron diffraction (amplitude contrast) or to electron interference (phase contrast). With phase contrast, which was used in the present investigation, one obtains the images of atomic planes of appropriate Miller indices by interference of diffracted beams with the undiffracted beam in the image plane.

Changes in Si-SiO_2 interface roughness and asperities were observed directly from Si (111) lattice images using a TEM.[30] Specimens were prepared from Si-SiO_2 cross sections cleaved parallel to the [100] direction by argon milling the interfacial area to a thickness of about 1800 Å. Figure 6 shows lattice image pictures of the Si-SiO_2 interface for thermal and stacked SiO_2 films. There was a drastic reduction in interfacial roughness (less than 10 Å) for the stacked interface. In comparison, the standard thermal SiO_2 interface has a roughness of about 25 to 35 Å. The silicon layer near the interface—indicated by parallel lines from Si (111) planes at a 54.7° angle with respect to the [110] direction—showed different degrees of phase contrast in conventional and stacked oxide films. The relatively large contrast modulation in the lattice image of the silicon layer near the interface for thermal SiO_2 was due to localized strain fields. Strain fields were minimized in stacked SiO_2 films because the SiO_2 formed during densification generated very little stress in the underlying silicon. These results were confirmed by XRMD stress data. Figure 6 also shows the TEM bright-field picture of a virtual interface formed between the grown and the deposited SiO_2 layers before the densification anneal.

Dielectric Breakdown and Defect Density. The test structure[31] used for D_0 measurements in oxide films involved an actual device structure (a 1-megabit DRAM) processed through LOCOS isolation, polysilicon deposition

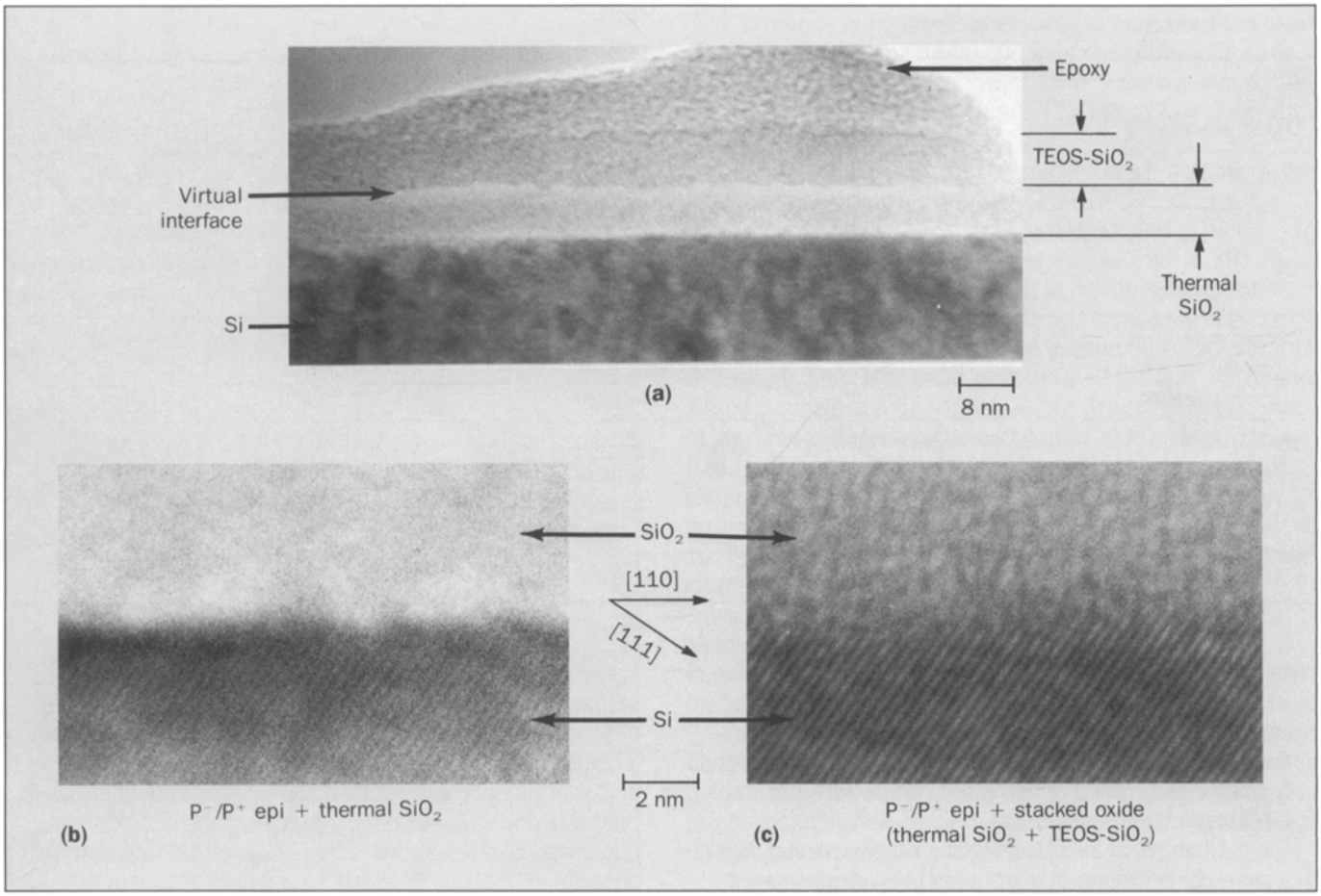

Figure 6. Bright-field electron micrograph of virtual interface (a) and Si (111) lattice images at Si-SiO_2 interface for two different gate oxides (b) and (c).

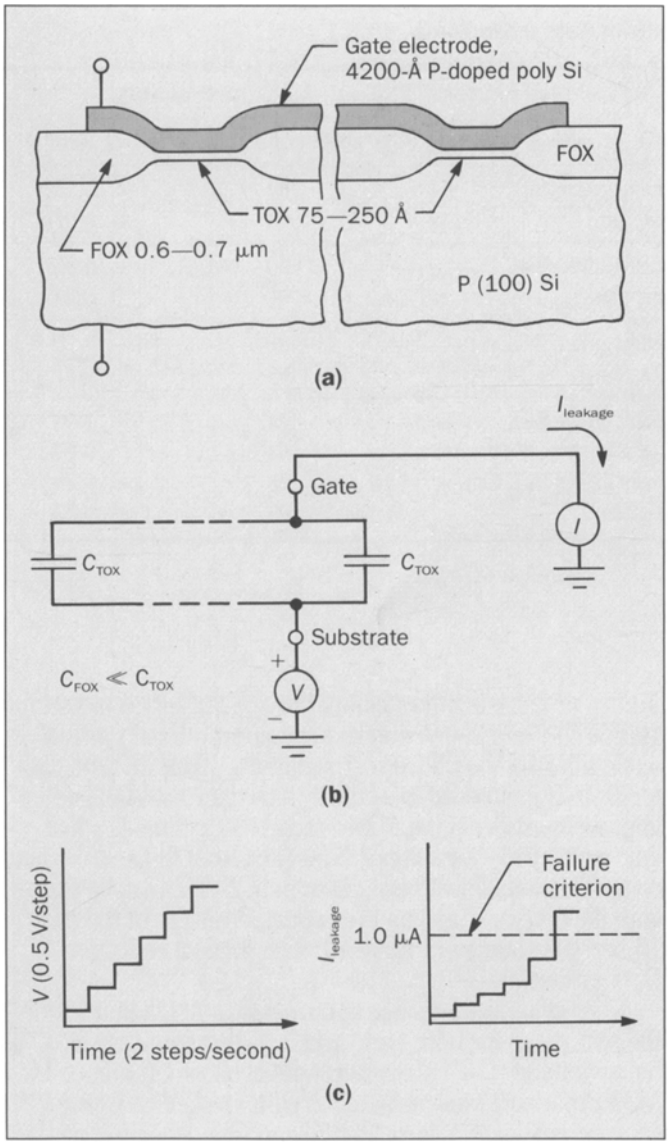

Figure 7. Measuring leakage and breakdown of gate oxides: (a) physical structure, (b) electrical schematic, (c) applied bias.

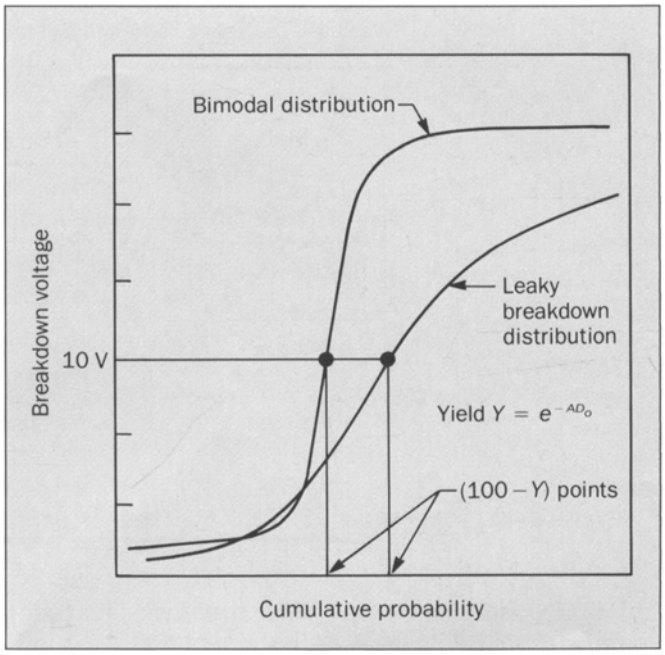

Figure 8. Probability distribution of measured breakdown voltages for different leakage criteria (20 nA, 1 μA, and destructive breakdown). The defect density D_o is calculated from the dielectric yield (the percentage of sites passed under a field of 6.67 MV/cm).

Table III. Dielectric Yield and Defect Density in Gate Oxide Films

Technology	Thermal SiO_2 growth process	Gate oxide quality	
		Dielectric Y (%)	D_o (cm^{-2})
1.25 μm (1 Mb DRAM)	250-Å conventionally grown SiO_2	90	0.35
	250-Å stacked SiO_2 film	98	0.07
1.25 μm	210-Å conventionally grown SiO_2	90	0.35
	210-Å stacked SiO_2 film	97	0.10
0.9 μm	150-Å conventionally grown SiO_2	81	0.70
	150-Å stacked SiO_2 film	95	0.17
0.6 μm	125-Å conventionally grown SiO_2	74	1.00
	125-Å stacked SiO_2 film	94	0.20
	100-Å conventionally grown SiO_2 film	68	1.28
	100-Å stacked SiO_2 film	92	0.28

and doping, and patterned to provide one single field plate over the entire chip (Figure 7). Tests were performed by applying a negative ramp [− 1 volt/second (V/s)] and measuring the leakage current as a function of applied bias until 1 microampere (μA) was reached. The negative polarity with respect to P substrates forces the capacitor into accumulation, thus minimizing surface depletion and voltage loss in the silicon regions.[32] The setup recorded both self-healing and destructive breakdown (Fowler-Nordheim tunneling into the oxide) events.

To assure high levels of confidence, 2000 capacitors were tested in each run, typically. Such a large number of measurements was essential for determining and detecting very small changes in D_o for various gate oxides. Results were described as probability distribution plots of the measured breakdown voltages for 1-μA leakage and destructive breakdown criterion shown schematically in Figure 8. D_o was calculated from the yield (Y) data [percentage of sites passed under 6.67 megavolts/centimeter (MV/cm) for area A (0.3 cm^2)] from the equation

$$Y = e^{-AD_o}$$

Figure 9 shows comparative distribution plots[32] for 100-, 150-, and 250-Å stacked and conventional thermal oxide films on the above test structure. Table III lists data for D_o in thin stacked SiO_2 films (less than 150 Å). The improvement in D_o and Y for stacked SiO_2 films is apparent, particularly for thinner (150 Å or less) films. A comprehensive Pareto bar diagram in D_o for various thin gate dielectrics based on the reported results of the past 15 years is shown in Figure 10. The gradual reduction of D_o is evident.

Capacitance-Voltage Characteristics. A schematic of the test setup for both high- and low-frequency capacitance-voltage (C-V) measurements is shown in Figure 11. MOS capacitors were fabricated with stacked as well as conventional gate oxides. Polysilicon was deposited on the oxides and doped with phosphorus. After removal of glass from the back, an aluminum layer, 1 μm on the front and 0.1 μm on the back, was deposited and sintered. The poly-

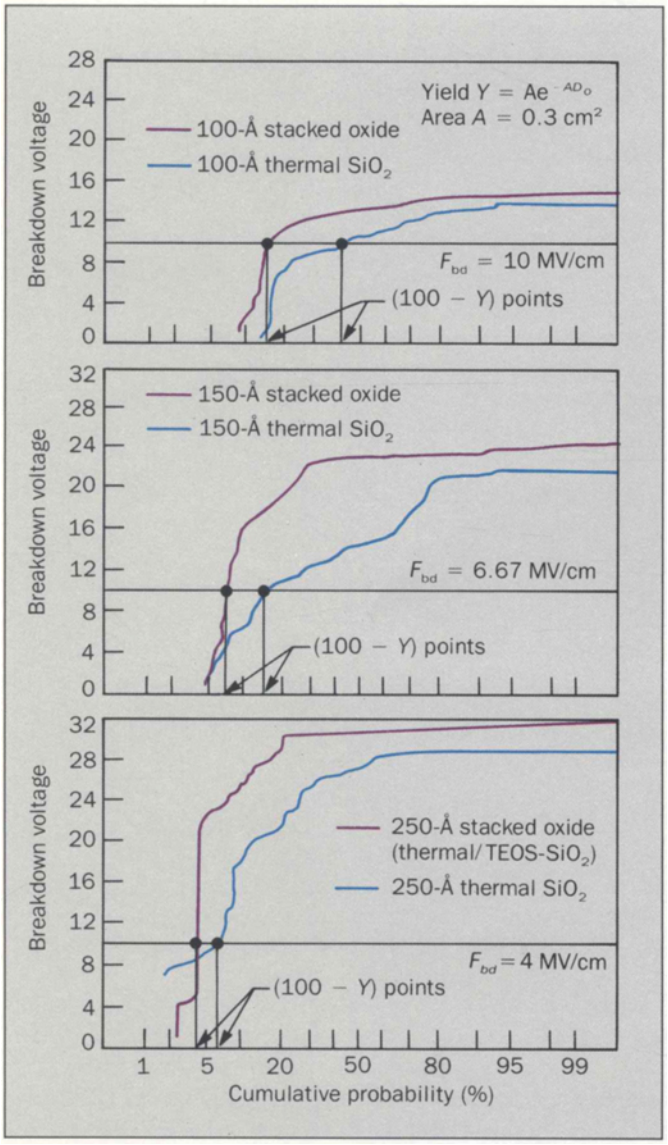

Figure 9. Comparative cumulative probability distributions of breakdown voltage for stacked and thermal SiO_2 films.

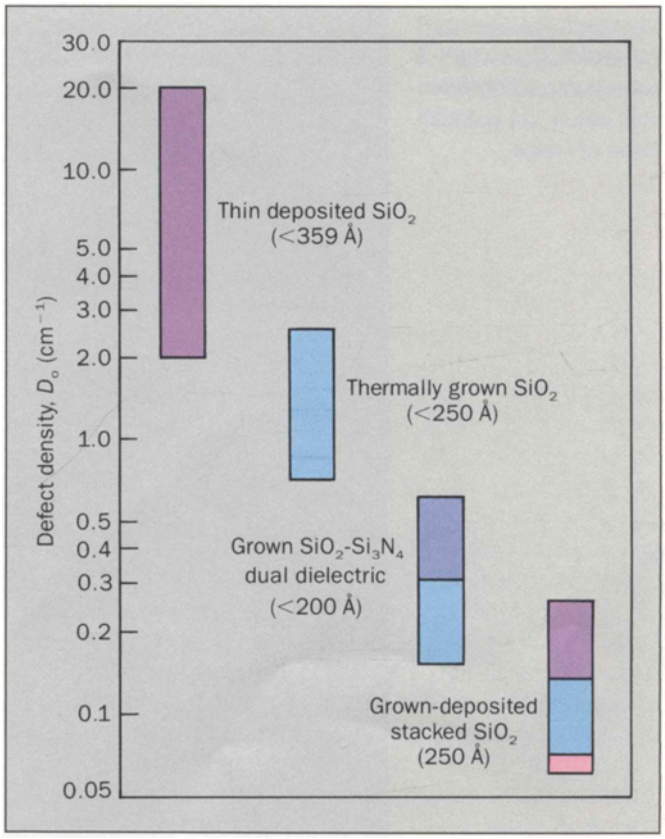

Figure 10. Decrease of defect density in thin dielectric films.

silicon layer was then selectively etched using the aluminum as an etch mask.[33] The *C-V* stability of the oxides was measured by applying bias-temperature stress (BTS)[1,7] to the oxide at 250°C under a 2-MV/cm field for 10 minutes and monitoring the flat-band voltage shift (ΔV_{FB}) in the high-frequency *C-V* curves.

Figure 12 shows BTS effects on *C-V* characteristics for MOS capacitors fabricated from 100-Å stacked and thermal SiO_2 films and 100-Å SiO_2/100-Å Si_3N_4 dual dielectric layers. Stacked oxide films showed virtually no

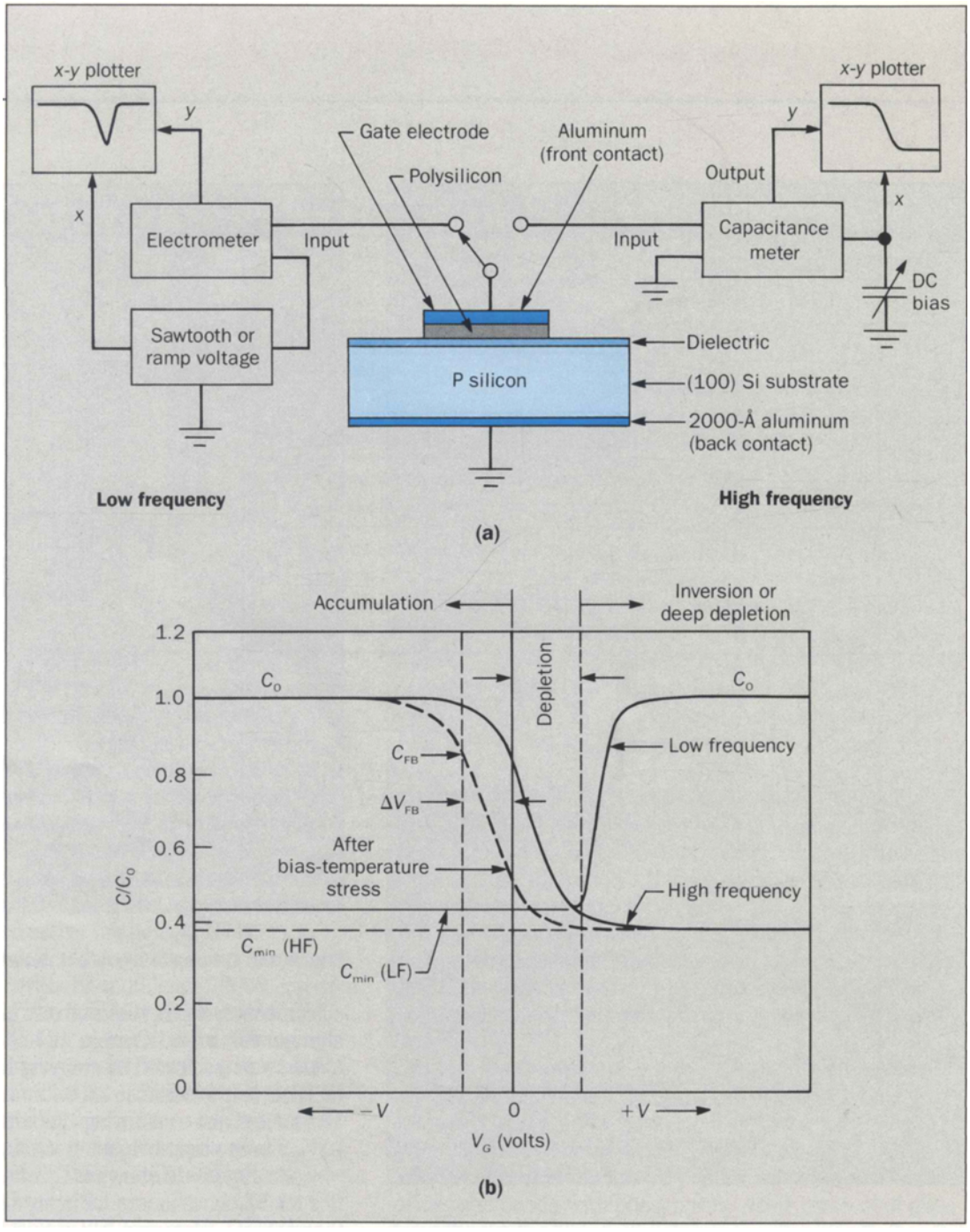

Figure 11. Measuring MOS *C-V* curves for thin gate oxides: (a) test setup, (b) definitions of terms.

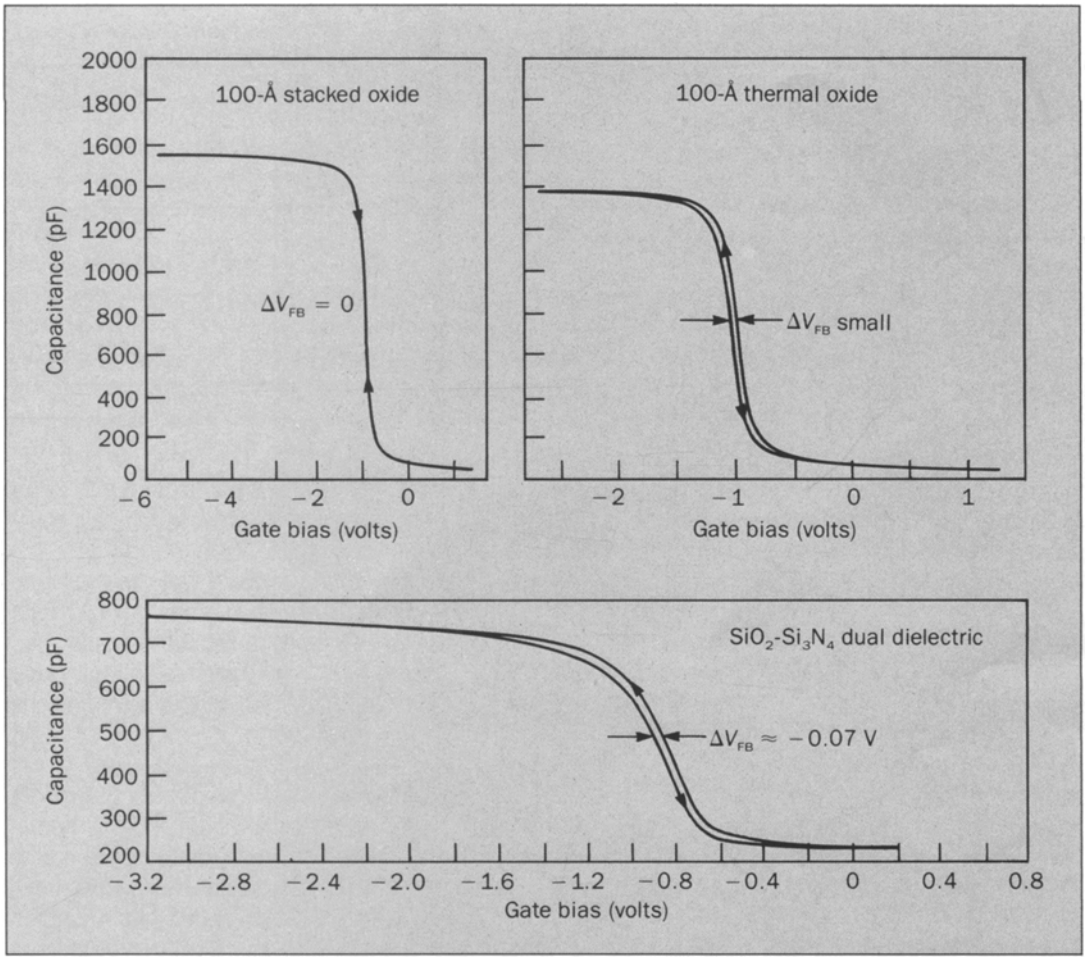

Figure 12. Shifts in C-V plots with bias-temperature-stress aging.

instabilities, and the thermal SiO_2 control films showed only a slight flat-band voltage shift (-0.03 V). In comparison, MOS capacitors made from dual dielectric films showed a rather large ΔV_{FB} of -0.07 V, most likely caused by buildup of positive charge at the interface.

Figure 13 shows the combined high- and low-frequency *C-V* plots on these MOS capacitors. The large difference in capacitance at the onset of inversion for high- and low-frequency plots in SiO_2-Si_3N_4 films was probably due to a high density of interface traps.[8,33] These traps generate additional structures in the low-frequency *C-V* plot in the inversion region. In contrast, thermal and stacked SiO_2 films showed virtually no difference in high- and low-frequency *C-V* characteristics. Additional struc-

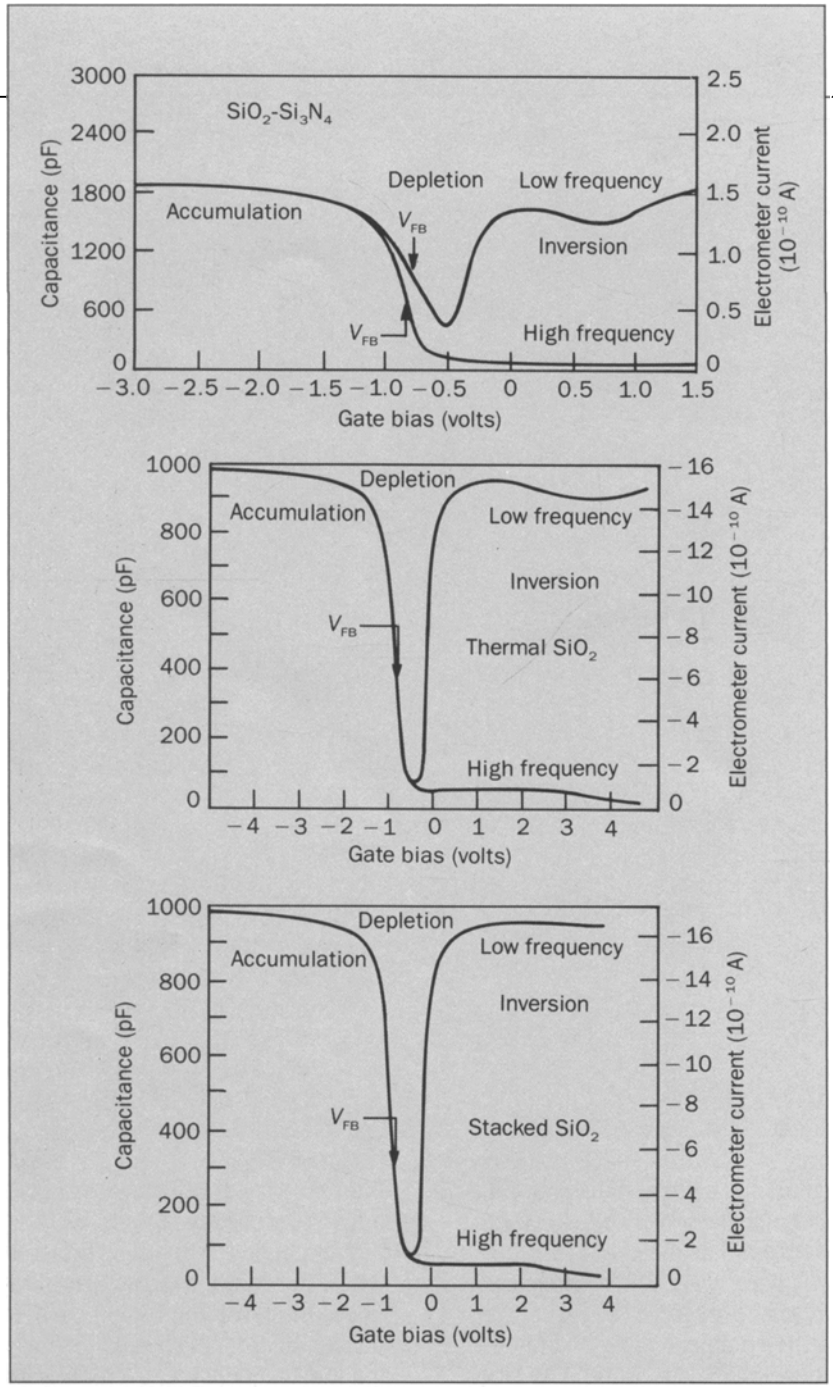

Figure 13. Combined high- and low-frequency *C-V* curves on MOS capacitors.

Table IV. MOS Capacitance-Voltage Results*

Gate dielectric	Nominal thickness (Å)	Trapped charge, $Q_f + Q_{it}$ (10^{10} cm^{-2})	Flat-band voltage, V_{FB} (volts)	Flat-band shift, ΔV_{FB} (volts)	Mobile ion concentration, N_{mi} (10^{10} cm^{-2})
Thermal SiO_2	100	11.4	−0.97	0.03	4.53
Stacked SiO_2	100	3.0	−0.85	0.01	1.51
Thermal SiO_2	150	9.0	−0.98	0.03	4.05
Stacked SiO_2	150	0.5	−0.78	0.00	0.55
Dual SiO_2-Si_3N_4	100/100	15.5	−0.70	−0.70	8.10

*Bias-temperature stressing was done at 2 MV/cm and 250°C for 10 minutes.

tures due to alkali ions in the low-frequency *C-V* curves were also not present.

Results of BTS aging are shown in Table IV. They indicate very low trapped charge (Q_f and Q_{it}), flat-band shift (ΔV_{FB}), and mobile ion concentration (N_{mi}) in stacked SiO_2 films compared to thermally grown SiO_2 films with equivalent thickness. The dual dielectric, as expected, showed even higher density of interface states, ΔV_{FB}, and N_{mi}.

Device Current-Voltage Characteristics. Devices were fabricated in 1.25-μm (1-megabit DRAM), 0.9-μm (64-kilobit SRAM), and 0.6-μm (test structure) technologies, which respectively use 250-, 150-, and 125-Å gate oxides. Transistors were fabricated in other special test structures using 90- and 100-Å stacked oxides. Figure 14 shows the comparative output characteristics (drain current I_D vs. drain voltage V_D for various gate voltages V_G) of N- and P-channel devices fabricated in 0.9-μm technology. The curves indicate good switching characteristics and gate modulation behavior. The transistors with stacked-oxide gates were superior in terms of subthreshold swings and channel mobility degradation. These transistors also show relative insensitivity to hot-carrier effects. At 5.5 V or lower (for 3.3-V and 5.0-V technology), the lifetime is estimated to be 20 years for the stacked oxide as opposed to 10 years for the conventional oxide devices. The stacked oxide gate also shows a low tendency toward hole trapping under ionizing radiation, and thus has superior radiation resistance.

Summary

This study describes synthesis of a thin stacked SiO_2 structure with superior electrical and substructural properties. The dramatic improvement in the quality has been achieved through a novel three-step process which involves growing, depositing, and growing SiO_2 layers on silicon substrates by thermal oxidation, LPCVD deposition, and densification/oxidation, respectively. The stacked oxides have ultra-low defect density (D_o less than 0.15 cm^{-2}) with excellent breakdown and interfacial characteristics.

Such a low defect density is comparable to that previously believed possible only for dual-dielectric Si_3N_4-SiO_2 structures. But the present structure offers an important advantage in that it does not suffer from the high density of traps associated with Si_3N_4-SiO_2 interfaces. MOS capacitor *C-V* analyses on the stacked oxides show well-behaved characteristics with very little charge trap-

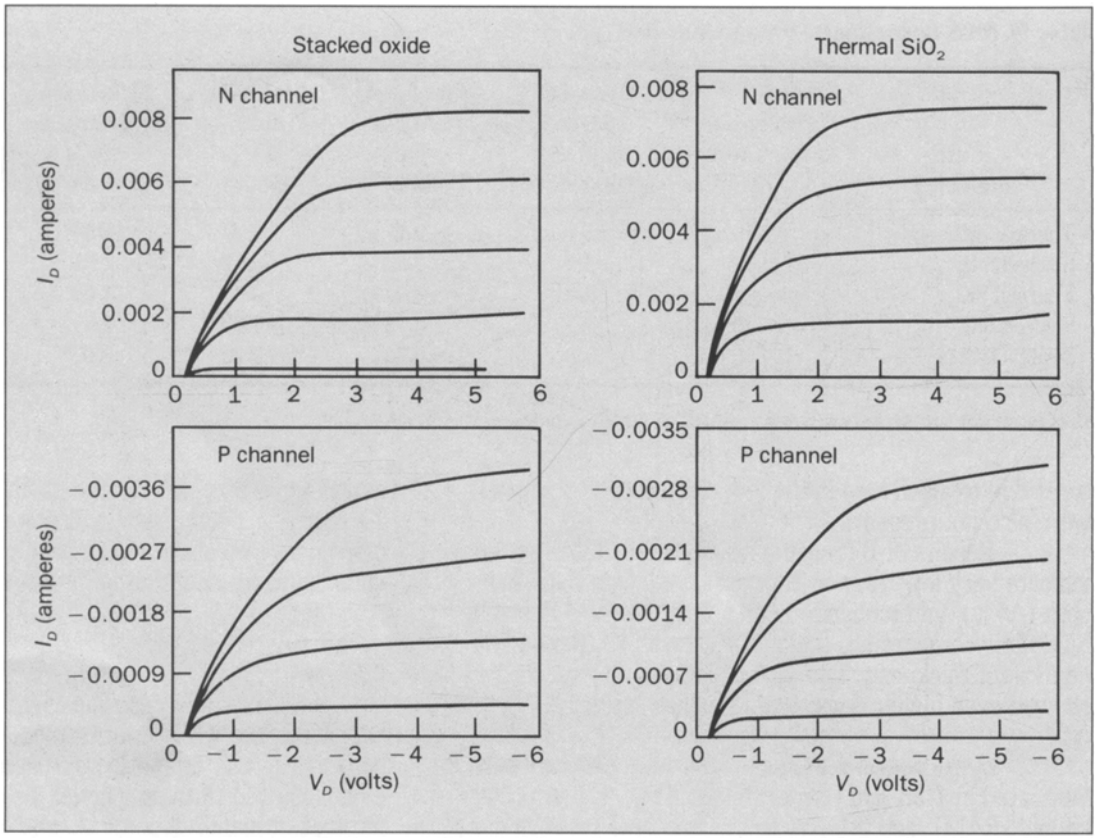

Figure 14. Output characteristics of transistors with 150-Å gate oxide thickness (0.9-μm technology).

ping, mobile-ion contamination, and bias-temperature-stress aging instability.

The drastic lowering in defect density results from misaligning the micropores and other interconnecting defects within the stacked oxide layer and from annihilation of defects during densification/oxidation by the defect sink provided by the virtual interface between the thermally grown and LPCVD-deposited SiO_2 layers.

Superior Si-SiO_2 interfacial characteristics of the stacked oxide are due to the excellent substructure of the SiO_2 grown during densification/oxidation annealing in near-equilibrium conditions in the presence of a stress-accommodating virtual interface layer.

Transistors fabricated from the stacked-oxide gate films show good output characteristics and subthreshold swings and low channel mobility degradation. The relative insensitivity of the stacked-oxide films to hot carrier effects and hole trapping under ionizing radiation allows ULSI circuits in the sub-0.5-μm range to be realized. The reliability of the circuits is expected to be improved because of the ultra-low defect density and planar, stress-free Si-SiO_2 interface.

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Biographies (continued)

a B.E. from the Indian Institute of Science, Bangalore, and a Ph.D. from Oxford University, England, both in materials science. He joined AT&T in 1970.

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