III-V DEVICE TECHNOLOGIES FOR ELECTRONIC APPLICATIONS

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The electronic and optical properties of III-V materials can be engineered by materials growth and fabrication techniques with various degrees of freedom in design, such as in the bandgap, doping, and thickness of the material. These properties have been used to make state-of-the-art high-speed electronic circuits and optical devices suitable for a broad range of applications. AT&T is committed to these techniques of electronics and photonics to maintain its leadership in communications and information technology. In this paper, we review the use of III-V compound semiconductors for ultra-high-speed electronics, in particular the heterostructure field-effect transistor (HFET) and the heterojunction bipolar transistor (HBT), based on gallium arsenide (GaAs) and indium phosphide (InP) technology. We also discuss future trends, including the integration of electronic and optical functions on the same chip.

19

Introduction

III-V compound semiconductors consist of many materials with distinct electronic and optical properties. AT&T has been successful in exploiting the potential of these materials by creating microstructures with precisely engineered properties. This technique of engineering the properties of a material to obtain optimal optical or electronic functions has been called *bandgap engineering* and has progressed from early ideas and concepts in physics to well-defined manufacturing methods and products based on III-V materials.

This paper focuses on the development of III-V heterostructure devices from research through development to application. (See Panel 1 for a list of terms and acronyms used in this paper.) We outline the concept of heterostructures and bandgap engineering for electronic devices and then review the basic technologies that allow us to achieve these structures.

Panel 1. Terms and Acronyms in This Paper

AlGaAs	aluminum gallium arsenide
CAD	computer-aided design
DCFL	direct-coupled FET logic
GaAs	gallium arsenide
HBT	heterojunction bipolar transistor
HFET	heterostructure field-effect transistor
IC	integrated circuit
InGaAs	indium gallium arsenide
InP	indium phosphide
LSI	large-scale integration
MBE	molecular-beam epitaxy
MESFET	metal-semiconductor FET
MIMIC	millimeter-wave and microwave integrated circuit
MOCVD	metal-organic chemical vapor deposition
MOS	metal-oxide semiconductor
MOMBE	metal-organic molecular-beam epitaxy
OEIC	optoelectronic integrated circuit
QWIP	quantum-well infrared photodetector
SARGIC	self-aligned refractory gate IC
SEED	self-electro-optic-effect device
SFFL	source-follower FET logic
Si	silicon
SiO_2	silicon dioxide
SQT	single quantum-well transistor
SRAM	static random-access memory
VLSI	very-large-scale integration

We have chosen two major classes of devices to show how present and potential products are being developed. These are the *heterostructure field-effect transistor* (HFET) and the *heterojunction bipolar transistor* (HBT). The HFET has progressed from demonstrations by AT&T in the late 1970s of the physical principles of mobility enhancement at hetero-interfaces to manufacture at the AT&T Microelectronics facility in Reading, Pennsylvania. The HBT has tremendous speed advantage, but only through recent innovations in

materials and process technology have we begun to glimpse a new era of ultra-high-speed integrated circuits (ICs).

Finally, in this paper, to review future trends in III-V compound devices, we examine the integration of already-mature optical devices onto III-V materials and their potential monolithic integration with electronic functions. The resulting *optoelectronic integrated circuit* (OEIC) could be a significant contribution to both ultra-high-speed electronics and optical devices built on III-V semiconductors.

III-V Compound Semiconductors for Electronics

The carrier transport in III-V compounds is superior to that in silicon because of the electronic structure of the compound semiconductor crystals. This is seen in the higher mobility and saturation velocity in III-V devices. In addition, the direct bandgap of GaAs and other III-V materials makes them suitable for optical devices. Historically, GaAs was used to give FETs better electron transport properties and to provide a semi-insulating substrate that would reduce the detrimental effect on speed due to capacitance associated with a low-resistivity substrate. The overriding rationale for the present generation of FETs is their potential in large-scale integrated circuits operating at very high speeds over a large range of operating temperatures at low voltage with low power dissipation.

Innovations in materials growth technology at AT&T in molecular-beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), and, more recently, in metal-organic molecular-beam epitaxy (MOMBE), have created a class of synthetic materials called *heterostructures*. (See Panel 2.) Heterostructures allow the device designer to confine carriers and to alter their transport properties so that the device characteristics can be tailored to a specific application. This control of the band structure of materials by precise control of the composition, thickness, and doping of the semiconducting layers is known as *bandgap engineering*. Controlling

20

both the electrical and optical properties of a material is a powerful combination.

Field-Effect Transistors

The early work on compound semiconductor transistors started with the GaAs metal-semiconductor FET (MESFET), which has had a significant role in the history of AT&T's telecommunication systems. In 1982, AT&T Microelectronics was one of the largest manufacturers of high-performance MESFETs for terrestrial microwave communications and for the Telstar III satellite system. By 1983, development of GaAs ICs for the FT Series G 1.7-gigabit-per-second (Gb/s) repeaters had begun; and by 1986, AT&T Microelectronics had full-scale production of laser drivers, decision circuits, and preamplifiers. These are all high-performance, small-scale circuits, now available for commercial sale. The experience gained in producing reliable, high-speed components in fully characterized and packaged form can now be applied to the next generation of development.

GaAs MESFETs have been widely used for discrete microwave and millimeter-wave devices. AT&T has received contracts from the government's MIMIC program to develop monolithic circuits for applications at these frequencies. (MIMIC stands for millimeter-wave and microwave integrated circuit.)

Developing the HFET. The heterostructure FET is a class of devices in which the conducting channel of the transistor is confined in a low-bandgap material bounded on one or both sides by a high-bandgap material. Most of these structures have impurity doping only in the high-bandgap material, which results in a large low-field mobility in the device channel because of reduced impurity scattering and in a larger saturation velocity than in conventional homojunction devices. The fundamental physics of the mobility enhancement and two-dimensional nature of a quantum-confined charge layer in modulation-doped structures was studied in the late 1970s at AT&T Bell Laboratories.[1] This discovery led to a

new class of FETs with high charge density, large transconductance, and charge control superior to conventional FETs, especially when devices were scaled to small dimensions to achieve high-frequency performance. HFET technology has challenged epitaxial growth techniques of III-V compounds to produce very uniform layers of known thickness, composition, doping, and heterointerface quality commensurate with the requirements of defect density, yield, and reproducibility for large-scale IC production.[2]

The development of the HFET involved a simple fabrication process, known as recess-gate technology, to yield record-breaking performance on frequency dividers [13 gigahertz (GHz) at 77 kelvin (K)], ring oscillators [10 picoseconds/gate (ps/gate) at 300K and < 6 ps/gate at 77K], and the largest HFET multipliers at the time: 1.6-nanosecond (ns) multiplication on 4-by-4-bit parallel multipliers.[3] This technology was suited to small- and medium-scale integrated circuits, and to very short channel devices for the exploration of fundamental limits. The United States Air Force and Army provided partial funding for the early research and development on HFET and related materials programs.

The fundamental studies on device scaling at short channel lengths have included development of a direct-write electron-beam resist technology for fabricating submicron gates with a high yield. Recent results have also included frequency dividers operating at more than 12 GHz at room temperature, with 0.5-micrometer (μm) gates. In addition, devices with gate lengths as short as 0.2 μm have been fabricated (Figure 1), with cutoff frequency (f_T) approaching 100 GHz. The scaling of devices to short gate lengths results in higher speeds, but also causes degradation of the device characteristics (known as the short-channel effect) because of the very high fields in a submicron device. The short-channel effect is seen as an excessive drain conductance in submicron HFETs. Figure 2 shows the voltage gain (i.e., the ratio of transconductance to drain conductance) as a function of gate length for three device structures:

21

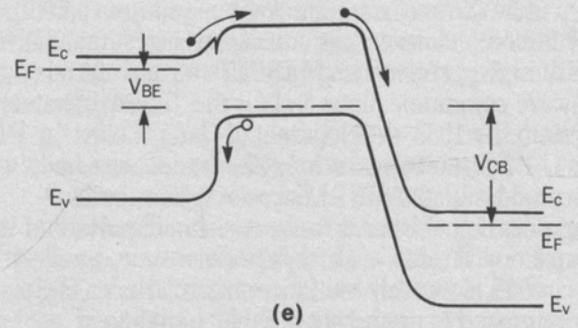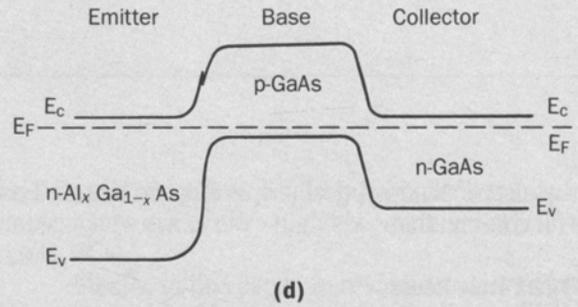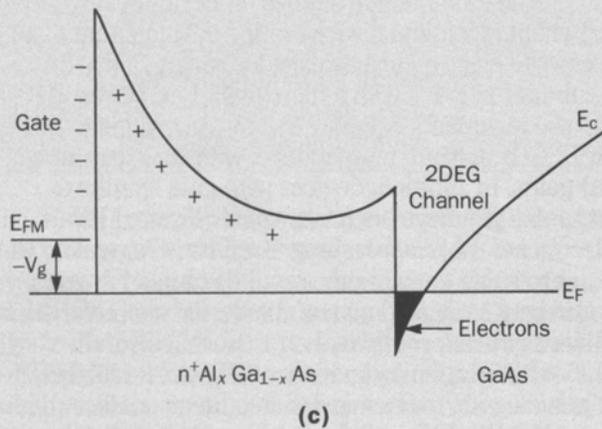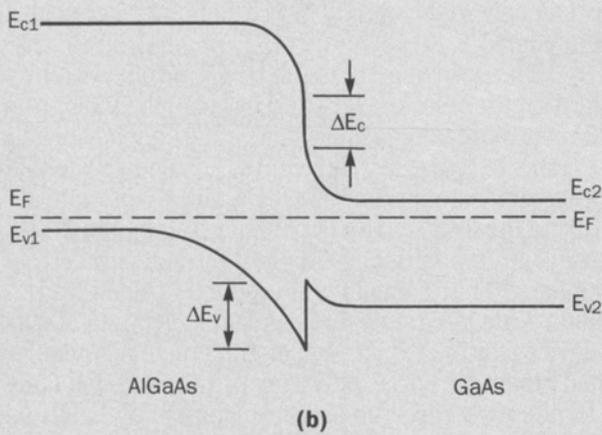## Panel 2. Bandgap Engineering: HFETs and HBTs

E_{c1} ΔE_c E_{c2} E_{F2}

E_{v2} ΔE_v

E_{F1} E_{v1}

AlGaAs GaAs

Interface

(a)

E_{c1} ΔE_c E_{c2} E_F

E_F E_{v1} ΔE_v E_{v2}

AlGaAs GaAs

(b)

Gate

E_{FM} $-V_g$

2DEG Channel E_c

E_F

Electrons

$n^+Al_x Ga_{1-x} As$ GaAs

(c)

Emitter Base Collector

p-GaAs

E_c E_c

E_F E_F

E_{v2}

$n-Al_x Ga_{1-x}$ As n-GaAs E_v

E_v

(d)

E_c E_F V_{BE}

V_{CB}

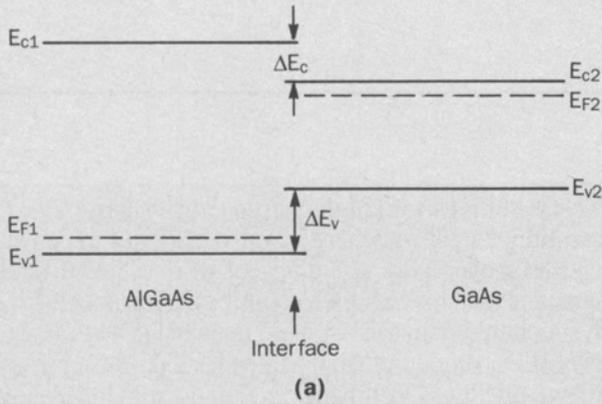E_v E_c E_F

E_v

(e)

Figure (a). Energy band diagram for two different semiconductors, showing the conduction-band ($E_{c1,2}$) and valence-band ($E_{v1,2}$) energies and the size of their discontinuities ($\Delta E_c, \Delta E_v$). $E_{F1,2}$ are the Fermi energies in the semiconductors.

Figure (b). Energy band diagram of the same two semiconductors, when joined at the hetero-interface, in thermal equilibrium.

Figure (c). Energy band diagram of an n^+AlGaAs/GaAs heterostructure FET, indicating the gate and 2-dimensional electron gas (2DEG) channel, with a gate voltage V_g applied.

Figure (d). Energy band diagram of an n-p-n heterojunction bipolar transistor in thermal equilibrium.

Figure (e). Energy band diagram for the same device under active mode of operation.

22

Panel 2 (continued)

The physics of heterojunction structures allows the charge transport within an electronic device to be optimized. Figure (a) shows that, when two semiconductor materials with different bandgaps are joined together to form a heterojunction, discontinuities in both the conduction and valence band edges occur at the hetero-interface [Figure (b)].

For the n-AlGaAs/GaAs heterostructure FET (HFET), the AlGaAs layer is doped with n-type donors. The added charges bend the band edges and create a triangular potential well in the conduction band edge of the lower bandgap material, which, in this case, is GaAs [Figure (c)]. Electrons accumulate in this well and form a sheet of charge analogous to the inversion channel in an SiO_2/Si metal-oxide semiconductor (MOS) structure. The physical separation of the electrons from the donors (impurities) reduces the impurity scattering and, therefore, enhances the mobility of the electrons. This sheet of high-mobility electrons can be used as the active channel of an FET and modulated by the field effect from a gate electrode.

The HBT takes advantage of the other major properties of heterojunctions. Figure (d) shows the band edges of an n-p-n HBT transistor with a wide bandgap emitter. When it is biased [Figure (e)], the heterojunction acts as a barrier to the transport of holes from the base to the emitter. Also, the barrier launches electrons at a high energy from the emitter into the base. This causes the preferential transport of electrons over holes and, thus, a larger current gain in the transistor than in a homojunction bipolar device.

The other major difference between these two classes of heterostructure devices becomes apparent when we compare Figures (c) and (e). In HFETs, the current flows parallel to the surface; in the HBTs, it is perpendicular to the surface. In other words, the critical dimension that determines the intrinsic speed of an HFET is the lateral length of the control gate, which is limited by the capability of the lithography to about 100 nanometers. For an HBT, the intrinsic speed is determined by the vertical thickness of the epitaxy layers, which can be controlled to better than 1 nanometer by MBE, MOMBE, and MOCVD. For further discussion of these epitaxy technologies, see the articles by Panish[4] and by Johnston et al.[5] in this issue of the *AT&T Technical Journal*.

- A single heterojunction FET in AlGaAs/GaAs (aluminum gallium arsenide/gallium arsenide)
- A single quantum-well channel in AlGaAs/GaAs
- An InGaAs-channel (indium gallium arsenide) HFET on GaAs substrates.

These trends show that, as the gate length is reduced, the gain decreases to unusable levels (i.e., < 10). However, because the confinement in the InGaAs-channel device is superior to the conventional AlGaAs/GaAs HFET, this device is more suited to high-speed operation at short gate lengths. This is just one example of the continuing improvements in the engineering of the HFET.

Self-Aligned Refractory Gate IC Technology. Bell Laboratories developed the self-aligned refractory gate IC (SARGIC) technology for GaAs HFETs to respond to the need for a large-scale integration (LSI) manufacturing technology and also as part of a commitment to a long-term strategy for high-performance ICs. AT&T Microelectronics was involved from the inception to ensure the success of this venture.

Because of the need for a high-yield technology, the simpler recess-gate approach was abandoned in favor of the SARGIC technology, which follows the fabrication techniques of silicon very-large-scale integration technology (VLSI). More aggressive design rules and high-yield processing techniques have led to high-performance circuits with high levels of complexity. A logic family, called *source-follower FET logic* (SFFL), was developed to give better current drive, more robust performance, and stability over the military temperature range (i.e., –55°C to +125°C). SFFL provides a realistic manufacturing process compared to the *direct-coupled FET logic* (DCFL), which has lower complexity and higher speed, but makes too stringent a demand on the fabrication technology for sufficient yield.

The 3-inch GaAs wafer fabrication for pilot line production of circuits was created in parallel with the development of this manufacturing technology. In addition, a range of integrated and comprehensive modeling,
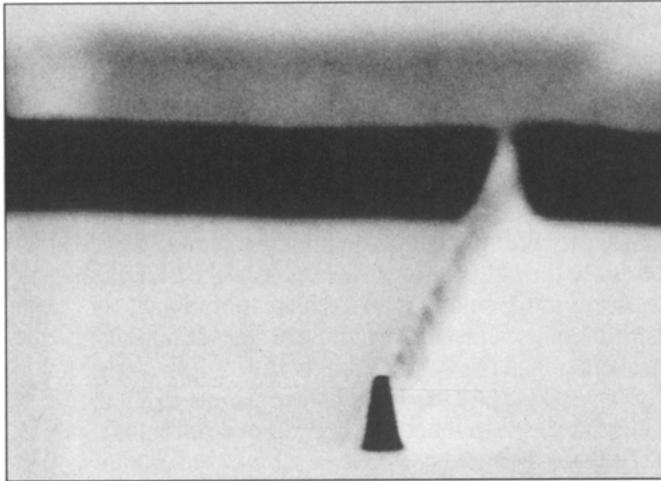
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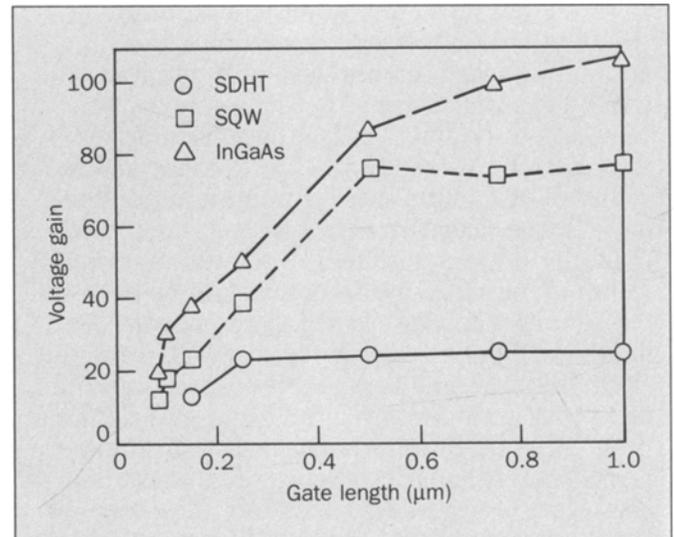**Figure 1.** Scanning electron micrograph of an FET with a gate length of 0.2 μm.

Figure 2. Voltage gain versus gate length for submicron-gate HFETs with three different device layer structures. SDHT = a single heterojunction FET in AlGaAs/GaAs; SQW = a single quantum-well channel in AlGaAs/GaAs; InGaAs = an InGaAs channel HFET on GaAs substrates.

simulation, design, layout, and verification tools was developed. With these, the customer can not only purchase circuits but also have access to the SARGIC HFET technology as a foundry operation; the reliability and packaging and radiation hardness of the parts are part of the technology support as well. The computer-aided design (CAD), like the fabrication technology, follows the silicon approach. Physical device models, parameter extraction from devices, and circuit simulation and layout tools are derived from existing tools for silicon IC design. A standard cell and macrocell approach has been used for maximum flexibility of circuit design.

AT&T received a contract from the Defense Advanced Research Projects Agency for partial funding of the pilot line of heterostructure FET logic circuits with up to 5000 equivalent gates and 4K static random-access memory (SRAM) that would operate at clock frequencies of 200 MHz. Single quantum-well transistors (SQTs) are also being developed that could increase this frequency to 400 MHz. Recently, a 6-by-6-bit parallel multiplier circuit was successfully fabricated using enhancement/depletion mode devices in the SFFL logic family with a

full custom design. (See Figure 3.) The circuit has 3,072 transistors, equivalent to 465 logic gates. Fully functional chips have been fabricated with a multiplication time of 4.5 ns, in which the longest delay path consisted of 32 gates, giving an average gate delay of 141 ps, at a power of 600 milliwatts (mW). This is the first successful prototype in a large range of digital products for small-, medium-, and large-scale integration.

The Future of HFET products. Future applications of HFETs will be in several areas, including their use in large-scale circuits for high-speed signal processing at low cost and power, using either standard cell or custom designs. Fast SRAMs are also being developed with the SARGIC HFET technology, as well as analog ICs and circuits for fiber optic communications. We expect that developments in design rules and submicron device geometries will allow HFET circuits to operate at up to 10
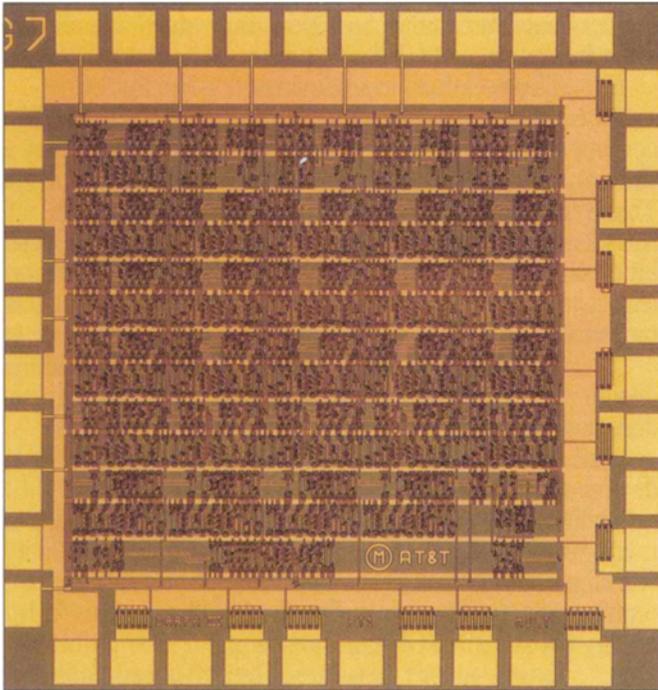
Figure 3. Micrograph of a 6-by-6-bit parallel multiplier circuit fabricated with the SARGIC HFET manufacturing technology.

Figure 4. Eye diagram of a 4.0-Gb/s decision circuit made with AlGaAs/GaAs HBTs.

GHz, for small-to-medium-scale digital ICs. The ultrahigh frequencies and low noise characteristics of HFETs will be exploited for millimeter-wave and microwave monolithic ICs.

Heterojunction Bipolar Transistors

Heterojunction bipolar transistors (HBTs) take advantage of the band structure of different III-V semiconductors to create high-gain devices with numerous applications in high-speed circuits. HBT technology is a major building block for ultra-high-speed digital and lightwave circuits that require high transconductance, high current drive, and uniformity of threshold voltage. To date, discrete HBTs have shown impressive
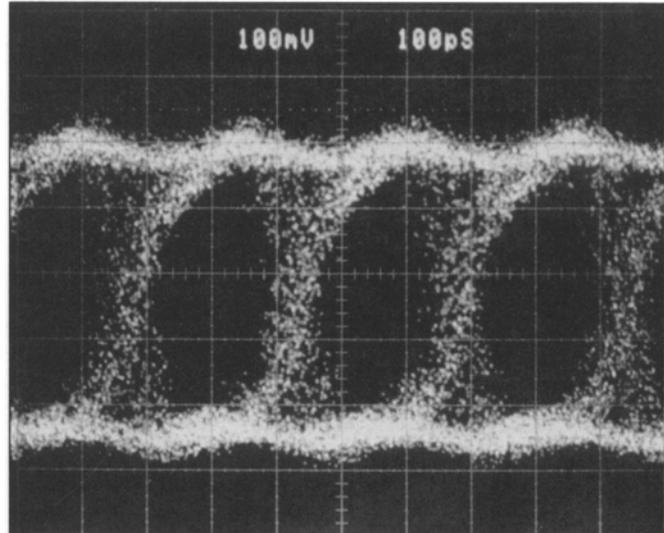
microwave and digital circuit speeds. HBT frequency divider circuits have achieved a toggle frequency above 26 GHz, with device geometries above 1 μm. Advanced FETs have achieved these speeds only by very fine-line lithography of sub-0.2 μm. Bipolar speed is controlled not by the lithographic dimensions of the structures built on the wafer, but by the thickness, doping, and composition of the epitaxial layers that form the heterostructures of the device. HBTs have a more uniform threshold voltage than FETs, which makes them more suitable for precision analog circuits such as analog-to-digital converters. The threshold voltage of the HBT is determined by the bandgaps of the materials; in the FET, it relies on the absolute values of doping and the thickness of the layers.

GaAs/AlGaAs HBT Technology. Bell Laboratories has had a major role in developing an understanding of the GaAs/AlGaAs HBT. A few examples of the company's numerous inventions and demonstrations include the compositional grading of the base in the n-p-n GaAs/
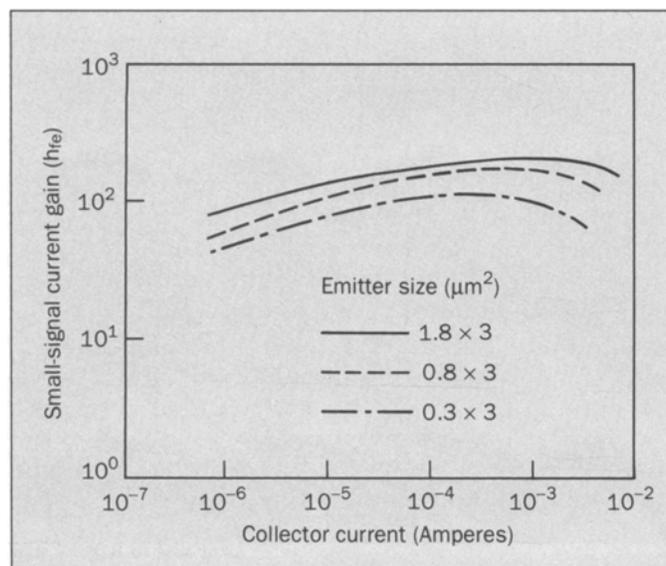
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Figure 5. Small-signal current gain plotted against collector current for different emitter sizes for the InP/InGaAs HBT.

AlGaAs materials system, which improves transport by imposing a quasi-electric field across the base.[6] In addition, planar doping in the base has been used to explore the limits of the base transit time; and carbon doping has been used to maximize the hole concentration in the base. The efficiency of the emitter has been improved by the grading of the emitter-base junction.

Double heterojunction HBTs have been studied to suppress hole injection into the collector when the device is in saturation; this type of double-heterojunction structure has also been used to measure the energy of electrons traveling across a heterojunction—a technique called *hot-electron spectroscopy*.

Bell Laboratories has explored the use of the AlGaAs/GaAs HBT in ultra-high-speed electronic digital and analog test circuits. Ring oscillators have shown propagation delays of 42 ps/gate in nonthreshold logic and 75 ps/gate in current-mode logic. Frequency

dividers have been fabricated to operate at a maximum input frequency of 4 GHz using current-mode logic.

The decision circuit is critical to the lightwave repeater system. It translates an analog signal from an incoming optical fiber into digital 1s or 0s and also retimes the signal to remove phase noise in the datastream. These circuits were designed and implemented in the AlGaAs/GaAs HBTs, and operated up to 4.2 Gb/s, with a bit error rate of 1×10^{-9}. Figure 4 shows an eye diagram, a measure of the fidelity of detection of these signals, measured at 4.0 Gb/s.

These results were achieved with conservative design rules and a non-self-aligned process, as a demonstration of the potential of this technology. The present drive is to minimize the leading parasitics in the device, with emphasis on manufacturability and reliability. A fully self-aligned structure is under development, with a dry-etched emitter, dielectric sidewalls for a self-aligned emitter-base metallization, and nonalloyed ohmic contacts. These improvements will allow this technology to exceed 10-GHz IC operation.

InGaAs/InP HBT Technology. The InP-based HBT has recently shown very high-speed performance on discrete devices. The InP/InGaAs HBT has an InP emitter with an InGaAs base and collector in which all materials are lattice-matched to InP. The first successful scaling of high-gain submicron HBTs was recently achieved with this technology. Common-emitter current gains of 115 and 170 were obtained in transistors with emitter dimensions of 0.3×3 and $0.8 \times 3 \ \mu m^2$, respectively.[7] These results are comparable to scaling experiments reported for silicon bipolar devices. Figure 5 shows the small-signal current gain, h_{fe}, plotted against collector current for a range of device geometries. These results show that the InP/ InGaAs HBT is relatively insensitive to the leading parasitic that limits the GaAs/AlGaAs HBT (namely, the high-surface recombination velocity on GaAs). The reduction in device geometries does not contribute to the speed of these devices, but results in lower power and a smaller area per device. Thus, where large scales of integration

26

and ultrahigh speed are required, these small-geometry InP HBT devices are very attractive.

A record performance for discrete devices with an f_T of 165 GHz and an f_{max} of 100 GHz has been set with a $3 \times 3 \ \mu m^2$ emitter size in the InP/InGaAs HBT. The average electron velocity through this device was close to 4×10^7 centimeters per second (cm/s) through the thin, heavily p-doped base and the collector space charge region. The transit delay in this device was below 1 ps, and an f_T of well over 300 GHz has been predicted for this technology. The exceptional performance in this device comes from several physical properties of the hetero-structures and materials.

The bandgap between InP and InGaAs causes electrons from the emitter to be launched into the base at a high energy. It is also possible to achieve high doping in the InGaAs base, thereby reducing its resistance. Finally, the large separation in the collector between the Γ-valley and L-valley for electrons in InGaAs means that the electrons stay in the Γ-valley, where fast transport exists, rather than being scattered into subbands, where electron transport is poorer.

Applications for the HBT

The GaAs-based and InP-based HBTs are better than FETs for certain applications. In particular, discrete devices for millimeter-wave power applications, broadband amplifiers, and lightwave circuits (e.g., the laser driver and decision circuit) are natural candidates for this technology. As levels of integration improve and integration with optical devices becomes a reality, the HBT holds much promise for the future.

Optoelectronic Integrated Circuits

The fabrication technology of LSI electronics for III-V compounds has been used to make optical devices in the past few years. The potential for monolithic integration of optical and electronic components is being explored. In this issue of the *AT&T Technical Journal*, Dutta cites the integration of lasers with FETs and photodiodes
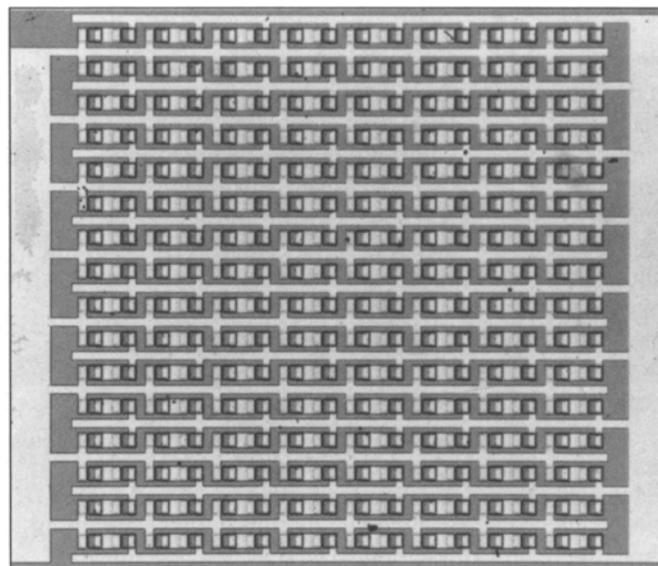

Figure 6. Micrograph of an array of self-electro-optic-effect devices (SEEDs).

27

with FETs as a demonstration of OEICs, to add amplification or gain in a monolithically integrated form.[8] The aim of the OEIC is to add the signal processing capabilities of electronics to optical devices.

The *self-electro-optic-effect device* (SEED) is a multiple quantum-well device that acts as an optical modulator relying on absorption of light by excitons trapped in the quantum wells. It has been used in several materials systems, but most often in GaAs/AlGaAs structures, for demonstrations of optical switching. For practical use, optical switching requires a large and dense array of uniform devices with a high functional yield for switching at rates of terabits per second. Therefore, fabrication techniques that were the domain of III-V electronics have been used to make these arrays. Figure 6 shows a SEED device array. Another device that will require similar arrays is the quantum-well infrared photodetector (QWIP), which senses wavelengths of 10 μm for imaging.

The integration of electronics with optical devices has many potential benefits. The driving of a monolithically integrated optical modulator with high-speed electronics could lead to high-speed optical interconnects between chips, with larger bandwidth than in conventional packaging. In the case of the SEED, the combination of optical and electronic switching elements can be fabricated to create "smart pixels." These would allow very compact logic for optical switching. As we move into these technologies, the role of optical and electronic CAD becomes critical in making reliable products. CAD for electronic devices is at a mature stage; however, it is in its infancy for optical devices.

The development of integrated electronic and optical technologies is the key to a generation of optoelectronic devices in which both the optical and electronic properties are used to their limits. Combining the large bandwidth of optical signals with the ultrafast electronic processing of data is an inevitable evolution that will overcome the limitations of both technologies.

Conclusion

By combining an understanding of III-V compound semiconductor materials with innovations in fabrication technologies, we have succeeded in applying the electronic and optical properties of these materials to integrated devices and circuits. The exploration of these technologies continues to be a critical component of the communications systems of AT&T.

Acknowledgments

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