BULK III-V COMPOUND SEMICONDUCTOR CRYSTAL GROWTH

Jim E Clemans, Theophilus I. Ejim, William A. Gault, and Eric M. Monberg

Within AT&T, III-V compound semiconductor crystals are used for the manufacture of photonic and high-speed integrated circuit devices. But commercial processes have limitations that prevent them from producing crystals of the quality these devices require. Therefore, AT&T has developed the vertical-gradient-freeze (VGF) technique into a process that can produce large, high-quality gallium phosphide (GaP), indium phosphide (InP), and gallium arsenide (GaAs) crystals. In this paper, we first survey the major crystal-growth processes and then present the improved results of VGF growth for InP and GaAs. The VGF-grown material has very low levels of crystalline defects distributed uniformly throughout the crystal. Growth striations are planar and are greatly reduced from those observed in other materials. We attribute the low defect density to reduced temperature gradients during growth.

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Introduction

High-quality, single-crystal substrates of InP and GaAs are important for the advancement of III-V compound-semiconductor electronic and photonic technologies. Progress in cost-effective manufacturing, performance, and complexity of devices is partly related to improvements in the chemical and structural perfection of single crystals. Single-crystal substrates affect the quality of epitaxial layers and diffused or implanted regions in the substrate. Chemical purity determines the electrical properties of substrates, and structural perfection influences device yields, carrier recombination, impurity gettering, and device reliability. This paper discusses the production of state-of-the-art compound semiconductor substrates, with emphasis on structural perfection and chemical homogeneity. (Panel 1 defines terms and acronyms used in this paper.)

The importance of achieving low substrate-dislocation den-

Panel 1. Terms and Acronyms

Ar	argon
As	arsenic
EDGF	electrodynamic-gradient freeze
EL2	a deep level that absorbs infrared light
EPD	etch-pit density
Fe	iron
g	fraction of melt solidified
GaAs	gallium arsenide
GaP	gallium phosphide
Ge	germanium
HB	horizontal Bridgman
InP	indium phosphide
IR	infrared
LEC	liquid-encapsulated Czochralski
MESFET	metal-semiconductor field-effect transistor
n-type	material with $N_D - N_A > 0$
N_A	concentration of ionized acceptors
N_D	concentration of ionized donors
P	phosphorus
p-type	material with $N_A - N_D > 0$
PBN	pyrolytic boron nitride
S	sulfur
Si	silicon
T_m	melting temperature
VGF	vertical-gradient freeze
Zn	zinc

sities varies with the design and cost objective of each device type. For minority-carrier photonic devices such as lasers, light-emitting diodes (LEDs), and avalanche photodetectors (APDs), there is a body of evidence that dislocations adversely affect their performance. Nonradiative recombination at dislocations reduces quantum efficiency, and dark-line defects that limit lifetime have also been traced back to dislocations. For majority-carrier devices, the field currently lacks consensus that low-dislocation substrates are needed to meet today's device performance and yield objectives. But defect-free substrates will be required as the III-V electronics technology advances to larger scales of integration and feature sizes are reduced.

Common Production Processes. The most common process for large-scale production of round InP and semi-insulating GaAs single crystals has been liquid-encapsulated Czochralski (LEC), while the horizontal Bridgman (HB) process is used for silicon-doped, n-type GaAs. The LEC process, with a molten boric oxide encapsulant, readily accommodates the high phosphorus (P) vapor pressure associated with InP. The reduction of silicon (Si) dopant levels, necessary for growing undoped semi-insulating GaAs, is readily achieved via LEC using pyrolytic boron nitride (PBN) crucibles. Even though the HB quartz ampoule is fragile and the cross section of the crystal is D shaped, HB is a commercially feasible process because of its relatively simple and inexpensive processing equipment.

One of the most serious drawbacks with the LEC process is the large axial-temperature gradient needed to maintain diameter control. The resulting thermoelastic stresses in the crystal have been shown[1] to exceed the low yield strength of these compound semiconductors and create a high level of dislocations. Typical dislocation densities for undoped InP and GaAs range from $10^4/cm^2$ (per square centimeter) to $10^5/cm^2$. Significant worldwide effort has been focused on this problem, but all partial solutions involve either a significant increase in equipment complexity or the addition of various dopants that also alter the crystal's chemical properties. If we use elements—such as sulfur (S), zinc (Zn), and germanium (Ge)—to dope at the low to mid-$10^{18}/cm^3$ (per cubic centimeter) level, the high dislocation densities typical of LEC growth can be mitigated by a "lattice hardening" mechanism.[2] Although this technique has been extensively used to reduce dislocation levels in LEC-grown crystals, the penalties are higher levels of unrelieved strain and increased optical absorption.

A second drawback of the LEC process is that the melt is coolest at the top surface. This leads to consid-

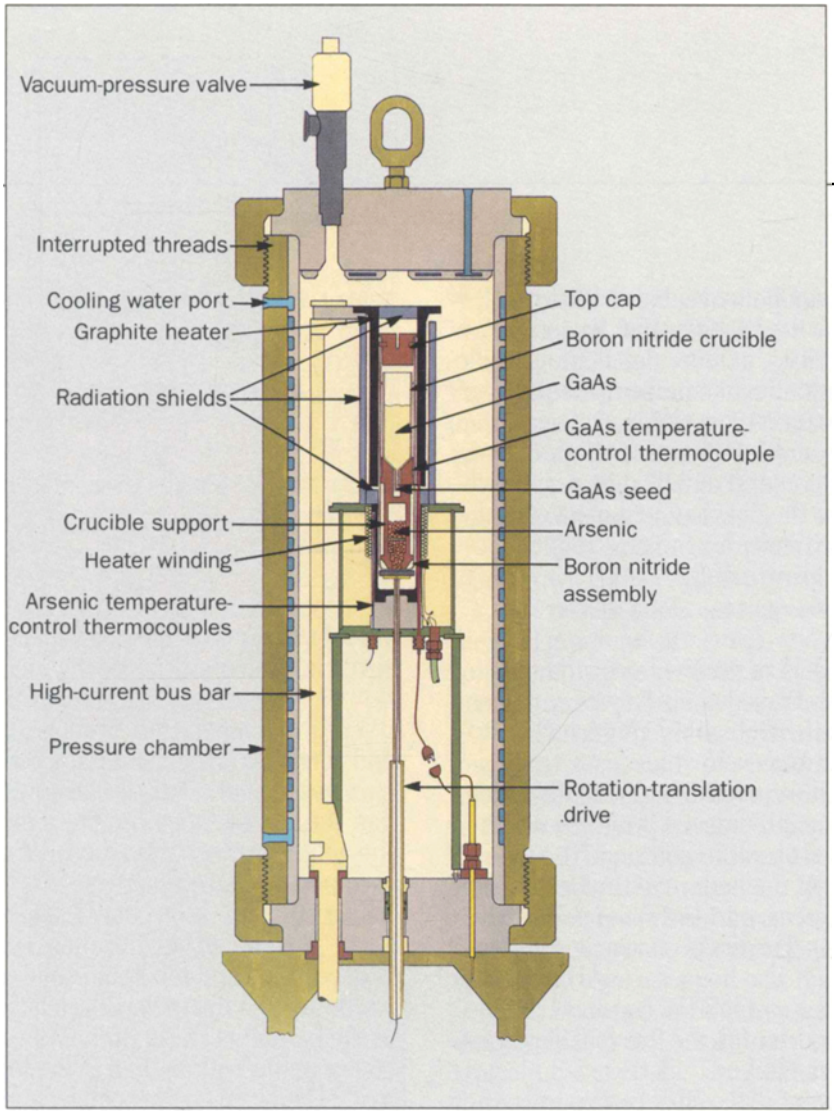

Figure 1. Cross-sectional view of vertical-gradient-freeze (VGF) crystal-growth equipment for gallium arsenide (GaAs).

erable buoyancy-driven convection that creates nonhomogeneities in the crystal dopant and incorporates point defects. Such convection can be diminished if a large magnetic field is applied to the melt, but only at the expense of considerable increase in complexity.

A New Process. The drawbacks of the LEC growth of GaAs and InP have been overcome with a variation of the vertical-gradient-freeze technique (Figure 1) developed at the AT&T Engineering Research Center in Princeton, New Jersey. With the VGF technique, growth in low axial- and radial-temperature gradients is combined with the diameter control imposed by a crucible. The VGF technique uses a monotonically increasing temperature gradient to keep the hottest melt at the top and, therefore, suppress buoyancy-driven convection.

As reported earlier in this journal[3] and elsewhere,[4] AT&T had developed a process—named the Gault process—that has produced state-of-the-art substrates of GaP, GaAs, and InP. Indeed, this production process is being used for InP and GaAs at the AT&T Microelectronics Reading Works in Reading, Pennsylvania. Crystals are routinely produced that have defect levels one to two orders of magnitude lower than comparable LEC crystals. The VGF crystals have been

shown to have a more homogeneous distribution of dopants and point defects than seen in LEC material.[3,4]

This paper describes, in more detail, the specific growth and characterization results for semi-insulating, undoped GaAs as well as for n-type, p-type, and semi-insulating InP. The GaAs and InP processes have been scaled-up to 75 mm (millimeters) and 63 mm, respectively. In addition, we discuss the development of a vertical, multizone, high-pressure heater for the electrodynamic-gradient-freeze (EDGF) growth of InP.

The VGF-GaAs Process

The major elements of the VGF growth hardware are a microprocessor-based control system, power supplies, and a large pressure chamber (Figure 1) that contains the heater assembly.

The heater and the surrounding insulation are designed to produce a smooth thermal profile in which the temperature increases from the bottom to the top of the crystal-growth zone. At the bottom of the heater package, a small, separate heater controls the temperature of the arsenic (As) reservoir. The GaAs charge is contained in the PBN crucible, which also houses a seed crystal at the bottom. The growth assembly's top cap and crucible-support elements are important to the thermal engineering of the temperature gradient.

At the melting point of the III-V compounds, the equilibrium vapor pressures of the group V elements are high and decomposition can occur (Table I). In the process for VGF-grown GaAs, the pressure chamber is filled with argon (Ar) to facilitate composition control. We prevent decomposition and adjust the melt's arsenic concentration by controlling the temperature of a solid arsenic charge at the coldest point in the growth vessel (Figure 2).

To balance the pressure between the hot growth vessel and the cold-wall pressure chamber, a limited exchange of arsenic vapor and argon is allowed through a channel in the top cap. The loss rate of arsenic is slow compared to the time required to grow a crystal.

Table I. Physical Properties of Semiconductors

Property	Compound	
	GaAs	InP
Melting point (°C)	1238	1062
Vapor pressure (atmospheres)	0.9	25
Thermal conductivity at T_m (W/cm °C)	0.07	0.09

As losses occur, arsenic from the bottom of the growth vessel sublimes to maintain the appropriate partial pressure and stoichiometry of the melt.

Growth Process. The growth sequence consists of a series of temperature "ramps" that are measured by, and controlled from, a microprocessor. After the pressure vessel fills to the desired pressure of inert argon gas, the arsenic heater temperature is raised to increase the arsenic vapor inside the PBN growth vessel. When the operating arsenic pressure is established, the polycrystalline GaAs charge is melted.

To begin solidification, the control temperature is decreased, and the liquid-solid interface sweeps upward through the melt. Crystallization starts at the seed in the bottom of the crucible. Because the crucible is cooler at the bottom than at the top, the system is thermally stabilized against convection. Temperature stability is critical to control the liquid-solid interface. During VGF growth, the temperature deviates less than 0.05°C from the desired set-point temperature. The thermal and mechanical stability achieved with the process suppresses striae in VGF crystals.

After solidification, controlled cooling brings the crystal to room temperature at a rate that minimizes thermal stress and optimizes point-defect quenching. When cooled, the GaAs contracts about 1 percent, which is greater than the contraction of the PBN crucible. The small gap formed between the crystal and the crucible wall permits easy removal of the crystal.

Because of these engineering and process-

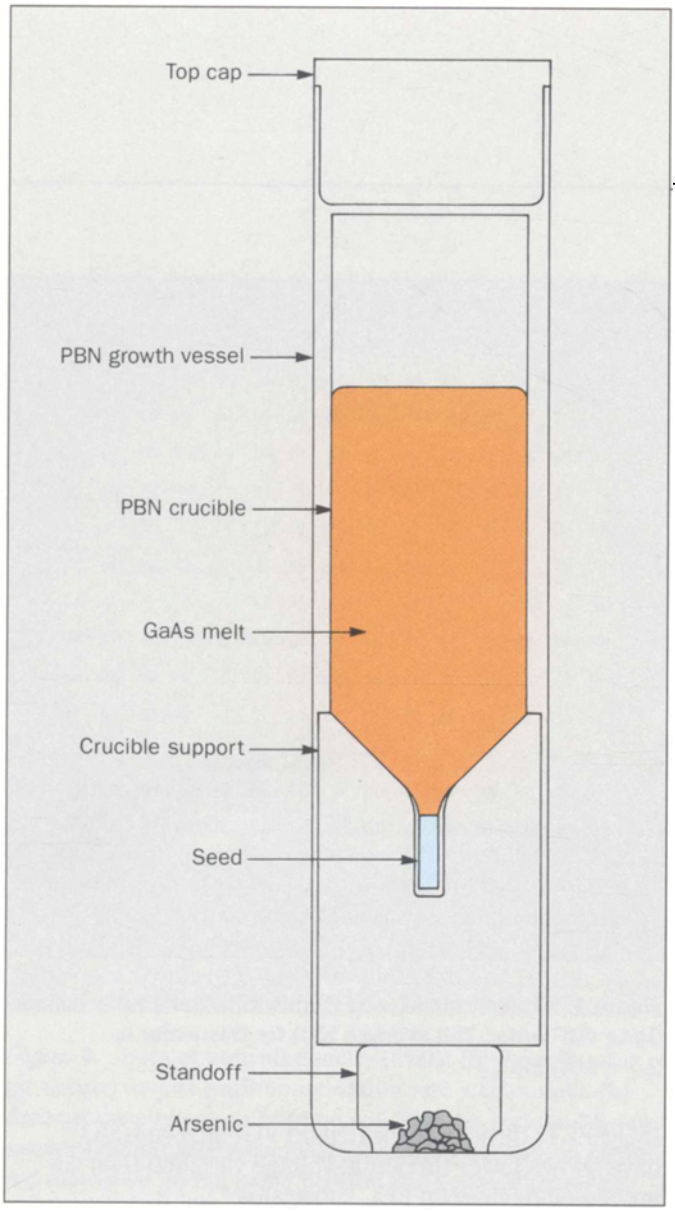

Figure 2. Detailed cross section of the growth-vessel assembly. PBN is pyrolytic boron nitride.

control designs, the VGF system has axial-thermal symmetry, low axial- and radial-temperature gradients, and slow stable solidification and cooling. These conditions have proven important in producing:

- Low levels of thermal stress, which result in low dislocation densities in the crystal
- Thermally stable growth that eliminates growth striae
- High radial uniformity of the electrical properties across wafers.

Figure 3 shows a 75-mm diameter, 3-kg (kilograms) undoped, GaAs single crystal grown on the <100> axis orientation.[5]

VGF-GaAs Characterization

This section describes the characteristics of the VGF-grown GaAs crystals.

Thermal Stress and Dislocations. In the VGF system, thermal gradients are small, and associated stresses are considerably smaller than in LEC-grown crystals. Figure 4 shows a dislocation-count distribution for a typical VGF wafer. Although the VGF dislocation levels are very low, a statistical study of several wafers shows that a significant difference exists between the dislocation levels near the edge of the wafer in the <100> and <110> axis directions (Figure 5a). This difference corresponds to the four-fold pattern expected for stress-induced dislocations, which confirms that some fraction of the dislocations in the current 75-mm crystals are caused by thermal stress.

Undoped VGF crystals have an average etch-pit density (EPD) of $2.5 \times 10^3/cm^2$ compared to $10^5/cm^2$ for typical LEC crystals. The EPD average is an average over the entire wafer surface with measurements taken on a 5-mm grid. The data in Figure 5b show that the EPD density is uniform throughout the length of an ingot. The lowest EPD (the squares in Figure 5b) occurred for a crystal that had the slowest growth and cooling rates. This indicates that the process parameters can directly influence the EPD.

Electrical Tests and Uniformity. Hall-test results for 75-mm material show mobilities typically near 7×10^3 $cm^2/V\text{-}s$ (square centimeters per volt per second). Samples that had carbon concentrations between $2 \times 10^{15}/cm^3$ and $2 \times 10^{14}/cm^3$ had resistivities between 2 and 7×10^7 Ω-cm (ohm-centimeter). Standard deviations of these electrical properties across the <110> axis diameter

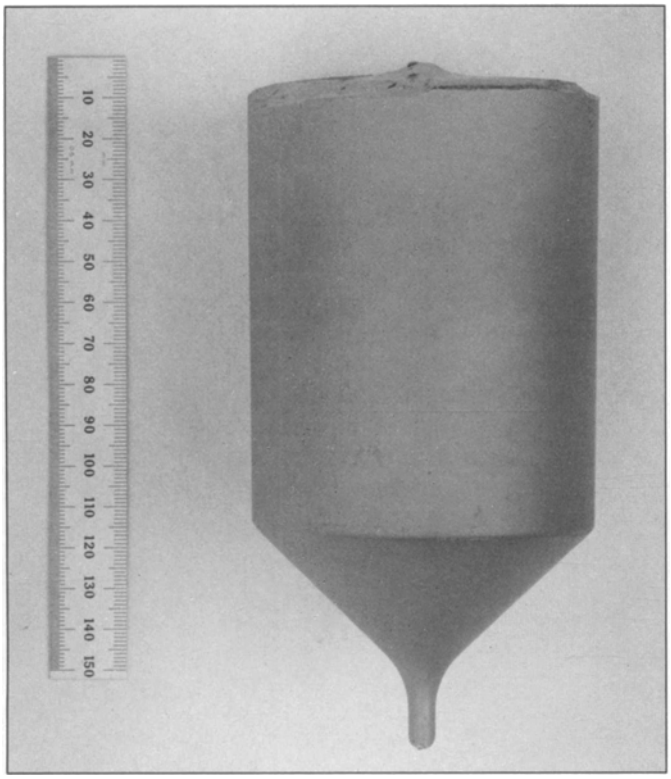

Figure 3. A 75-mm diameter, 3-kg, GaAs single crystal.

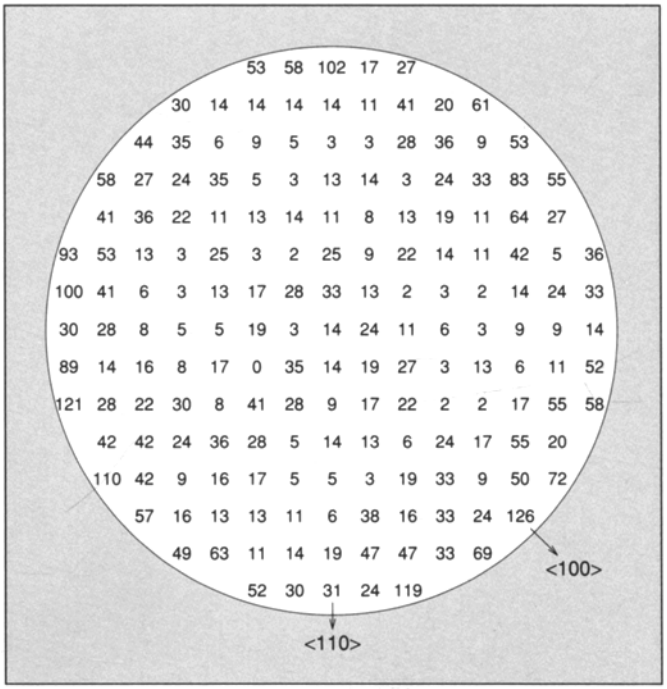

Figure 4. Etch-pit count map (times 100/cm^2) for a typical GaAs VGF wafer. The average EPD for this wafer is 2.7×10^3/cm^2.

are 14 percent for resistivity and 9 percent for mobility. Figure 6 gives plots of typical values for VGF crystals.

The semi-insulating nature of undoped GaAs depends on the uniformity of a deep level that is intrinsic to melt-grown GaAs. This level, which is called EL2, absorbs infrared (IR) light. Figure 7 is an IR map of a typical EL2 distribution in a VGF wafer. The level of EL2 in as-grown 75-mm crystals was 0.7 to 1.2×10^{16}/cm^3. The typical variation of EL2 on an as-grown VGF wafer is ±25 percent. Variations in EL2 concentrations between seed and tail have not been observed in VGF crystals.

GaAs metal-semiconductor field-effect transistor (MESFET) devices fabricated on VGF-grown GaAs have shown lower threshold-voltage variation than co-processed devices on LEC substrates.[6]

The VGF-InP Process

As Table I shows, there are several important differences between InP and GaAs that influence the design of the VGF-process conditions:

- The melting point of InP is significantly lower, while the thermal conductivity is somewhat higher than GaAs. As a result, the heat flow patterns will be different. Therefore, the heater's thermal geometry must be specifically tailored for each material to achieve the

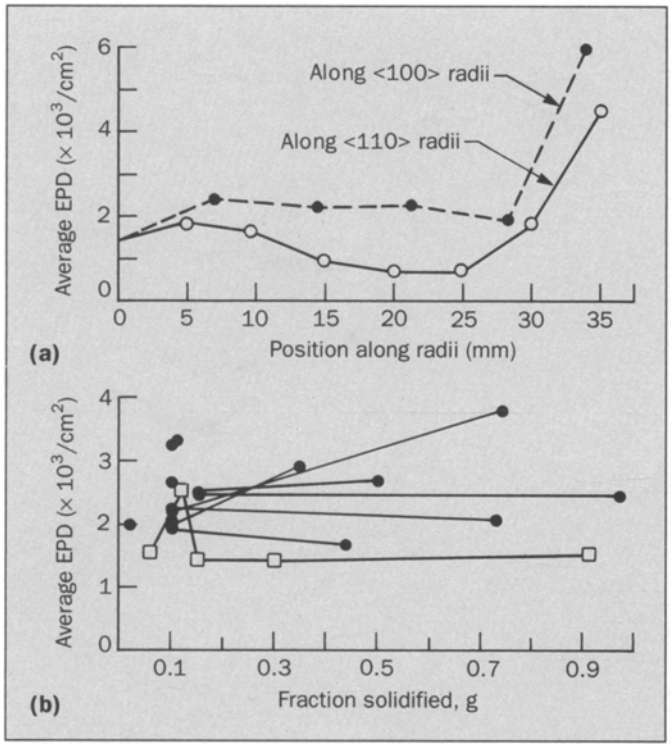

Figure 5. Plots of etch-pit density (EPD). (a) Average etch pit density versus position on <100> and <110> radii. (b) Etch-pit density versus fraction solidified for sixteen 75-mm semi-insulating VGF-grown GaAs crystals. Connected points are measured on the same crystal. The squares represent the lowest EPD; this crystal had the slowest growth and cooling rates.

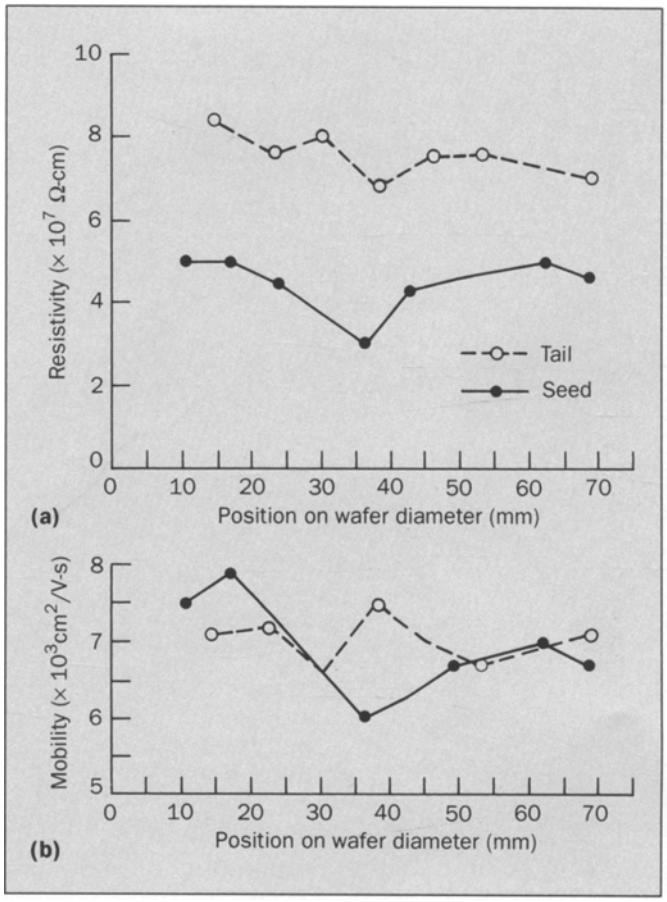

Figure 6. Resistivity and mobility of seed and tail wafers.

desired planar isotherms.

- The equilibrium vapor pressure of phosphorus at the melting point of InP is much higher than that of arsenic over GaAs. Besides the engineering requirements to contain this pressure, we must also consider the increased convection of the argon gas that occurs and a higher level of temperature instability.
- Because of the higher degree of ionicity in InP and a resulting lower stacking-fault energy,[7] we see a significantly higher incidence of twin formation in InP growth than in GaAs growth. The twins are incompatible with subsequent epitaxial processes and must be eliminated. For InP crystal growth, it is critical that we reduce destabilizing conditions that would promote twinning.

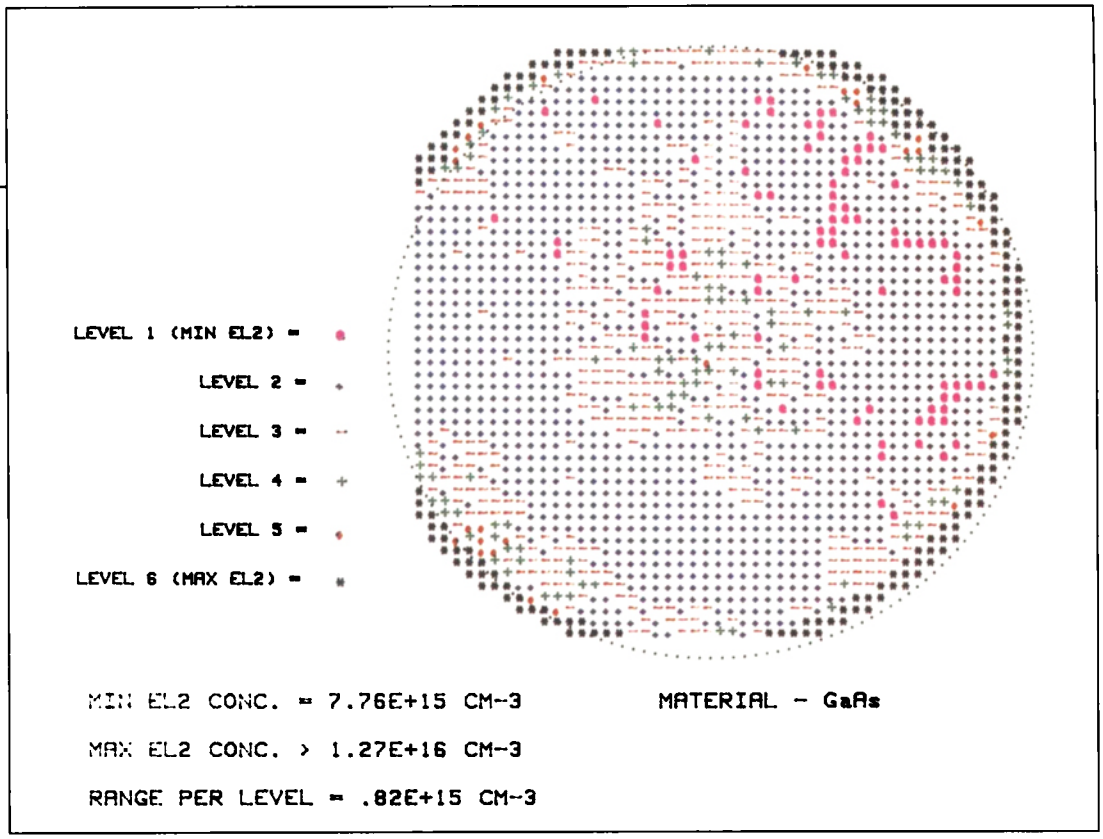

Figure 7. EL2 variations for VGF-grown GaAs. EL2 levels do not depend on melt-arsenic concentration or position in the ingot.

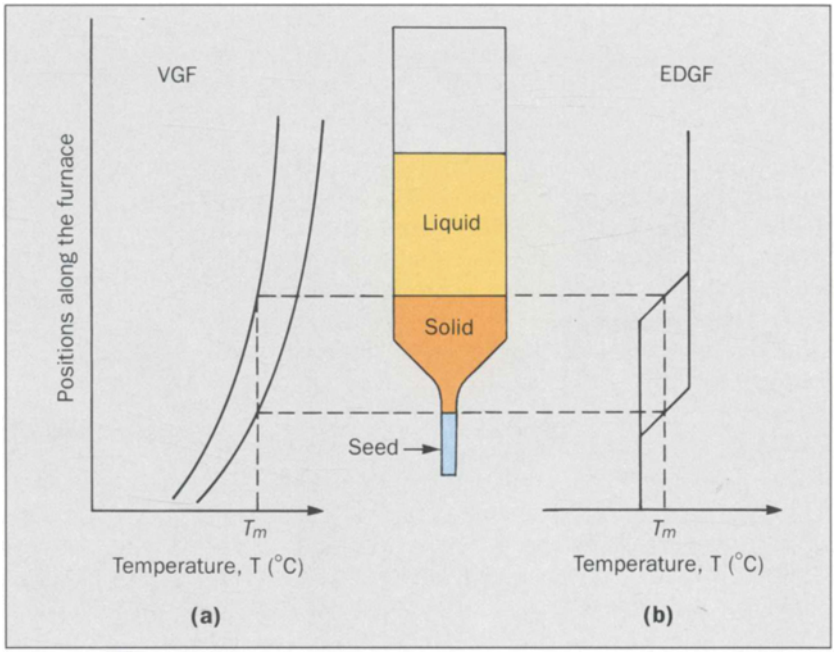

Figure 8. Comparison of VGF and EDGF techniques; T_m is the melting temperature. (a) In the VGF technique, a single-heater zone impresses a monotonically increasing temperature gradient over the melt. Power to this single zone is reduced, resulting in upward movement of the solidification front. (b) In the EDGF technique, several independently controlled heating zones are programmed to give a desired temperature profile. A small gradient segment is then passed from one zone to the next through the otherwise isothermal melt.

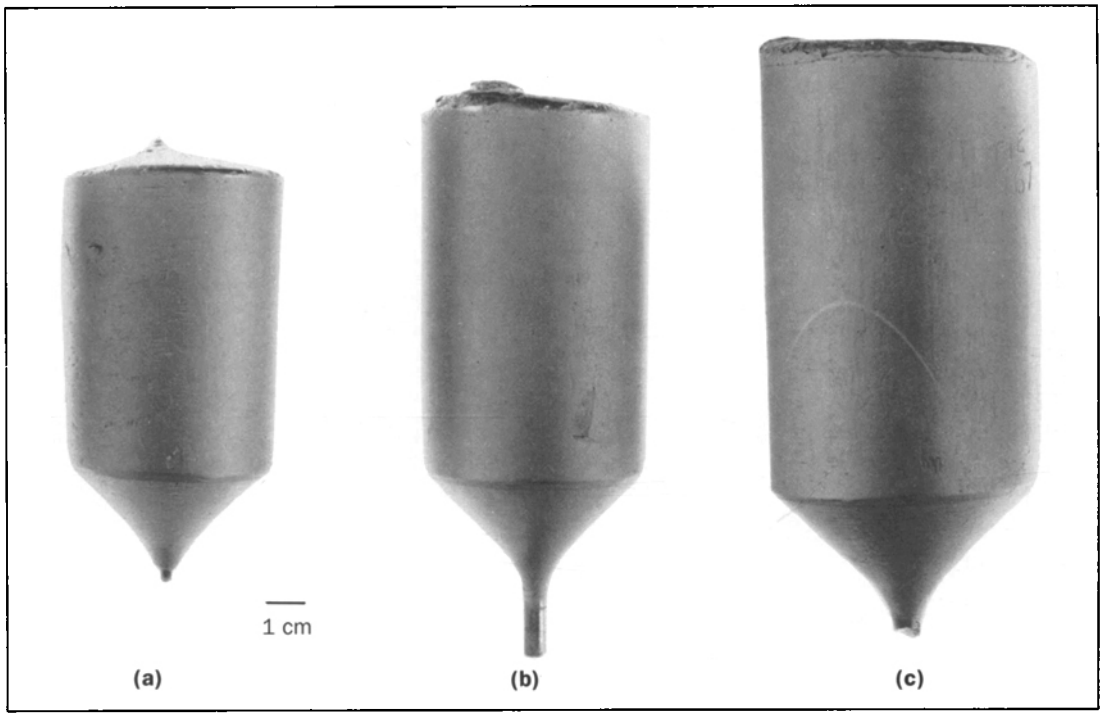

Figure 9. This series of <111> axis, seeded, single crystals shows the progress achieved in scaling up the VGF process for InP: (a) The first VGF-grown InP crystal, 50-mm diameter, 0.75 kg; (b) a 50-mm diameter, 1-kg crystal; (c) current capability is a 63-mm diameter, 1.7-kg crystal. In all cases, the last-to-freeze portion remains single-crystalline, with no second-phase inclusions.

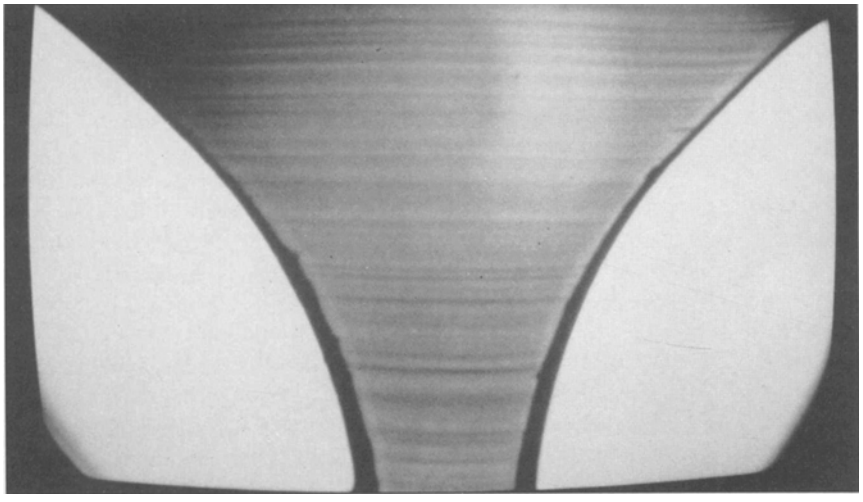

Figure 10. Infrared transmission striagraph of the seed end of a VGF-grown, sulfur-doped InP crystal. The striations result from differential dopant incorporation during VGF growth.

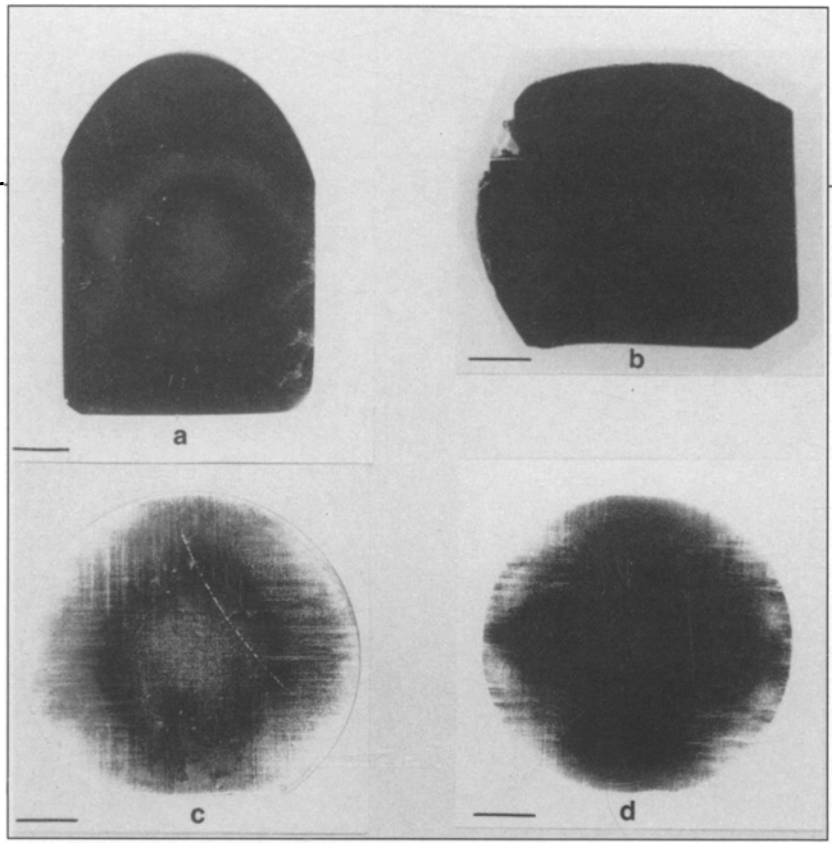

Figure 11. Four <100> axis, sulfur-doped InP wafers after polishing and a defect-revealing etch. Wafers a and b are VGF-grown material with carrier concentrations of $2 \times 10^{18}/cm^3$ and $3 \times 10^{17}/cm^3$, respectively. Wafers c and d are LEC-grown material with carrier concentrations of $3 \times 10^{18}/cm^3$ and $5 \times 10^{18}/cm^3$, respectively.

In addition to the equipment described above that is used for the VGF growth of GaAs and InP, we have developed a high-pressure, multizone, vertical electrodynamic-gradient-freeze apparatus for InP.[8] Figure 8 is a schematic of the thermal profile used in the VGF and EDGF techniques. Both techniques employ very low thermal gradients.

In the VGF technique, a single heater zone impresses a monotonically increasing temperature over the charge material; for crystal growth, we gradually reduce power to the heater. In the EDGF technique, several independently controlled heating zones are programmed to impress a temperature profile over the charge material. A small gradient-segment is then passed from one zone to the next through the otherwise nearly isothermal melt. Although the EDGF technique has been used as a research tool to complement the VGF process, the EDGF technique also grows 50-mm diameter, high-quality, InP crystals.[8,9]

Initial VGF-InP development work occurred for S-doped crystals at the 0.75-kg, 50-mm diameter size. Since implementation of the first VGF manufacturing process at AT&T's Reading Works, the size of the S-doped crystals (Figure 9) has been steadily increased. Figure 9c shows the current crystal size of 1.7 kg and 63-mm diameter. This scale-up has been successful because of enhanced control of the melt composition and growth rate.

VGF-InP Characterization

This section describes the characteristics of the VGF-grown InP crystals.

Sulfur-Doped Indium Phosphide. Figure 10 shows the growth striations at the seed end of a sulfur-doped VGF-InP crystal. These striations map the shape of the liquid-solid interface as growth progresses. The growth isotherms are nearly planar.

Within AT&T, the most important application for InP continues to be n-type, sulfur-doped substrates for photonic applications. Substrate requirements for specific devices generally include: uniformly low dislocation levels, absence of crystallographic slip, low free-carrier absorption, low level of grown-in strain, and homogeneity

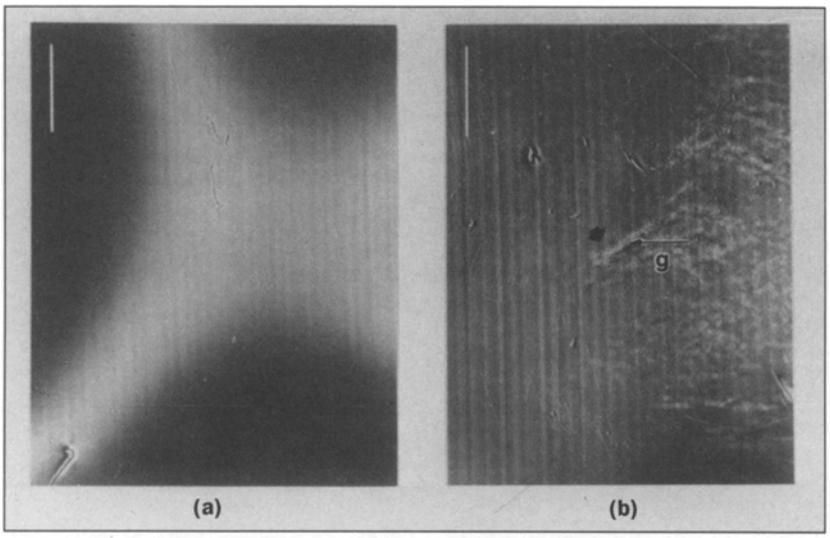

Figure 12. Transmission X-ray topographs of (a) VGF- and (b) LEC-grown sulfur-doped InP. Dislocation tangles in the LEC material are indicated by the arrow. The marker (in the upper left of each topograph) represents 2 mm.

of dopant incorporation.

VGF crystals exhibit low absorption coefficients and low dislocation levels without having to use high doping levels and lattice hardening. Figure 11 shows four <100> axis, VGF- and LEC-grown sulfur-doped InP (S:InP) wafers that have been polished and subjected to a defect-revealing etch. The crystals were grown with doping levels both above and below the threshold for lattice hardening. The LEC wafer with lower doping (Figure 11c) has extensive slip and high levels of dislocation. Even the highly doped LEC wafer (Figure 11d) has extensive peripheral defect levels that must be trimmed. In comparison, the VGF material (Figures 11a and 11b) shows very low defect levels and no slip at either level of doping. This low defect level and absence of slip has been maintained as the crystal sizes increased from 50 mm to 63 mm in diameter. In both crystal sizes, the average dislocation density is less than $10^3/cm^2$, more than an order of magnitude less than comparable LEC material.

Figure 12 displays transmission X-ray topographs of an LEC-grown and a VGF-grown sulfur-doped InP wafer and shows dislocation tangles inside the bulk LEC wafer. The highly concave dopant striations are also visible for LEC material (Figure 12b). As we can see, the VGF material (Figure 12a) is free of dislocations, and the weaker striations are nearly planar.

Semi-Insulating Indium Phosphide. The most common way to make semi-insulating InP is to use an iron (Fe) dopant. Iron acts as a deep acceptor to compensate (counter balance) the residual donors that are always present in "undoped" InP. The iron acts as a deep trap for the residual electrons, thus increasing the resistivity of the material to the level of 10^7 Ω-cm.

Figure 13 plots the dependence of substrate resistivity for three different iron concentrations in InP, as a function of the fraction of the charge that has solidified. The addition of more than 0.03-wt-% (weight percent) iron is necessary to obtain high resistivity (greater than 10^7 Ω-cm from seed to tail). Because the solubility of iron in the InP matrix is relatively low, lattice hardening is not a factor. Consequently, LEC-grown iron-doped InP has been characterized by defect densities that range from $10^4/cm^2$ to $10^5/cm^2$.

LEC- and EDGF-grown <100> axis wafers have

been polished and etched to reveal defects (Figure 14). Both VGF and EDGF have consistently grown crystals with an EPD of less than $2 \times 10^3/cm^2$ from the seed end to the tail end. This is considerably lower than the LEC results.

Zinc-Doped Indium Phosphide. High-quality, p-type substrates have been used to make high-power heterostructure injection lasers and radiation-resistant photovoltaic cells. Zinc is the most commonly used dopant to produce p-type InP crystals. At Zn concentrations above $1 \times 10^{18}/cm^3$, dislocations are reduced through lattice hardening. But anomalous dopant-diffusion behavior, increased twinning during growth, and high free-carrier absorption have all been observed with heavily doped,

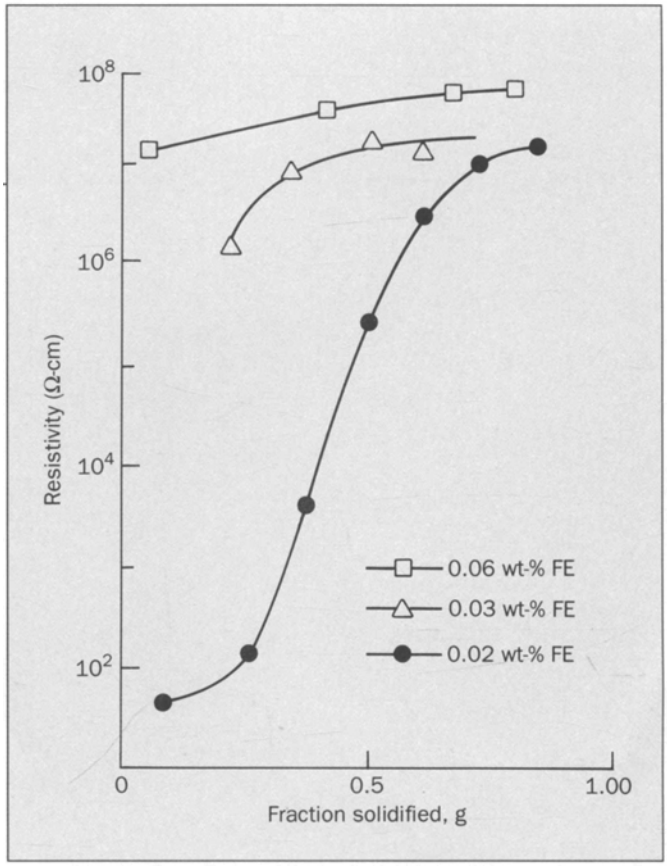

Figure 13. Room-temperature Hall measurements of bulk resistivity as a function of mass fraction solidified for three InP single crystals with 0.02, 0.03, and 0.06 wt-% Fe, respectively.

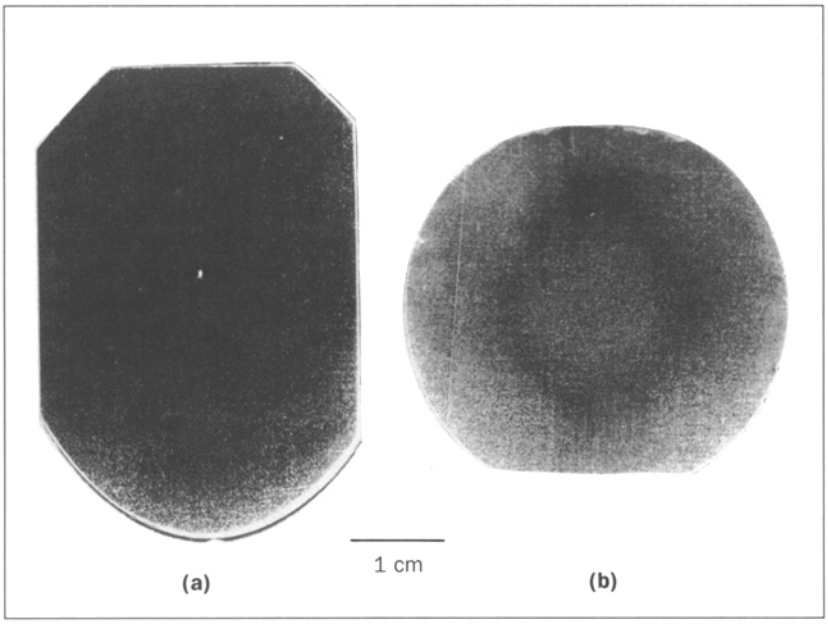

Figure 14. Iron-doped, semi-insulating InP, <100> axis wafers grown by the (a) EDGF and (b) LEC techniques. The EDGF wafer has defect levels below $10^3/cm^2$, except for the tail end where the onset of FeP_2 precipitates raise the defect level. The defect level in the LEC wafer ranges from $10^4/cm^2$ to $10^5/cm^2$.

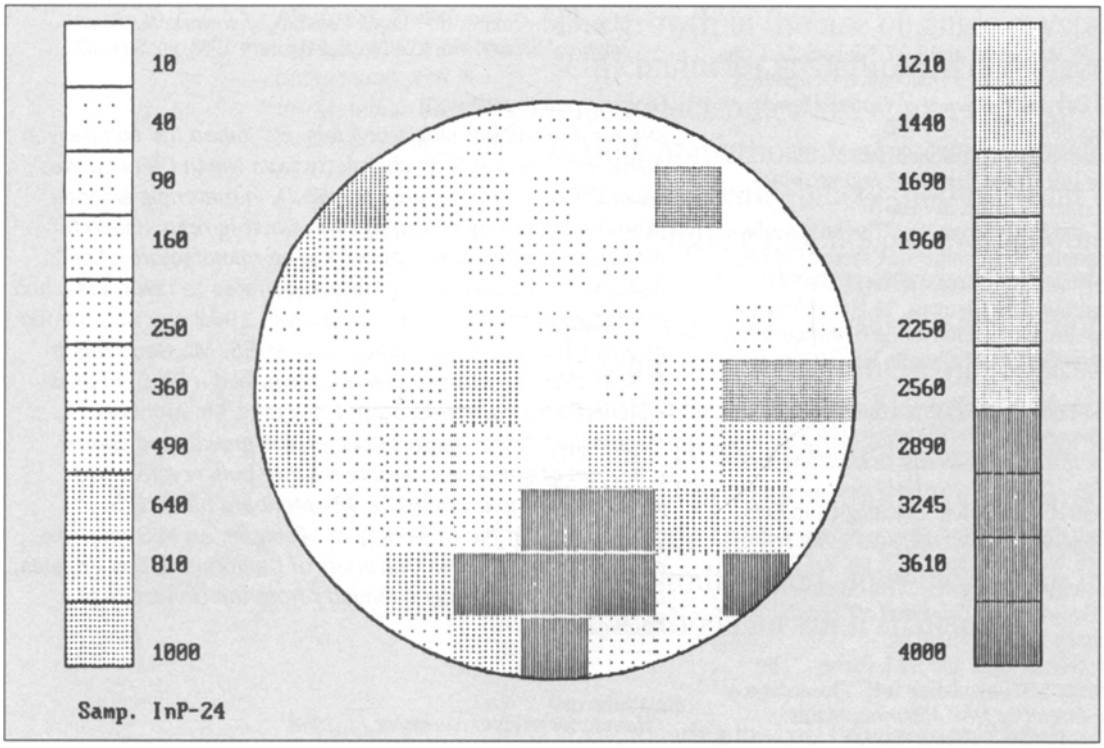

Figure 15. Dislocation map for a 50-mm diameter, <111> axis, Zn:InP single-crystal wafer with a net free-carrier concentration ($N_D - N_A$) equal to $5 \times 10^{17}/cm^3$. The EPD counts were taken at the nodes of a 5-mm grid. More than 60 percent of the area has an EPD of less than $10^3/cm^2$.

LEC-grown zinc-doped InP (Zn:InP).

Figure 15 shows an EPD map of a high-quality, EDGF-grown, 50-mm diameter, <111> axis, round wafer. Defect levels were measured at the nodes of a 5-mm square grid. More than 60 percent of the wafer has an EPD of less than $10^3/cm^2$, and the average defect density ranges from $8 \times 10^2/cm^2$ to $12 \times 10^2/cm^2$ for Zn-doping levels between 1 to $5 \times 10^{17}/cm^3$. This is an order of magnitude lower than comparable LEC-grown material.

Summary

To improve the quality of bulk III-V substrates, a team of engineers and scientists at AT&T has developed a vertical-gradient-freeze process. The VGF process is being used at AT&T's Reading Works to manufacture high-quality GaAs and InP crystals. The major quality features of VGF crystals relate to very low crystalline-defect levels and very uniform properties within a crystal. Yields compare favorably with other commercial crystal-growth processes.

Acknowledgments

The authors acknowledge the assistance of the following people in growing crystals: H. Brown, J. Conway, F. Dominguez, A. Gajewski, A. Merwin, J. Samppala, F. Simchock, P. Smith, S. Trapani, N. Tzafaras, G. Whicker, and R. Wistrom. The following people performed the characterization measurements: A. Akselrad, P. Bridenbaugh, S. N. G. Chu, M. Gray, L. Seibles, J. Spadafora, and H. Temkin.

References

1. A. S. Jordan, R. Caruso, A. R. VonNeida, and J. W. Nielsen, "A Comparative Study of Thermal Stress-Induced Dislocation Generation in Pulled GaAs, InP and Si Crystals," *Journal of Applied Physics*, Vol. 52, No. 5, May 1981, pp. 3331-3336.
2. Y. Seki, J. Matsui, and H. Watanabe, "Impurity Effect on the Growth of Dislocation-Free InP Single Crystals," *Journal of Applied Physics*, Vol. 47, No. 7, July 1976, pp. 3374-3376.
3. J. E. Clemans, W. A. Gault, and E. M. Monberg, "The Production of High Quality, III-V Compound Semiconductor Crystals," *AT&T Technical Journal*, Vol. 65, No. 4, July/August 1986, pp. 86-98.
4. W. A. Gault, E. M. Monberg, and J. E. Clemans, "A Novel Application of the Vertical Gradient Freeze Method to the Growth of High Quality III-V Crystals," *Journal of Crystal Growth*, Vol. 74, No. 3, April 1986, pp. 491-506.
5. J. E. Clemans and J. H. Conway, "The VGF Growth of GaAs," *Proceedings of the 5th Conference on Semi-Insulating III-V Materials*, Malmo, Sweden, Institute of Physics, Bristol, England, 1988.
6. H. Gottschalk, G. Patzer, and H. Alexander, "Stacking Fault Energy and Ionicity of Cubic III-V Compounds," *Physica Status Solidi (a) Applied Research*, Vol. 45, No. 1, January 1978, pp. 207-217.
7. E. M. Monberg, H. Brown, and C. E. Bonner, "The Electrodynamic Gradient Freeze Growth of InP," *Journal of Crystal Growth*, Vol. 94, No. 1, January 1989, pp. 109-114.
8. E. M. Monberg, H. Brown, S-N. G. Chu, and J. M. Parsey, "The Growth of Low Defect Density Semi-Insulating InP," *Proceedings of the 5th Conference on Semi-Insulating III-V Materials*, Malmo, Sweden, Institute of Physics, Bristol, England, 1988.
9. E. M. Monberg, W. A. Gault, F. Dominguez, F. Simchock, S.-N. G. Chu, and C. M. Stiles, "The Growth and Characterization of Large Size, High Quality, InP Single Crystals," *Journal of the Electrochemical Society*, Vol. 135, No. 2, February 1988, pp. 500-503.

Biographies (continued)

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(Manuscript received November 11, 1988)