FABRICATION TECHNOLOGIES FOR III-V COMPOUND SEMICONDUCTOR PHOTONIC AND ELECTRONIC DEVICES

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This paper describes process technologies for fabricating III-V photonic and high-speed electronic devices. The major processes involved are contact metallization, dielectric film deposition, wet and dry etching, diffusion, implantation, photolithography, wafer separation, and die bonding. For the photonic devices, the emphasis is on those long-wavelength devices that are fabricated with the InP/InGaAsP material system. In contrast, for the high-speed electronic devices, we discuss the fabrication of field-effect transistors with the GaAs/AlGaAs system. We present representative examples in detail and, where possible, identify commonalities and contrasts in their processing and in the process criticality. We review specific constraints that determine the processing technique, and give examples of how processing influences device performance and reliability. Finally, we assess the current trends in process development that are relevant to III-V device fabrication.

Introduction

The fabrication of III-V semiconductor photonic and electronic devices consists of a sequence of processes applied directly to a polished single-crystal wafer,[1] or to a wafer on which one or more epitaxial layers have been grown by liquid- or vapor-phase epitaxy (LPE or VPE)[2] or by molecular-beam epitaxy (MBE).[3] (Panel 1 defines acronyms and terms used in this paper.) The output of this wafer processing is a collection of chips of either discrete devices or integrated circuits (ICs). After appropriate testing, the chips are then bonded to packaging components such as headers or ceramic carriers. In this form, the devices undergo functional tests and reliability screens to select those that will be packaged.[4]

In its simplest conception, the processing sequence produces

localized contacts and conductive regions for channeling current into or from certain sections of the device. For photonic devices, the process also produces appropriate windows through which photons are emitted and received.

In this paper, we describe the structures and materials systems of some representative devices (two photonic—one an emitter, the other a detector—and one high-speed electronic). We discuss some constraints that III-V materials impose on processing, and then present an overview of the major processes used to fabricate these devices. Finally, we suggest current directions in the evolution of processing technology that relate to III-V materials.

III-V Device Structures and Materials

Earlier in this issue, Dutta reviewed[5] the types of photonic devices used in lightwave transmission systems. These devices include:

- Light-emitting diode (LED) and laser sources
- Positive-intrinsic-negative (PIN) photodetectors and avalanche photodetectors (APDs)
- Next generation devices, such as optical amplifiers and optoelectronic integrated circuits (OEICs).

Most devices manufactured today are for long-wavelength systems [1.3 and 1.55 μm (micrometer)] and are fabricated from indium gallium arsenide phosphide/indium phosphide (InGaAsP/InP) material. Only small numbers of devices are made of aluminum gallium arsenide/gallium arsenide (AlGaAs/GaAs) for short-wavelength systems (around 0.8 μm) that operate at low bit rates over relatively short distances. In general, the communications devices we are concerned with are fabricated from InP, InGaAsP, and indium gallium arsenide (InGaAs) lattice-matched, epitaxial layers grown on an InP, <100> axis substrate. Usually, this is an n-type substrate.

Photonic Sources. In Figure 1, we show a structural cross section of the channeled-substrate buried heterostructure (CSBH) laser as an example of a lightwave source. Elsewhere in this issue, Dutta discusses[5] this laser (and its AT&T system applications) and other laser structures.

The highest performance InGaAsP lasers need the tighter lateral optical and electrical confinement of a buried heterostructure, which typically requires two sets of epitaxial growth. An initial stage of wafer processing is needed between the epitaxial growth stages to define the width of the active buried waveguide. In the CSBH laser, for example, we can achieve this by initially growing current-blocking layers and etching a channel through them. We then use a second growth stage to grow the double heterostructure in the channel. The heterostructure consists of an n-type InP (n-InP) layer, an undoped active InGaAsP layer, and a p-type InP (p-InP) layer.

The other approach to achieving a buried heterostructure is currently being used to manufacture distributed feedback (DFB) lasers. Here, we initially grow the double heterostructure that contains the active layer. In the first processing stage, the heterostructure is etched to leave a narrow mesa, and then a blocking-layer structure is regrown around the mesa.

Regardless of the approach, final wafer processing is the same.

Several structures in lasers and LEDs have recently been reviewed.[6] The LEDs also consist of a double heterostructure. For example, an edge-emitting LED (EELED) may have exactly the same cross section as a laser, but with nonreflective facets through which the LED's light is emitted. However, the two epitaxial growths needed for lasers are not used for an LED's buried heterostructure.

Instead, LEDs are usually fabricated from a single-growth, planar, buried heterostructure that has a much thicker active layer than is used for a laser. Here, the light-emitting region is defined by processing steps that cause the drive current to be channeled through a restricted area of the active layer, a stripe (in an EELED), or a dot [in a surface-emitting LED (SELED)]. In an SELED, light is emitted through a window in the InP

Panel 1. Terms and Acronyms

2DEG	two-dimensional electron gas
Al	aluminum
AlGaAs	aluminum gallium arsenide
AlN	aluminum nitride
APD	avalanche photodetector
AR	antireflection
As	arsenic
Au	gold
AuBe	beryllium gold alloy
AuGe	germanium gold alloy
AuGeNi	gold germanium nickel alloy
Be	beryllium
Br	bromine
CSBH	channeled-substrate buried heterostructure
CF_2Cl_2	diflourodichloro methane
CF_4	carbon tetraflouride
CF_4:O_2	carbon tetraflouride and oxygen mixture
CH_3OH	methanol
CH_4	methane
CH_4:H_2	methane and hydrogen mixture
CHF_3	trifluoromethane
Cr	chromium
Cu	copper
DFB	distributed feedback
DFET	depletion-mode field-effect transistor
EELED	edge-emitting light-emitting diode
EFET	enhancement-mode field-effect transistor
Fe	iron
FET	field-effect transistor
GaAs	gallium arsenide
H_2O_2	hydrogen peroxide
H_2SO_4	sulfuric acid
H_2SO_4:H_2O_2:H_2O	sulfuric acid, hydrogen peroxide, and oxygen mixture
HCl	hydrochloric acid
HBr	hydrobromic acid
HBr:H_2O_2	hydrobromic acid and hydrogen peroxide mixture
HF	hydroflouric acid
HFET	heterostructure field-effect transistor
HR	high reflection
I	iodine
IC	integrated circuit
InGaAs	indium gallium arsenide
InGaAsP	indium gallium arsenide phosphide
InP	indium phosphide
InP:Fe	iron-doped InP
KI	potassium iodide
KI:I_2	potassium iodide and iodine mixture
LED	light-emitting diode
LPE	liquid-phase epitaxy
LR	low reflection
MBE	molecular-beam epitaxy
n-type	material in which electrons carry the current; n^+ is heavily doped and n^- is lightly doped
Ni	nickel
OEIC	optoelectronic integrated circuit
p-type	material in which holes carry the current; p^+ is heavily doped and p^- is lightly doped
OMVPE	organometallic vapor-phase epitaxy
P	phosphorus
Pb	lead
PECVD	plasma-enhanced chemical-vapor deposition
PIN	positive-intrinsic-negative
Pt	platinum
RC	resistance capacitance product
RIE	reactive-ion etch
SARGIC	self-aligned refractory gate, integrated circuit
SELED	surface-emitting light-emitting diode
Si	silicon
SI	semi-insulating
SiC	silicon carbide
SiN_x	silicon nitride
SiO_2	silicon dioxide
SiO_xN_y	silicon oxynitride
SL	superlattice
Sn	tin
Ti	titanium
Ti/Pt/Au	titanium platinum gold layered metallization
VPE	vapor-phase epitaxy
WIn	tungsten indium alloy
WSi	tungsten silicide
Y	yttrium
Zn	zinc
ZrO_2	zirconia

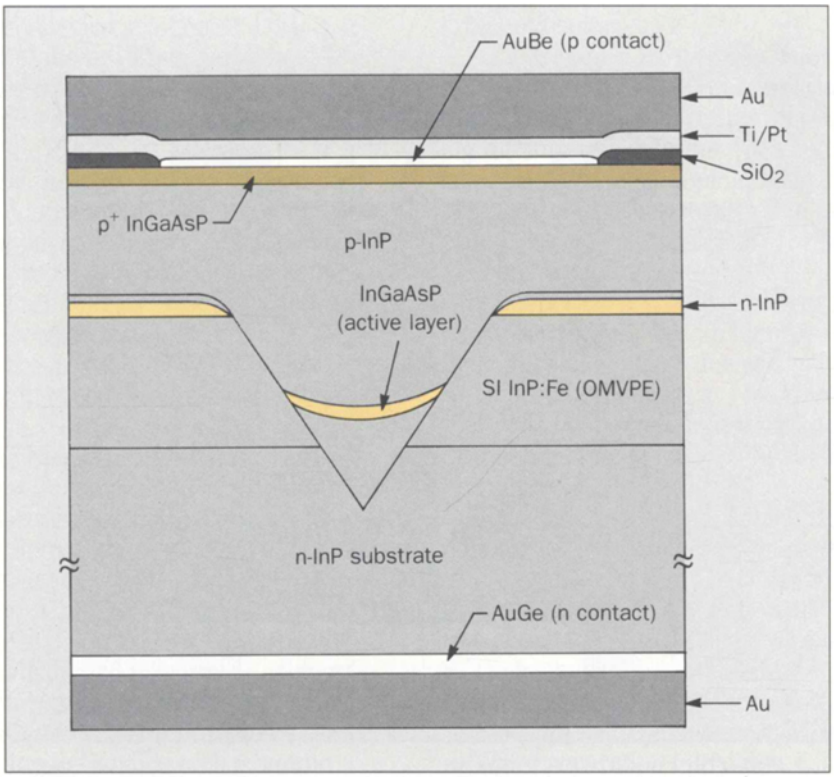

Figure 1. Structural cross section of a CSBH laser chip.

substrate rather than from a facet.

Other than these geometrical differences, the basic wafer processing for an LED is the same as for a laser.

Photonic Detectors. Photodetectors are fabricated from single epitaxial-growth heterostructures that use a ternary InGaAs absorbing layer, which is sensitive to both 1.3-μm and 1.55-μm radiation. Figure 2 shows a cross section of AT&T's planar APD. To define the detector's sensitive region, a p-type dopant is diffused through a window in a dielectric mask. Ion implantation is used to form a p^- guard ring around the periphery of the p^+ diffused center to eliminate edge-breakdown effects. The p^+ junction is positioned so that the photocurrent can multiply at operating voltages.

If we remove the guard ring and multiplication layers from Figure 2, we have AT&T's PIN photodetector. As Dutta discussed,[5] the PIN photodetector has lower performance (no multiplication) but can be produced at lower cost.

Emerging Photonic Devices. Different processing is required for the next-generation devices that Dutta described[5] elsewhere in this issue. Optical amplifiers are longer-length laser chips (for additional gain) with facets of extremely low reflectivity. The facets are produced by coatings of nearly perfect antireflection material, or the active waveguide is oriented off normal from the facet. Monolithically integrated devices, such as source-monitor detector pairs or arrays of sources or detectors, use semi-insulating InP epitaxial layers and novel process-

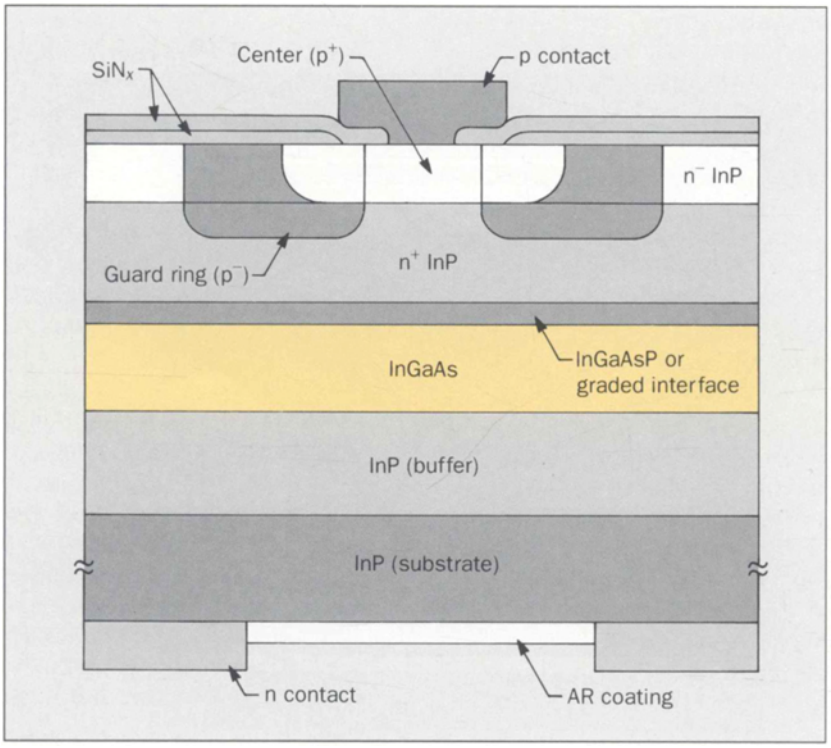

Figure 2. Structural cross section of a planar avalanche photodiode chip.

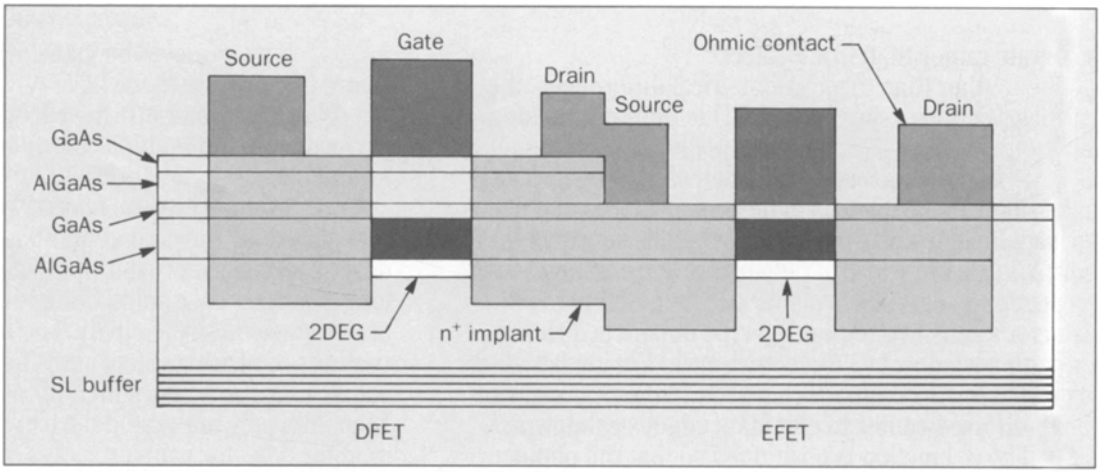

Figure 3. Structural cross section of the SARGIC HFET element of a GaAs IC.

ing to isolate the individual device structures. OEICs take this a step further; but for InGaAsP/InP long-wavelength devices, the less well-advanced, high-speed electronics technology in InGaAs or InP hinders progress.

High-Speed Electronic Devices. These integrated circuits consist of multiple components. Thus, besides fabricating the individual devices, the wafer fabrication process must provide appropriate interconnections between them. The desired function of the circuit determines the particular interconnection scheme.

Figure 3 shows the SARGIC HFET (for self-aligned refractory gate, integrated-circuit, heterostructure field-effect transistor). The SARGIC HFET incorporates two building blocks—the AlGaAs/GaAs enhancement-mode field-effect transistor (EFET) and the depletion-mode field-effect transistor (DFET), which Shah and Pei described[7] in this issue—that are illustrative of III-V high-speed electronic devices.

The SARGIC HFET is designed to combine the performance of heteroepitaxial structures with the yield-enhancing aspects of a self-aligned process; i.e., the gate acts as an implant mask for creating the n^+ source and drain regions. The self-aligned implant provides a uniform and repeatable, low-resistance path from the source to the two-dimensional electron-gas (2DEG) channel, further enhancing performance. A refractory gate serves both as the implant mask and as an encapsulant for the channel during the high-temperature, implant-activating annealing stage. In addition, the gate provides the Schottky characteristics of the transistor. Ion implantation is also used to produce nonconducting regions for device isolation, which maintains the relatively planar structure that is essential for high-yield interconnection of tens of thousands of these devices.

Two device types, EFETs and DFETs, are fabricated from the epitaxial substrate. A single, doped AlGaAs layer provides charge for the 2DEG channels for the EFET and DFET. The doping in the donor layer and the spacing from gate to channel determine the threshold voltages.

For EFETs, gate-to-channel spacing is adjusted by selective etching of undoped GaAs and AlGaAs layers. Tight threshold-voltage control is necessary in fabricating the integrated circuit. MBE provides tight control of layer thickness and doping. High selectivity of AlGaAs etching over GaAs is required to avoid thinning of the GaAs layer to maintain EFET threshold-voltage control afforded by MBE.

Commonalities. From Figures 1 through 3 and the above discussion, we can identify several processing commonalities in all these device structures:

- Deposited dielectrics. These are used for etching or diffusion masks, contact-area definition, reflectivity modification, surface passivation, or low-capacitance intermetal insulators.
- Photoresist for lift-off or etching procedures for dielectric and metallization patterning.
- Wet or dry etching of semiconductor and dielectric layers.
- Contact formation (either ohmic or Schottky contacts).
- Deposited barrier metals and noble-metal bonding pads. (A *noble metal*—e.g., gold, silver, or platinum—has high resistance to corrosion and oxidation.)
- Wafer separation into chips.
- Chip bonding to heat-sink carriers or headers.

In addition, these procedures frequently incorporate surface preparation and thermal treatment. A few other processes are used only for specific devices.

General Constraints on Processing

The sensitivity of III-V materials imposes constraints on the processing used; so do the device's performance requirements. InP—and to a lesser extent, GaAs—is very susceptible to processing-induced damage.

During thermal processing, III-V compounds tend to lose the more-volatile group V component. InP loses phosphorus (P) by incongruent evaporation above 360°C, and GaAs loses arsenic (As) above about 600°C. Thus, if high-temperature processing is required, we

must provide an overpressure of the group V element or must protect the surface with a thermally stable, dielectric cap layer. For similar reasons, dry etching can also produce a group-III-rich surface. III-V materials are also more sensitive to damage from ion bombardment than silicon. These considerations mean lower temperatures and energies are necessary to produce high-performance, reliable devices.

A constraint imposed by device performance is the need for very tight line-width control—for the width of the active layer in a laser and the gate in a high-speed field-effect transistor (FET). In a buried heterostructure laser, for example, a typical requirement is to hold the width to about 1.0 μm in an active layer about 2.5 μm below the surface. This places severe demands on the photolithography, etch mask, and etching processes.

The AT&T SARGIC digital process relies on tight control of a 1.0-mm gate length, while the highest speed analog versions strive for 0.5-mm gate lengths, which require the use of electron-beam lithography and/or elaborate photoresist processes.

Process Sequences and Stages

Device fabrication entails not only the application of a collection of processes, but also the sequencing of those processes in a compatible way. For example, one cannot use a downstream process whose temperature exceeds the stability limit of an upstream process, nor use an etchant that is indiscriminate. Because process interactions can be subtle, a newly developed process requires extensive prove-in before it is introduced into an established process flow. This involves detailed analysis of how the new process affects initial device performance and long-term reliability.

We now present and discuss the processing sequences for fabricating the photonic sources, detectors, and high-speed electronic devices depicted in Figures 1 through 3, respectively.

CSBH Laser Processing. Figure 4 shows the processing flow for the CSBH laser in Figure 1.

The first stage is base-structure processing. Here, the input is an n-InP substrate with a blocking layer of semi-insulating (SI), iron-doped InP (InP:Fe). The output of this process is a wafer with an etched V groove that penetrates the blocking layer by a well-controlled amount and that has a precise V profile. This precision is essential to achieve high yields of low threshold, low leakage, single lateral-mode lasers. The key to tight control of this V profile's depth is surface treatment of the InP before the silicon dioxide (SiO_2) etch mask is deposited. This surface treatment is required to obtain reproducible mask undercut during crystallographic selective etching.[8] Also essential is tight control of the etched window width in the SiO_2 mask.

Next is epitaxial growth of the double heterostructure, with a buried crescent section of the active layer confined at the correct depth in the channel. The wafer then goes into the final wafer-processing sequence shown in Figure 4. In this stage, we:

1. Establish a dielectric refined, restricted-area, ohmic contact to the epitaxially grown p side of the wafer.
2. Thin the wafer to a thickness suitable for cleaving later.
3. Make the substrate (n side) ohmic contact.
4. Deposit gold (Au) bonding pads on both sides of the wafer. On the p side, where metallization is close to the active layer, a titanium platinum (Ti/Pt) bilayer was deposited earlier to act as a barrier that prevents long-term diffusion of Au from this bonding pad into the underlying semiconductor.
5. Scribe and cleave the wafer to form chips with high-quality laser mirror facets that can then be tested.
6. Use current pulses to test the chips to determine their light- and voltage-current characteristics. Those that meet the initial screening requirements are then bonded to heat-sink packaging components for further functional testing.

If facet coating is being used, it can be deposited at any stage after the mirror facets are exposed.

We have just described the base-structure (or

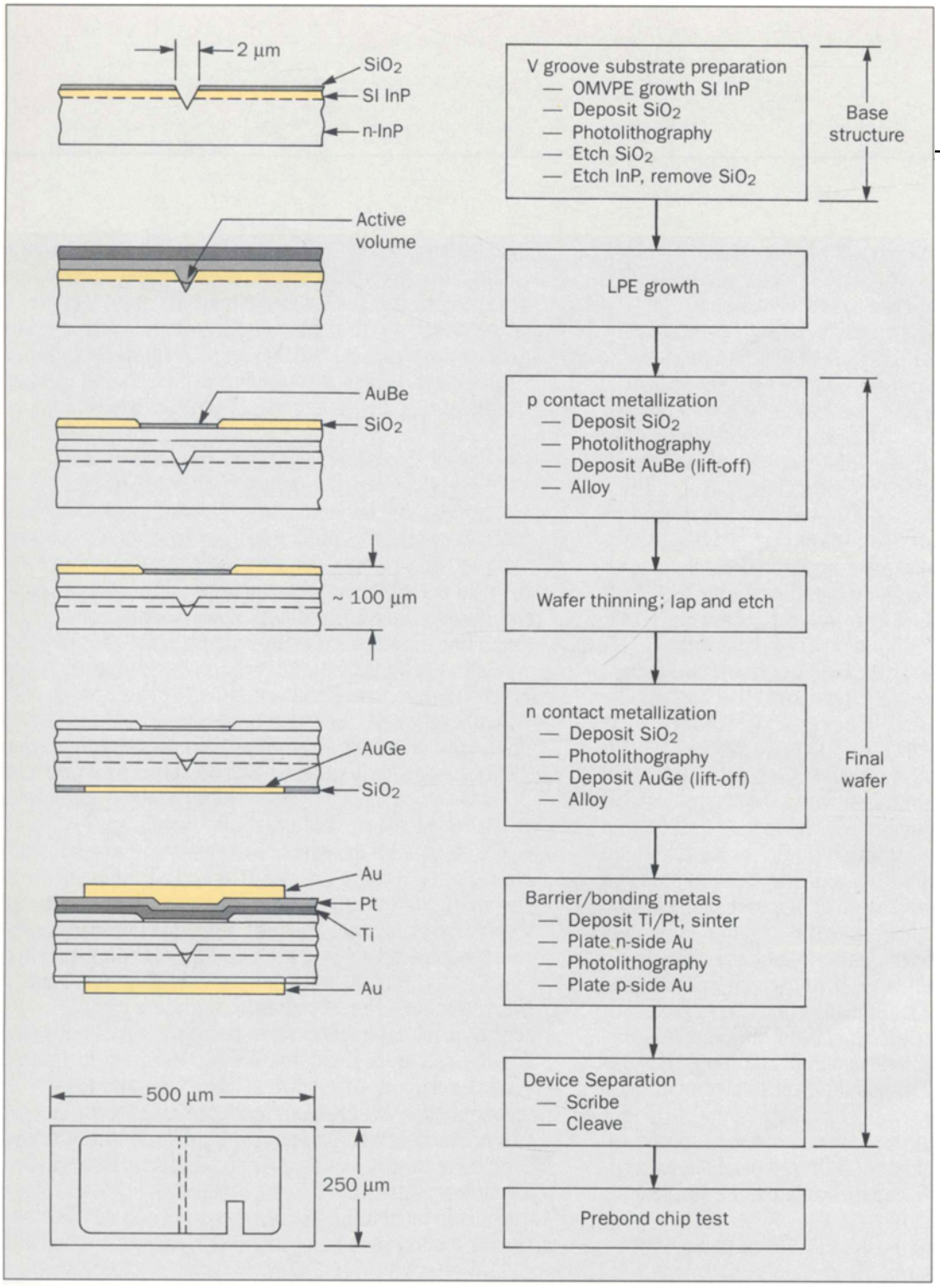

Figure 4. Processing sequence for the fabrication of the CSBH laser.

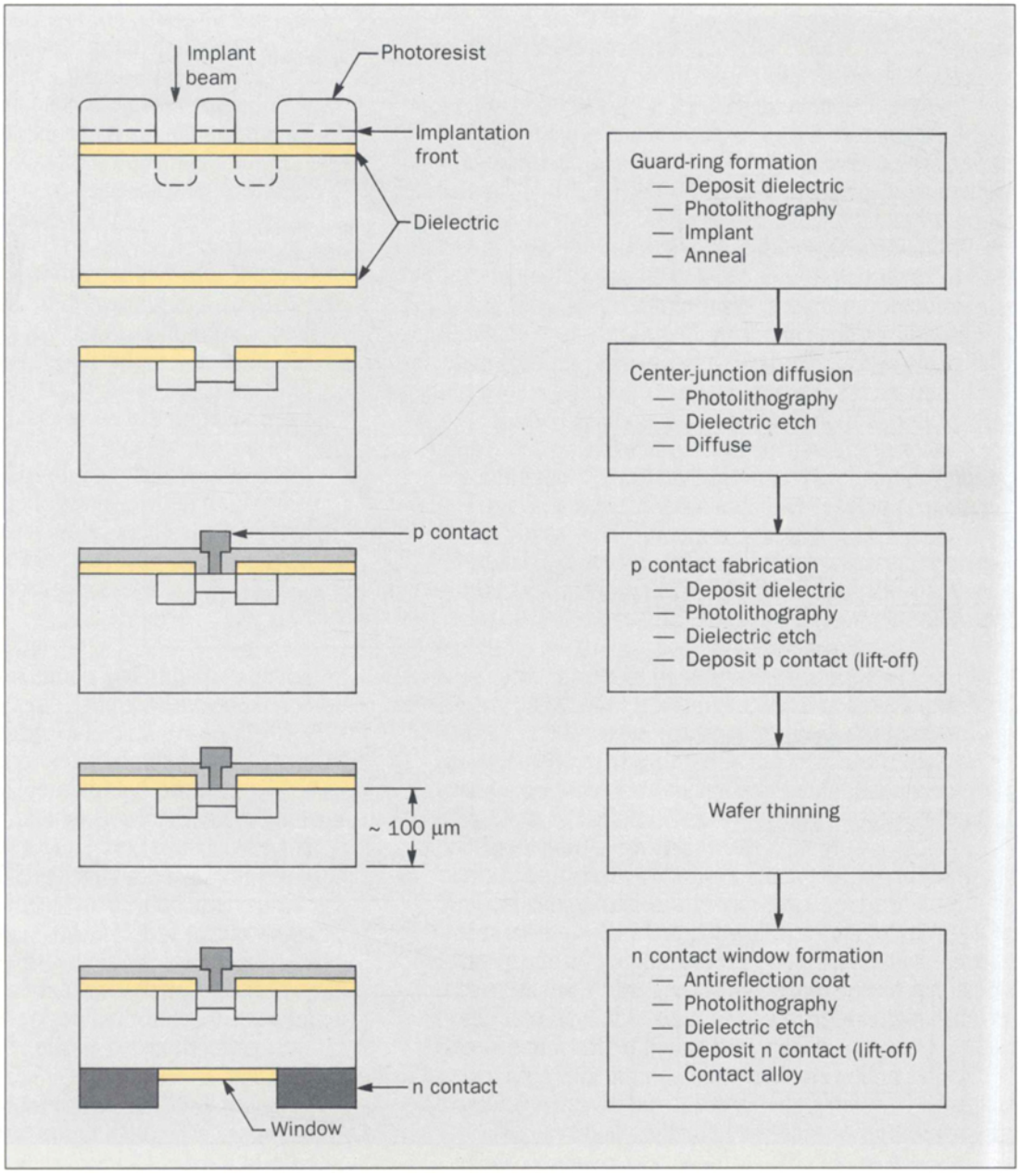

Figure 5. Processing sequence for the fabrication of the avalanche photodiode.

inter-epitaxial) processing and final wafer (post-epitaxial) processing required to fabricate a Fabry-Perot multi-frequency laser. Of the devices we are discussing, only lasers require these multiple stages of wafer processing. In addition, single-frequency DFB lasers require a third stage of processing, generally a pre-epitaxial stage in which a DFB grating is patterned and etched into the substrate wafer.

APD Processing. Figure 5 gives the process sequence for APDs. In contrast to the laser (Figure 4), fabrication here proceeds on a finished epitaxial wafer to produce planar devices. The general sequence of wafer-level processing is to form guard rings, create the p^+ doped diode, and then pattern the metal contacts.

Implantation requires coating the wafer on both sides with a dielectric for thermal protection, and using photolithography to create "donut" shaped openings on the epitaxial side. The photoresist is made thick enough to stop implanted ions from reaching the wafer surface outside these openings. Both implantation energy and total dose are carefully controlled to create the desired guard-ring doping profile.

After implantation, the photoresist layer is removed, and the wafer is annealed to remove the implantation damage. To create the diode's center junction, we first use photolithography and plasma etching to form openings in the dielectric that are concentric with the guard-ring donuts, and then diffuse a p-type dopant through the opening.

Next, a second dielectric layer is deposited and patterned to form a p contact window. Metal is deposited through a photoresist mask and lifted off to form the circular p contact. To complete wafer processing, we thin the wafer from the back side to about 100 μm, deposit an antireflection (AR) coating, and pattern this coating to form n side contacts by steps similar to those used on the p side. The metal contacts are alloyed for low resistance. The wafer is sawed to separate the individual devices, which are then tested to ensure that only good devices are packaged.

If we remove the guard-ring formation steps, Figure 5 also describes the fabrication sequence for the PIN photodiode.

SARGIC HFET Processing. Figure 6 outlines the process sequence for the SARGIC HFET. Processing begins with etching of alignment marks onto the MBE-grown layers, followed by ion implantation for device isolation. EFET regions are then defined by selective etching of undoped GaAs and AlGaAs layers in regions where EFETs are to be formed. A wet hydroflouric acid (HF) etch over the entire EFET region provides an etch selectivity of more than 100 to 1 of AlGaAs over GaAs, thus satisfying the requirement that layer thicknesses are to be maintained during processing.

Gates are then defined on both the EFET and DFET regions by sputter deposition of tungsten silicide (WSi) and reactive-ion etching. After gate definition, source and drain regions are formed by implanting silicon (Si), activation annealing the implant with an arsenic (As) overpressure, and forming ohmic contacts with a gold germanium nickel (AuGeNi) alloy. Au-based alloyed ohmic contacts are required to provide adequately low contact resistance, but upper temperatures are limited for subsequent processing. Furthermore, the attendant need for lift-off patterning (because a selective dry-etch process for Au does not exist) limits the minimum feature size and is more likely to result in interlevel shorts.

To complete wafer fabrication, two levels of interconnects are formed by means of silicon oxynitride (SiO_xN_y) deposition, via etching, and lift-off patterned titanium platinum gold (TiPtAu) metallization. (A *via* is a vertical electrical conductor that connects between conductors on two different levels in a layered structure.) The Au-based ohmic contacts preclude the use of the aluminum (Al) interconnects employed in Si integrated circuits, because the Al/Au interface that results is unstable under thermal or current stress, unless a diffusion barrier is placed between the Al and Au.

Common Processes. From these process-sequence flowcharts, we can see that many steps—often themselves consisting of several substeps—are required to fabri-

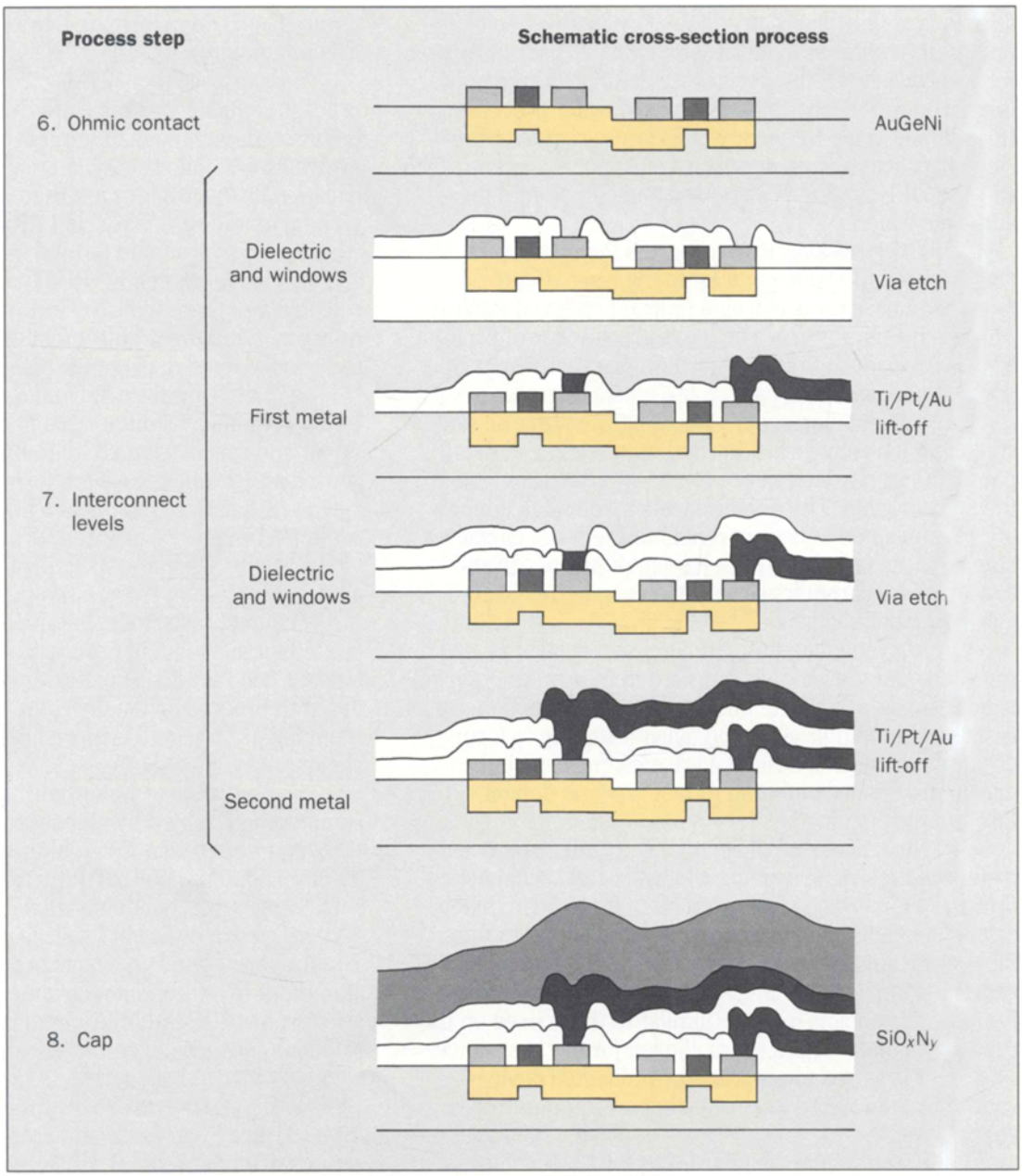

Figure 6. Processing sequence for the fabrication of the SARGIC HFET.

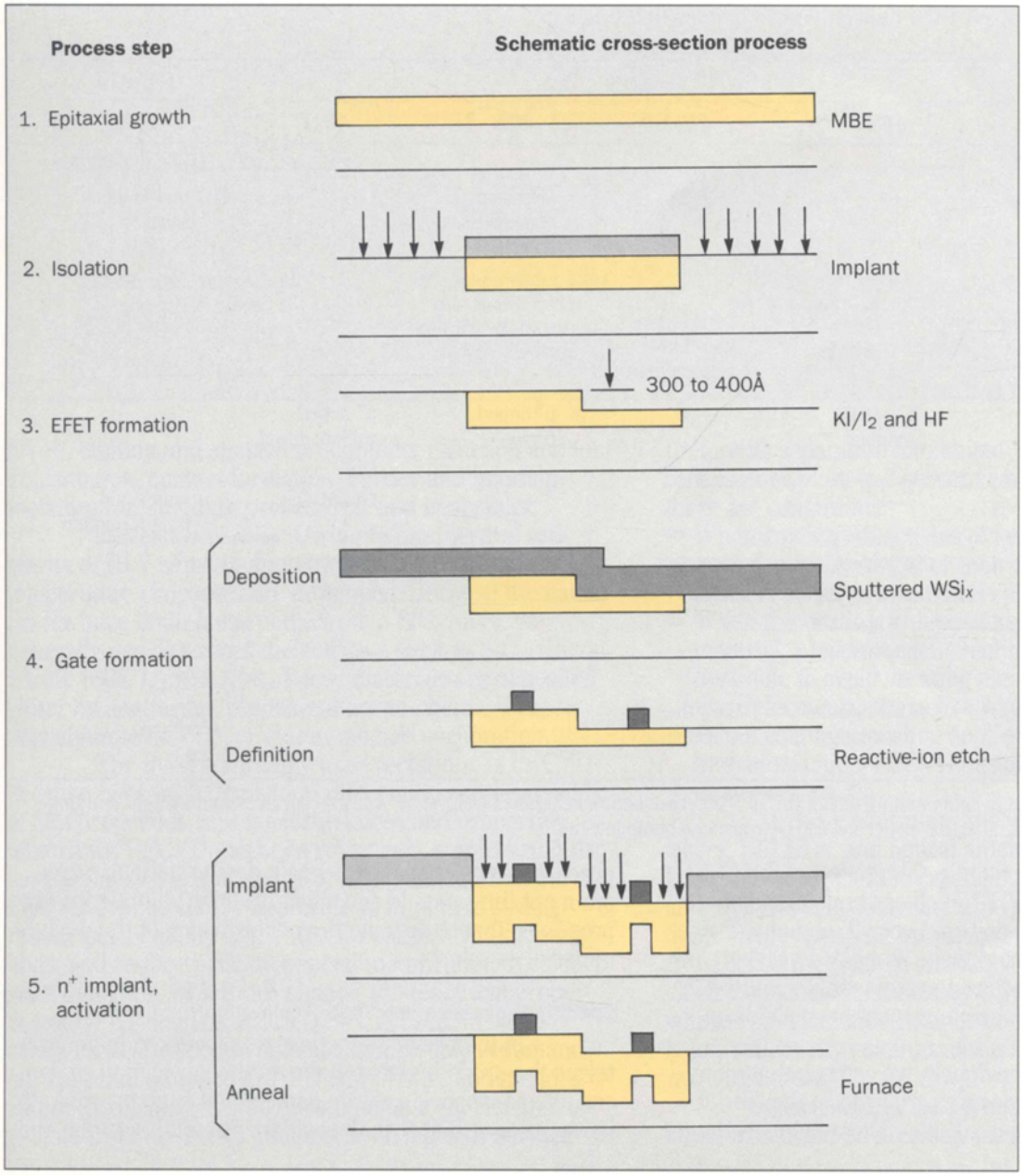
Process step
Schematic cross-section process
1. Epitaxial growth
MBE
2. Isolation
Implant
300 to 400Å
3. EFET formation
KI/I2 and HF
4. Gate formation
Deposition
Sputtered WSix
Definition
Reactive-ion etch
5. n+ implant, activation
Implant
Anneal
Furnace

Table I. Critical Processes and Their Applications in Various III-V Devices

Critical process	InGaAsP photonic					GaAs IC
	Laser	EELED	SELED	PIN	APD	HFET
Lithography	Etch mask	—	—	—	—	Gate definition
Dielectric deposition	Etch mask	—	—	Diffusion mask, passivation layer	—	Interconnect isolation
Dry etching	Etch mask	—	—	—	—	Via hole
Wet etching	Channel or mesa	—	Lens formation (photoelectrochemical)	—	—	FET definition
Diffusion	—	Current guiding	—	p^+ doped region	p^+ doped region; guard ring	—
Implantation	—	—	—	—	Guard ring	Source and drain formation
Contact metallization	p contact	p contact	p contact	—	p contact	—
Dielectric deposition	AR, LR, and HR facet coatings	AR facet coating	—	—	—	—
Bonding to heat sink	Low thermal impedance bond	Low thermal impedance bond	Low thermal impedance bond	—	—	Low thermal impedance bond

NOTE: EELED = edge-emitting light-emitting diode; HFET = heterostructure field-effect transistor; SELED = surface-emitting light-emitting diode; PIN = positive-intrinsic-negative diode; and APD = avalanche photodetector.

cate these devices. For example, fabrication of the CSBH laser, the APD, or the HFET involves about 30 major process steps, excluding epitaxial growth and any device testing. If each of these composite steps had a 90-percent yield, the cumulative processing yield would be only 4.2 percent. Clearly, most of the steps must have yields approaching 100 percent.

As mentioned previously, we can see that many of the same or similar processes are used in the fabrication of most of these devices. But as Table I shows, the processes most critical to a given device structure are often not the same. In the table, we have identified those processes that determine the performance of the devices under discussion.

Specific Processes and Their Applications

In the previous section, we discussed in general terms the processes that make up the fabrication sequences. We now provide a little detail about each process and its variations: dielectric deposition, photolithography and

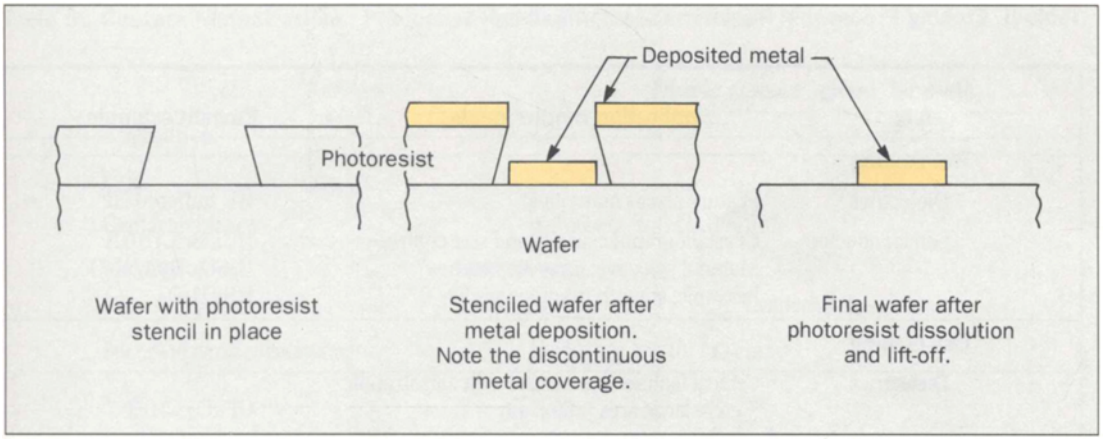

Figure 7. Schematic representation of a lift-off process.

lift-off, etching and surface preparation, diffusion and ion implantation, contact formation, barrier and bonding metallization, bonding procedures, and heat sinks.

Dielectric Deposition. Owing to the thermal sensitivity of III-V semiconductors described earlier, low temperature processes are employed. Because the native oxides have limited use compared to SiO_2 on Si, we generally use deposited dielectrics—such as SiO_2, silicon nitride (SiN_x), or SiO_xN_y. These materials are deposited either by sputtering, plasma-enhanced chemical-vapor deposition (PECVD), or electron-beam evaporation.

The most commonly used technique is PECVD because of its high deposition rates, good reproducibility of film properties, and good thickness and properties uniformity. PECVD has been reviewed,[9] emphasizing its application to the processing of III-V semiconductors. PECVD conditions are optimized to minimize stress; reduce permeability of the film for reliability considerations; and reduce plasma-induced modification of surface-state densities, which can change the electrical properties of HFET devices. PECVD SiN_x is used, in some cases, for antireflection optical coatings in less-demanding applications (such as APD and PIN photodetectors) where the coating can be deposited on a surface that is remote from the active junction or on a planar surface (before its separation into chips), and where coating reflectivities of up to 2 percent can be tolerated. But there are constraints:

- When coating reflectivies of less than 1 percent are required, a material (other than SiN_x) whose refractive index is closer to optimum is needed.
- When the coating is deposited on exposed active material, a less-energetic technique than PECVD is desirable to avoid creating electrically and optically active defects near the active layer.
- When coatings must be applied to the cleaved facets of individual chips, PECVD has difficulty providing adequate uniformity.

All three contraints apply to coating the facets on lasers, EELEDs, and optical amplifiers. Sputtering has been shown to produce crystallographic damage in InP[9] and, therefore, is not a desirable process for these applications. However, some manufacturers still use sputtering. At AT&T, our choice of technique is the relatively gentle electron-beam evaporation of yttria-stabilized zirconia, whose refractive index can be controlled to give extremely low reflectivity coatings at the appropriate quarter-wave thickness.[10]

Photolithography and Lift-Off. The use of organic films, which can be precisely patterned by exposure to

Table II. Etching Processes: Requirements and Examples

Material being etched	Application requirements	Etchant example
Wet etching		
Dielectrics	Feature size is noncritical	HF, buffered HF
Semiconductor	Crystallographic: profile and size control	HCl, Br:CH_3OH
	Material selective: layer stop-etches	H_2SO_4:H_2O_2:H_2O
	Isotropic: smooth, rounded profile	HBr:H_2O_2
Dry etching		
Dielectrics	Critical feature-size control with anisotrophic etch; large area uniformity	CF_4:O_2,CHF_3
Semiconductor	Anistropic: feature-size control	CF_2Cl_2,CH_4:H_2
	Nonselective: profile constant across interfaces	CH_4:H_2

light and subsequent development, is critical to the fabrication of most microelectronic devices. The device fabrication discussed here uses a positive photoresist, i.e., a material that becomes soluble in developer after exposure to ultraviolet light. The photoresist process consists of depositing a film of carefully controlled thickness on the device wafer, aligning and exposing this wafer to ultraviolet light through a mask that exposes only those regions from which photoresist is to be removed, and then developing the film.

A patterned, positive photoresist film can be used as a stencil for creating metal patterns on a device wafer. This is the lift-off process illustrated in Figure 7, which is done by depositing metal on top of a patterned photoresist film on the wafer and then dissolving the underlying photoresist. The parts of the metal film that lie on top of the photoresist are then "lifted-off," leaving only the desired metal pattern.

Lift-off requires a metal thickness that is less than that of the photoresist; the photoresist's edges must be free of metallization, if the solvent is to get underneath. To achieve this reproducibly, elaborate thermal and optical processing of the photoresist film are required.

Etching and Surface Preparation. A deposited dielectric or the III-V semiconductor itself may be etched in either the liquid or the vapor phase. Table II summarizes where each is used and gives etchant examples.

The anisotropic dry etching referred to is reactive-ion etching (RIE) or low-frequency plasma etching; the directionality of the ion bombardment enhances the etch rate, which produces the etch anisotropy. These processes have been reviewed by Burton et al.[11] and by Dautremont-Smith et al.[9]

In both crystallographic and isotropic wet etching of III-V materials, we must pay great attention to the details of how the etch mask-semiconductor interface is formed, because it can have a profound effect on the degree of mask undercut and the resultant etched profile. As discussed earlier for CSBH laser base-structure processing, tight control of this profile is critical to achieving the desired width of the laser's active layer.

Surface preparation is also critical to reproducibility of the barrier height of Schottky contacts and

Table III. Contact Metallizations: Processes and Their Characteristics

Location	Ohmic contact	
	Alloyed	Nonalloyed
p side		
Contacting layer	p^+ InGaAs, InGaAsP, or InP	
Materials	Au:Zn; Au:Be	Ti/Pt; Cr/Au; Ni
Deposition method	Evaporation	Evaporation; sputtered
Specified contact resistance	$< 1 \times 10^{-6}$ to 1×10^{-4} Ω-cm^2	
n side		
Contact layer	n-InP, n-GaAs (~ 10^{18} cm^{-3})	
Materials	AuSn; AuGe(Ni)	Ti/Pt (InP only); WIn (GaAs only)
Deposition method	Evaporation	Sputtered or evaporation
Specified contact resistance	~ 1×10^{-6} Ω-cm^2	~ 3×10^{-7} to 1×10^{-5} Ω-cm^2

to adhesion of both Schottky and ohmic contacts. Thus, in these and many other cases, reproducible surface preparation is essential. This typically involves multiple organic-solvent cleanings, followed by a light etch of the material and removal of surface oxides.

Diffusion and Ion Implantation. Properly operating semiconductor devices require careful control of electrically active dopants. The dopant can be incorporated throughout a wafer during epitaxial growth. But *patterned* incorporation is done most easily through diffusion or implantation of an electrically active species into a wafer. The wafer is masked by a patterned film that is impermeable to the diffusant or thick enough to prevent penetration of the implanting ions. (See Figure 5.)

Diffusion is done by exposing the patterned wafer to a diffusant vapor at a temperature that is high enough for a diffusion front to proceed into the wafer in a controlled way. The physics of the process fix the resulting vertical dopant profile.

Implantation, on the other hand, is more flexible in that the profile is determined from the ion beam's dose and energy, both of which are controlled externally. High-temperature treatment must follow implantation to activate the dopant and anneal any crystal damage.

For the AT&T devices discussed here, the more-elaborate implantation process is essential for dopant grading in APDs (Figure 5) and to form sources and drains in HFET ICs (Figure 6).

Contact Formation. Processes that form contacts, either ohmic or Schottky, are critical to device performance and reliability. Photonic devices use ohmic contacts; usually, the n contact is made to the n-InP substrate, and the p contact is made to heavily doped epitaxial layers of InGaAs, InGaAsP, or InP. The magnitude of the contact resistance is not critical for photodetectors, which produce very low current densities. But for photonic sources that operate at very high current densities through the p contact, reproducibly low

specific-contact resistance is critical to both performance and long-term reliability. Lasers and LEDs operate at contact current densities up to 3×10^4 A/cm^2 (amperes per square centimeter). To prevent the contact from increasing the power dissipation appreciably over that at the junction, the specific contact resistance of p contacts must not exceed about 1×10^{-5} Ω–cm^2 (ohm-centimeters squared). On HFETs, a low specific-contact resistance less than or equal to 1×10^{-6} Ω–cm^2 is required for the source and drain contacts to prevent an increased resistance × capacitance (RC) time constant from limiting the speed of response.

In Table III, we show both alloyed and nonalloyed contact metallurgies. The former are gold-based, and involve deposition of an alloy of Au, with an acceptor [beryllium (Be) or zinc (Zn)] for the p contacts or a donor [germanium (Ge) or tin (Sn)] for the n contacts. In the heat treatment used later to produce a low contact resistance, this metallization alloys (at around 400°C) into the semiconductor surface up to a depth of a few times the initial metal thickness, thus forming a complex, nonhomogeneous, multicomponent layer. In contrast, the nonalloyed contacts use metals that are far less reactive with the III-V surface.

Currently, the alloyed contacts are the most commonly used in manufacture. However, we have observed that, under certain contact-forming conditions, Au migration from the contact into the active layer enhances the high-temperature degradation rates of the highest current density device (the SELED). This (and many other advantages) has fueled a move toward nonalloyed contacts, although their reliability benefits on any other devices have not been substantiated.

Schottky contacts serve as the gate metal for high-speed switching of HFET devices. Reproducibility of a device's electrical parameters requires that a noninteracting metal-GaAs interface be maintained after gate deposition and all subsequent processing steps. If appropriate surface preparation is used before gate deposition, the WSi-GaAs contact satisfies this requirement for

Panel 2. Chip Bonding

Considerations:

- Thermal impedance (laser, LED, FET)
- Bond stress (performance, reliability)
- High-temperature accelerated aging (reliability assurance)
- Bond stability (package stability)
- Positional precision (packaging yield)
- Step soldering constraints (packaging).

Bond material:

Material	Melting point (°C)	Comment
In	156	Foil preforms, or masked deposition
Pb:Sn	182	
Au:Sn	280	
Au:Ge	356	
Epoxy	100-150	—

Heat-sink material (laser, LED, FET):

Material	Thermal conductivity (W/m/K; 20-100°C)
BeO	230
SiC	230
Si	140
AlN	240
Diamond (2A)	2000
Cu	400

Heat-sink metallization:

Au, thickness may be important in determining final bond composition.

Chip polarity:

Epitaxial layer up or epitaxial layer down? Determined by tradeoff between thermal impedance and chip positional tolerance requirement.

processing temperatures up to 800°C.

Barrier and Bonding Metals. All the devices discussed require pure Au bonding pads, if only to permit thermosonic or compression bonding of Au wires for electrical connection to the outside world. For the power dissipating devices, Au pads are also needed to spread heat and allow low-thermal-impedance solder bonding to Au-plated heat sinks (see the next section). Generally, a compromise of the functions needed determines the thickness of the Au. For the thinner pads, evaporation or sputtering is used for Au deposition, whereas electroplating is used for the thicker pads.

The Au pad could act as a huge reservoir of Au and provide the potential for long-term degradation of the contact or the underlying active layer. To prevent this, a metallurgical barrier bilayer of Ti/Pt—deposited by evaporation or sputtering—often is interposed between the Au pad and the underlying Au-based contact. For nonalloyed contacts, the contact metal itself may be the barrier layer, so no additional deposition is necessary.

Bonding Procedures and Heat Sinks. Panel 2 summarizes the considerations that determine the bonding requirements, and the bonding and heat-sink materials used, along with their most relevant parameter. For power-dissipating devices, chip bonding is a critical technology. For example, a laser that operates at 60°C may well be dissipating 150 mW (milliwatts) through a thermal impedance of 80K/W (kelvins per watt), making the active layer temperature 12°C above that of the heat sink's periphery.

Laser threshold currents vary exponentially with temperature, with a characteristic temperature of about 50K; and aging rates double for every 10°C increase in temperature of the active layer. Clearly, thermal impedances must be kept both low and reproducible. Similar considerations apply to all the high-power devices.

Processing Technology Evolution

The technologies becoming of increasing importance are those that can further reduce process temperature or the dose and energy of energetic particle bombardment. The technologies of greatest relevance, which includes numerous developments of plasma processing techniques, are:

- Plasma processing advances—particularly microwave (both the direct and indirect downstream varieties), multipolar magnetron, and pulsed high power
- Low-energy, ion-bombardment assisted processing
- Photo-enhanced processing
- Rapid thermal processing (for more than just rapid thermal annealing).

A final technology that is likely to become important is hydrogenation.[12] Here, atomic hydrogen is indiffused to produce semi-insulating layers by donor or acceptor passivation, and to passivate a variety of native defect states.

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Biographies (continued)

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