DESIGN FOR MULTINATIONAL EMC COMPLIANCE

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Successful competition for global markets depends in part on corporations such as AT&T competing effectively in a world of diminished trade barriers, competitive pricing, and—the subject of the present discussion—complying with a variety of multinational electromagnetic compatibility (EMC) standards and regulations. (See Panel 1 for acronyms used in this paper.) We present a successful design process for EMC regulatory compliance that may be used as a model for developing new products. The EMC design process, testing for ensuring compliance, and appropriate quality metrics will be discussed from the perspectives of the circuit designer, printed wiring board (PWB) layout designer, and compliance test engineer.

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Introduction

Advances in telecommunications have created a global marketplace for many multinational firms such as AT&T. Successful competition for these new markets depends on accommodating three basic factors:

- Diminishing trade barriers
- Competitive pricing through low-cost product development and manufacture
- Complying with various multinational standards and regulations in electromagnetic compatibility (EMC).

This paper stresses the successful EMC practices that are applied during product development, and the product team's role in realizing them. AT&T's ability to profitably access global markets in a timely way depends on cooperative interaction on EMC matters among all organizations that contribute to the final product.

We present a successful design process for EMC regulatory compliance that may be used as a model for new product development. EMC represents the assurance that a product will operate without performance degradation (i.e., immunity), and that it will not be a source of interference (i.e., emission) in its intended electromagnetic environ-

Panel 1. Terms and Acronyms in This Paper

AC	alternating current	EMI	electromagnetic interference
ACL	advanced CMOS logic	FCC	Federal Communications Commission
CAD	computer-aided design	HCL	high speed CMOS logic
CISPR	International Special Committee on Radio Interference	I/O	input/output
CMOS	complementary metal oxide semiconductor	LSI	large scale integration
DC	direct current	LSTTL	Low Power Schottky Transistor-Transistor Logic
DES	design engineering services	MHz	megahertz
DFX	design for *X*, where *X* stands for manufacturability, installability, reliability, safety, serviceability, and other downstream considerations beyond performance and functionality	MLB	multi-layer board
DSR	double-sided board	nsec	nanosecond
ECL	emitter coupled logic	PWB	printed wiring board
EID	engineering information department	RF	radio frequency
EMC	electromagnetic compatibility	RFI	radio frequency interference
		VCCI	Voluntary Control Council for Interference (Japan)
		VDE	Verbund Deutscher Electrotechniker (W. Germany)
		VLSI	very large-scale integration

ment at the customer location. The EMC design process, testing for ensuring compliance, and appropriate quality metrics, will be discussed from the perspectives of the circuit designer, PWB layout designer, and test engineer. We are from these disciplines, and have been associated with cost-effective EMC designs, starting with EMC requirements in the systems requirements document, and proceeding through both initial and ongoing compliance testing processes.

Domestic EMC compliance requirements for commercial products originated when the Federal Communications Commission (FCC) issued its "Computing Device" rules in 1979, with an effective date of 1983.[1–2] Since then, almost all modern electronic products using microprocessors have had to meet FCC emission standards before being considered marketable in the United States. Failure to suppress undesirable radiated (electromagnetic) and conducted (power cord and input/output [I/O] cables) radio frequency emissions may have a disastrous impact on product marketing. For example, the FCC is authorized to have non-compliant products confiscated and fines levied on the manufacturer.

When AT&T ventured into the international marketplace, it became aware that other nations have their own compliance requirements. Though their radiated and conducted emission requirements may be similar to the FCC's, the allowable radio frequency (RF) emission levels differ in many frequency ranges. Products designed for domestic emission compliance could be marketed abroad if, at the very least, the targeted country's emission limits were equal to or less stringent than the FCC limits, and the method of compliance measurement were similar. However, this is not always the case. Meeting more stringent limits generally requires product modification or outright redesign requiring development effort and cost, and the associated delay to

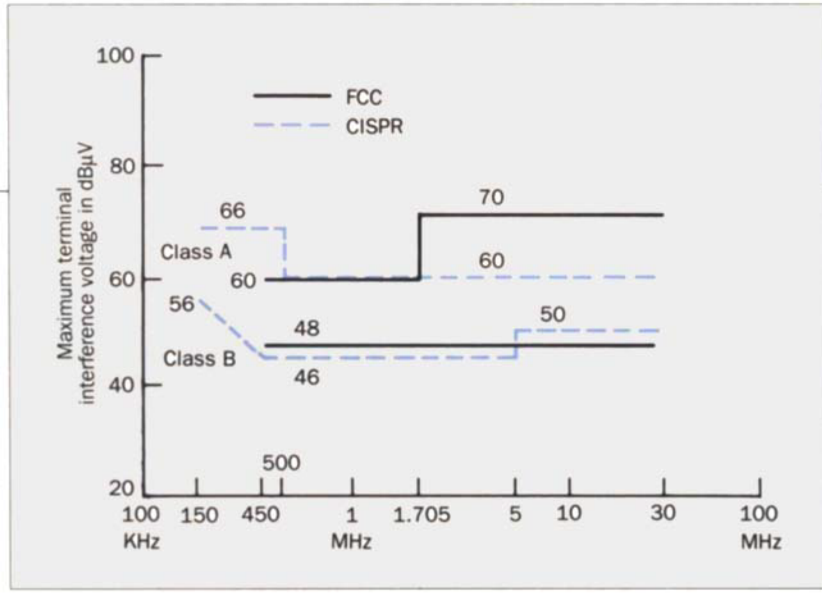

Figure 1. Comparison of maximum terminal narrowband interference voltage using average detector.

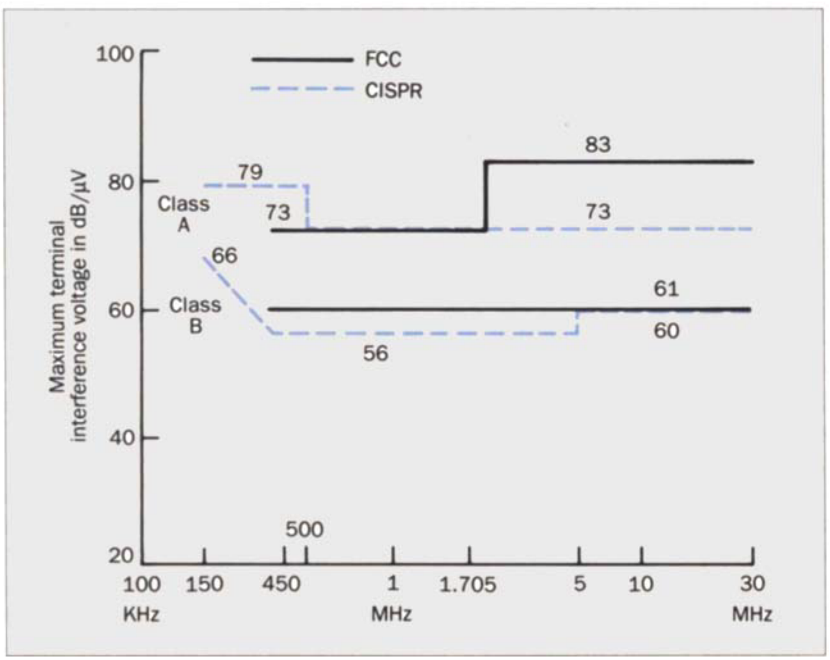

Figure 2. Comparison of maximum terminal broadband interference voltage using quasipeak detector.

market entry. If the rework expense and delay are significant, international marketing efforts could be halted. This potential loss of revenue can be avoided if the product is designed for multinational compliance from the outset.

Immunity also is a major factor in EMC. (*Immunity* means no performance degradation is expected.) Products must not only suppress RF emissions, but also must be immune to the RF ambient (i.e., the operating environment) existing on the customer premises. Presently, the FCC does not regulate product immunity. This will not be the case in Europe by 1992, where the European Community will mandate a minimum product immunity. In addition, contractual obligations may impose

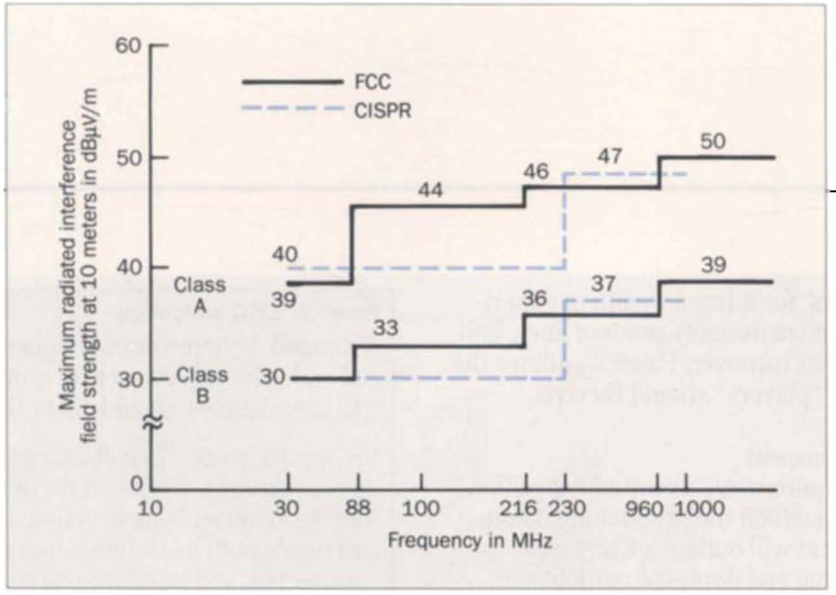

Figure 3. Comparison of maximum radiated interference field strength at 10 meters for FCC and CISPR specifications.

additional emission and basic immunity requirements.

This paper will concentrate on emission considerations. To minimize development and manufacturing costs, EMC requirements must be considered at every stage of the product realization process. This process is known as *designing for EMC.*

Preparing For EMC Design

EMC rarely is taught in the university. Consequently, few newly-graduated designers know much about its concepts. Thus, the first step in a good EMC design program is *training.* Most companies—AT&T among them—provide training internally or through consulting firms specializing in EMC instruction. The purpose of EMC education is to instill in each designer the basic concepts needed to have a reasonable expectation of meeting FCC and international emission limits during compliance testing at the end of the design process.International limits, for example, generally are based on those specified in publications written by the International Special Committee on Radio Interference (CISPR), the Japanese Voluntary Control Council for Interference (VCCI), and the West German Verbund Deutscher Electrotechniker (VDE).[3-4]. Figures 1–3 show both FCC and CISPR limits in graphic formats.

Because the VDE and VCCI limits will be or are already heading toward the CISPR limits, it is sufficient for argument's sake to show only this comparison. To summarize the principal differences, the CISPR limits for radiated emissions between 88 and 230 megahertz (MHz), and for conducted emissions between 1.705 and 30 MHz, are more stringent than the FCC commercial (Class A) limits. Between 150 and 450 kHz, CISPR has limits in effect for conducted emissions, whereas the FCC does not.

Basic EMC design tests and rules will go far toward meeting regulatory limits. Many of these basic principles will be explained in the next section. The point to remember for now is that EMC does not happen by chance. The initial EMC design intent is to provide margin (in decibels) of EMC to be achieved below the maximum levels allowable by law.

The initial steps toward compliance, if taken early in the design phase, are inexpensive (on average less than 1 percent versus 10 percent or more of product and development costs when EMC is not considered early) and have little impact on the schedule. Factors such as proper component placement can aid the layout and interconnection process. Conversely, steps taken after the initial layout are more costly and have a substantial impact on the development schedule. Education should be provided to everyone involved in the design and layout of the product to provide a heightened sensitivity to EMC.

EMC education should be tailored to meet the needs of the key personnel involved. If a particular organization experiences high turnover, it is essential to keep the EMC effort focused as new designers join the organization. The EMC test organization is a valuable resource to help train such designers, for it has a wealth of experience and knowledge that spans many product lines, and it is less prone to engineer turnover. Panel 2 outlines the type of EMC training the "players" should receive.

Panel 2. EMC Education

Managers. EMC overview, concentrating on the financial and schedule impacts of non-compliant designs. (*All* EMC courses should cover this facet.)

Circuit designers. Formal alternating current (AC) and direct current (DC) circuit theory and field and wave theory, followed by instruction in emission modeling and prediction, interconnection and cabling for EMI control, FCC and international regulations, electromagnetic propagation effects, compliance testing, and preparing documentation for the PWB layout designer who specifies PWB layout requirements.

Physical designers. An overview of the circuit designer course description with a concentration in electromagnetic emission environment, interconnection and cabling at both PWB and system/full assembly level for EMI control, enclosure design for EMC.

PWB Layout designers. Frequently overlooked, the PWB designer is charged with the PWB realization process. A basic understanding of PWB-level EMC layout and routing techniques is essential for designing a compliant product and correctly interpreting the PWB layout requirements document.

System Requirements Document

The system requirements document specifies the EMC regulations with which the product must comply. Ideally, this document will outline a worst-case composite of multinational and domestic compliance requirements, including the appropriate FCC regulations. This composite is a major step toward our global marketing objective. In the United States, Class A products are designed for the commercial market, and may not be used for Class B (residential) applications. Class A products meet less stringent standards than those that apply to residential products. The decision on which international regulations to meet will be dictated by market opportunity.

Once the total market picture is clear, the applicable EMC requirements are compiled and compared. Work on drafting a composite requirements document can then begin. As a rule, if EMC is an initial design consideration, compliance is achievable in a single design cycle. In fact, designing for EMC even makes the product more robust operationally. The robustness factor implies the product will be less likely to fall prey to internal and external RF emission sources. Thus, EMC significantly increases product quality.

Design Process

Designing for EMC can be attacked at several levels, as shown in Figure 4. This paper will concentrate on the basic level 1 EMC design since it is the cornerstone for radiated emission suppression. If level 1 suppression is under control, the higher levels are then addressed. These levels have larger loop areas and, as we will see later, a higher potential for emissions. Thus, keeping interference off these levels by good PWB suppression techniques is always most effective in EMC compliance design. We will show later that at these higher levels, currents on cables may play a significant role as an emission source. Hence, attention is paid to good EMC design at all levels.

This section presents an overview of the steps to design PWB layouts for emission control. Interactions between the development organization and the appropriate PWB layout organization are described from an EMC perspective.

Before First Layout. Once the system requirements are specified, an overall product architecture must be determined. From that point, the device technology can be selected. EMC design reviews should be a standard

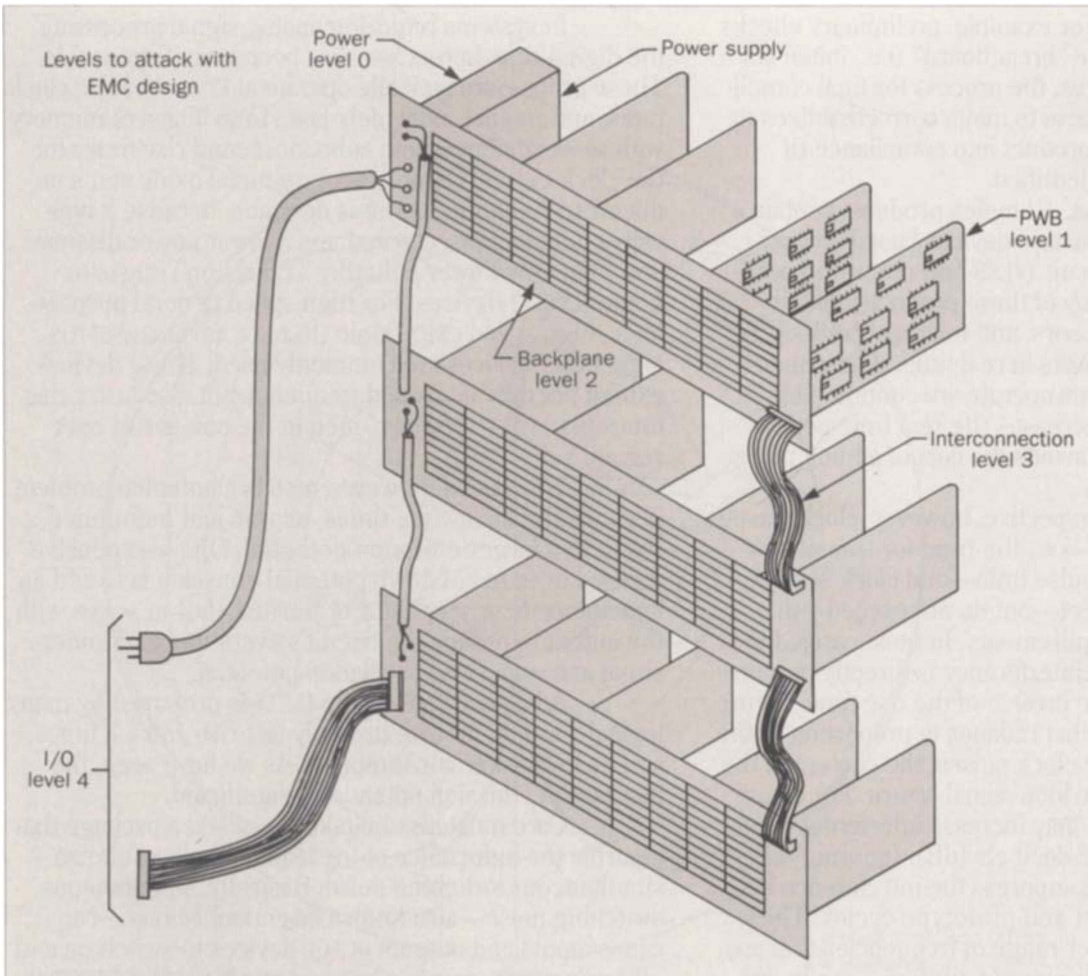

Figure 4. Levels to attack with EMC design, showing power supply, PWB, backplane, interconnection, and I/O levels.

milestone early in the development schedule. The reviews should be attended by circuit and physical designers, and by representatives from the PWB layout and EMC test or consultation organizations involved in the product realization process. All critical compliance issues should be discussed and documented during these reviews. Failure to document and thoroughly distribute the findings and recommendations from this review can seriously affect schedule issues and design staff resources that have to be diverted later to fix EMC problems. Failure to incorporate EMC in even one portion of the product may cause failure when the entire system is tested.

Quality metrics must also be established in the development schedule. For example, preliminary checks for compliance during the "breadboard" (i.e., initial lab model) or prototype stages, the process for final compliance testing and the process to make corrective fixes to bring the manufactured product into compliance (if required) should all be identified.

Technology Selection. Complex products contain a mix of commercial and custom devices based on very large-scale integrated circuit (VLSI) and other microprocessor technologies. Many of these products contain several VLSI chips, processors, and microcontrollers. To perform more complex tasks in real time, the frequencies at which these devices operate are continuously being increased. This increases the real time performance of the device and avoids the cost of adding more processors to the design.

From an EMC perspective, however, clock waveform rise and fall times—i.e., the time for transitions between 0's and 1's in a pulse train—and clock speeds should be picked that meet—but do not exceed—the product's operational requirements. In most cases, the product's risk of causing interference is directly proportional to the square of the inverse of the rise time. Figure 5 shows a simple circuit that radiates in proportion to the frequency squared of the clock pulses, the current in the circuit and the area of the loop signal return. For example, halving the rise time may increase interference levels up to 4 times, or by 12 decibels (dB). Ignoring this leads to excessive cost to suppress the interference in the product development and prototype cycles. The bandwidth—i.e., the major range of frequencies that are generated as potential sources of emission—can be calculated with the equation

$$\frac{1}{\pi t_r},$$

where t_r is the rise time. For a 2.0 nanosecond (nsec) rise time pulse, frequencies up to 150 MHz can readily be generated, well within the 30 to 1000 MHz spectrum regulated by the FCC.[5]

In systems requiring analog signal processing, the digital signal processor has become indispensable. These processors typically operate at 25 to 45 MHz clock rates, and require extremely fast (15 to 30 nsec) memory with associated nsec and subnanosecond rise times for the clock pulses. Complementary metal oxide semiconductor technology (CMOS) is desirable because it typically offers increased speed and a lower power dissipation than Low Power Schottky Transistor-Transistor Logic (LSTTL) devices. For high-speed general purpose logic, high-speed CMOS logic (HCL) or advanced CMOS logic (ACL) devices are commonly used. These devices exhibit not only increased frequency but also faster rise times than LSTTL devices, often in the one to two nsec region.

This speed, however, also is a potential problem because the faster rise times, as was just mentioned, result in a larger emission potential. One inexpensive method used to cut down potential emission is to add an impedance (e.g., a resistor or ferrite bead) in series with the output to reduce the circuit's overshoot and undershoot and undesired oscillation potential.

Advanced CMOS logic (ACL) is preferred by many logic designers for its extremely fast rise and fall times, and its low power consumption. As we have seen, the increase in emission potential is significant.

Care must also be taken to select a package that controls the inductance of the leads to help minimize simultaneous switching noise. Basically, simultaneous switching noise—also known as *ground bounce*—can cause inputs and outputs of ACL devices to switch on and off erroneously, causing large currents that lead to even more emissions during switching.[6] During this intermittent phenomenon, emission levels increase, and the source of the interference is all but impossible to locate. Such circuit performance is also intolerable in terms of the product's level of error-free internal operation, and in terms of development and service costs for corrective action to handle customer field complaints. PWB emissions are generally modeled by the equation shown in Figure 5, namely, at a given distance, the radiated

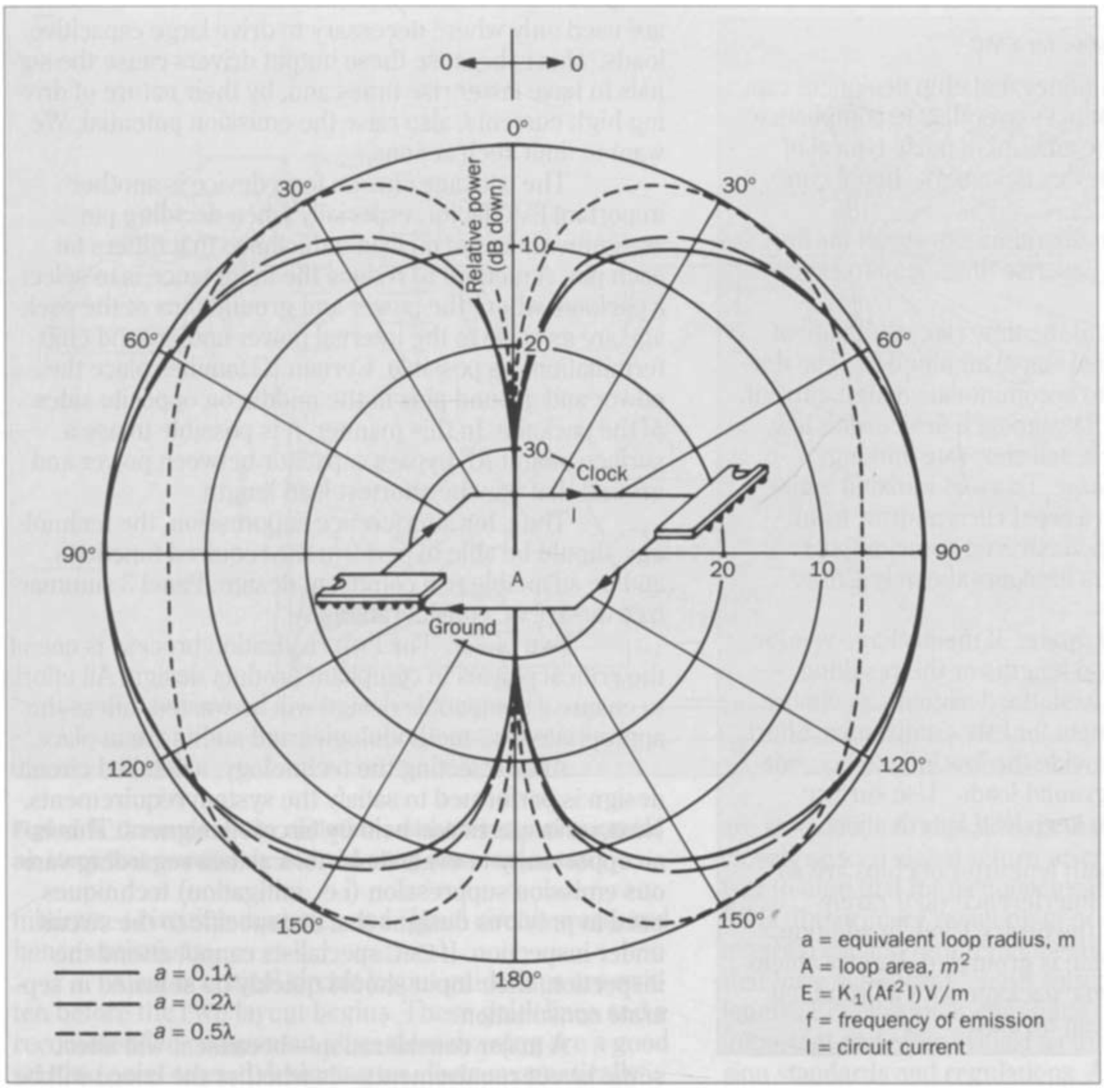

Figure 5. Differential mode radiated emission elevation angle amplitude pattern.

electric field strength is proportional to

$$Af^2I,$$

where A is the area of the signal loop, f is the frequency of the emission, and I is the circuit current.

In systems with multiple devices all clocked at frequencies between 10 and 50 MHz, it is occasionally useful to supply the devices with independent clocks. The clock frequencies are chosen to avoid in-phase amplitude addition at several frequencies by spreading the energy

Panel 3. Designing Devices for EMC

There are several techniques that chip designers can use to improve the product's overall EMC compliance level while reducing the amount of noise typical of high-speed devices. Device designers should concentrate on:

- *Clock speed.* Choose the minimum speed for the design application. Fast rise times lead to excessive emissions.
- *Slew rate.* Minimizing the time rate of change of voltage shifts in digital signal amplitudes. The device will still be able to accommodate a high current.
- *Low current buffers.* Designing a device with low current buffers that is self-slew rate limiting.
- *Stagger output switching.* To avoid radiated emissions resulting from a rapid current draw from many gates simultaneously, run some outputs through extra buffers for approximately 1 nsec delay per gate.
- *Low inductance lead frames.* If the package vendor gives the internal lead lengths or the resulting inductance on each lead, the designer can choose the best pin assignment for EMC compliance. Short leads lengths will provide the low inductance suitable for power and ground leads. Use surface mount technology to keep lead length short.

Because the internal path length(s) of chips are so short, radio frequency interference (RFI) rarely presents a problem on the device level. In addition, the chips entire substrate is grounded. If extra shielding is required, a ceramic package with a grounded metallic cavity and lid can be used.

throughout a broad frequency spectrum of the various clock harmonics. At these frequencies, the probability of such combined amplitude clock harmonics causing the emissions to exceed regulatory limits is reduced.

When customized large scale integration and VLSI devices are designed, high-current output drivers are used only where necessary to drive large capacitive loads. This is because these output drivers cause the signals to have faster rise times and, by their nature of driving high currents, also raise the emission potential. We want to limit such actions.

The package chosen for a device is another important EMC factor, especially when deciding pin assignments based on lead inductance that differs for each pin. A method to reduce the inductance is to select a package where the power and ground pins of the package are as close to the internal power and ground chip terminations as possible. Certain IC families place the power and ground pins in the middle on opposite sides of the package. In this manner, it is possible to use a surface-mount RF bypass capacitor between power and ground that has the shortest lead length.

Thus, for interference suppression, the technology should be able to perform the required functions, and be adaptable to a compliant design. Panel 3 summarizes these EMC considerations.

PWB Layout. The PWB realization process is one of the critical phases in compliant product design. All efforts to ensure a compatible design will be wasted unless the appropriate EMC methodologies and audits are in place.

After selecting the technology, a detailed circuit design is performed to satisfy the system requirements. Next, an inspection is held by circuit designers. This is an opportunity to evaluate historical data regarding various emission suppression (i.e., mitigation) techniques used in previous designs that are specific to the circuit under inspection. If EMC specialists cannot attend the inspection, their input should quickly be solicited in separate consultation.

A major consideration—because it will affect some layout requirements—is whether the board will be double-sided or multi-layer. EMC, circuit technology, and the PWB density, size, and cost, are important factors in this decision. With respect to EMC, choosing multi-layer PWB technology over double-sided PWB technology has distinct advantages. Ground planes on multi-layer PWBs provide the most direct signal-return circuit path. This

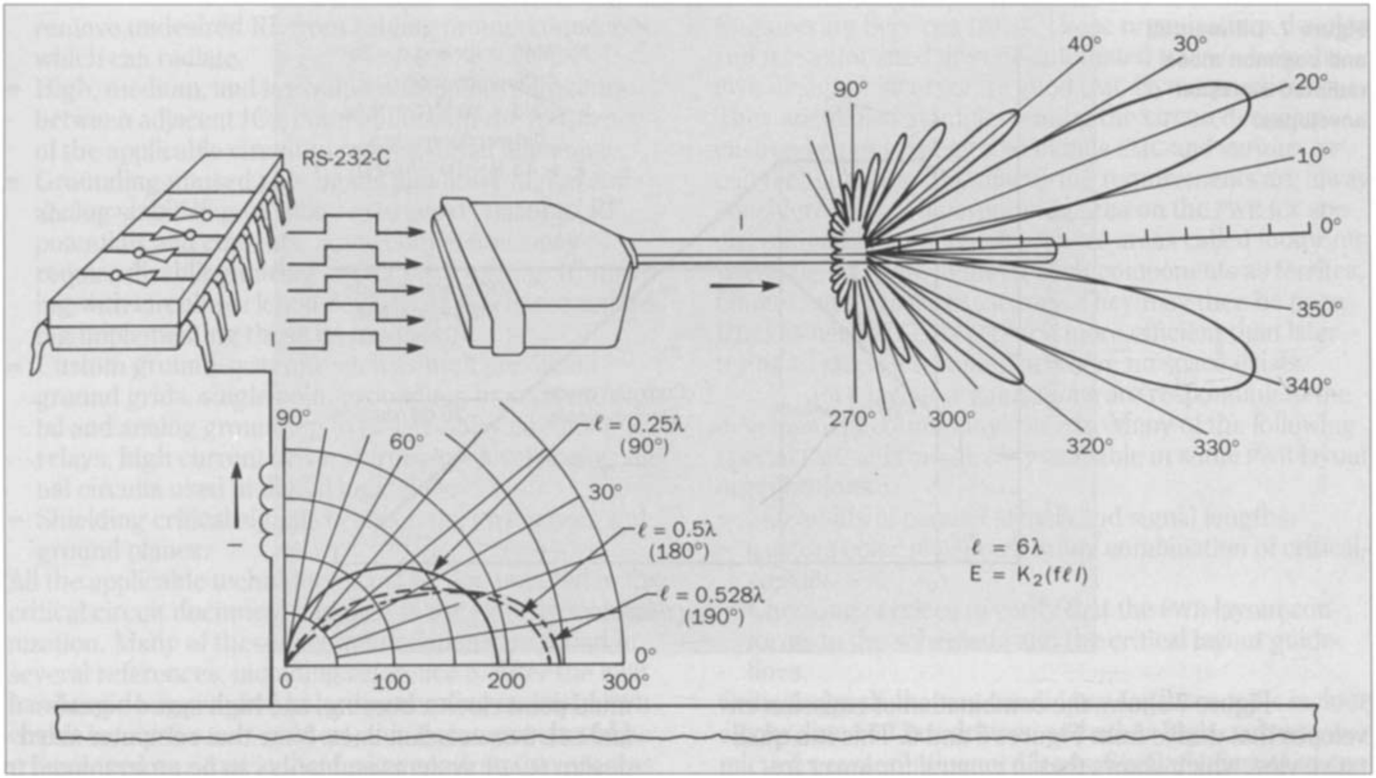

Figure 6. Common mode radiated emissions showing cables as electrical monopoles and traveling wave antennas.

minimizes circuit inductance and signal circuit areas, and hence emissions.

A set of critical circuit layout guidelines are written before the PWB layout begins. These guidelines and a recommended component placement drawing are a good starting point toward designing an electromagnetically-compatible PWB. The parts are placed by functionality and to isolate certain high-frequency clocked parts from circuits that go first to connectors, then to other portions of the product, or to external cabling. Concurrent with the guidelines, some notations have been defined that specify—directly on the schematic drawing—when leads are shielded, i.e., signal leads that are paralleled by closely spaced signal return or ground paths. It is important to note that for frequencies under approximately 150 MHz, the primary radiating generator or antenna is the external cabling or interconnects within the equipment that have significant length with respect to the wavelength. Keeping such emissions off these cables is an important and often critical factor in meeting EMC emission standards and regulations. As seen in Figure 6, the radiated electric field strength at a given distance from such cables is proportional to

$$flI$$

where f is the frequency of the emission, l is the length of the trace or cable, and I is the circuit current.

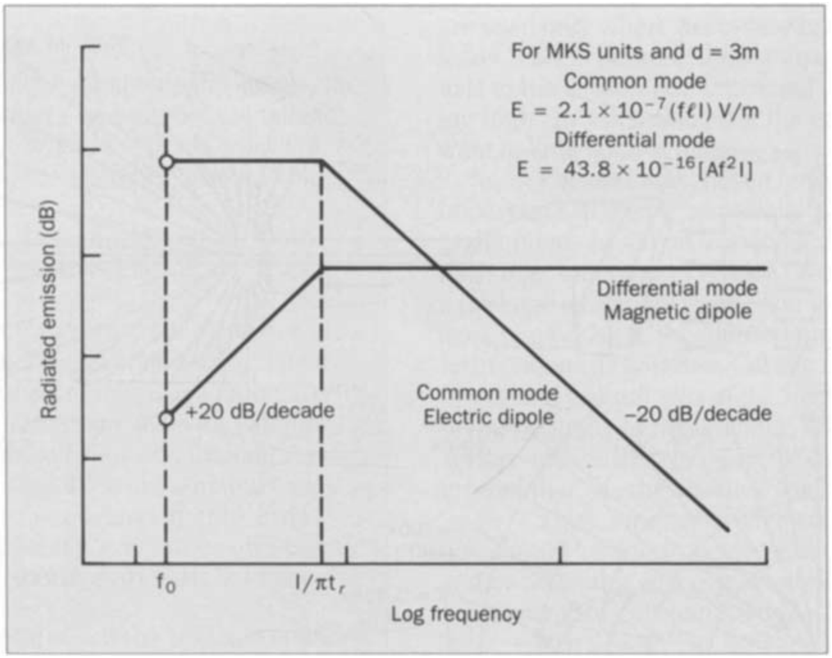

Figure 7. Differential and common mode radiated emission envelopes.

Figure 7 shows the combination of emission envelopes that derive from Figures 5 and 6. This is a qualitative view which shows that in general for lower frequencies (up to $\frac{1}{\pi t_r}$), the dominant interference model is that shown in Figure 6, i.e., cable emissions. At higher frequencies, the model shown in Figure 5, i.e., current loop emissions, dominates.

There is no EMC "cookbook" or set of rules, because all circuits and their interrelation with other parts of the product, including cabling, are different. However, certain EMC practices should be used wherever possible:

- Placement partitioning by functionality, i.e., digital logic, analog circuitry, and noisy control and power circuits.
- Routing and placement to achieve pulse timing objectives and minimal interconnection lengths.
- Low impedance and small loop areas associated with multi-point clocks, bussing, and high-speed signals and ECL transmission lines. Note that computer-aided design (CAD) systems and tools can be programmed to identify clocks and other critical traces which can be excluded from auto-routing. This allows the manual positioning of such critical paths and clocks. Likewise, analog signals and other critical leads can be isolated from digital trace auto-routing.
- Isolation techniques for electromagnetic field containment by parts rotation (e.g., transformers, optical couplers), fine-line ground path shielding, and physical separation between critical components.
- Using 45° cornering of traces on high-speed digital PWB paths to avoid right-angle connections where reflections of the clock harmonic high frequencies inhibit performance and adversely affect radiated emissions.
- Capacitive suppression and bypassing techniques for digital drivers and receivers near connectors to

remove undesired RF from cabling or interconnects which can radiate.
- High, medium, and low-value decoupling capacitors between adjacent ICs, compatible with the frequency of the applicable circuit to reduce signal line noise.
- Grounding unused gate inputs and other digital and analog stabilizing techniques to avoid "floating" RF potentials and currents. Some connections may require disabling during circuit pack testing. (Consulting with circuit pack test developers is advised regarding implementing these techniques.)
- Custom ground systems, such as multiple digital ground grids, single-point grounding, or separate digital and analog grounding to isolate noisy circuits (e.g., relays, high current drivers) from low level analog signal circuits used in digital logic flow.
- Shielding critical signals between the PWB power and ground planes.

All the applicable techniques must be documented in the critical circuit document supplied to the PWB layout organization. Many of these recommendations are found in several references, including reference 5. After the PWB has been designed, and before generating an initial PWB circuit layout (i.e., art master), this document should be reemployed as a tool in the design confirmation process.

At all phases of the layout, communication between the circuit design engineer, physical design engineer, EMC consultant, and PWB designer must be maintained. PWB design decisions are based on EMC, functionality, PWB design feasibility, manufacturability, testability, cost and schedule factors. No single factor is discounted in the decision process. If a decision affects any factor, the appropriate design personnel must be notified.

Interaction With The PWB Layout Organization. The development organization should be aware that many PWB layout organizations have trained their design staff in EMC PWB design and the appropriate interaction with the engineering customer. Such layout organizations are called many names; within AT&T they are known as the Engineering Information Department (EID) and Design Engineering Services (DES). These organizations develop and use automated or semi-automated tools to help the PWB designer incorporate good EMC layout practices. They are skilled at implementing the circuit designer's custom layout strategy that blends EMC and various circuit technologies. Manufacturing requirements are always considered when incorporating area on the PWB for special mitigation components. These areas called footprints would be set aside to insert such components as ferrites, chokes, and bypass capacitors. They may then be populated as needed. This is much more efficient than later trying to insert a component where no space exists.

PWB layout organizations are responding to the development community's needs. Many of the following special EMC aids are already available in some PWB layout organizations:
- CAD audits of parallel signals and signal lengths.
- Custom color plots to view any combination of critical signals.
- Checking services to verify that the PWB layout conforms to the schematic and the critical layout guidelines.

Critical signals that are candidates for these tools include clocks, line and bus drivers, and other high-current microprocessor-influenced leads. Similarly, inputs to analog amplification circuits and cable interface areas are additional candidates.

EMC and DFX. Designing for EMC is a part of the overall DFX process, where *X* in this case represents EMC. The following outlines DFX-EMC considerations that should be observed throughout the product planning and development process.
- Clearly defining all potential markets permits drafting a worst-case composite of multinational regulatory requirements (both limits and methods of measurement) for the system requirements document. Failure here ultimately implies various levels of missed market opportunity.
- After technology selection has been made, and the findings from the prelayout design for EMC meetings

Panel 4. Effectively Communicating EMC Requirements

Effective communication of EMC requirements can be achieved with the following aids:

- PWB layout requirements document.
- Schematic notation for shielded interconnections and suppression devices.
- Frequent interaction between design engineers, PWB layout, and EMC specialists during layout.
- Suggested component placement scheme including footprints for ferrite beads, chokes, toroids, and other suppression devices. Many devices are now available in surface mount packages that lessen lead inductance and manufacturing costs.
- EMC education
- Early and continuing consultation with EMC specialists
- EMC newsletter publicizing successful EMC designs

are known, a crucial act follows: documenting and distributing the findings to *all* designers in the project including the PWB layout organization. Not doing so jeopardizes the system's overall compliance integrity. Panel 4 summarizes methods to communicate successful EMC practices.

- Once the circuit and emission suppression requirements are known, the schematic containing EMC symbols and notes, and the layout guidelines, are sent to the PWB layout organization. These tools and communications are part of the design methodology that keeps the emerging design on the road to compliance.
- Suppression devices should be included in the tools mentioned above whenever there is a reasonable chance the design will require mitigation. Note: Once the footprints are in place on the PWB, these devices are installed only if preliminary compliance testing establishes their usefulness.

Design for EMC compliance is only one DFX factor. Compliance must be blended with other DFX factors (i.e., manufacturability and testability) to realize the lowest-cost design in the shortest time. The concerted efforts of physical and electrical design engineers, the PWB design team, and the EMC specialist, are invaluable in monitoring this blending process.

EMC Testing

Once the design has taken shape and hardware is assembled on a PWB, preliminary tests are done to assess the potential for meeting FCC and international limits. It is not necessary to have a production-quality model to get an idea of emission levels and harmonic content. Once models are available and the design approaches the final production-quality layout, more useful quantitative emission data can be recorded. Alternately, preliminary testing is not performed, and all testing takes place when the completed product is submitted for the final compliance test. This is risky, however, because at this stage of the process, there will be fewer degrees of freedom to make changes, and those that are made usually are more costly, e.g., hand insertion of suppression components.

Preliminary Testing. The purpose of preliminary testing is to identify major sources of RF noise, and to determine if further suppression techniques are needed at the PWB level beyond those stated in the previous section. It is hoped that such techniques will make use of the area on the PWB we have already set aside for suppression components. Areas, especially next to I/O connectors, usually are used. The more footprints or space to add suppression components, the less the need to consider a second changed layout that may add considerably to development costs and delay the project.

Ideally, all parts—including custom LSI devices—will be available for preliminary testing of the assembled circuit pack. The product should have enough software to initialize the circuits and put the unit into one or more operating modes. Sometimes special EMC test software is written that simultaneously activates as many leads as possible. This technique generally simulates a worst-case operational environment where data and emission-causing signals are forced into all leads. This, of course, seldom happens simultaneously in normal operation. The test equipment used during this phase can range from a fully equipped EMC lab to a simple handheld probe (i.e., a sniffing coil) that picks up emissions next to the component. At this stage, it may be necessary to install a simple model of an as-yet unavailable complex LSI device. If preliminary tests reveals any EMI problems in the design, mitigation efforts can begin.

If necessary, designers can quickly add signal and clock-shaping capacitors and resistors, as well as ferrite beads, to the power supply conductive signal traces (i.e., paths) of high-speed chips with fast rise time clock pulses. Retesting can begin almost immediately without the delay of a relayout. Of course, using the space previously set aside for suppression components should be considered first if it is most useful in emission reduction.

Once all the parts are available, mitigation components have been added, and the appropriate software has come together, the unit is retested to determine the emission potential. During this second preliminary testing phase, the unit or units used during the retest—comprising all the PWBs and functioning circuitry inside its mechanical frame—should be the *final* prototype versions, with all specified components and the final PWB layout and interconnection traces. This version of the product often is so close to the manufactured version that an initial compliance test may be performed and if the product passes, the manufacturer proceeds with its fabrication. If the margin with respect to the emission limits is small (less than 6 dB), a further compliance test or check is performed as described in the next section.

Compliance Testing. When samples are available from the factory, the product is subject to the final phase of compliance testing. At this stage, the retest effort may be limited to comparing the emission results of the prototype preliminary test with those of the manufactured version. Final software is used in this step.

If the results are comparable, and there is adequate margin with respect to the limit (including allowances for measurement inaccuracies), the results can be regarded as equivalent, and compliance is considered verified. If the comparisons are significantly different by several dB, it is prudent to perform another full compliance test. If there is any doubt, a full compliance test on the manufactured version should take precedence. A test report is then issued to the development organization and the process of labeling, inserting FCC required language in the user's manual, etc., goes forward.

Compliance testing should only be a formality if good EMC design techniques were practiced. Unfortunately, this ideal situation cannot be assumed. Compliance testing will identify further EMC design problems that may have been missed earlier, or that have surfaced due to changing conditions such as inattention to EMC requirements during manufacturing (see the next section). The solution will require careful and quick investigation. If the usual EMC suppression techniques are not sufficient, more sophisticated or costly techniques will have to be applied, such as special shielding, cabling, enclosures, and RF filters. These should be considered the last line of defense because they are costly and suggest that insufficient attention was paid to EMC early in the design. Even where techniques such as shielding are required, shielding should be performed selectively on the PWB before whole-product shielding is undertaken. This is much more cost effective. The EMC specialist and test engineer are the key players during this phase, and work closely with the design team.

It is interesting to note that the manufactured product's emissions may be appreciably lower than the emissions from the prototypes tested in the preliminary testing phase. This may be because the prototypes had connections between parts of the PWB made with temporary wires that acted as antennas. By replacing these wires (sometimes referred to as "white" wire changes) with properly routed PWB traces, the emissions enhanced by them may no longer be significant.

Effect of Small Compliance Margin. If prototype testing reveals a small compliance margin, the product team may be in for some production phase surprises. Even a change as small as component substitution or misrouting of interface cabling may alter the compliance margin. Although relayout of circuits on the PWB level should be avoided at all costs, marginal designs occasionally require such drastic measures.

At this late point, PWB or circuit pack redesign significantly increases product development costs and may cut into the profit margin. These occurrences can be expected when inadequate time is spent designing for EMC. The PWB layout organization experiences a swell in design queue as PWB designers are assigned to rework non-compliant designs. Further, engineering resources in R&D and manufacturing are diverted from starting designs on newer products.

Postponing full ramped-up manufacturing creates a "domino" effect. That is, production of other products queued for that particular assembly line may be affected, even to the extent of postponement, until decisions are made on the most effective way to bring the product back into compliance.

Once a solution is found, corrective measures are usually limited to "add-on" mitigation, e.g., mitigation requiring costly manual insertion effort. After mitigation is introduced to the design, it is important to check compliance on the first product manufactured as well as on those from a fully ramped-up process. The first manufactured sample test will show if mitigation and other specified important controls for EMC were correctly incorporated.

Strategic measures are in order even for designs that have narrowly achieved compliance. Investigating the most effective mitigation techniques with an eye to gaining margin with respect to the limit, cost, and circuit functionality, may take many days. These measures should be milestones in the development schedule, and should be a priority effort of the design team, testers, and often the manufacturer. The manufacturer may not want a suppression technique that is difficult to automatically insert.

In any case, the product manager—in cooperation with the manufacturer—is responsible for building a compliant product. The manufacturer expects the development organization to provide a compliant design. The above process should be used to assure this.

Ongoing Compliance. Manufacturing control of continued emission compliance is achieved by performing ongoing compliance checking. Retest intervals generally depend on at the least the following:

- Margin with respect to the emission limit.
- Variability of the RF emissions from one product sample to another.
- Quantity of product manufactured.
- Any reported interference complaint from the field.

The FCC is especially concerned with seemingly unimportant changes, such as rerouting a wire. Ongoing compliance checks verify that the product in production continues to achieve compliance. (Panel 5 reproduces excerpts from the FCC's Public Notice of April 7, 1982, "Commission Cautions Against Changes in Verified Computing Equipment," unequivocally stating its cautionary position on such changes.)

Products that have achieved compliance by a substantial margin will need less frequent retesting than products that have narrowly achieved compliance, i.e., close to the FCC or appropriate international limit. Specifically, retest intervals of even less than a month or—a very worst case—on a sampling basis would be indicated for products that comply by a small margin; semi-annual or annual intervals may be sufficient for products with large margins, i.e., greater than 6 dB.

If the product has RF emissions that vary considerably from sample to sample, a shorter retest interval is needed. The same is true for large production volumes or those massed-produced for critical applications, i.e., in proximity to sensitive equipment on customer premises. The manufacturer must catch non-compliant conditions before too many products are already in the pipeline to the customer.

A production shutdown must be used if any check reveals a non-compliant product. Using the appropriate statistical models developed by the manufacturer's quality

Panel 5. Excerpt from FCC Notice on Modifications

"It has come to the Commission's attention that manufacturers are making changes in computing equipment on the mistaken assumption that a 'minor' change will not affect the compliance of the computer with the FCC requirements. . . .

It cannot be stressed too strongly that the manufacturer has the responsibility to avoid changes unless a firm determination is made that the change will not throw the product out of compliance. While a detailed analysis will help make such a determination, the preferred method is by testing the revised product.

The manufacturer is cautioned that many changes which on their face seem insignificant, are in fact very significant. Thus a change in the layout of a circuit board, or the addition or removal or even the rerouting of a wire, or even a change in the logic will almost surely change the emission characteristics (both conducted as well as radiated) of the device. This is particularly true of a device housed in a non-metallic enclosure. Whether this change in characteristics is enough to throw the product out of compliance can best be determined by retesting.

Manufacturers of computing equipment are urged to test products coming off the production on a regular schedule. Such testing provides assurance that the quality of the final product has not deteriorated. Secondly, such a regular schedule of testing will detect any changes that may inadvertently creep into the production process."

assurance group will show the company's dedication to compliance. It also has the benefit of heading off any potential action by regulatory authorities who may conduct audits.

It should also be pointed out that any repairs or maintenance performed on a compliant product must be carried out by field service or factory repair staff so as not to compromise the compliant design. Instructions should be written to ensure this and especially to highlight those critical EMC parts and layout areas.

Quality Metrics

The authors recommend AT&T's non-proprietary manual *Quality by Design, Issue 1.1*[8] to any organization formulating or revising its quality metrics for the EMC compliance design process. The guide applies to any design process, and assists in designing and executing a systematic approach to quality that focuses on the parameter design process.

We now revisit the regulatory compliance design process using the guidance in the AT&T manual in the context of a rigorous quality program.

- *PWB Layout.* The objective is to establish EMC review and action metrics that will allow the design team to control the critical EMC physical layout of the circuit and PWB design. These design parameter values should be selected to predict the emission characteristics of the product, and the level of noise reduction attainable within desired cost levels. The following are five steps toward designing and implementing EMC quality metrics:
  1. *Determine Objectives.* Define EMC objectives for achieving compliance with known circuit and equipment design, and the emission qualities of components and technology used.
  2. *Select Metrics.* Verify that the EMC measurement techniques are appropriate and current.
  3. *Collect and Analyze Data.* Evaluate successful EMC designs, and determine what EMC design characteristics led to compliance. Evaluate designs that have failed to achieve EMC, determine the cause or causes, and avoid them in the future.
  4. *Report.* Distribute the results of this EMC characteristic data using a format that will help users understand the concepts and the need for appropriate action.
  5. *Take Action.* Once the EMC diagnostic and

Panel 6. Quality By Design—PWB Mitigation Example

A portion of product XYZ uses a high-frequency circuit that has introduced EMI in past designs. Consulting with high-frequency device manufacturer ABC yields the recommendation that a grounded shield in the form of a costly metal can to contain the emissions. After determining that the objective is to avoid EMI, from this and other aspects of the circuit, the design team concludes it will measure its progress towards compliance via a formal inspection of the critical signals. The inspection is established as a milestone in the development schedule, and will measure the layout against an as-yet undetermined solution that will be documented in the critical circuit guidelines. Historical data is gathered from projects across product lines that have used this high-frequency circuit. Analysis reveals success rates at 50 percent compliance and 50 percent noncompliance during the preliminary compliance test phase. The attributes of both are documented quickly and inexpensively in graphics and text, and reported to the development team and management.

The team concludes that containing the high-frequency circuit is indeed in order. Moreover, the efforts to secure historical data uncovered a quality improvement project that eliminated the metal can altogether: by routing the high frequency circuit on the innermost layers and shielding it with fine line ground traces and adjacent layers of power and ground, the PWB itself can provide the same containment (virtually cost free), that an expensive hand inserted metal can would provide. In a storybook ending, the device manufacturer's costly containment "can" solution is replaced by the quality improvement concept of a virtual no-cost PWB level containment. The cost of quality (research, etc.) was minimal compared to the expensive corrective "can" solution, or the consequences of taking no action at all.

To verify the EMC compliant design, request the appropriate approval plots of placement, critical signal routing and power/ground distribution schemes early on. Once the board is fully routed, little opportunity for low cost corrective action exists or is needed.

administrative processes have been confirmed, corrective action and quality improvement (i.e., prevention) can begin.

Panel 6, "Quality By Design," shows one example of the process.

- *Mitigation.* Panel 6 details one form of low-cost (or no-cost) PWB mitigation. A design is high quality if it facilitates low-cost, low-effort emission suppression.
- *Margin.* Designs with large-margin with respect to the emission limits avoid the risks inherent in narrow-margin designs, and consequently are of higher quality.
- *EMC Control in Manufacturing.* The product should be manufactured as specified by the design information, with particular attention to those components identified as affecting EMC.
- *Parts Substitution.* Any part substitution should perform in an equivalent manner from an EMC perspective. To assist in this process, a parts substitution list of acceptable EMC components should be provided to the manufacturer. Any change in the PWB layout or interconnections will trigger a retest for compliance.
- *Added Features.* Often features are added after the critical circuit is designed for EMC. Methods must be in place to ensure that additional circuitry does not disturb EMC aspects of the design. EMC concerns can never be put to rest.

Conclusions

Whether products are designed with good EMC practices for the domestic or multinational marketplace, designing for emission compliance:

- Lowers product development and manufacturing cost and time when taking into account wasted efforts to suppress emissions after the design is mature.

- Enhances functional performance and overall product quality.
- Facilitates the product's timely release for marketing.
- Avoids costly factory retrofit and PWB relayout.

The product manager is in an excellent position to control EMC costs. The cost to design and manufacture products that comply by a large margin with respect to the regulatory limit should be much less than the cost to design and manufacture products that narrowly comply. A product with a small margin requires frequent compliance tests that drain revenue and divert staff resources. Because a compliant product is more operationally robust, any cost or potential delay in the product's release associated with the time invested in preliminary compliance efforts will be more than offset by the product's improved functionality and overall customer satisfaction.

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Biographies (continued)

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